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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E43RG54880LWAM400-C

Overview:

- 4.3-inch TFT: 480x800 (69.16x120.05)
- 3SPI+16/18/24- bit RGB Interface
- 16.7M colors
- 3.3V
- White LED back-light
- Transmissive/ Normally Black
- Capacitive Touch Screen
- 400 NITS
- Controller: ILI9806E, GT911
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit and back-light unit. The resolution of a 4.3" TFT-LCD contains 480x800 pixels, and can display up to 65K/262K/16.7M colors.

Features

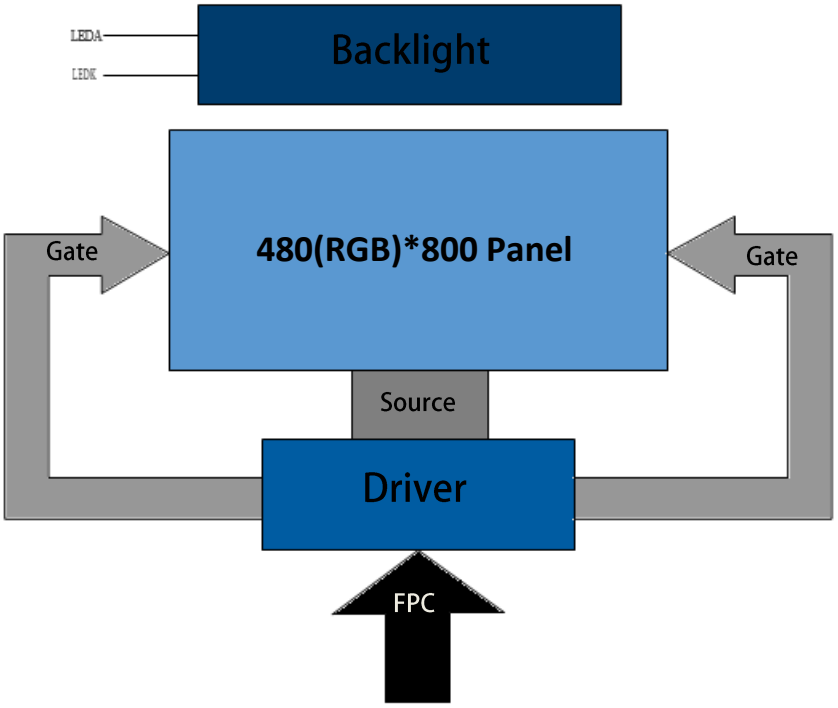
Low Input Voltage: 3.3V (TYP)
Display Colors of TFT LCD: 65K/262K/16.7M colors
TFT Interface: 3/SPI+16/18/24-bit RGB
CTP Interface: I2C

General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display area (AA)	56.16(H)*93.6(V) (4.3 inch)	mm	-
CTP view area	57.16(H)*94.60(V)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K/262K/16.7M	colors	-
Number of pixels	480(RGB)*800	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.039(H)*0.117(V)(217 ppi)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	ILI9806E	-	-
CTP Driver IC	GT911		
Display mode	Transmissive/Normally Black	-	-
Simultaneous Touch Points	5	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

Mechanical Information

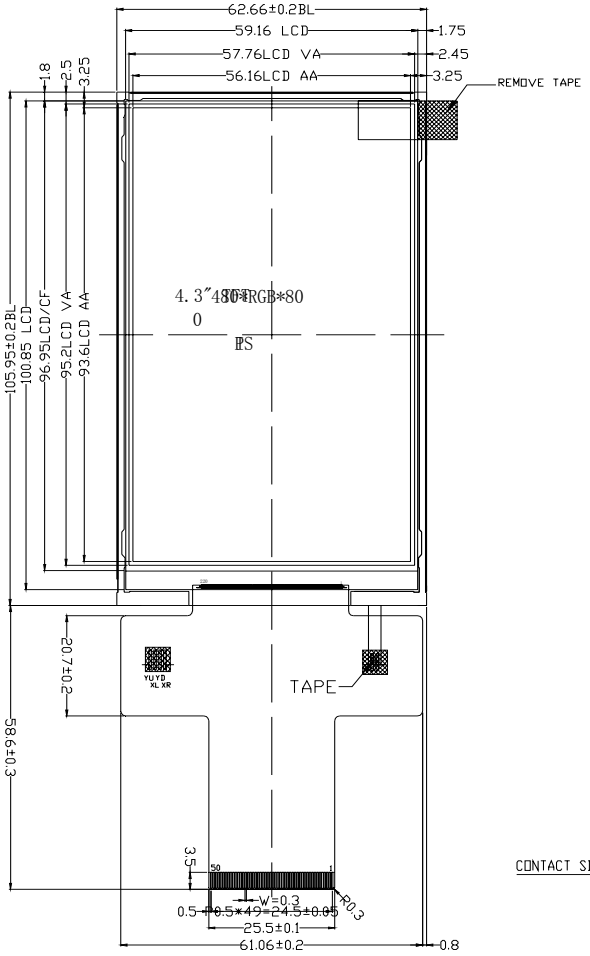
Item		Min	Typ.	Max	Unit	Note
Module size	Horizontal(H)		69.16		mm	-
	Vertical(V)		120.05		mm	-
	Depth(D)		4.13		mm	-
Weight			TBD		g	-

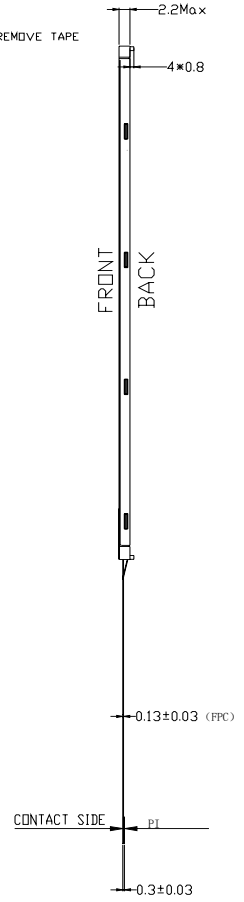
1. Block Diagram

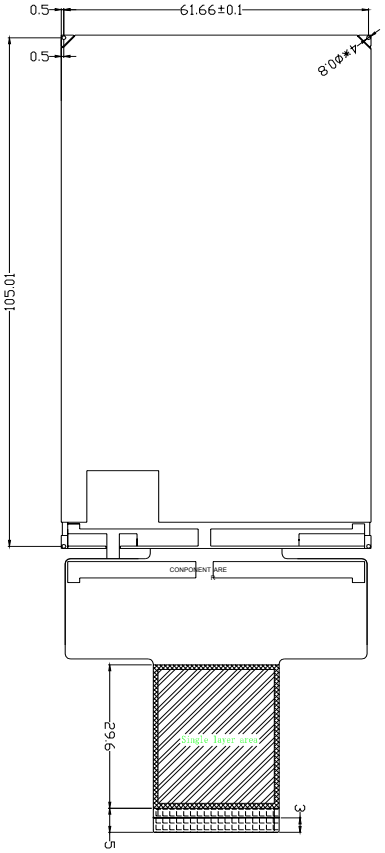


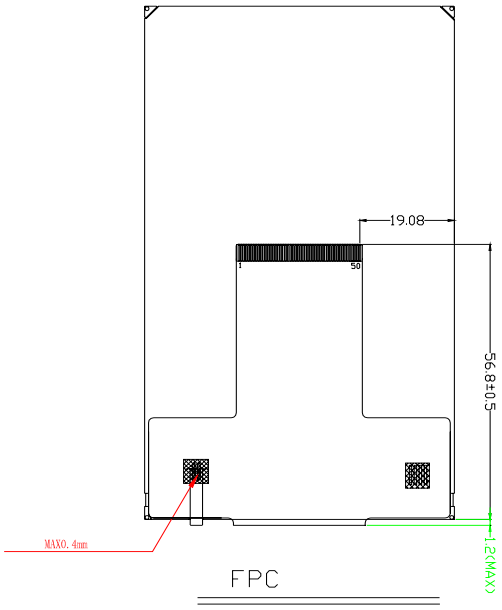
2. Outline dimensions

2.1 LCM









NO.	Pin Name
1	LEDK
2	LEDA
3	NC
4	GND
5	GND
6	VCI
7	VCI
8	NC
9	NC
10	NC
11	NC
12	RESET
13	DB23(R7)
14	DB22(R6)
15	DB21(R5)
16	DB20(R4)
17	DB19(R3)
18	DB18(R2)
19	DB17(R1)
20	DB16(R0)
21	DB15(G7)
22	DB14(G6)
23	DB13(G5)
24	DB12(G4)
25	DB11(G3)
26	DB10(G2)
27	DB9(G1)
28	DB8(G0)
29	DB7(B7)
30	DB6(B6)
31	DB5(B5)
32	DB4(B4)
33	DB3(B3)
34	DB2(B2)
35	DB1(B1)
36	DB0(B0)
37	NC
38	NC
39	SCL
40	CS
41	SDI
42	SDO
43	VSYNC
44	HSYNC
45	DE
46	PCLK
47	XR
48	YD
49	XL
50	YU

NOTE: Used RGB(DPI) interface

RGB Interface	DB Pin in use
16 Bit(565) RGB interface	DB0-DB4, DB8-DB13, DB16-DB20
18 Bit(666) RGB interface	DB0-DB5, DB8-DB13, DB16-DB21
24 Bit(888) RGB interface	DB0-DB7, DB8-DB15, DB16-DB23

NOTE: If used RGB mode must select serial interface!

NOTES:

1. DISPLAY TYPE: 4.3", TFT-LCD, 65K/262K/16.7M COLORS
2. DISPLAY MODE: NORMALLY BLACK
3. VIEWING DIRECTION: ALL
4. DRIVER IC: ILI9806E (COG)
5. VCI: 3.3V
6. OPERATING TEMP: -20° C TO 70° C
   STORAGE TEMP: -30° C TO 80° C
7. BACK LIGHT: LED WHITE, 8 LED, 18-20mA, 25.6V±0.3V
8. RoHS COMPLIANT.

LED(B/L) CIRCUIT

ReV	Revision content description	Date

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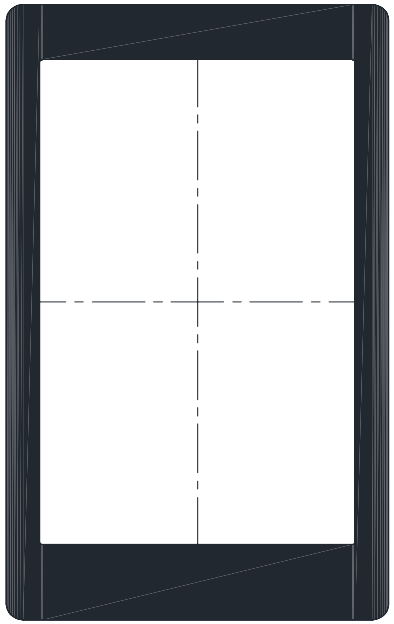
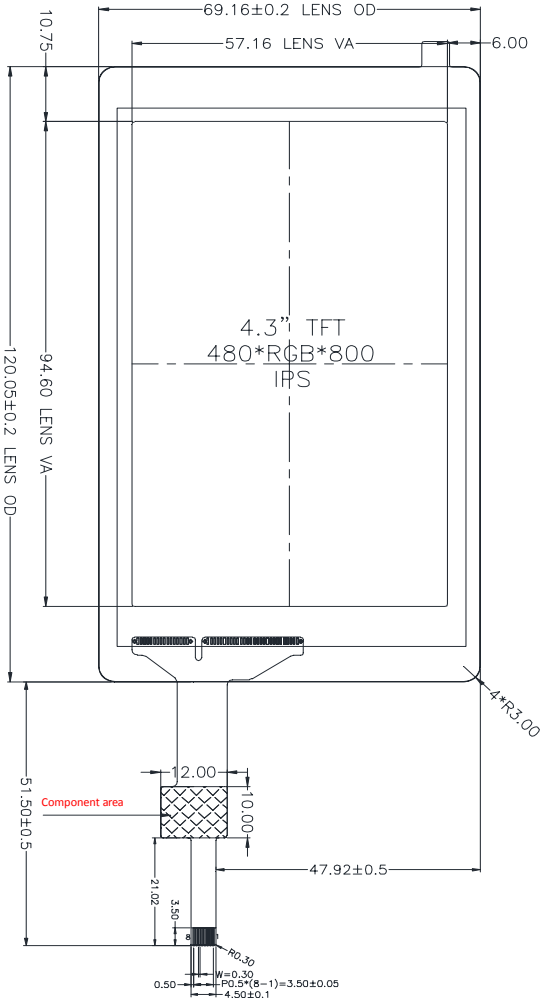
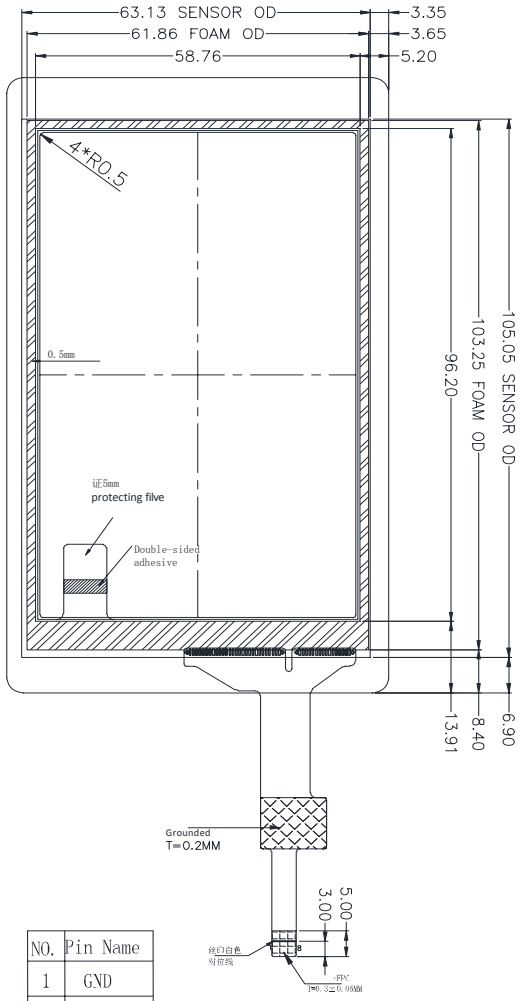
TOLERANCE( )		DRAWING NAME	E43RG54880LWAM400-C	
TOLERANCE UNLESS OTHERWISE SPECIFIED	X.X±0.3 X.XX±0.2	Drawn		Unit
Scale 1:1		Checked		mm
		Approve		Page 1/1

2.2 CTP







NOTES:
1.DRIVER IC: GT911
2.WORKING VOLTAGE: 3.3V
3.LIGHT TRANSMISSION: ≥86
4.SURFACE HARDNESS: 6H
5.OPERATING TEMP: −20℃~+70℃, ≤90%RH
6.STORAGE TEMP: −30℃~+80℃, ≤90%RH
7.UNMARKED TOLERANCE±0.2mm
8.PRECISE DIMENSION IN<>

NO.	Pin Name
1	GND
2	VDDIO
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

ReV.	Revision content description	Date
A	FIRST	2013/03/29

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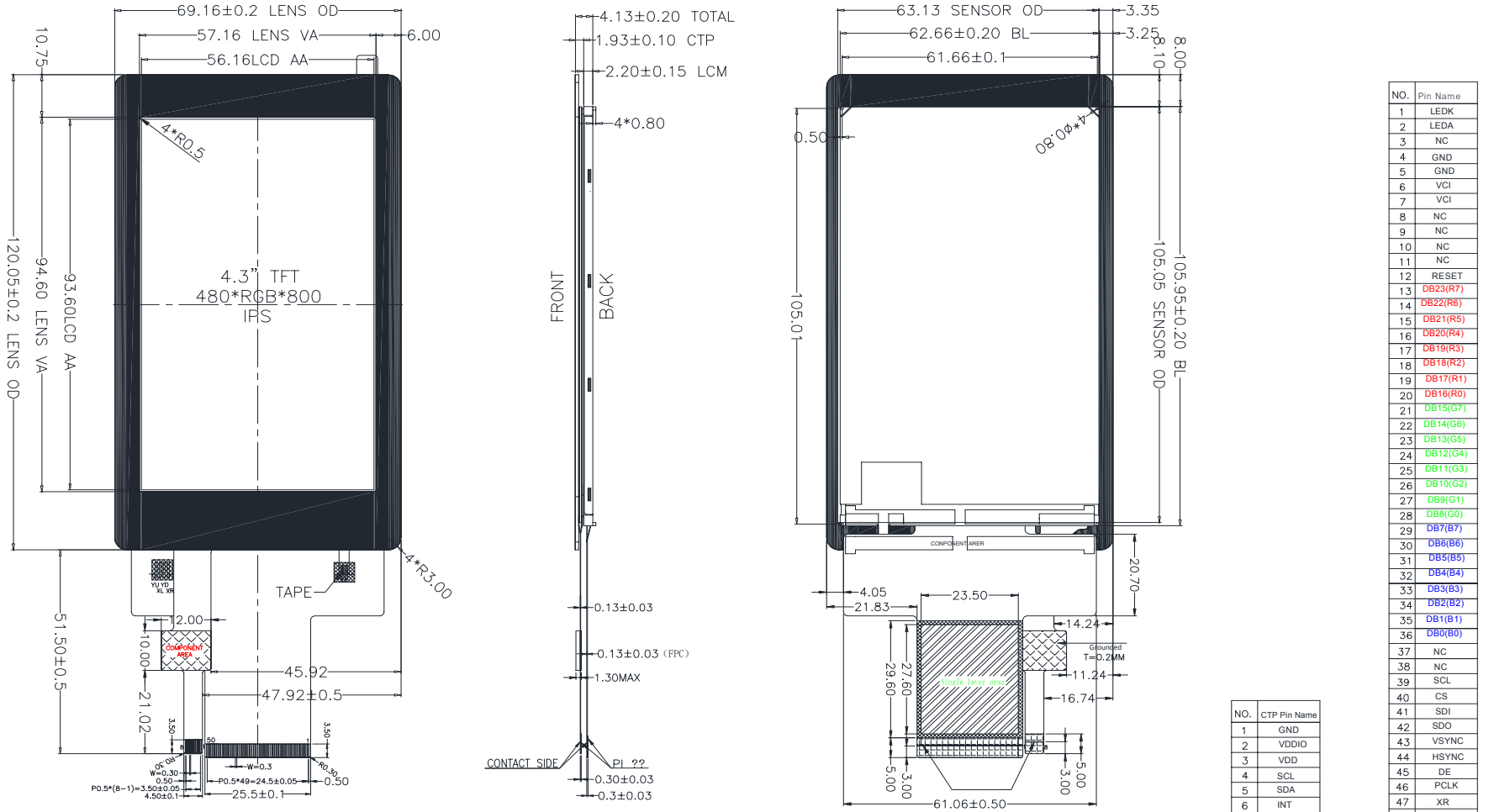
TOLERANCE		DRAWING NAME	E43RG54880LWAM400-C
TOLERANCE UNLESS OTHERWISE SPECIFIED	X.X±0.3 X.XX±0.2		Unit
Scale			Page 1/1

2.3 LCM+CTP



NO.	Pin Name
1	LEDK
2	LEDA
3	NC
4	GND
5	GND
6	VCI
7	VCI
8	NC
9	NC
10	NC
11	NC
12	RESET
13	DB23(R7)
14	DB22(R6)
15	DB21(R5)
16	DB20(R4)
17	DB19(R3)
18	DB18(R2)
19	DB17(R1)
20	DB16(R0)
21	DB15(G7)
22	DB14(G6)
23	DB13(G5)
24	DB12(G4)
25	DB11(G3)
26	DB10(G2)
27	DB9(G1)
28	DB8(G0)
29	DB7(B7)
30	DB6(B6)
31	DB5(B5)
32	DB4(B4)
33	DB3(B3)
34	DB2(B2)
35	DB1(B1)
36	DB0(B0)
37	NC
38	NC
39	SCL
40	CS
41	SDI
42	SDO
43	VSYNC
44	HSYNC
45	DE
46	PCLK
47	XR
48	YD
49	XL
50	YU

NO.	CTP Pin Name
1	GND
2	VDDIO
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

NOTES:
1. DISPLAY TYPE: 4.3", TFT-LCD, 65K/262K/16.7M COLORS
2. DISPLAY MODE: IPS NORMALLY BLACK
3. VIEWING DIRECTION: ALL
4. TFT DRIVER IC: ILI9806E (COG)
   CTP DRIVER IC: GT911
5. VCI: 3.3V(TFT)
   VDD: 3.3V(CTP)
6. CTP SURFACE HARDNESS: 6H
7. OPERATING TEMP: -20°C TO 70°C
   STORAGE TEMP: -30°C TO 80°C
8. TFT BACK LIGHT: LED WHITE, 8 LED, 20mA, 25.6±0.3V
9. RoHS COMPLIANT.

LED(B/L) CIRCUIT

NOTE: Used RGB(DPI) interface

RGB Interface	DB Pin in use
16 Bit(565) RGB interface	DB0-DB4, DB8-DB13, DB16-DB20
18 Bit(666) RGB interface	DB0-DB5, DB8-DB13, DB16-DB21
24 Bit(888) RGB interface	DB0-DB7, DB8-DB15, DB16-DB23

NOTE: If used RGB mode must select serial interface!

ReV.	Revision content description	Date
A	FIRST	2014/09/22

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TOLERANCE( )	DRAWING NAME	E43RG54880LWAM400-C
TOLERANCE UNLESS OTHERWISE SPECIFIED X.X±0.3 X.XX±0.2		Page 1/1

3. Input Terminal Pin Assignment

Recommended TFT Connector: FH12S-50S-0.5SH(55) | Recommended CTP Connector: FH12-8S-0.5SH(55)

NO.	Symbol	Description	I/O
1	LEDK	Cathode pin of backlight	P
2	LEDA	Anode pin of backlight	P
3	NC	NC	
4	GND	Ground	P
5	GND	Ground	P
6	VCI	Supply voltage (3.3V)	P
7	VCI	Supply voltage (3.3V)	P
8-11	NC	NC	
12	RESET	Reset pin. Setting low initializes the LSI. Must be reset after power is supplied.	I
13-36	DB23-DB16 (R7-R0) DB15-DB8 (G7-G0) DB7-DB0 (B7-B0)	Data bus pins. 24-bit bi-directional data bus. 8-bit bus: use DB7-DB0 9-bit bus: use DB8-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0, 24-bit bus: use DB23-DB0. When operation in MIPI DPI mode, it is an 18-bit bus RGB data bus. 24-bit bus: use DB23-DB0 16-bit bus: use DB15-DB0 18-bit bus: use DB17-DB0. If pins not used, connect to GND.	I/O
37	NC	NC	
38	NC	NC	
39	SCL	Serial clock input	I
40	CS	Chip select signal. Low: chip can be accessed, High: chip cannot be accessed	I
41	SDI	Serial data input pin for SPI. SDI: Serial data input pin, SDA: serial data input/output bi-directional pin.	I
42	SDO	Serial data output pin in serial bus system interface. If not used, leave open.	O
43	VSYNC	VS signal pin on RGB interface (input pad). If not used, connect to GND	I
44	HSYNC	Line synchronizing signal. Connect to GND or VCC if not used.	I
45	DE	Data enable signal for DPI I/F mode. If not used, connect to GND	I
46	PCLK	Dot clock signal. Connect to GND if not used	I
47	XR(NC)	NC	A/D
48	YD(NC)	NC	A/D
49	XL(NC)	NC	A/D
50	YU(NC)	NC	A/D

3.1 CTP

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	VDDIO	I/O power supply voltage	P
3	VDD	Supply voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host	I
7	RST	External reset. Low is active	I
8	GND	Ground	P

4. LCD Optical Characteristics

4.1 Optical Specifications

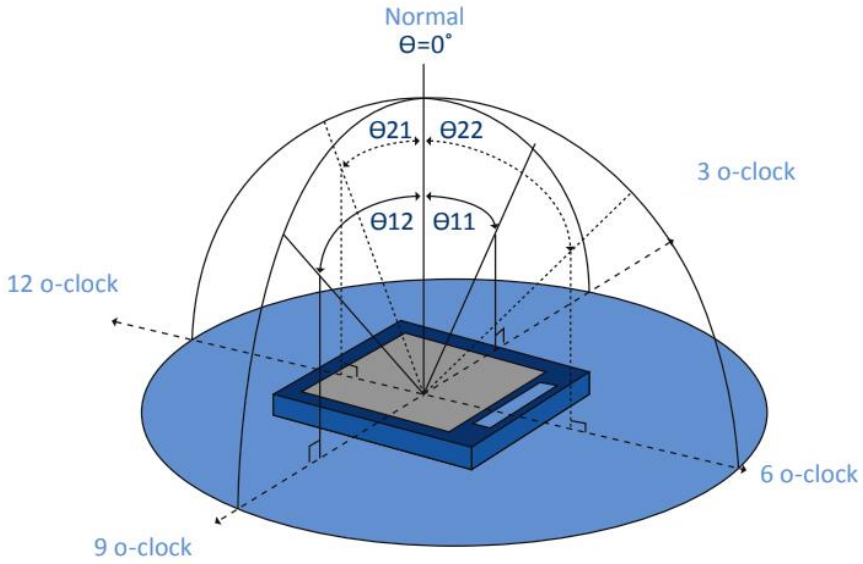
Item		Symbol	Condition	Min	Typ.	Max	Unit.	Note
Threshold Voltage		Vsat	Θ=0	3.4	3.6	3.8	V	
		Vth	Normal	1.5	4.6	--	V	
Transmittance		T(%)	viewing	4.1	4.5	--	%	(3)
Response time	Rising	TR	angle	--	16	20	msec	(4)
	Falling	TF		--	14	20		
Contrast Ratio		Cr		--	800	--	%	(2)
Color Filter Chromaticity	White	Wu'		--	0.192	--		(1)(5)
		Wv'		--	0.468	--		
	Red	Ru'		0.444	0.459	0.474		
		Rv'		0.516	0.526	0.536		
	Green	Gu'		0.111	0.120	0.129		
		Gv'		0.544	0.550	0.556		
	Blue	Bu'		0.121	0.136	0.151		
		Bv'		0.216	0.246	0.276		
Viewing angle	Hor.	ΘL	CR>10	--	80	--		(1)(6)
		ΘR		--	80	--		
	Ver.	ΘU		--	80	--		
		ΘD		--	80	--		
Option View Direction		FREE						(1)(6)

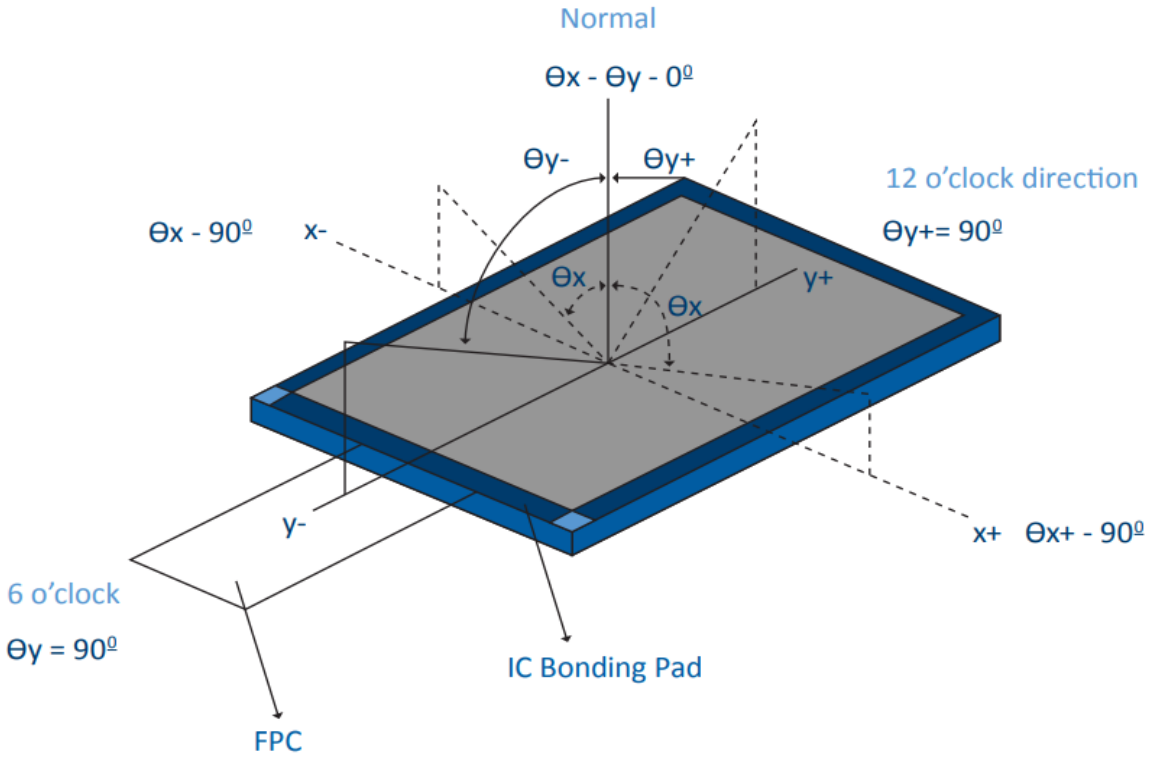
4.2 Measuring Condition

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25℃. The values are at an approximate distance 50 cm from the TFT-LCD surface at a viewing angle of Φ and Θ equal to 0°.

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

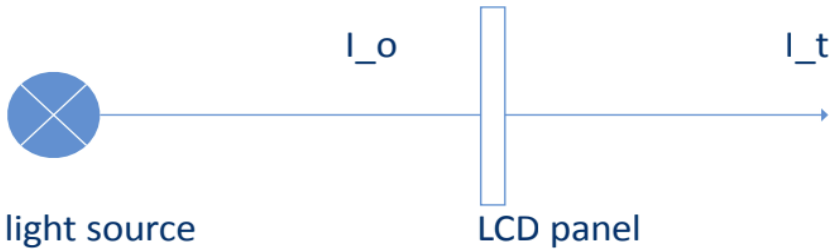




(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

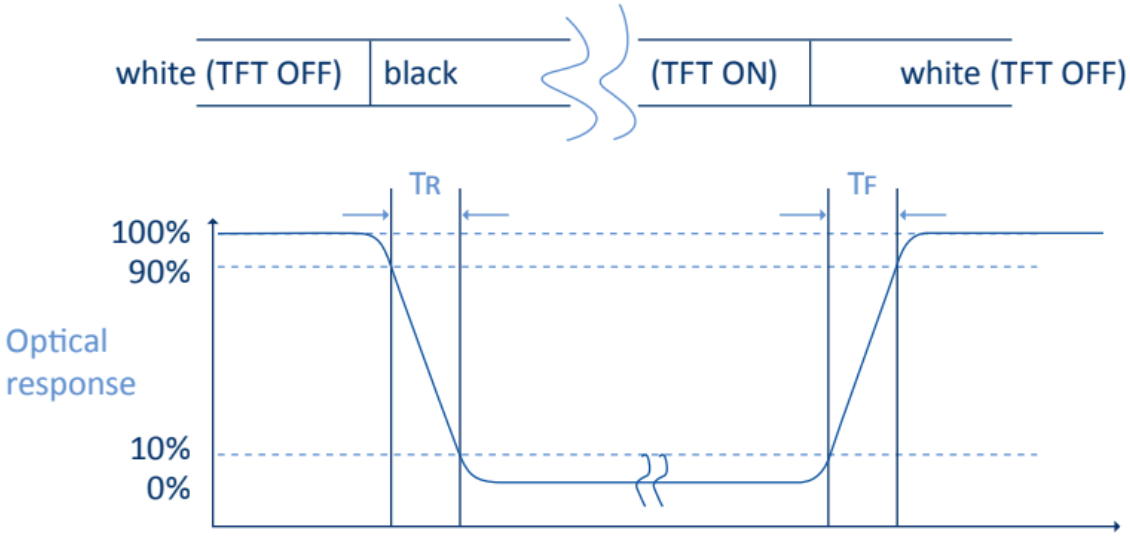


The transmittance is defined as:

$$Tr = \frac{It}{Io}\ x\ 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

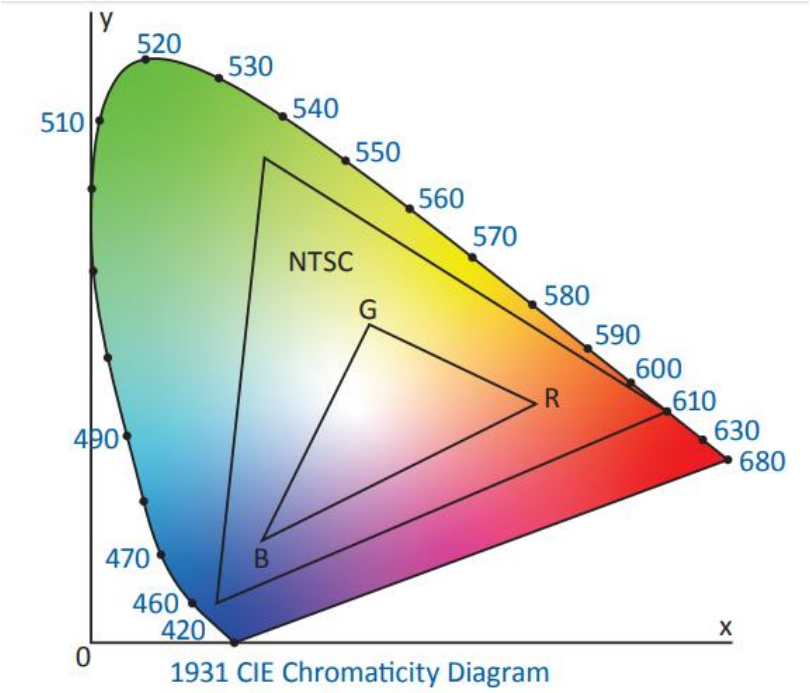
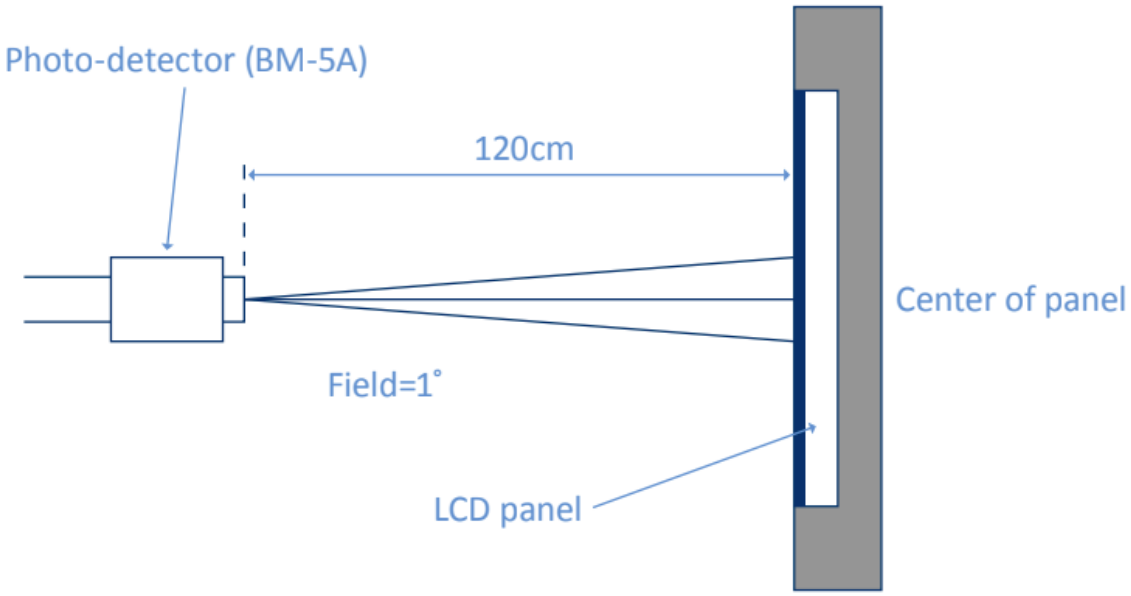


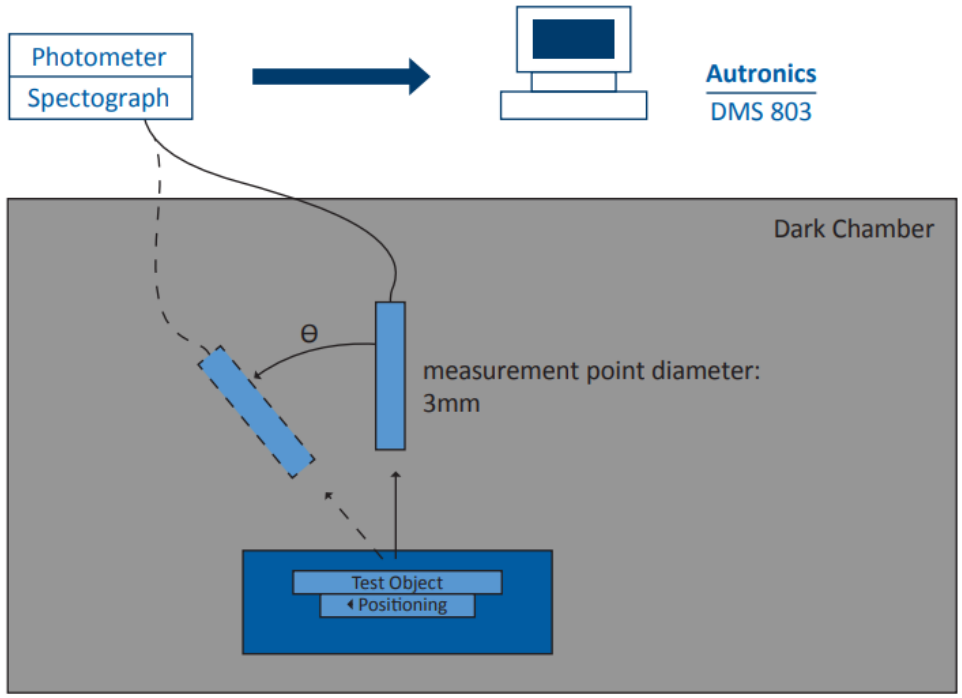
Fig. 1931 CIE chromacity diagram

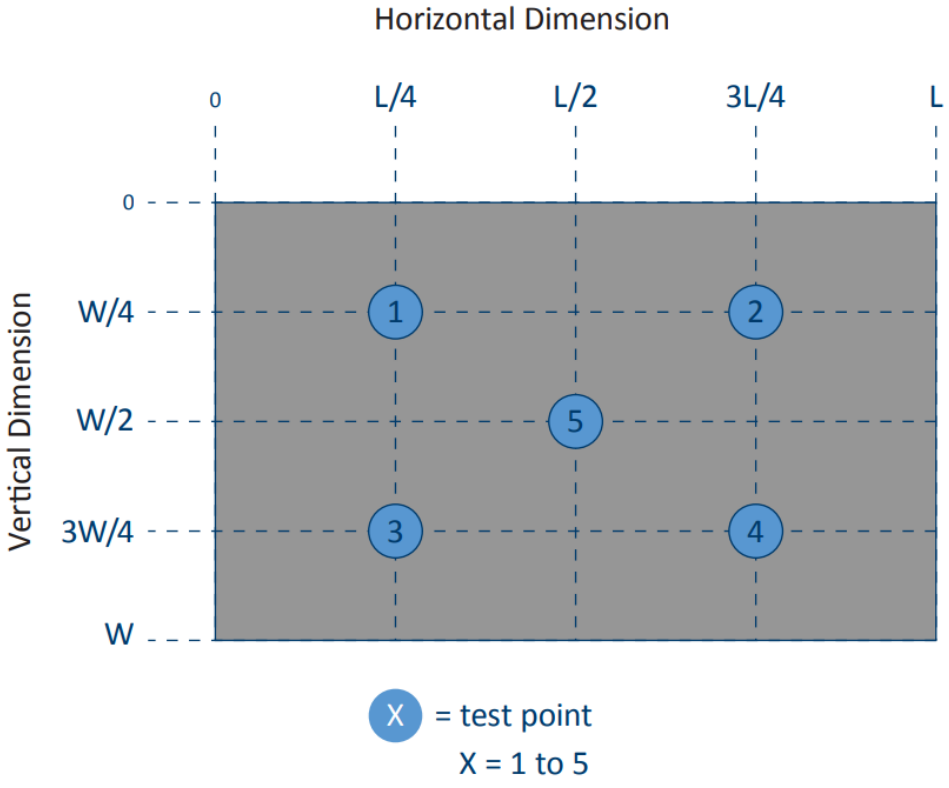
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	-0.3	4.6	V
Digital Interface Supply Voltage	VDDIO	-0.3	4.6	
Operating temperature	TOP	-20	+70	℃
Storage temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VDD	2.5	3.3	3.6	V	
Digital Interface Supply Voltage	VDDIO	1.65	3.3	3.6		
Normal Mode Current Consumption	IDD	--	30	--	mA	
Level input voltage	VIH	0.7 VDDIO		VDDIO	V	
	VIL	GND		0.3 VDDIO	V	
Level output voltage	VOH	VDDIO-0.4		--	V	
	VOL	GND		GND	V	

5.3 LED Backlight Characteristics

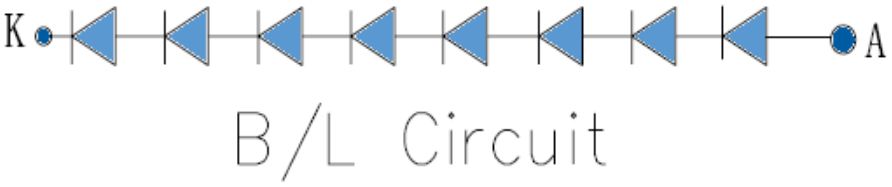
Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	15	20	--	mA	
Forward Voltage	VF	--	25.6	--	V	
LCM Luminance	LV	400	--	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	AVg	80	--	--	%	Note 3

The back-light system is edge-lighting type with 8 chips White LED

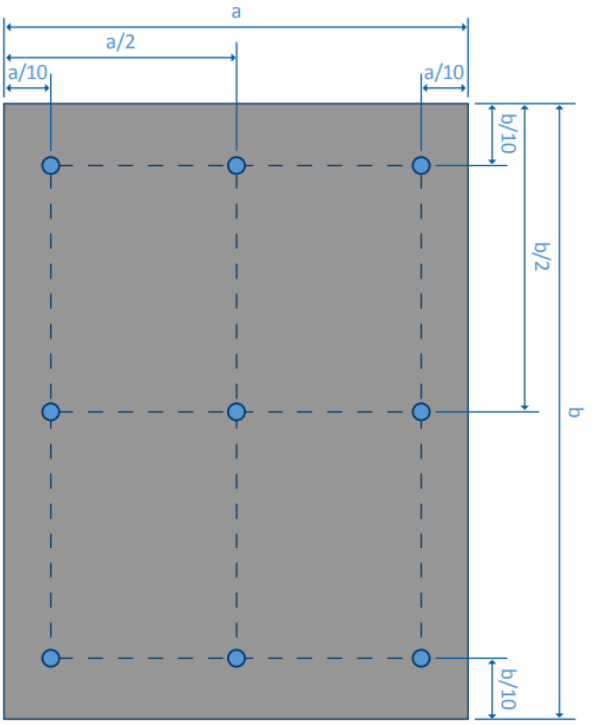
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition:

Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. AC Characteristic

6.1 Parallel 24/18/16-bit RGB Interface Timing Characteristics

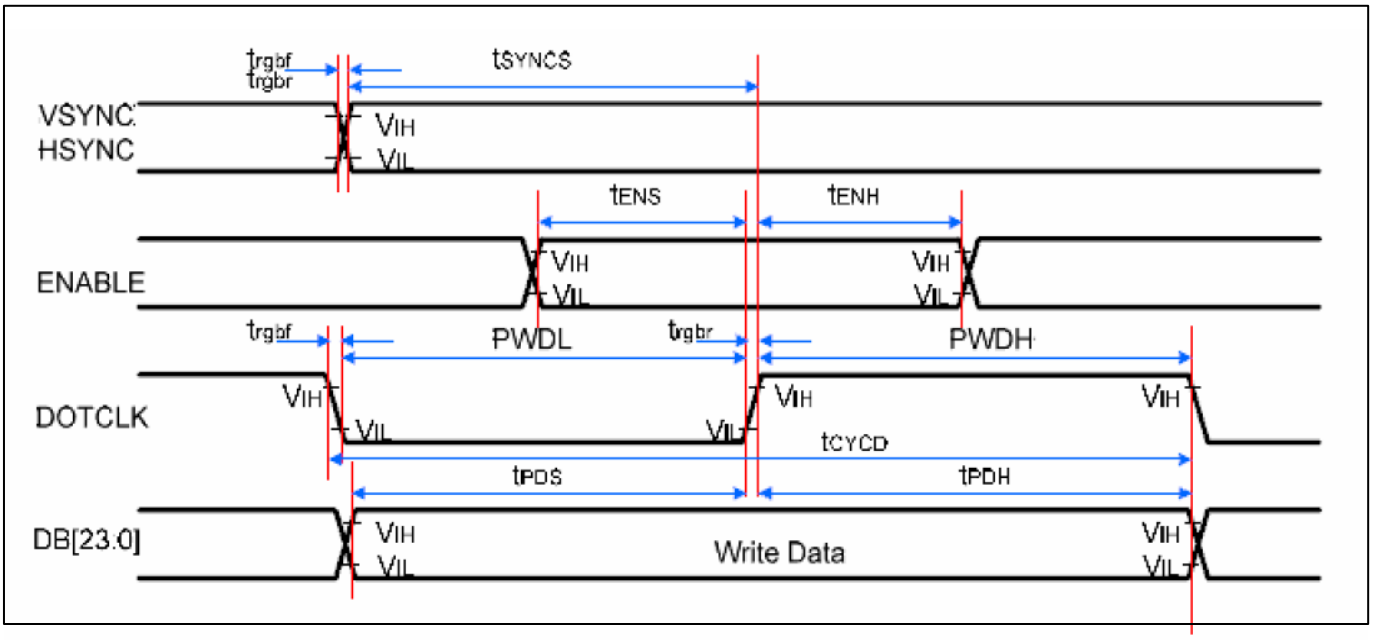


Figure 6.1: 24/18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	Min	Max	Unit	Description
HSYNC/ VSYNC	TSYNCS	VSYNC/HSYNC Setup Time	5	-	ns	16/18/24-bit bus RGB interface mode
	TSYNCH	VSYNC/HSYNC Hold Time	5	-	ns	
ENABLE	TENS	Enable Setup Time	5	-	ns	
	TENH	Enable Hold Time	5	-	ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	13	-	ns	
	PWDL	DOTCLK Low-level Pulse Width	13	-	ns	
	TCYCD	DOTCLK Cycle Time	28	-	ns	
	Trghr, Trghf	DOTCLK Rise/Fall Time	-	15	ns	
DB[23:0]	TPDS	PD Data Setup Time	5	-	ns	
	TPDH	PD Data Hold Time	5	-	ns	

Table 6.1: 24/18/16 Bits RGB Interface Timing Characteristics

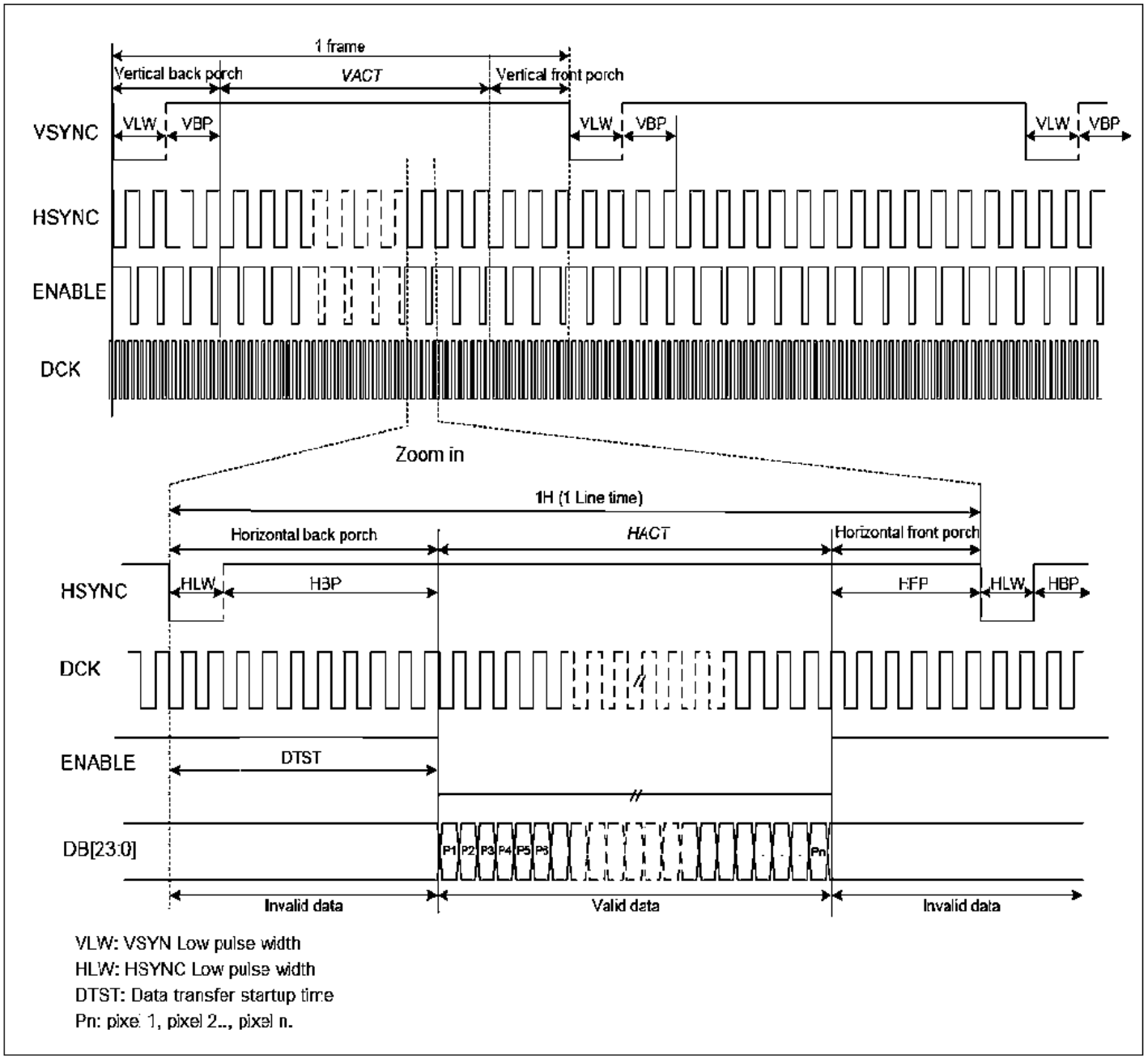


Figure 6.2: Clock and Data Input Timing Characteristics

Parameter	Symbols	Condition	Min	Typ.	Max	Units
Frame rate	FR			54	66	fps
Horizontal low pulse width	HLW			1		DOTCLK
Horizontal back porch	HBP			2	126	DOTCLK
Horizontal address	HACT					DOTCLK
Horizontal front porch	HFP			2		DOTCLK
Vertical low pulse width	VLW			1	126	Line
Vertical back porch	VBP			1	126	Line
Vertical address	VACT				864	Line
Vertical front porch	VFP			1	255	Line
Data clock	DCLK			16.6	41.7	MHz

Table 6.2: 24/18/16 Bits RGB Input Timing Characteristics

6.2 Display Serial Interface Characteristics (3-line SPI system)

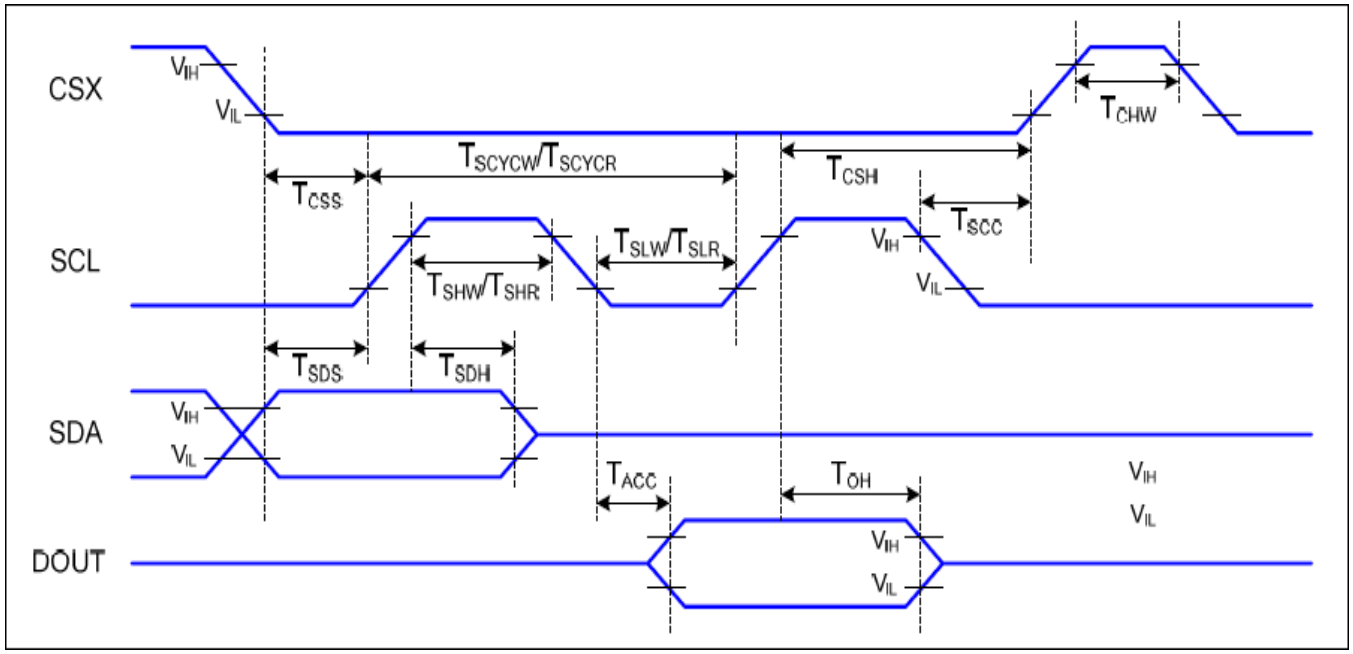


Figure 6.3: 3-line Serial Interface Timing Characteristics

VDDI = 1.64 to 3.3V, VDD = 2.4 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 C°

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setupt time (write)	15		ns	
	T_{CSH}	Chip select hold time (write)	15		ns	
	T_{CSS}	Chip select setup time (read)	15		ns	
	T_{SCC}	Chip select hold time (read)	15		ns	
	T_{CHW}	Chip select "H" pulse width	40		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	30		ns	
	T_{SHW}	SCL "H" pulse width (write)	10		ns	
	T_{SLW}	SCL "L" width (write)	10		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL "H" pulse width (read)	60		ns	
	T_{SLR}	SCL "L" pulse width (read)	60		ns	
SDA/SDI (Input)	T_{SDS}	Data setup time (write)	10		ns	
	T_{SDH}	Data hold time (Write)	10			
SDA/SDO (Output)	T_{ACC}	Access time (read)	10	100	ns	For max CL=30pF
	T_{OH}	Output disable time (read)	15	100	ns	For min CL=8pF

Table 6.3: 3-line Serial Timing Characteristics

Note: The rising time and falling time (Tr, Tf) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals

6.3 Reset Timing

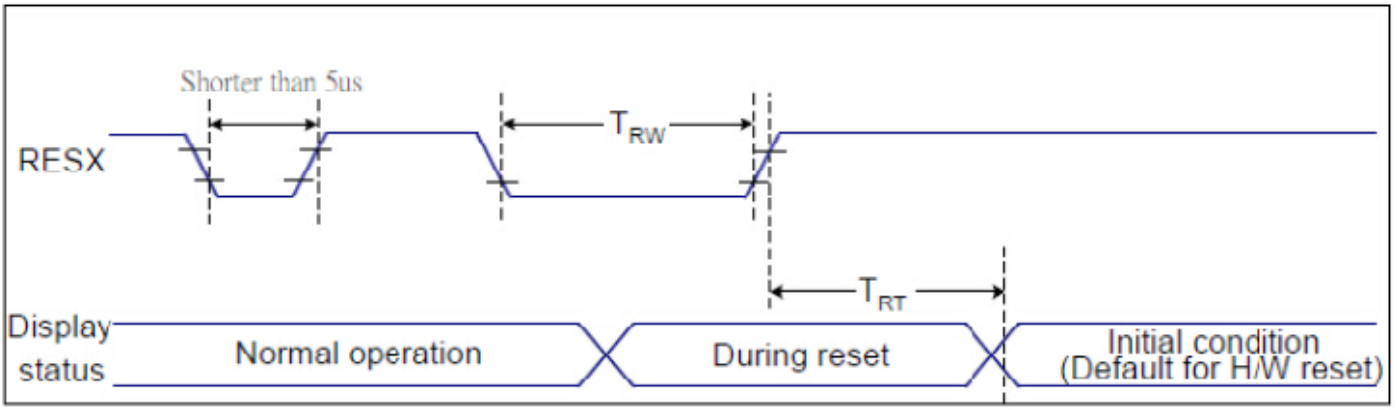


Figure 6.4: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

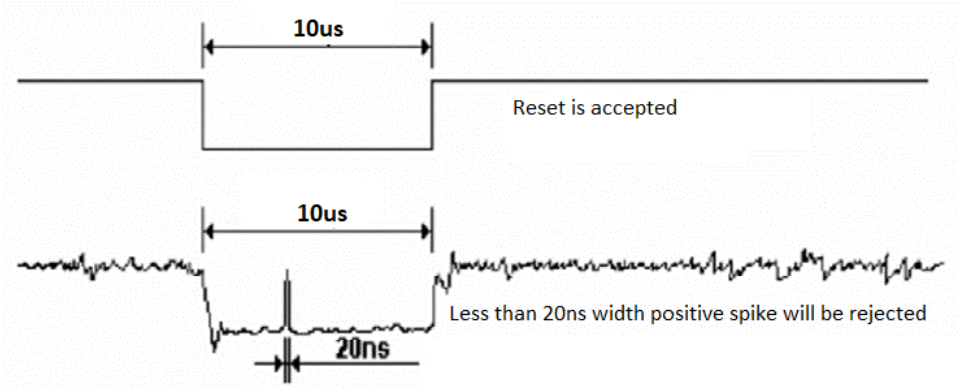
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. CTP Specification

7.1 Electrical Characteristics

7.1.1 Absolute Maximum Rating

Item	Symbol	Min	Max	Unit	Note
Power Supply Voltage	VDD	-0.3	3.47	V	1
I/O Digital Voltage	VDDIO	1.8	3.47	V	1
Operating Temperature	T	-20	+70	℃	-
Storage Temperature	T_{ST}	-30	+80	℃	-

Note: If used beyond the absolute maximum ratings, GT911 may permanently damage. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.

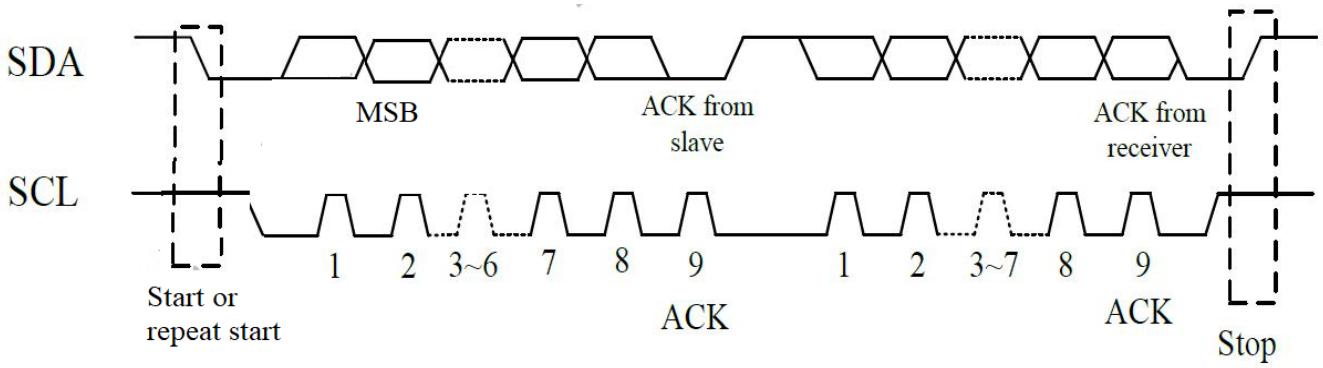
7.1.2 DC Electrical Characteristics (Ta=25℃)

Item	Symbol	Condition	Min	Typ.	Max	Unit	Note
Digital supply voltage	VDD		2.8		3.3	V	
I/O Digital supply voltage	VDDIO		1.8		3.3	V	
Normal operation mode current consumption	I_{OPr}	VDD=2.8V Ta=25℃ MCLK=17.5 MHz		8	14.5	mA	
Monitor mode current consumption	I_{mon}			3.3		mA	
Sleep mode current consumption	I_{sip}		70		120	uA	
Level input voltage	V_{IH}		0.75VDDIO		VDDIO+0.3	V	
	V_{IL}		-0.3		0.25VDDIO	V	
Level output voltage	V_{OH}	I_{OH}=-0.1mA	0.85VDDIO			V	
	V_{OL}	I_{OL}=0.1mA			0.15VDDIO	V	

7.2 AC Characteristics

7.2.1 I2C Interface Characteristics

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is recommended that transmission rate be kept at or below 400kbps. The figure shown below is the I2C timing:



Parameter	Symbols	Condition	Min	Max	Units
SCL low period	t_{lo}		1.3		us
SCL high period	t_{hi}		0.6		us
SCL setup time for start condition	t_{st1}		0.6		us
SCL setup time for stop condition	t_{st3}		0.6		us
SCL hold time for start condition	t_{hd1}		0.6		us
SDA setup time	t_{st2}		0.1		us
SDA hold time	t_{hd2}		0		us

Table 7.1: I2C AC Characteristics, 1.8V interface voltage, 400kbps transmission rate, 2k pull-up resistor

Parameter	Symbols	Condition	Min	Max	Units
SCL low period	t_{lo}		1.3		us
SCL high period	t_{hi}		0.6		us
SCL setup time for start condition	t_{st1}		0.6		us
SCL setup time for stop condition	t_{st3}		0.6		us
SCL hold time for start condition	t_{hd1}		0.6		us
SDA setup time	t_{st2}		0.1		us
SDA hold time	t_{hd2}		0		us

Table 7.2: I2C AC Characteristics, 3.3V interface voltage, 400kbps transmission rate, 2k pull-up resistor.

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. The configuration methods and timings are shown below:

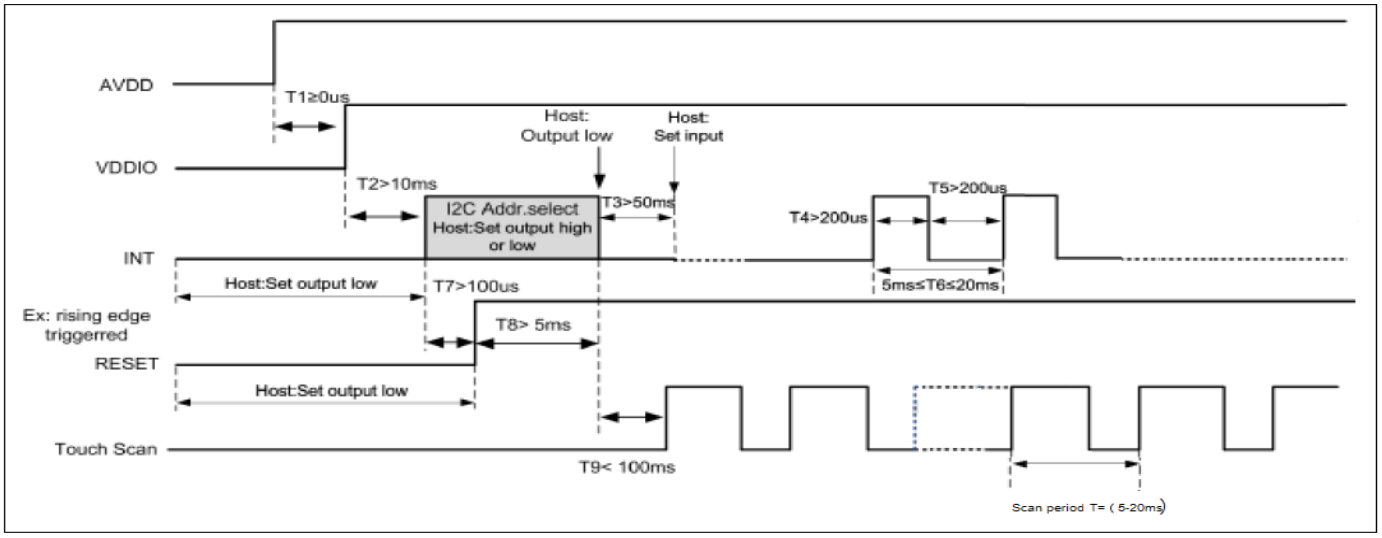


Figure 7.1: I2C Power on Timing

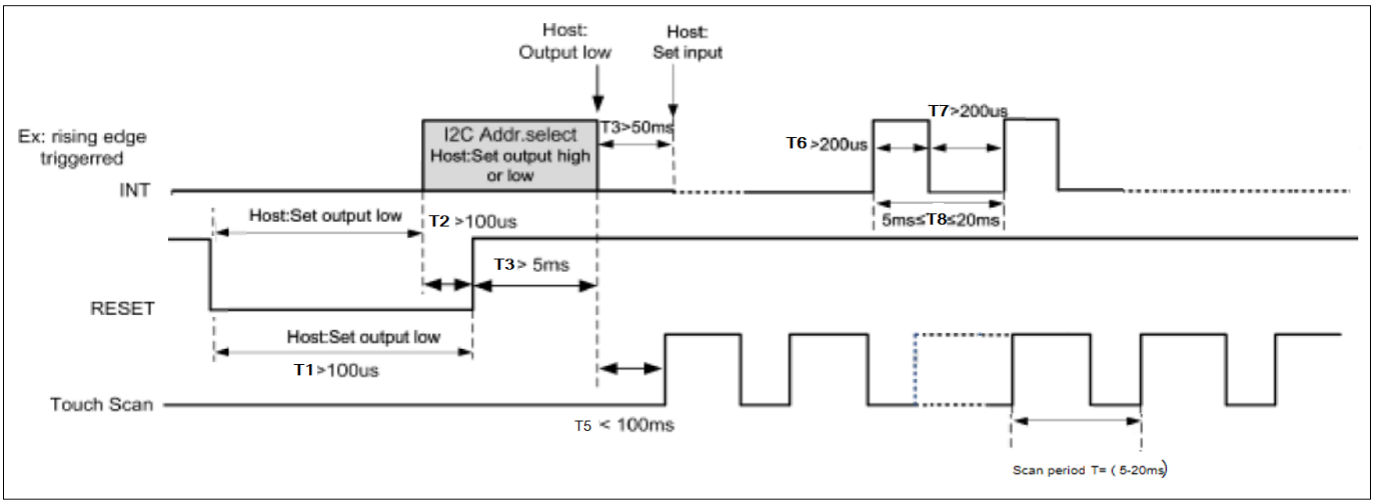


Figure 7.2: I2C Host Resetting Timing

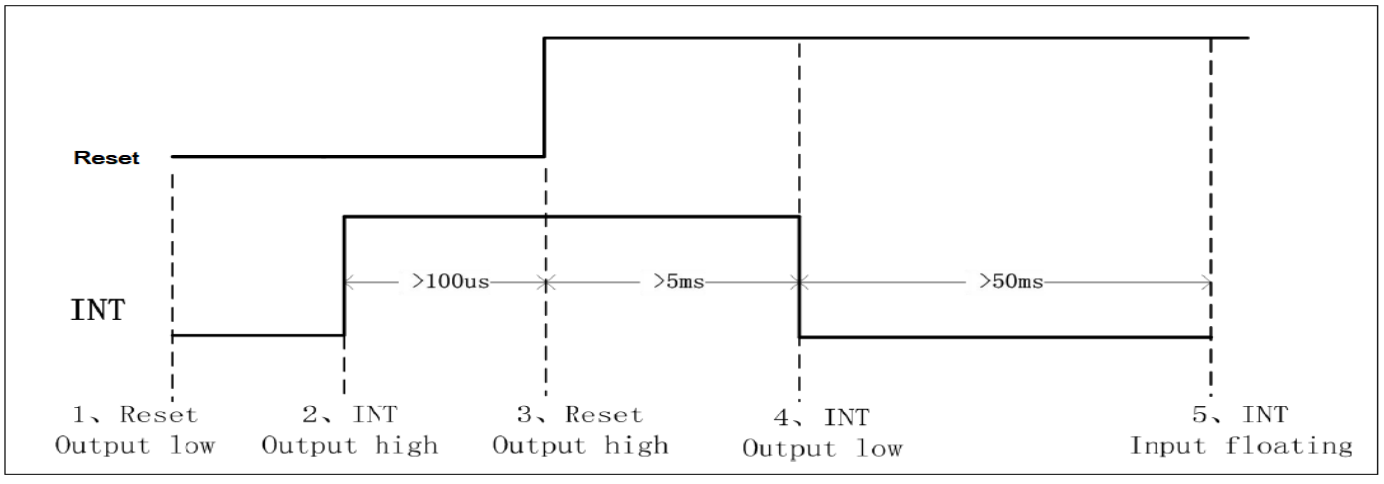


Figure 7.3: Setting Slave Address to 0x28/0x29 Timing

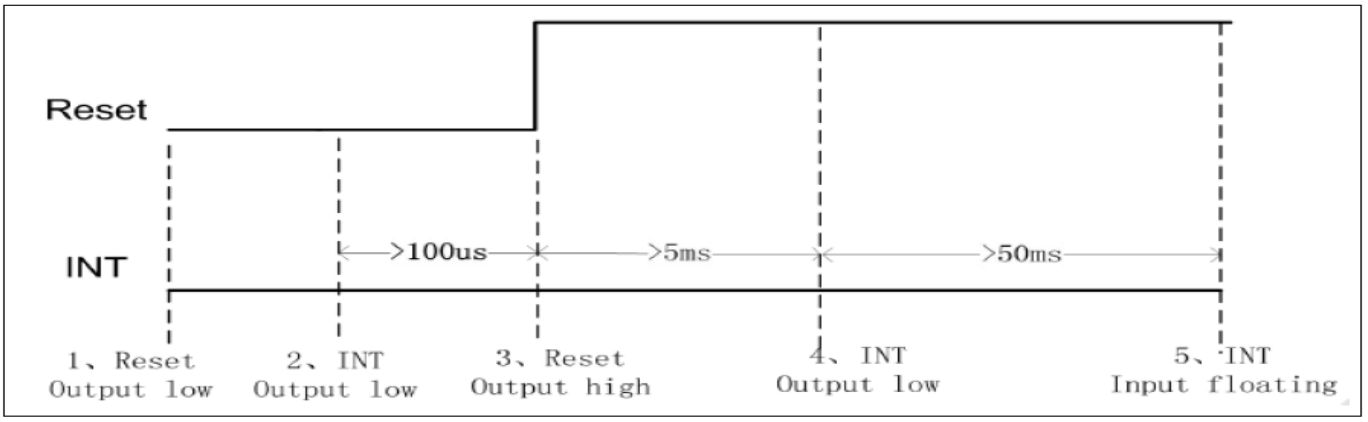


Figure 7.4: Setting Slave Address to 0xBA/0xBB Timing

Data Transmission

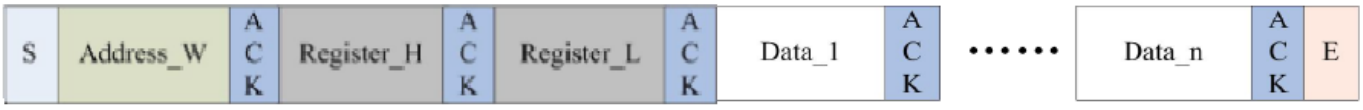
Communication is always initiated by the host. Valid start condition is signaled by pulling SDA line from high to low when SCL is high. Data flow or address is transmitted after the start condition.

All slave devices connected to I2C bus should detect the 8-bit address issued after start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely not 0xBA or 0xBB, GT911 will stay in an idle state.

For data bytes on SDA, each of the 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is high. When communication is completed the host will issue the stop condition. Stop condition implies the transition of SDA line from low to high when SCL is high.

Writing Data to GT911

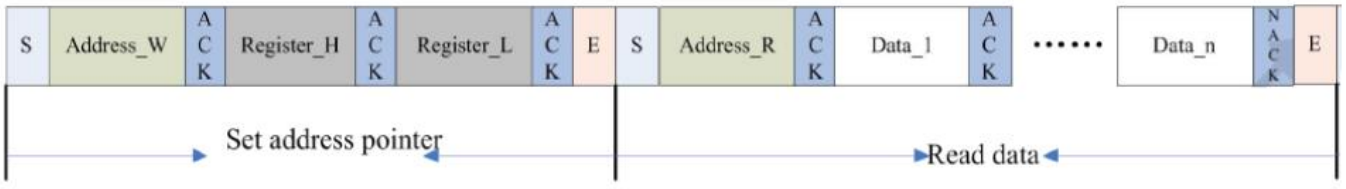
The diagram displays the timing sequence of the host writing data onto GT911. First the host issues a start condition. The host sends 0xBA (address bits and R/W bit; R/W bit as 0 indicates write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register)



The location of the register address pointer will automatically add 1 every write operation. When the host needs to perform write operations on a group of registers of continuous addresses it can write continuously. The write operation is terminated when the host issues the stop condition.

Reading Data from GT911

The diagram below is the timing sequence of the host reading data from GT911. The host issues the start condition and sends 0xBA (Address bits and R/W bit, R/W bit as 0 indicates write operation) to the slave device. After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.



The host issues the start condition once again and sends 0xBB (read operation). After receiving ACK, the host starts to read the data. GT911 also supports continuous read operation. When receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

8. Cautions and Handling Precautions

8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.