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TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

TFT Display Module

Part Number

E24RF-I-MS800-N

Overview:

- 2.4-inch TFT (42.92x60.26mm)
- MIPI DSI Interface
- 480x640 pixels
- All Viewing Angle
- White LED back-light
- Transmissive/ Normally Black
- No Touch Panel
- 800 NITS
- Controller: ST7701SI
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT LCD Panel, driver circuit and a backlight unit. The resolution of the 2.41" TFT LCD contains 480(RGB)x640 pixels and can display up to 16.7M colors.

TFT Features

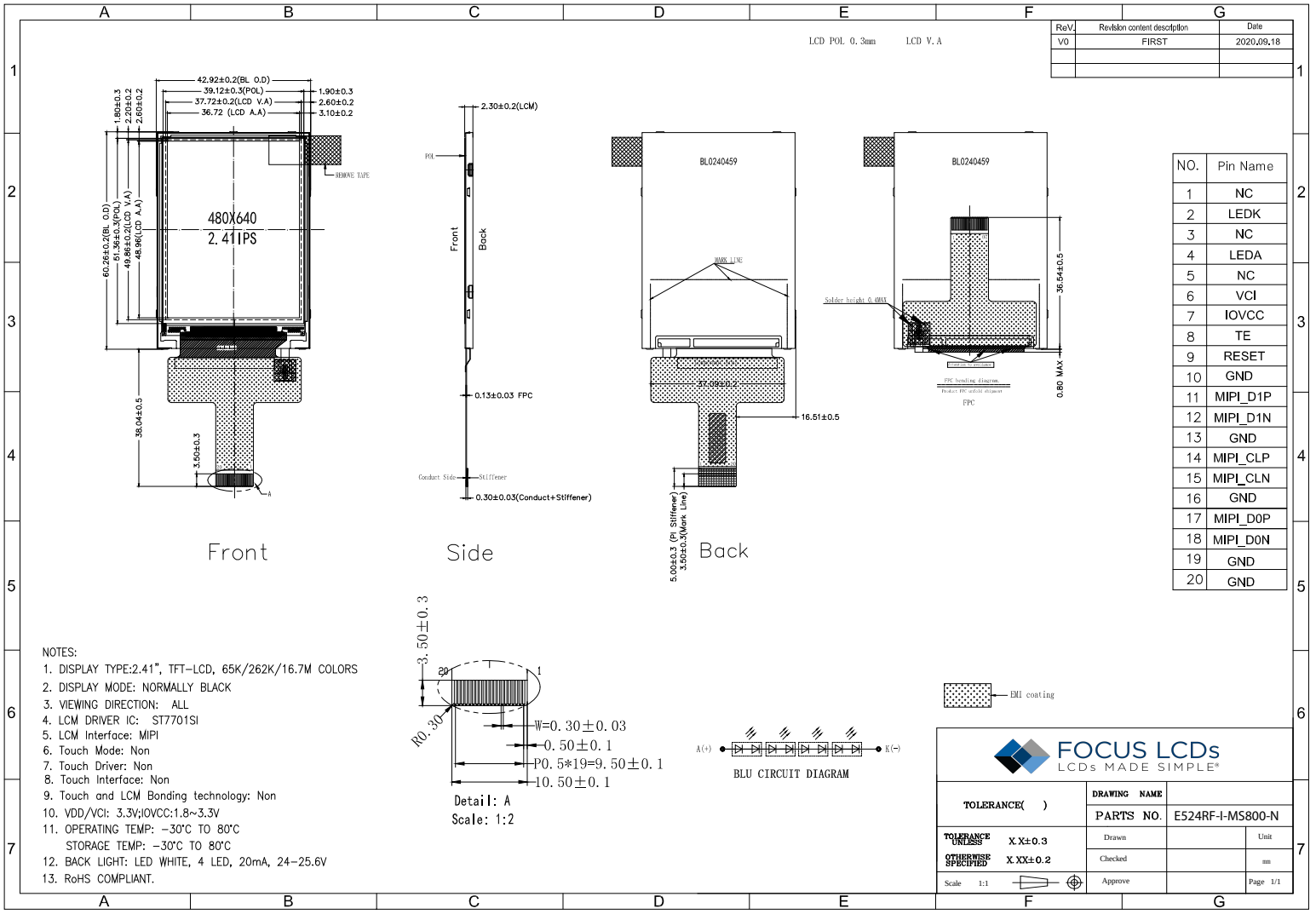
Low Input Voltage: 3.3V
Display Colors: 16.7M
TFT Interface: MIPI

General Information Items	Specification Main Panel	Unit	Note
TFT Display area (AA)	36.72(H) x 48.96(V) (2.41 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	16.7M	colors	-
Number of pixels	480(RGB) x 640	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel Pitch	0.0765(H) x 0.0765(V)	mm	-
Viewing angle	All	o'clock	-
Display mode	Transmissive, Normally Black	-	-
TFT Controller	ST7701SI	-	-
Operating temperature	-30-+80	℃	-
Storage temperature	-30-+80	℃	-

Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal (H)		42.92		mm	-
	Vertical (V)		60.26		mm	-
	Depth (D)		2.3		mm	-
	Weight		50		g	

1. Outline Dimensions



2. Input Terminal Pin Assignment

2.1 TFT

NO.	Symbol	Description	I/O
1	NC	--	--
2	LEDK	Cathode pin of the backlight	P
3	NC	--	--
4	LEDA	Anode pin of the backlight	P
5	NC	--	--
6	VCI	Supply voltage (3.3V)	P
7	IOVCC	I/O power supply voltage	P
8	TE	Tearing effect output. Leave pin open when not in use.	O
9	RESET	Reset signal of the device. Initializes the chip with a low input. Must be implemented to properly initialize the chip at power up.	I
10	GND	Ground	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-)	I/O
12	MIPI_D1N		I/O
13	GND	Ground	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-)	I
15	MIPI_CLN		I
16	GND	Ground	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-)	I/O
18	MIPI_D0N		I/O
19	GND	Ground	P
20	GND	Ground	P

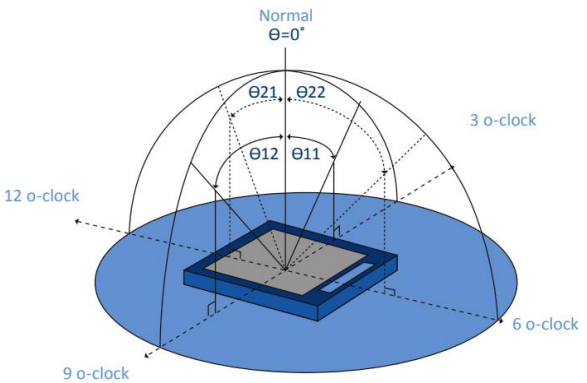
3. LCD Optical Characteristics

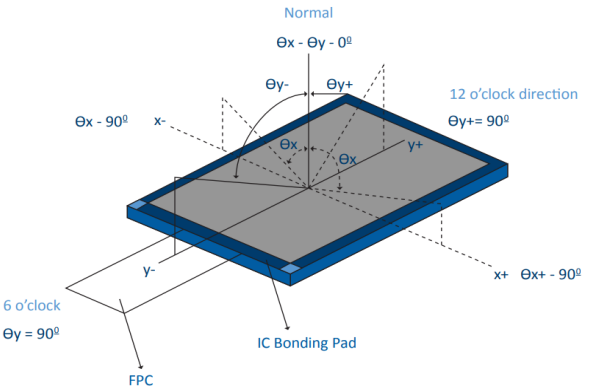
3.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Color Gamut		S	Normal viewing angle θ=0	50	55	--	%	(3)
Contrast Ratio		CR		800	1000	--	%	(2)
Response Time	Rising	TR		--	--	35	ms	(4)
	Falling	TF						
Color Filter Chromaticity	White	W_X		0.262	0.302	0.342		(5)(6)
		W_Y		0.285	0.325	0.365		
	Red	R_X		0.569	0.609	0.649		
		R_Y		0.312	0.352	0.392		
	Green	G_X		0.288	0.328	0.368		
		G_Y		0.540	0.580	0.620		
	Blue	B_X		0.114	0.154	0.194		
		B_Y		0.041	0.081	0.121		
Viewing Angle	Hor.	ΘL	CR≥10	70	80	--	degrees	(1)(6)
		ΘR		70	80	--		
	Ver.	ΘT		70	80	--		
		ΘB		70	80	--		
Option View Direction		All						(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.



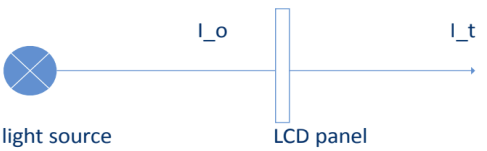


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

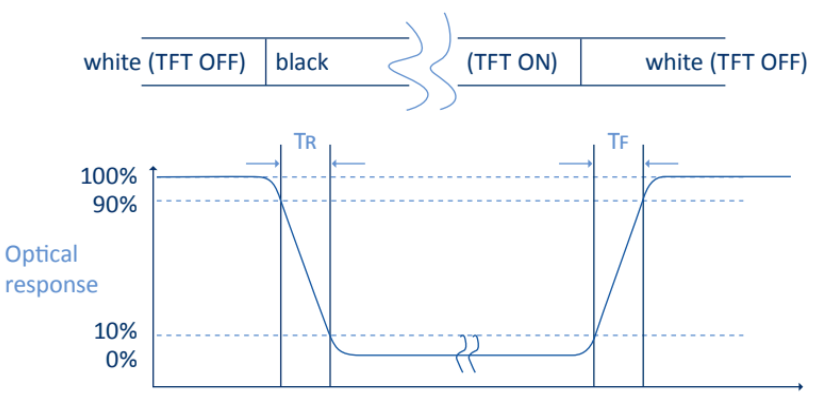
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io} x\ 100\%$$



Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90%to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:
Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

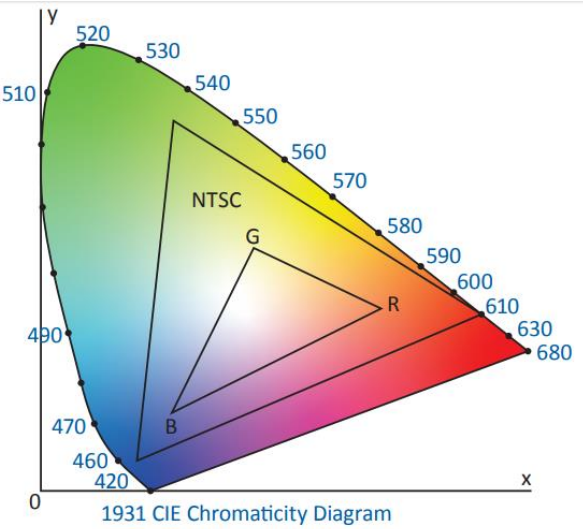
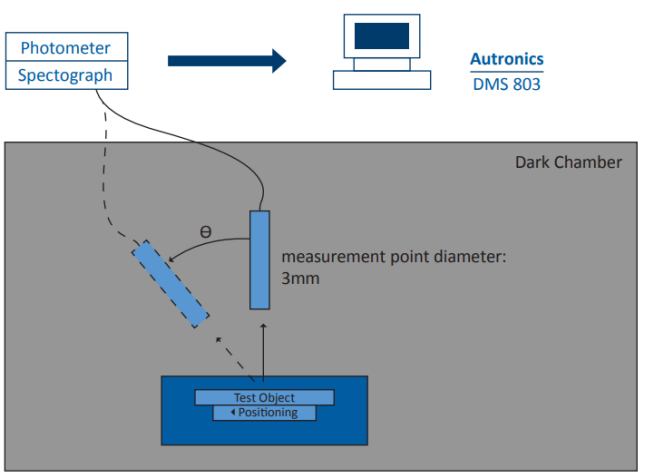


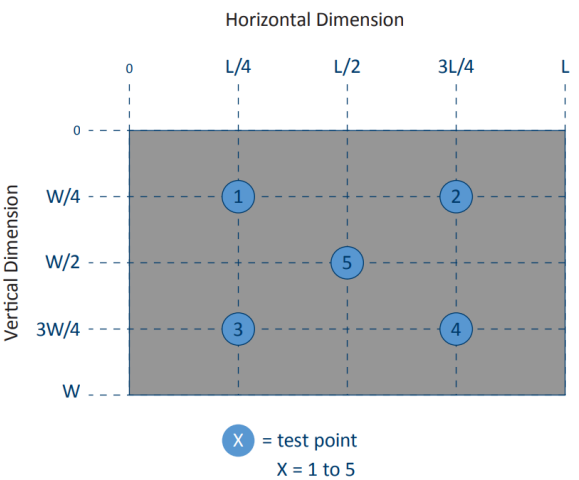
Fig. 1931 CIE chromacity diagram

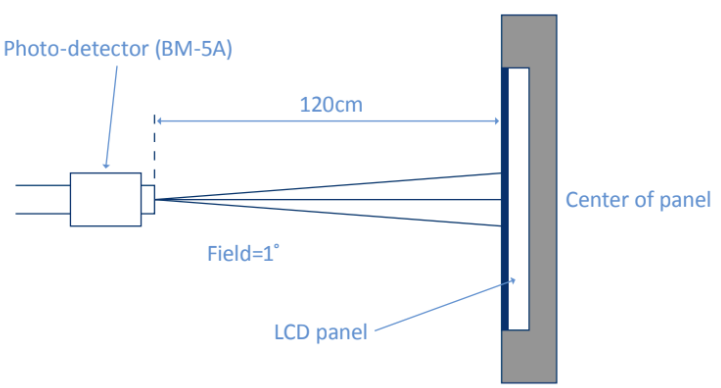
Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.







4. TFT Electrical Characteristics

4.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
I/O Supply Voltage	IOVCC	-0.3	4.6	V
Operating Temperature	TOP	-30	+80	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

4.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Digital Supply Voltage	VDD	2.5	3.3	3.6	V	
I/O Interface Voltage	IOVCC	1.65	1.8	3.3	V	
Normal Mode Current	IDD	--	20	40	mA	
Differential Input High Threshold Voltage	VIT+	--	0	50	mV	MIPI_CLK MIPI_Data
Differential Input Low Threshold Voltage	VIT-	-50	0	--	mV	
Single-ended Receiver Input Operation Voltage Range	VIR	0.5	--	1.2	V	

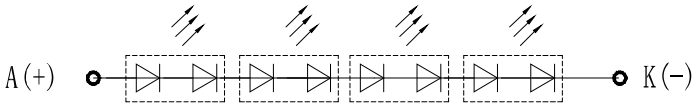
4.3 LED Backlight Characteristics

The backlight system is edge lighting type with 4 White LED chips.

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	I_F	--	20	--	mA	
Forward Voltage	V_F	--	24	25.6	V	
LCM Luminance	LV	750	800	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	Avg	80	--	--	%	Note 3

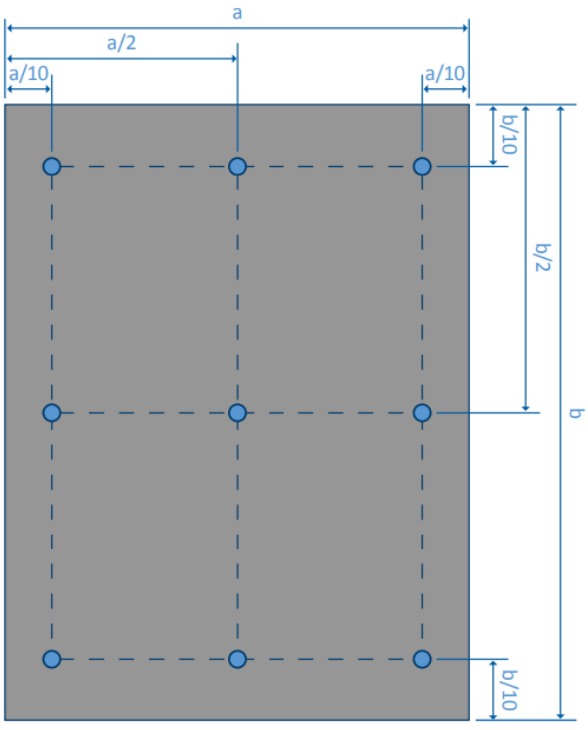
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL = 20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



BLU CIRCUIT DIAGRAM

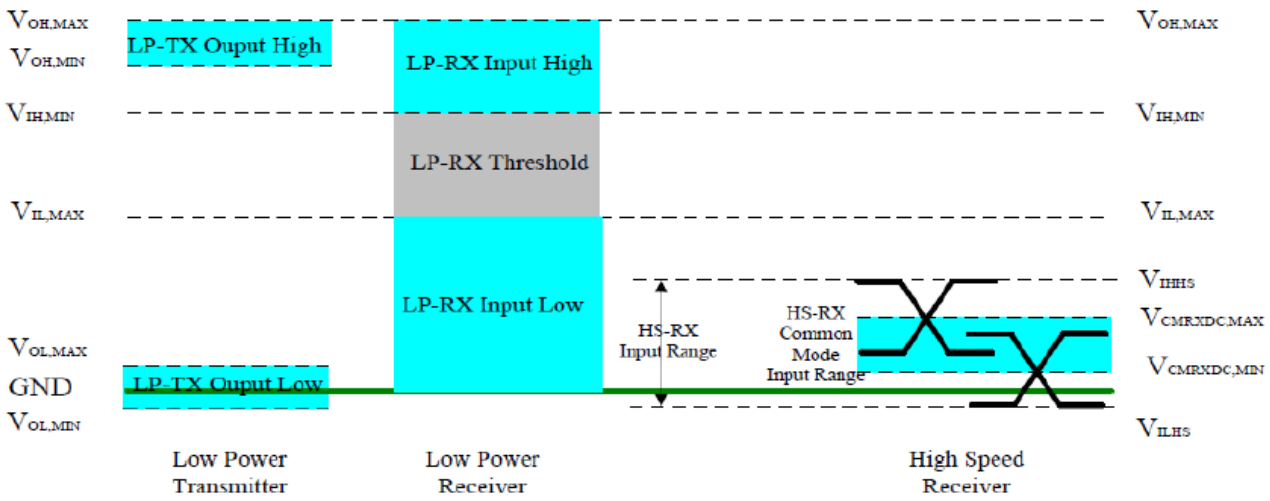
Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

4.4 MIPI DC Electrical Characteristics



Characteristics	Symbol	Min	Typ.	Max	Unit
Operation Voltage for MIPI Reciever					
Low power mode operation volage	VLPH	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage	VILHS	-40	-	-	mV
Single-ended input high voltage	VIHHS	-	-	460	mV
Common-mode voltage	VCMRXDC	70	-	330	mV
Differential input impedance		80	100	125	ohm
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-50	-	1350	mV
Logic 0 input threshold	VIL	0	-	550	mV
Logic 1 input threshold	VIH	880	-	1350	mV
Output low level	VOL	-50	-	50	mV
Output high level	VOH	1.1	1.2	1.3	V

5. MIPI Interface AC Characteristics

5.1 High Speed Mode

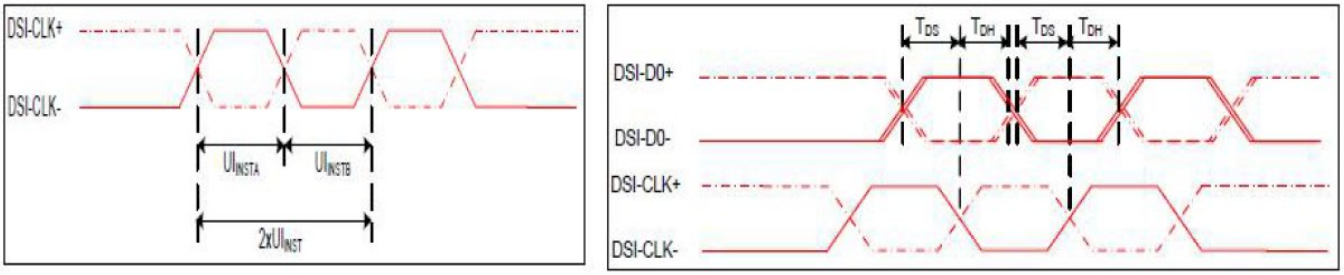


Figure 5.1: DSI Clock Channel Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
DSI-CLK+/-	2xUIINSTA	Double UI Instantaneous	4	25	ns	
DSI-CLK+/-	UIINSTA UIINSTB	UI Instantaneous Halves	2	12.5	ns	UI=UIINSTA=UIINSTB
DSI-Dn+/-	tDS	Data to clock setup time	0.15	--	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	--	UI	

Table 5.1: MIPI Interface High Speed Mode Timing Characteristics

5.2 Low Power Mode

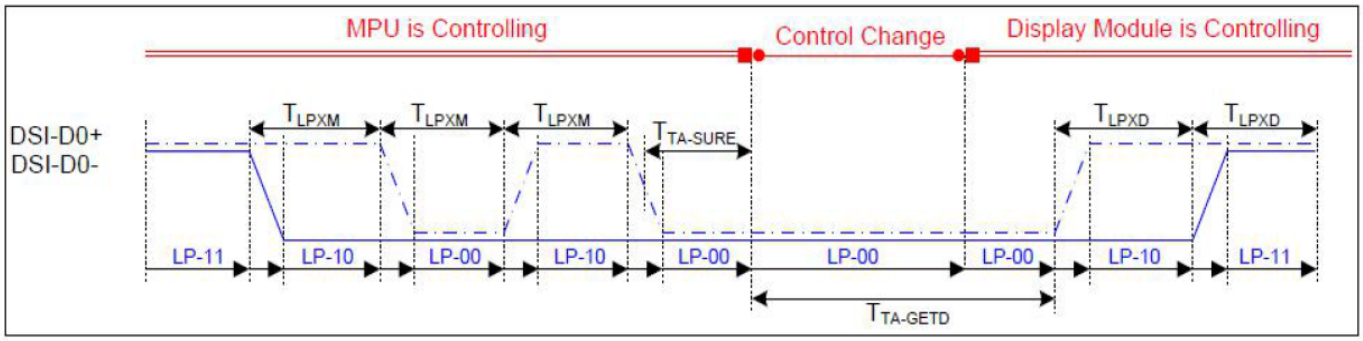


Figure 5.2: Bus Turnaround (BTA) from Display Module to MPU Timing Diagram

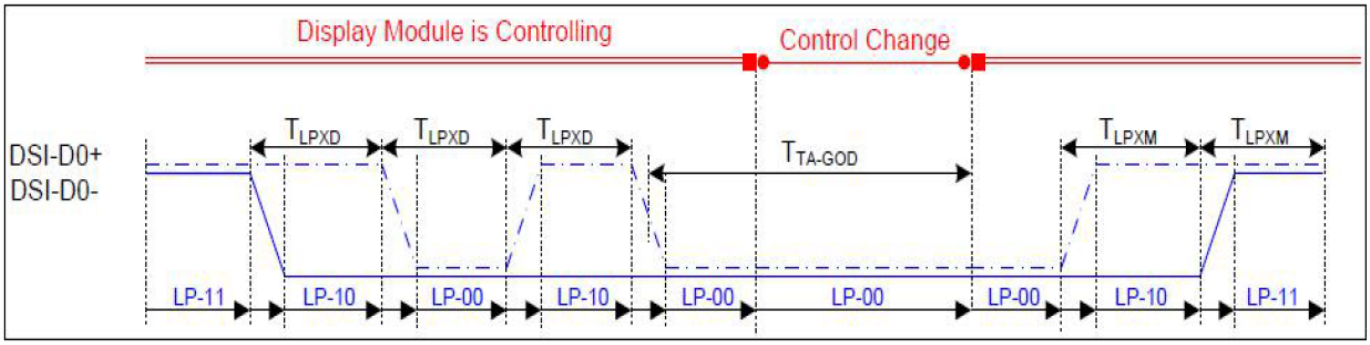


Figure 5.3: Buss Turnaround (BTA) from MPU to Display Module Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
DSI-D0+/-	TLPXM	Length of LP-00, LP_01, LP-10 or LP-11 periods MPU-> Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00, LP_01, LP-10 or LP-11 periods MPU-> Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU starts driving	TLPXD	2xTLPXD	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	5xTLPXD		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	4xTLPXD		ns	Output

Table 5.2: MIPI Interface Low Power Mode Timing Characteristics

5.3 Bursts Mode

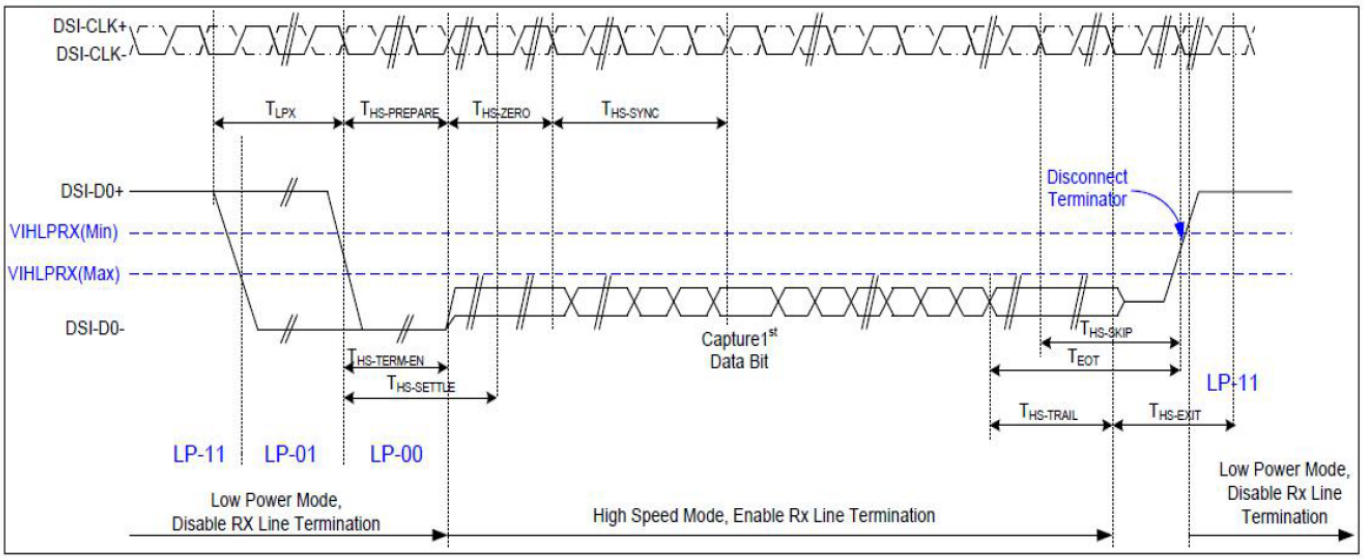


Figure 5.4: Data Lanes Low Power Mode to/from High Speed Mode Timing Diagram

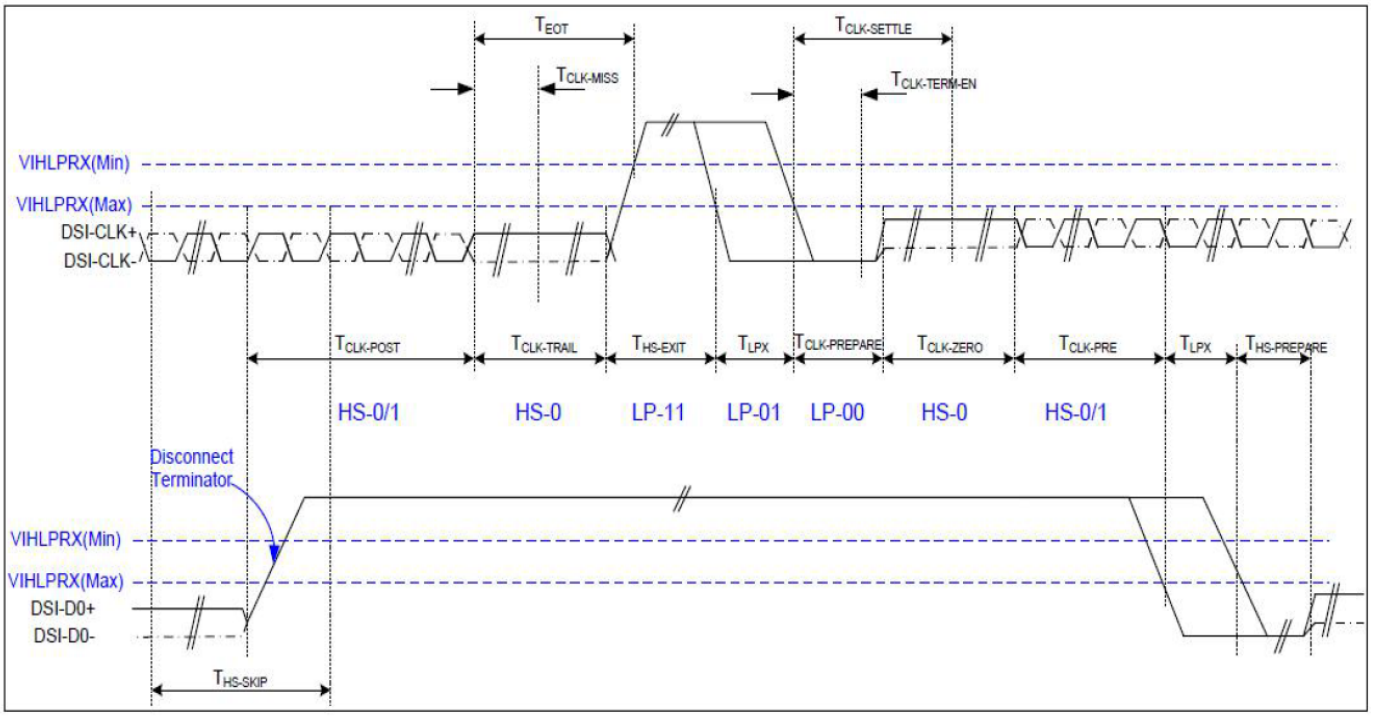


Figure 5.5: Clock Lanes High Speed Mode to/from Low Power Mode Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Note
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	--	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4UI	85+6UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	--	35+4UI	ns	Input
DSI-Dn+/-	THS-PREPARE+ THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	140+10UI	--	ns	Input
High Speed Mode to Low Power Mode Timing						
DSI-Dn+/-	THS-SKIP	Time-out at display module to ignore transition period of EoT	40	55+4UI	ns	Input
DSI-Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	--	ns	Input
DSI-Dn+/-	THS-TRIAL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4UI	--	ns	Input
High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transitioned to LP mode	60+52UI	--	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	--	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	--	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for Hs transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time out at clock ands display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE+	Minimum lead HS-0 drive period before starting clock	300	--	ns	Input
DSI-CLK+/-	TCLK-ZERO TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	--	ns	Input
DSI-CLK+/-	TEOT	Time from start of TCLK-TRAIL period to start of LP-11 state	--	105+12 UI	ns	Input

Table 5.3: Bursts Mode LP to/from HS Mode Timing Characteristics

5.4 Reset Timing

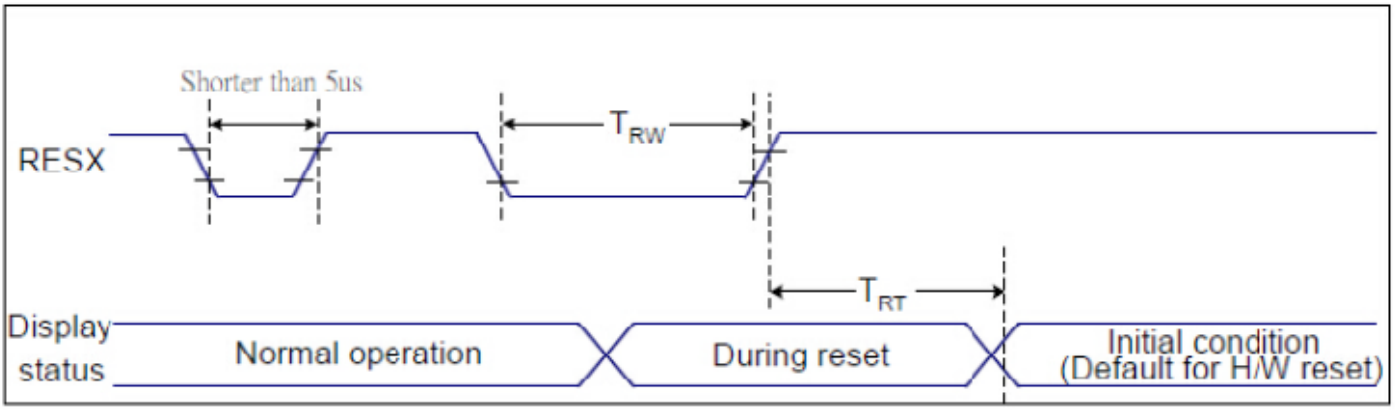


Figure 5.6: Reset Timing Diagram

Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

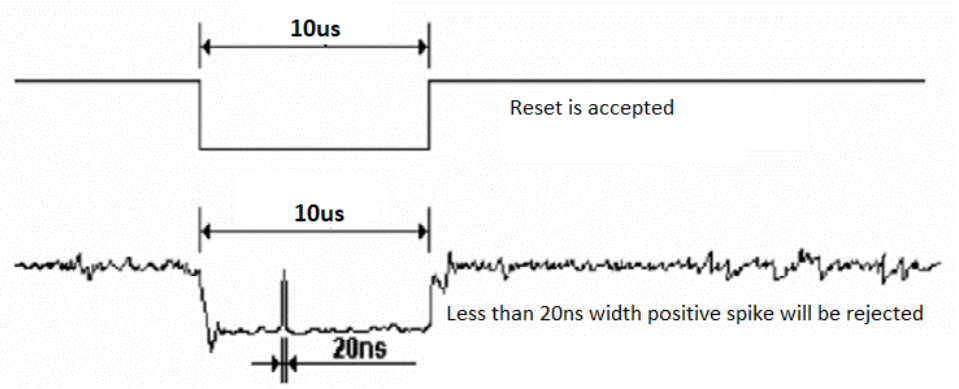
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.