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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

TFT Display Module

Part Number

E17RG11216LW6M300-N

Overview:

- 1.77 inch TFT: 128x160 (34.0x47.0)
- 16/18- bit RGB
- 8/9/16/18-bit MCU
- 3/4 wire SPI
- White LED back-light
- Transmissive
- No Touch Panel
- 300 NITS
- Controller: ILI9163V
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit and back- light unit. The resolution of a 1.77" TFT-LCD contains 128x160 pixels and can display up to 65K colors.

Features

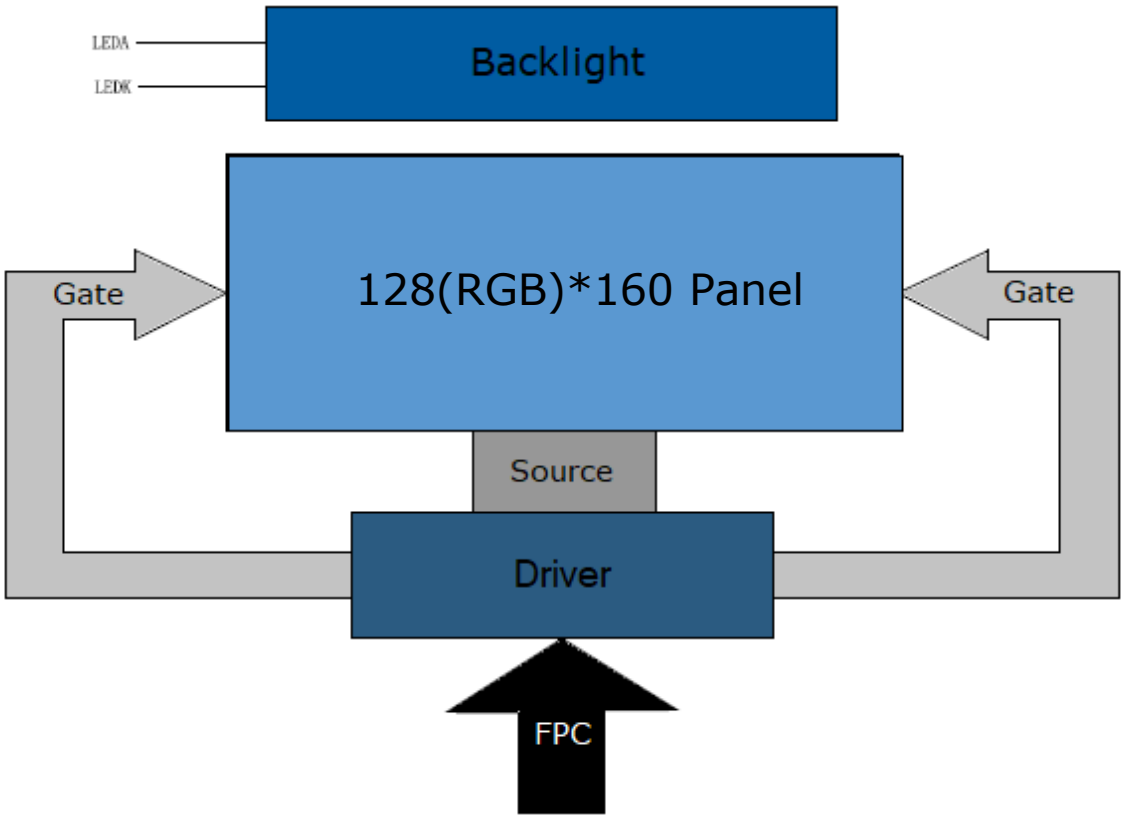
Low Input Voltage: 3.3V(TYP)
Display Colors of TFT LCD: 65Kcolors
Interface:
8/9/16/18Bit MCU
3/4SPI+16/18Bit RGB

General Information Items	Specification Main Panel	Unit	Note
Display area (AA)	28.02(H) *35.04(V) (1.77inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	65K	colors	-
Number of pixels	128(RGB)*160	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.219 (H) x 0.219 (V)	mm	-
Viewing angle	12:00	o'clock	-
TFT Controller IC	ILI9163V	-	-
Display mode	Transmissive/Normally White	-	-
Operating temperature	-20～+70	℃	-
Storage temperature	-30～+80	℃	-

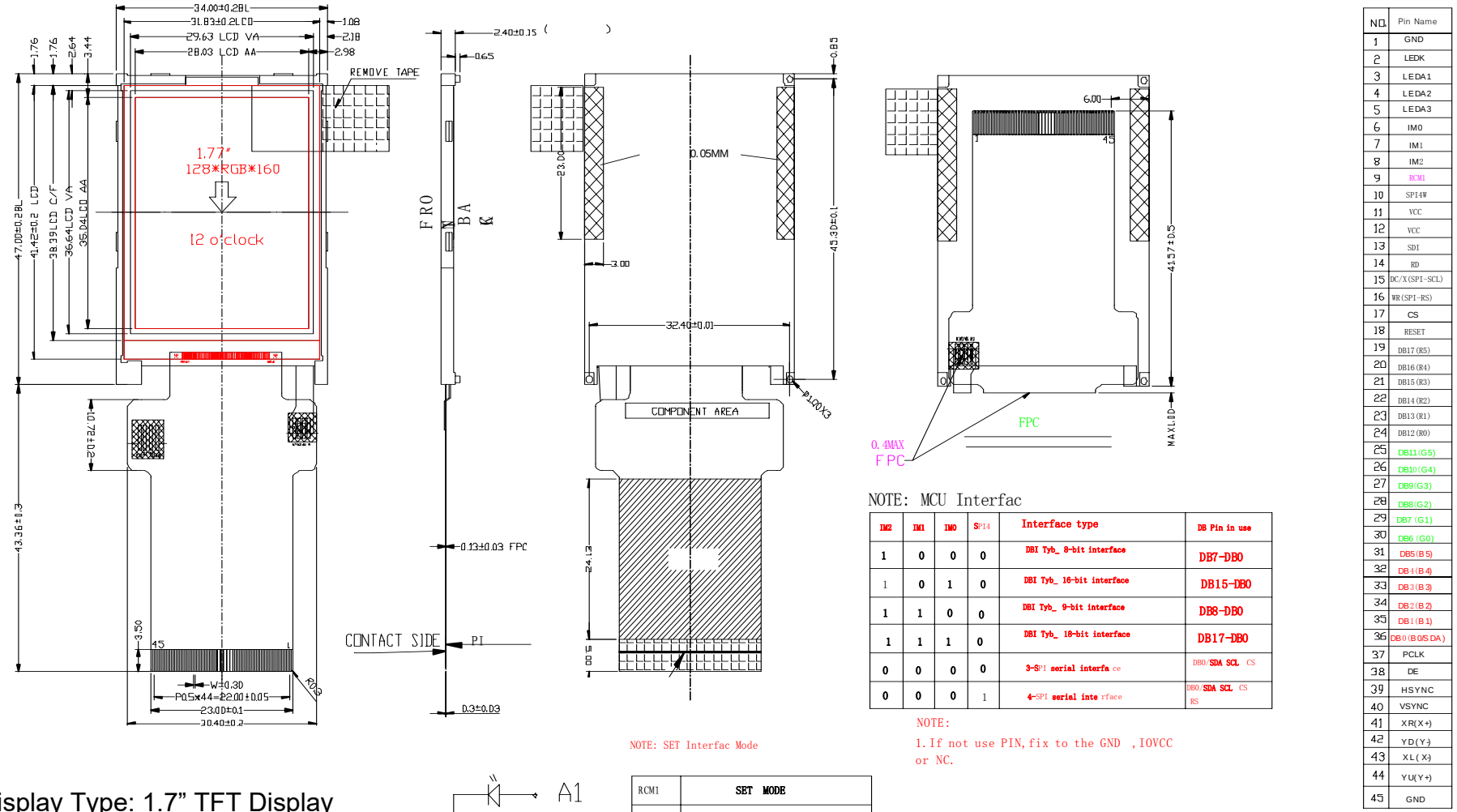
Mechanical Information

Item		Min	Typ.	Max	Unit	Note
Module size	Horizontal(H)		34.0		mm	-
	Vertical(V)		47.0		mm	-
	Depth(D)		2.4		mm	-
Weight			TBD		g	-

1. Block Diagram



2. Outline Dimensions



NO.	Pin Name
1	GND
2	LEDK
3	LEDA1
4	LEDA2
5	LEDA3
6	IM0
7	IM1
8	IM2
9	RCM1
10	SPI4W
11	VCC
12	VCC
13	SDI
14	RD
15	DC/X(SPI-SCL)
16	WR(SPI-RS)
17	CS
18	RESET
19	DB17(R5)
20	DB16(R4)
21	DB15(R3)
22	DB14(R2)
23	DB13(R1)
24	DB12(R0)
25	DB11(G5)
26	DB10(G4)
27	DB9(G3)
28	DB8(G2)
29	DB7(G1)
30	DB6(G0)
31	DB5(B5)
32	DB4(B4)
33	DB3(B3)
34	DB2(B2)
35	DB1(B1)
36	DB0(B0/SDA)
37	PCLK
38	DE
39	HSYNC
40	VSYNC
41	XR(X+)
42	YD(Y-)
43	XL(X-)
44	YU(Y+)
45	GND

NOTE: MCU Interfac

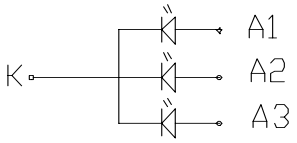
IM2	IM1	IM0	SPI4	Interface type	DB Pin in use
1	0	0	0	DBI Tyb_ 8-bit interface	DB7-DB0
1	0	1	0	DBI Tyb_ 16-bit interface	DB15-DB0
1	1	0	0	DBI Tyb_ 9-bit interface	DB8-DB0
1	1	1	0	DBI Tyb_ 18-bit interface	DB17-DB0
0	0	0	0	3-SPI serial interfa ce	DB0/SDA SCL CS
0	0	0	1	4-SPI serial inte rface	DB0/SDA SCL CS RS

NOTE:
1. If not use PIN, fix to the GND , IOVCC or NC.

NOTE: SET Interfac Mode

RCM1	SET MODE
1	RGB MODE
0	MCU MODE

NOTE: If used RGB mode must select serial interface!



LED CIRCUIT DIAGRAM

Display Type: 1.7" TFT Display
Mode: TN
Viewing direction: 12:00 Driver
IC: ILI9163V
VCI: 3.3 typical
Operating Temp: -20° to 70°c
Storage temp: -30°C to 80° C
Backlight: LED White, 60 Ma
RoHS Compliant

Rev.	Revision content description	Date
V0	FIRST	
V1		

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TOLERANCE	±0.2	DRAWING NAME	E17RG11216LW6M300-N
TOLERANCE UNLESS OTHERWISE SPECIFIED	X.X±0.3 X.XX±0.2	Drawn	Unit
		Checked	mm
Scale 1:1		Approve	Page 1/1

3. Input Terminal Pin Assignment

Recommended Connector: FH12S-45S-0.5SH(55)

NO.	Symbol	Description	I/O
1	GND	Ground.	P
2	LEDK	Cathode pin OF backlight.	P
3	LEDA1	Anode pin of backlight.	P
4	LEDA2	Anode pin of backlight.	P
5	LEDA3	Anode pin of backlight.	P
6	IM0	MCU parallel interface type selection IM1 / IM0 / Parallel interface 0 / 0 / MCU 8-bit Parallel 0 / 1 / MCU 16-bit Parallel 1 / 0 / MCU 9-bit Parallel 1 / 1 / MCU 18-bit Parallel	I
7	IM1		
8	IM2	MCU Parallel interface bus and Serial interface select. IM2='1'; Parallel Interface. IM2='0'. Serial Interface	I
9	RCM1	RGB and MCU interface mode selection pin. RCM1=1, RGB interface RCM1=0, MCU interface mode	I
10	SP14W	SPI interface selection pin.SPI4W='0': 3 wire SPI. SPI4W='1': 4-wire SPI. This pin is internal pull low.	I
11	VCC	Supply voltage (3.3V).	P
12	VCC	Supply voltage (3.3V).	P
13	SDI	When RCM1, RCM0='1X' (RGB I/F), serial input/ output signal in serial I/F mode. The data is in put on the rising edge of the SCL signal. The data is output on the falling edge of the SCL signal. When RCM1, RCM0='0X' (MCU I/F), this pin is not used, and fix at VDDI or GND level	I
14	RD	Read enable. If not used, please connect this pin to VDD.	I
15	DC/SCL	Display data / Command selection pin in parallel el and SCL in 3-pin SPI interface. D/CX='1': Display data. D/CX='0': Command data. If not used, please connect this pin to GND.	I
6	WR/SPI_RS	Write in parallel interface mode. WRX: for 8080 MCU D/CX: for 4-wire SPI. Pin to VDDI or GND if not used.	I
17	CS	Chip select ("Low" enable). This pin can be permanently fixed "Low" in MCU interface mode only.	I
18	RESET	Reset signal. Must be applied to properly initialize the chip.	I
19-36	DB17-DB0(SDA)	When RCM1='0' (MCU I/F), D[17:0] used to MCU parallel interface data bus. D0 is also the serial input/ output signal in SPI interface mode. In serial interface, D[17: 1] are not used and should be connected to ground. When RCM1='1' (RGB I/F), D[17:0] are used to RGB interface data bus.	I/O
37	PCLK	Pixel clock signal in RGB I/F mode. If it' s not used, please fix this pin at GND level	I
38	DE	Data enable signal in RGB I/F mode. If it's not used, please fix this pin at GND level.	I
39	HSYNC	Horizontal sync. Signal in RGB I/F mode. If it's not used, please fix this pin at GND level.	I
40	VSYNC	Vertical sync. Signal in RGB I/F mode. If it's not used, please fix this pin at GND level.	I
41	XR(NC)		
42	YD(NC)		
43	XL(NC)		
44	YU(NC)		
45	GND	Ground	P

4. LCD Optical Characteristics

4.1 Optical specification

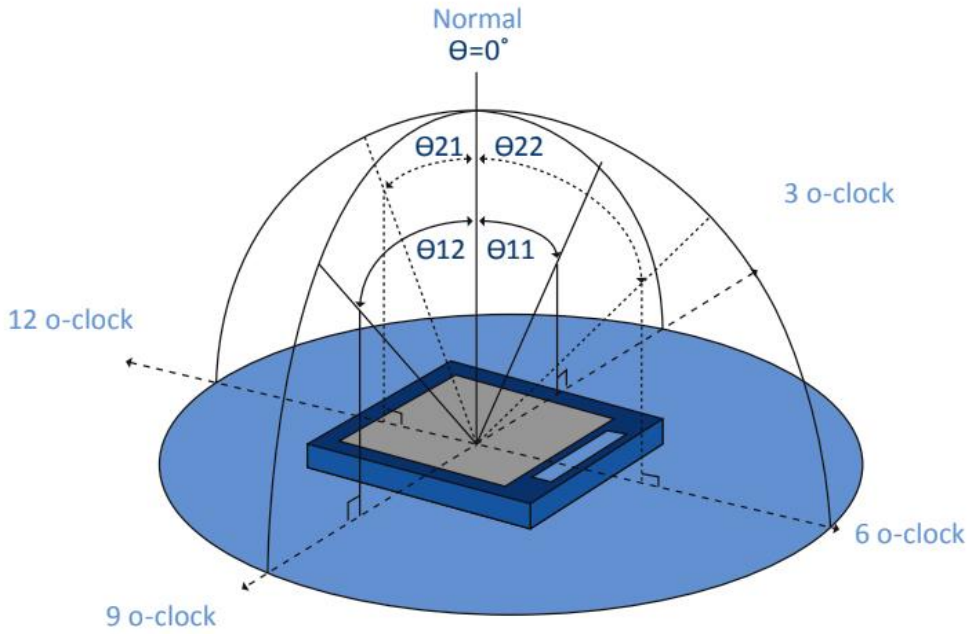
Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Transmittance (without Polarizer)		T(%)	-	-	19.1	-		(3)
Contrast Ratio		CR	Θ=0 Normal viewing angle	400	500	--		(2)
Response time	Rising+	TR		--	2	4	msec	(4)
	Falling	TF		--	6	12		
Color gamut		S (%)		--	60	--	%	(5)
Color Filter Chromaticity	White	W_X		0.283	0.303	0.323		(5)
		W_Y		0.305	0.325	0.345		
	Red	R_X		0.606	0.626	0.646		
		R_Y		0.314	0.334	0.354		
	Green	G_X		0.257	0.277	0.297		
		G_Y		0.529	0.549	0.569		
	Blue	B_X		0.122	0.142	0.162		
		B_Y		0.102	0.122	0.142		
Viewing angle	Hor.	ΘL	CR>10	35	45	--		(1)(6)
		ΘR		35	45	--		
	Ver.	ΘU		35	45	--		
		ΘD		10	20	--		
Option View Direction		12 O'clock						(1)

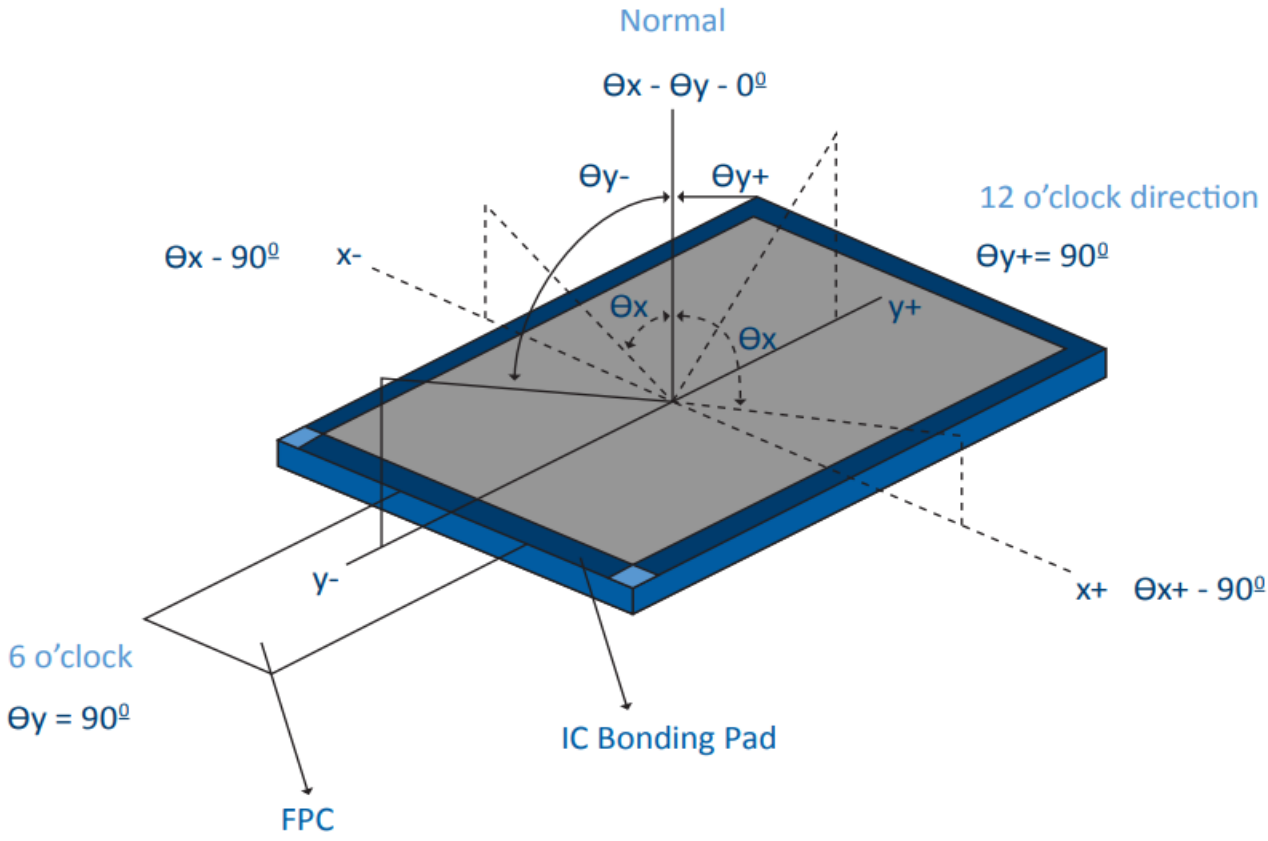
4.2 Measuring Conditions

Measuring surrounding: dark room
Ambient temperature: 25±2oC
15min. warm-up time.

Optical Specification Reference Notes:

(1) Definition of Viewing Angle:

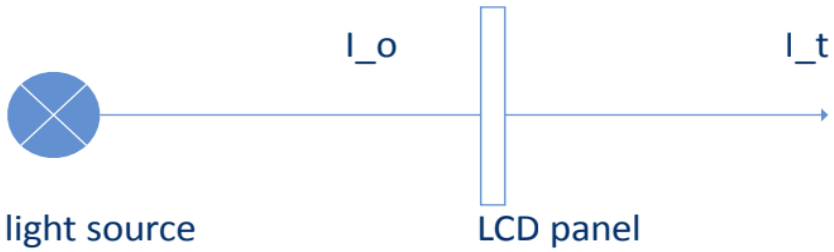




(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

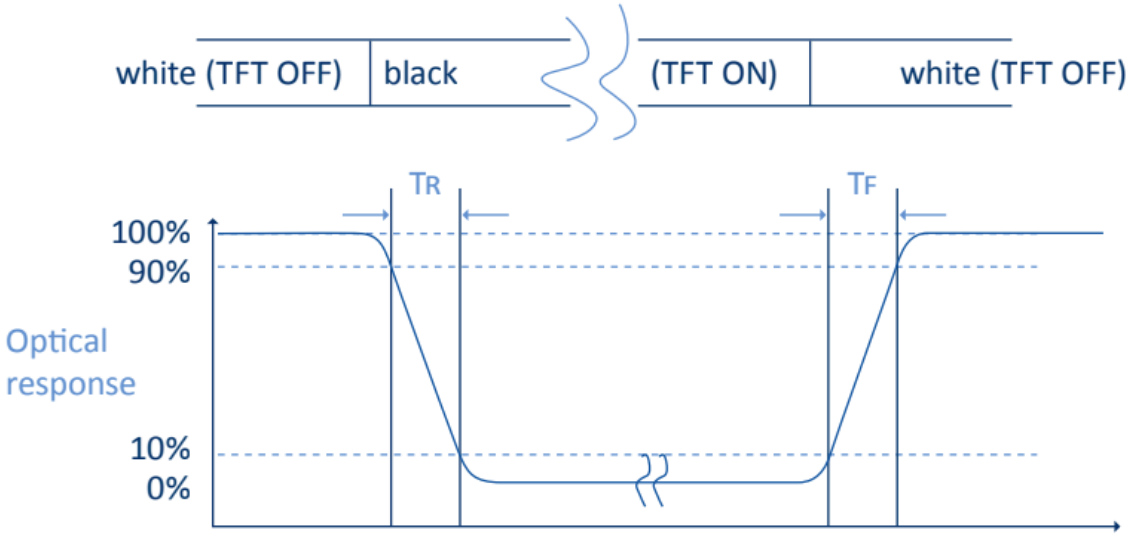


The transmittance is defined as:

$$Tr = \frac{It}{Io}\ x\ 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

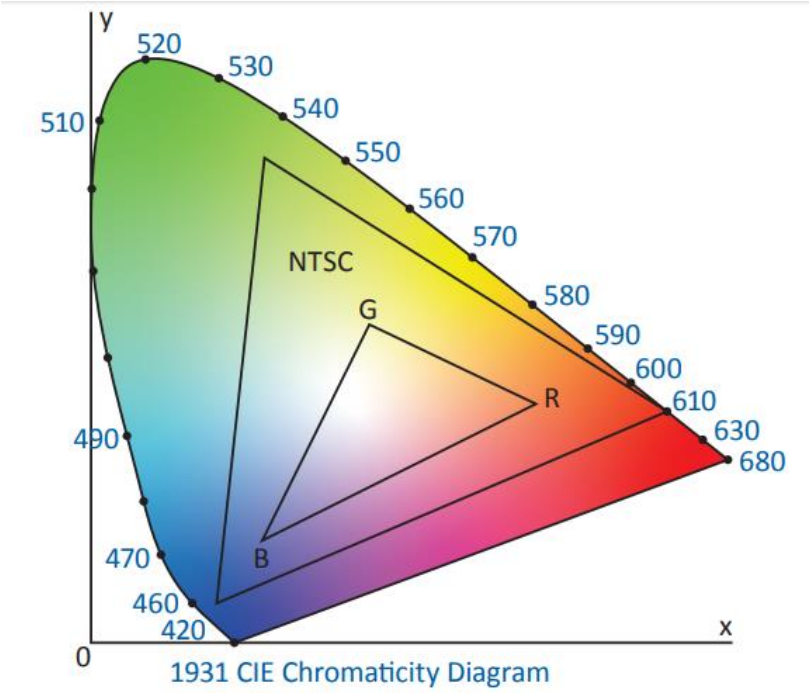
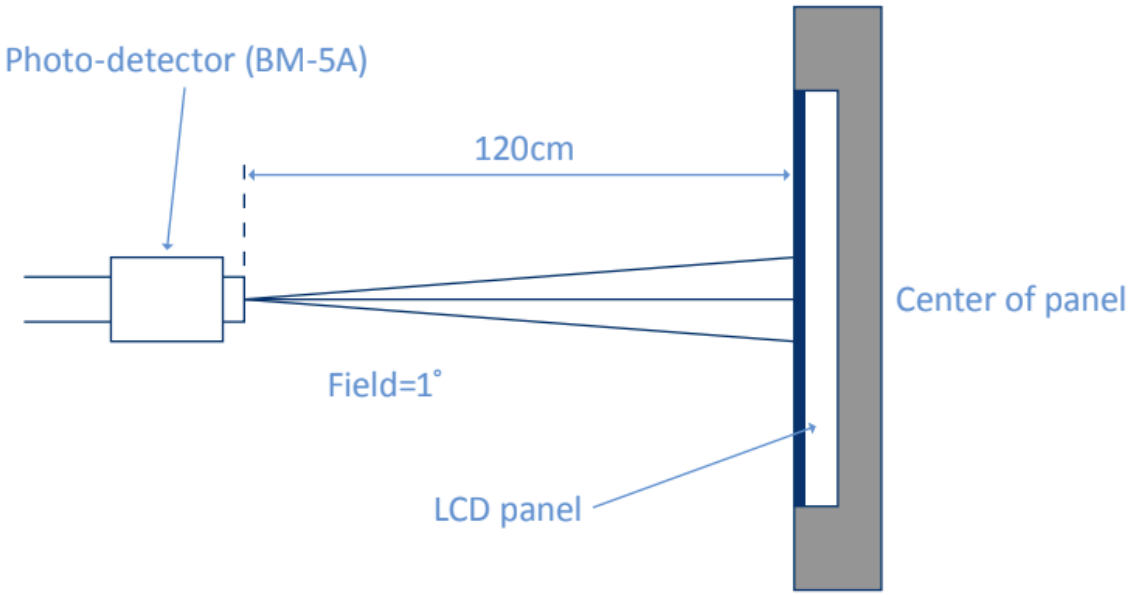


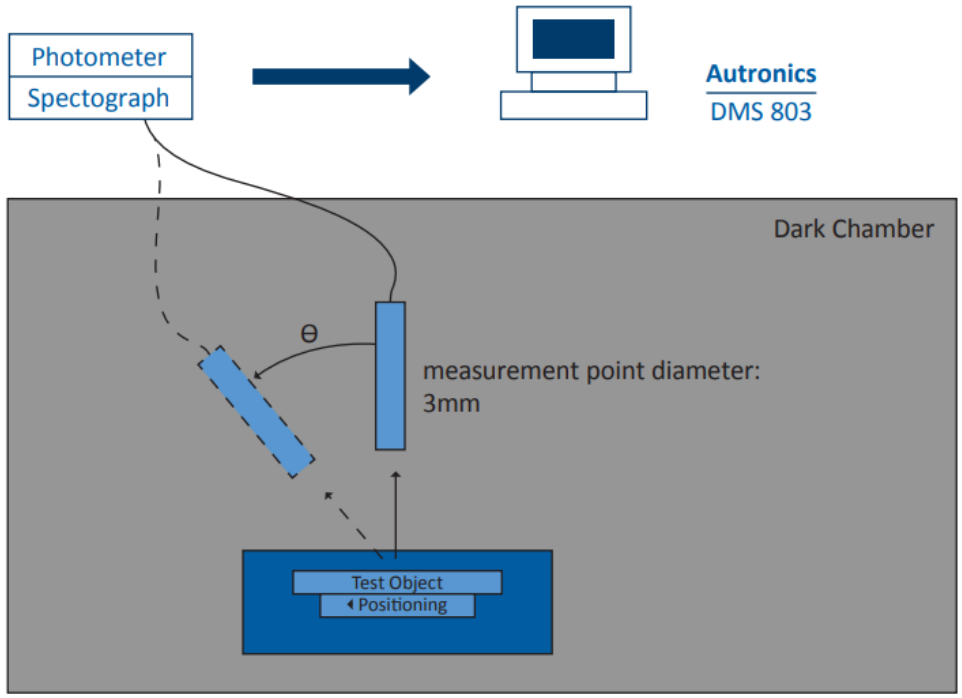
Fig. 1931 CIE chromacity diagram

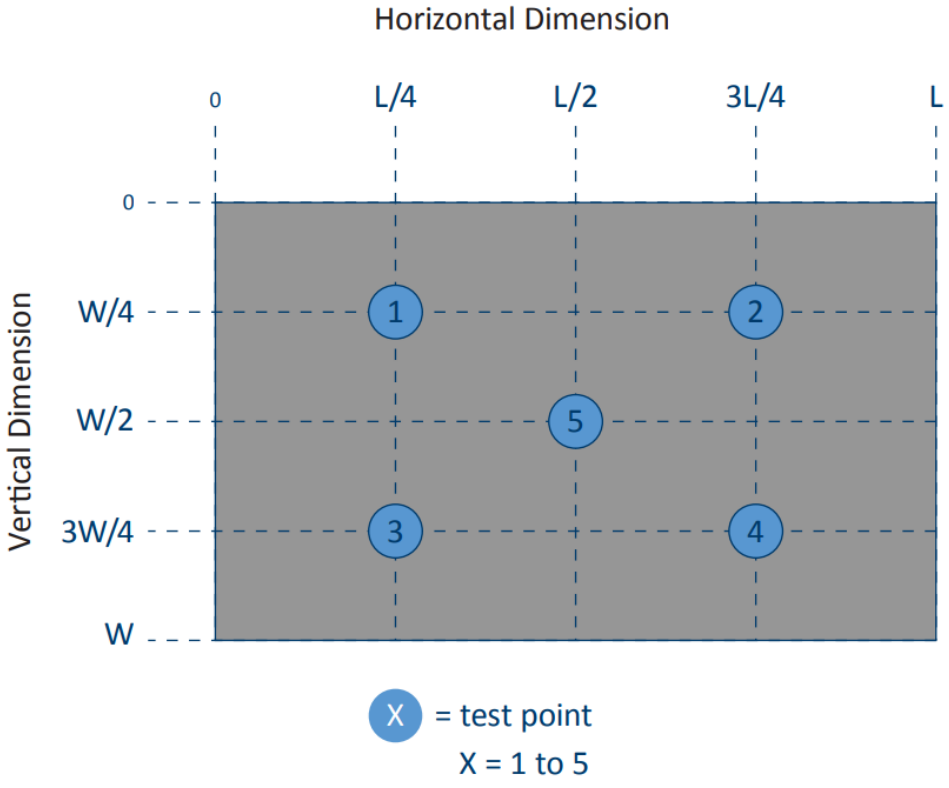
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.





5. Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VDD	-0.3	4.8	V
Interface Operation Voltage	VDDIO	-0.3	4.6	V
Operating temperature	TOP	-20	+70	℃
Storage temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VDD	2.5	3.3	4.2	V	
Interface Operation Voltage	VDDIO	1.65	3.3	4.2	V	
Normal Mode Current Consumption	IDD	--	1.5	--	mA	
Level input voltage	VIH	0.7 VDDIO		VDDIO	V	
	VIL	GND		0.3 VDDIO	V	
Level output voltage	VOH	0.8 VDDIO		IOVCC	V	
	VOL	GND		0.2 VDDIO	V	

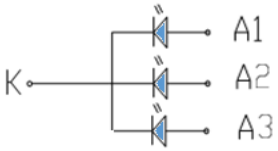
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 3 chips White LED

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	IF	45	60	--	mA	
Forward Voltage	VF	--	3.2	--	V	
LCM Luminance	LV	300	--	--	cd/m2	Note 3
Uniformity	AVg	80	--	--	%	Note 3

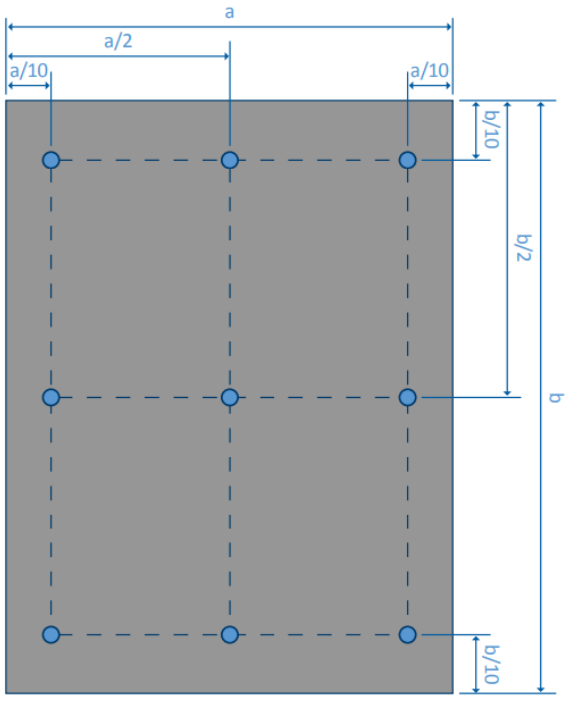
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.



LED Circuit Diagram

Note 3: Luminance Uniformity of these 9 points is defined as below:



$$\text{Luminance} = \frac{(\text{Total Luminance of 9 points})}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

6. AC Characteristics

6.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- system)

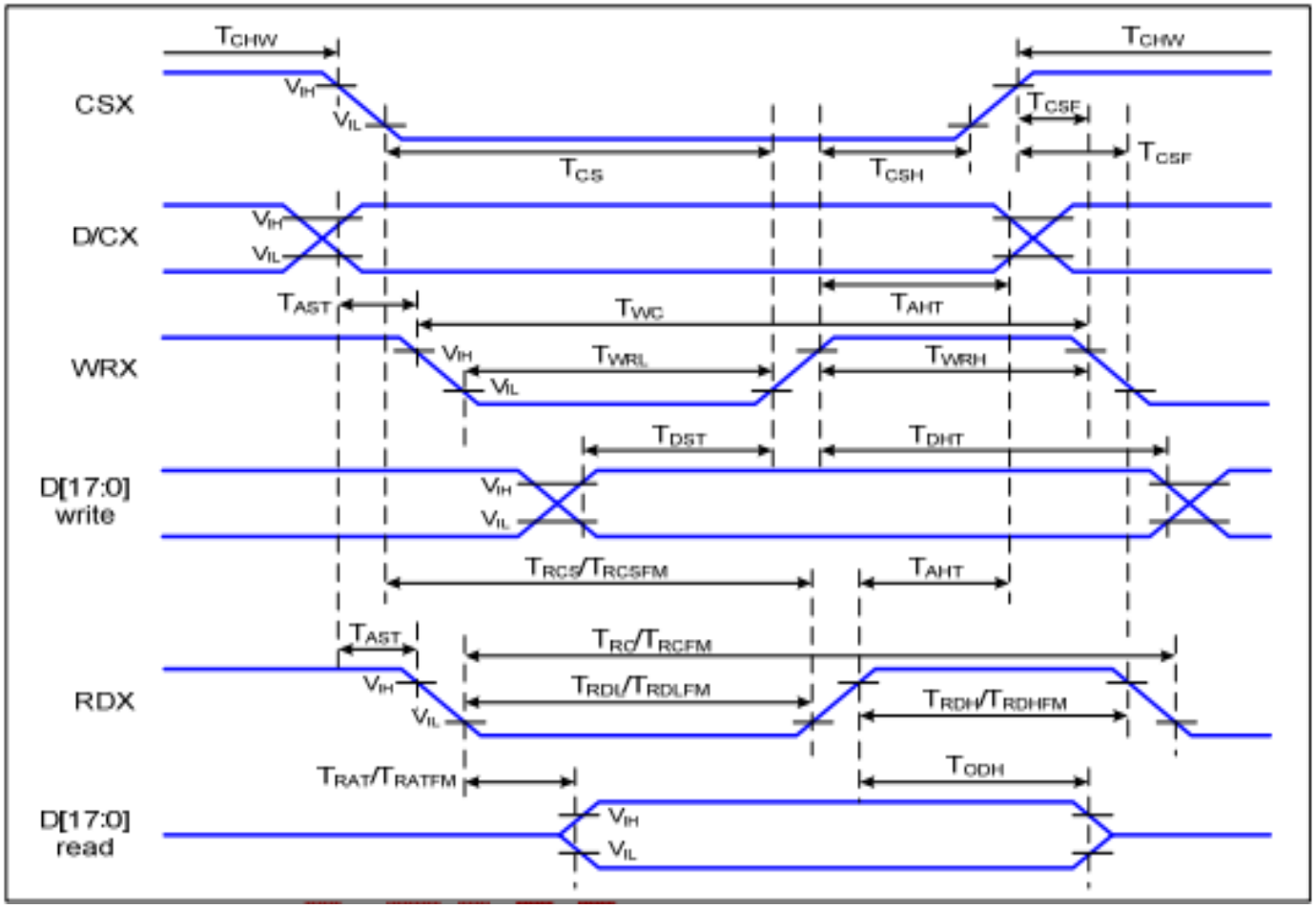
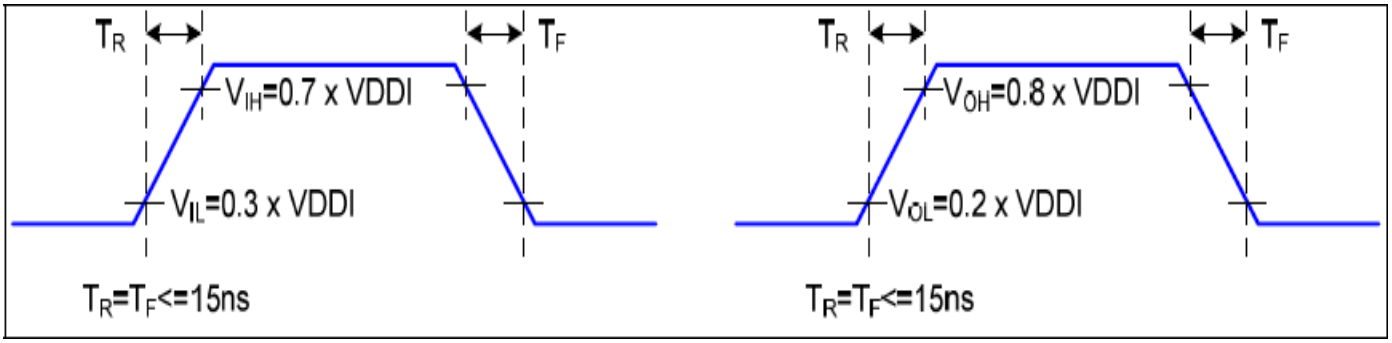


Figure 6.1: Parallel 8/9/16/18-bit Interface Timing Diagram

Note: Logic high and low levels are specified as 30% and 70% of VDDI for input signals.



6.1 Parallel interface timing characteristics (8080-system) Continued:

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select “H” pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	10		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse “H” duration	15		ns	
	T_{WRL}	Control pulse “L” duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse “H” duration (ID)	90		ns	
	T_{RDL}	Control pulse “L” duration	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse “H” duration (FM)	90		ns	
	T_{RDLFM}	Control pulse “L” duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For max CL=30pF, For min CL=8pF
	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)			ns	
	T_{RATFM}	Read access time (FM)			ns	
	T_{ODH}	Output disable time	20		ns	

Table 6.1: Parallel 8/9/16/18-bit Interface Timing Characteristics

Note 1: VDDI 1.65 to 3.3V, VCl=2.6 to 3.3V, AGND=GND=OV, Ta=-30 to 70 ·c (to +85°C no damage).

Note 2: This input signal rise time and fall time (tr, tf) is specified at 1:5 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

6.2 Serial Interface Characteristics (3-line serial)

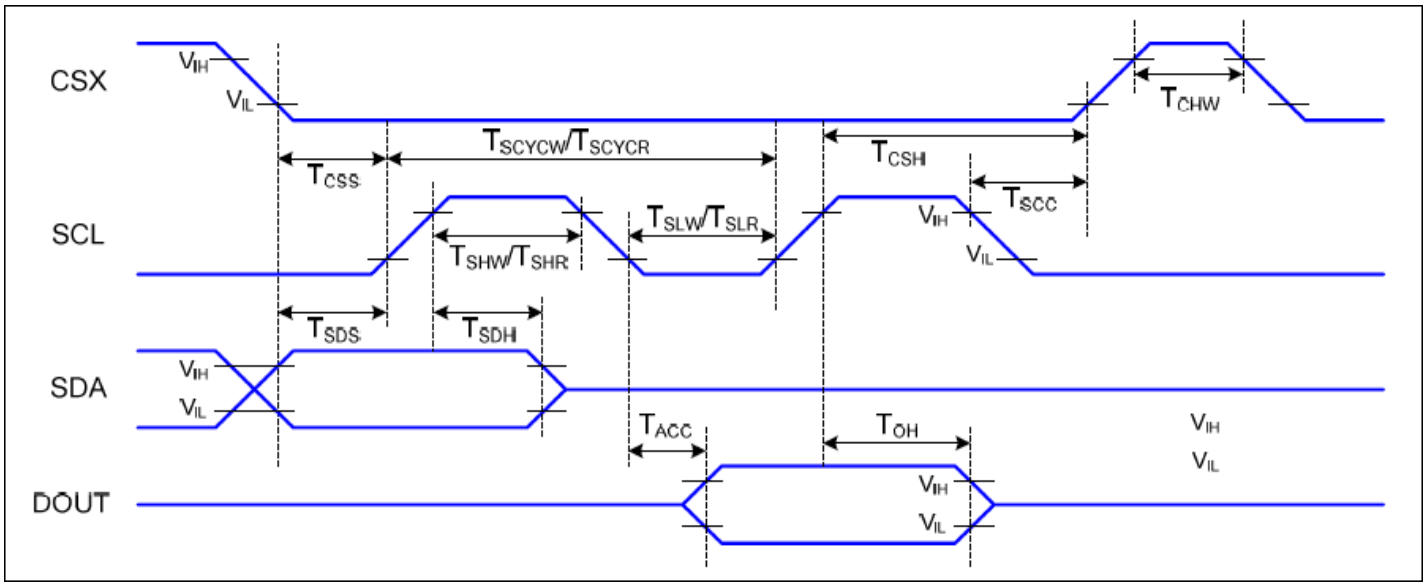


Figure 6.2: 3-line Serial Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	10		ns	-
	T_{CSH}	Chip select hold time (write)	30		ns	
	T_{CSS}	Chip select setup time (read)	30		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66		ns	
	T_{SHW}	SCL “H” pulse width (write)	15		ns	
	T_{SLW}	SCL “L” width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
SDA (DIN)	T_{SDS}	Data setup time	5		ns	For CL=30pF
	T_{SDH}	Data hold time	5			
DOUT	T_{ACC}	Access time	5	50	ns	For max CL=30pF
	T_{OH}	Output disable time	10			For min CL=8pF

Table 6.2: 3-line Serial Interface Timing Characteristics

6.3 Serial Interface Characteristics (4-line serial)

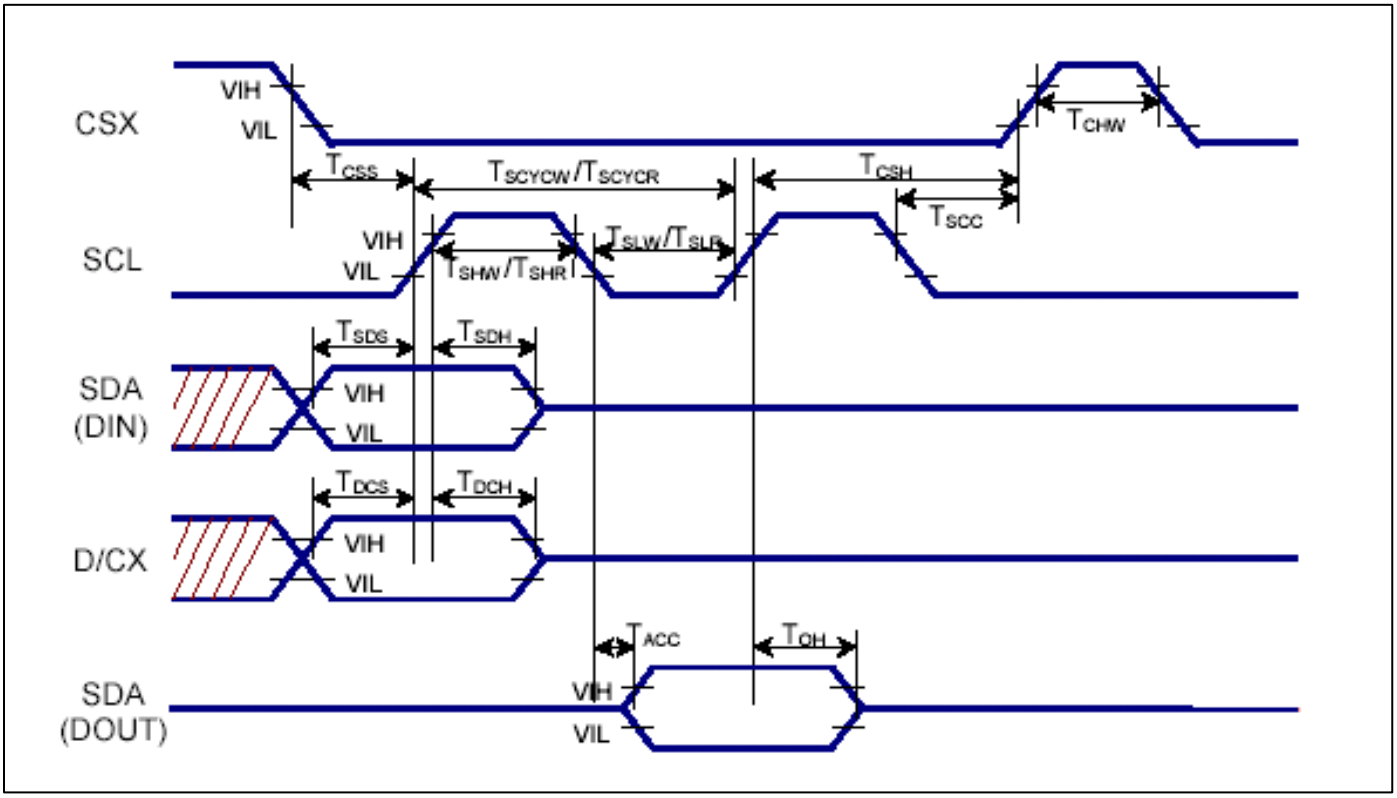


Figure 6.3: 4-line Serial Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	10		ns	
	T_{CSH}	Chip select hold time (write)	30		ns	
	T_{CHW}	Chip select setup time (read)	30		ns	
SCL	T_{SCYCW}	Serial clock cycle (write)	66		ns	
	T_{SHW}	SCL “H” pulse width (write)	15		ns	
	T_{SLW}	SCL “L” width (write)	15		ns	
	T_{SCYCR}	Serial clock cycle (read)	150		ns	
	T_{SHR}	SCL “H” pulse width (read)	60		ns	
	T_{SLR}	SCL “L” pulse width (read)	60		ns	
D/CX	T_{DCS}	D/CX setup time	5			
	T_{DCH}	D/CX hold time	5			
SDA (DIN)	T_{SDS}	Data setup time	5		ns	
	T_{SDH}	Data hold time	5			For max CL=30pF For min CL=8pF
DOUT	T_{ACC}	Access time	5	50	ns	
	T_{OH}	Output disable time	10			

Table 6.3: 4-line Serial Interface Timing Diagram

Note 1: VDDI 1.65 to 3.3V, VCl=2.6 to 3.3V, AGND=GND=OV, Ta=-30 to 70 c (to +85°C no damage).

Note 2: This input signal rise time and fall time (tr, tf) is specified at 1:5 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for input signals.

6.4 Parallel RGB 18/16/6-bit Bus

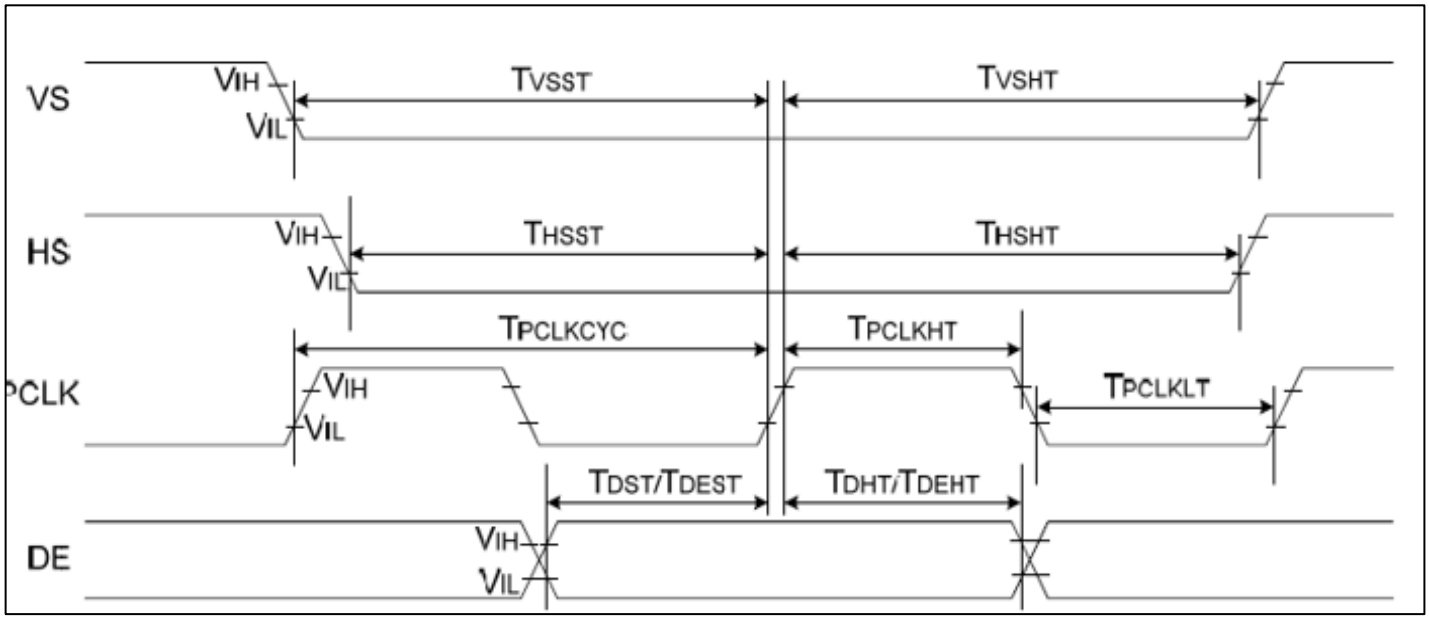


Figure 6.4: Parallel RGB 18/16/6-bit Interface Timing Diagram

Signal	Symbol	Parameter	Min	Max	Unit	Description
PCLK	$T_{PCLKCYC}$	TPCLK Cycle time	66		ns	
	T_{PCLKLT}	Pixel low pulse width	15		ns	
	T_{CLKHT}	Pixel high pulse width	15		ns	
VS	T_{VSST}	Vertical sync setup time	15		ns	
	T_{CVSHT}	Vertical sync. hold time	15		ns	
HS	T_{HSST}	Horizontal sync setup time	15		ns	
	T_{HSHT}	Horizontal sync hold time	15		ns	
DE	T_{DEST}	Data Enable setup time	15		ns	
	T_{DEHT}	Data Enable hold time	15		ns	
D[17:0]	T_{DST}	Data setup time	15		ns	
	T_{DHT}	Data hold time	15		ns	

Table 6.4: Parallel RGB 18/16/6-bit Interface Timing Characteristics

6.5 Reset Timing

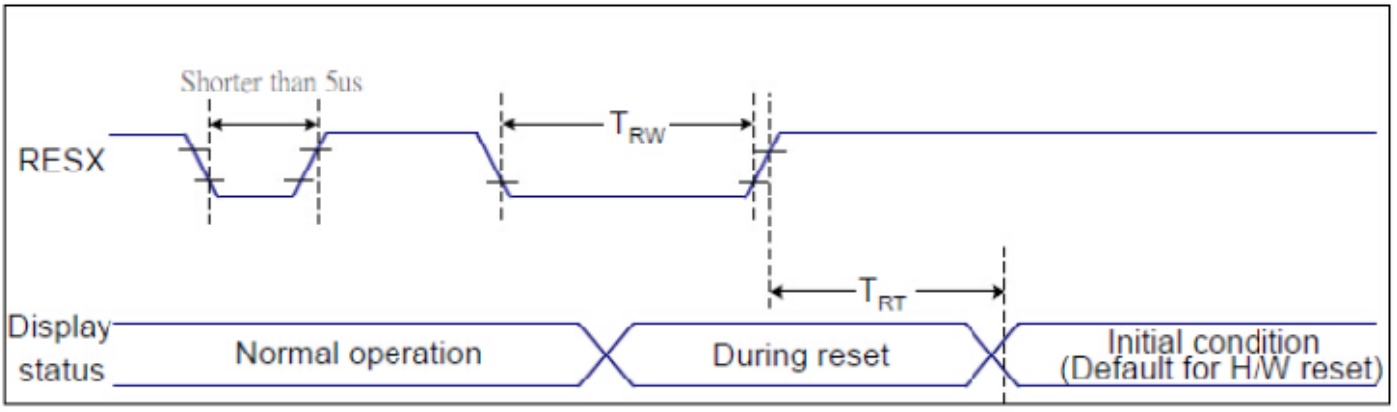


Figure 6.5: Reset Timing

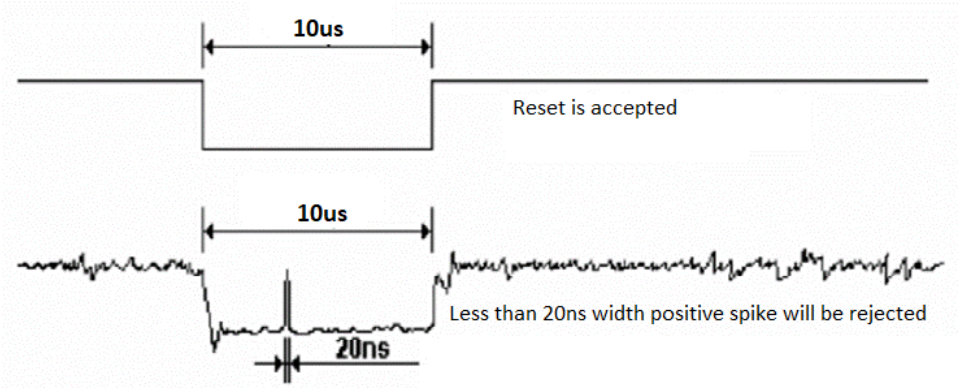
Related Pins	Symbol	Parameter	Min	Max	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1,5)	ms
				120 (Note 1, 6, 7)	ms

Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not because irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9 us	Reset starts

3. During the resetting period, the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when reset starts in Sleep Out mode. The display remains the blank state in Sleep in mode) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120ms.

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use finger stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence

7.2 Storage and Transportation

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.