NuMicro® Family

Arm® 32-bit Cortex®-M23 Microcontroller

NuMicro® Family
M254/M256/M258 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro M254/M256/M258 is a 32-bit low-power, low-leakage microcontroller series based on Arm Cortex-M23 core using Armv8-M architecture with COM/SEG LCD display driver and capacitive touch key functions for HMI of smart appliance; an USB 2.0 full speed device is also equipped to support the communication with PC/Mobile accessories. It runs up to 48 MHz and features 64 to 256 Kbytes Flash, 8 to 32 Kbytes SRAM, 1.75V to 5.5V wide operating voltage, 5V I/O tolerance, and -40℃ to +105℃ operating temperature. It features

Low-power Technology

The M254/M256/M258 series provides low power consumption in Normal Run mode 110 μA/MHz at 48 MHz, Power-down mode with 2.5 μA while RTC on and RAM retention, and it can supports down to 1.6uA while RTC off, and Deep Power-down mode is down to 1.5 μA. The M254/M256/M258 series integrates RTC with independent V_{BAT} voltage source pin to support low power mode with main power off and V_{BAT} only. Its low power, wide supply voltage and fast wake-up features make it suitable for battery-powered devices.

COM/SEG LCD Display Driver

An 8 x 44, 6 x 46, 4 x 48 COM/SEG LCD is available on the M254/M256/M258 series. The COM/SEG LCD driver built-in charge-pump function to support 3V to 5V LCD panel, with selectable bias voltage (1/2, 1/3, 1/4) and duty (1/4, 1/6, 1/8). The feature makes it suitable for Handheld devices that need high display quality in the outdoor environment to provide constant contrast ratio.

Capacitive Touch Key Sensing Function

The M256/M258 series supports up to 24 independent capacitive touch key sensing function with single-scan or programmable periodic key-scans modes; it also provides high noise resistance in harsh requirement and easy-to-use calibration tool regarding to development and mass production phase.

Crystal-less USB 2.0 full speed device complied with BC 1.2

The M258 series supports a crystal-less USB 2.0 full speed device that supports precise frequency required for USB protocol to reduce the BOM cost and PCB size. It also supports USB Battery Charging Detection v1.2 (BC 1.2) profile for high-speed battery charging.

Rich Peripherals for comprehensive product application scenarios

The M254/M256/M258 series is equipped with plenty of peripherals such as Timers, Watchdog Timers, RTC, PDMA, UART, Universal Serial Control Interface (USCI), SPI/ I²S, I²C, ISO-7816-3, GPIOs, up to 12 channels of basic PWM, making it highly suitable for connecting comprehensive external modules. It also integrates high performance analog circuit, such as 16 channels of 12-bit 730 kSPS ADC and up to 2 sets of 12-bit 1 MSPS DAC to reduce external components.

Supported packages include LQFP44 (10 mm x 10 mm), LQFP64 (7 mm x 7 mm), LQFP80 (14 mm x 14 mm) and LQFP128 (14 mm x 14 mm).

For the development, Nuvoton provides the NuMaker evaluation board and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, Eclipse IDE with GNU GCC compilers are also supported.

USCI*: supports UART, SPI or I^2C

Product Line	UART	I^2C	SPI/ I^2S	USCI*	32-bit Timer	BPWM	PDMA	ADC	DAC	ACMP	V_{BAT}	COM / SEG LCD Driver	Capacitive Touch	USB 2.0 FS Device (with BC 1.2)
M254	4	2	2	2	4	12	8	16	2	2	√	√	-	-
M256	4	2	2	2	4	12	8	16	2	2	√	√	24	-
M258	4	2	2	2	4	12	8	16	2	2	√	√	24	√

Table 1-1 NuMicro M254/M256/M258 Series Key Features Support Table

The M254/M256/M258 series is suitable for a wide range of applications that needs a smart LCD display with touch key inputs such as:

- Handheld Devices
- Thermostat with Smart LCD Display and Touch Key input
- Smart Home Appliance
- Industrial Control / Industrial Automation
- Temperature/Humidity Logger

2 FEATURES

2.1 M254/M256/M258 Features

Core and System	
Arm® Cortex®-M23 without TrustZone®	• Arm® Cortex®-M23 processor, running up to 48 MHz when V_{DD} = 1.75V ~ 5.5V • Built-in PMSAv8 Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Supports Programmble and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access • Supports XOM feature with 1 region
Low power mode and current	• Low Power mode: – Idle mode • Power-down mode (PD) – Fast Wake-up Power-down mode (FWPD) – Deep Power-down mode (DPD)
Wake-up source and wakeup time	• EINT, Touch key, USCI, RTC, WDT, I²C, Timer, UART, BOD, LVR, POR, GPIO, USBD, ACMP, Debug interface, NMI and Reset pin from Power-down mode or Fast Wake-up Power-down mode • RTC, Wake-up Timer, LVR, Wake-up pins, from Deep Power-down mode
Power supply and low voltage detect	• Built-in LDO for wide operating voltage from 1.75V to 5.5V • Core power voltage: 1.5V • Brown-out detector – With 7 levels: 4.4V/3.7V/3.0V/2.7V/2.4V/2.0V/1.8V – Supports Brown-out Interrupt and Reset option • Low Voltage Reset – Threshold voltage levels: 1.55V
Cyclic Redundancy Calculation Unit	• Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 • Programmable order reverse setting for input data and CRC checksum • Programmable 1's complement setting for input data and CRC

	checksum. • Supports 8-/16-/32-bit of data width • Programmable seed value • 8-bit write mode: 1-AHB clock cycle operation • 16-bit write mode: 2-AHB clock cycle operation • 32-bit write mode: 4-AHB clock cycle operation • Supports using PDMA to write data to perform CRC operation
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • AES-128, 192, 256
Memories	
Flash	• Up to 256 KB application ROM (APROM) • 4 KB Flash for user program loader (LDROM) • Up to 48 MHz with zero wait state for consecutive address read access • 12 bytes User Configuration Block to control system initiation. • 512B page erase for all embedded Flash • 32-bit and multi-word Flash programming function. • Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded Flash memory • Supports CRC-32 checksum calculation function • Supports Flash all one verification function (hardware can check page erase verify) • Hardware external read protection of whole Flash memory by Security Lock Bit • Supports XOM feature with 1 region
SRAM	• Up to 32 KB embedded SRAM • Supports byte-, half-word- and word-access • Supports PDMA mode
Peripheral DMA (PDMA)	• Up to 8 independent configurable channels for automatic data transfer between memories and peripherals • Channel 0, 1 support time-out function • Basic and Scatter-Gather Transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Two types of priorities modes: Fixed-priority and Round-robin

	modes • Transfer data width of 8, 16, and 32 bits • Single and burst transfer type • Source and destination address can be increment or fixed • PDMA transfer count up to 65536 • Request source can be form software, SPI/I²S, I²C, UART, USCI, EADC, DACand TIMER
Clocks	
Clock Source	• Built-in 4.032 MHz internal high speed RC oscillator (MIRC) for system operation • Built-in 48 MHz internal high speed RC oscillator (HIRC) for system operation • Built-in 38.4 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation. • Built-in 4~32 MHz external high speed crystal oscillator (HXT) for precise timing operation • Built-in 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock on-the-fly switch • Supports clock failure detection for high/low speed external crystal oscillator • HXT clock frequency accuracy detector • Supports exception (NMI) generated once a clock failure detected • Supports divided clock output
Timers	
32-bit Timer	**TIMER mode** • 4 sets of 32-bit timers with 24-bit up counters and 8-bit prescale counters • Independent clock source for each timer • One-shot, Periodic, Toggle and Continuous Counting operation modes • Event counting function to count the event from external pin • Input capture function to capture or reset counter value • External capture pin event for interval measurement. • External capture pin event to reset 24-bit up counter. • Chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Timer interrupt flag or external capture interrupt flag to trigger BPWM, EADC, DAC and PDMA.

	• Internal capture triggered source from ACMP output. • Inter-Timer trigger capture mode **PWM mode** • 16-bit compare register and period register • Double buffer for period register and compare register • Supports inverse in PWM output • PWM interrupt wake-up from system Power-down mode
BPWM	• Each module provides 6 output channels • Supports independent mode for BPWM output/Capture input channel • Supports 12-bit prescaler from 1 to 4096 • Supports 16-bit resolution BPWM counter, each module provides 1 BPWM counter – Up, down or up/down counter operation type • Supports mask function and tri-state enable for each BPWM pin • Supports interrupt on the following events: – BPWM counter match 0, period value or compared value • Supports trigger ADC on the following events: – BPWM counter match 0, period value or compared value • Capture Function Features – Up to 12 capture input channels with 16-bit resolution – Supports rising or falling capture condition – Supports input rising/falling capture interrupt – Supports rising/falling capture with counter reload option
Watchdog	• 20-bit free running up counter for WDT time-out interval • Clock sources from LIRC (default), HCLK/2048 or LXT • 9 selectable time-out period from 488us ~ 32 sec • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out • Selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Force WDT enabled after chip power on or reset. • WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT
Window Watchdog	• Clock sources from HCLK/2048 (default) or LIRC • Window set by 6-bit down counter with 11-bit prescaler

	• WWDT counter suspends in Idle/Power-down mode • Supports Interrupt
RTC	• Supports external power pin V_{BAT} • Software compensation by setting frequency compensate register (FCR),compensated clock accuracy reaches ±5ppm within 5 seconds • RTC counter (second, minute, hour) and calendar counter (day, month, year) • Alarm registers (second, minute, hour, day, month, year) • Selectable 12-hour or 24-hour mode • Automatic leap year recognition • Day of the Week counter • Daylight Saving Time software control • Periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 or 1 second • 1 Hz clock output for RTC calibration • Wake-up from idle mode and Power-down mode • 32 kHz oscillator gain control • RTC Time Tick and Alarm Match interrupt
Analog Interfaces	
EADC	• Conversion results held in up to 7 data registers with valid and overrun indicators. • Analog input voltage: 0~V_{REF} (Max to AV_{DD}). • Reference voltage from V_{REF} pin, AV_{DD} or internal V_{REF} • 12-bit resolution and 10-bit accuracy guaranteed • Up to 16 single-end analog external input channels • Supports 3 internal channels: – Band-gap VBG output or Internal voltage reference – Temperature sensor input – V_{BAT} voltage measure (V_{BAT}/4) • Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses. • ADC clock frequency up to 16 MHz. • Up to 730 KSPS conversion rate. • Configurable ADC internal sampling time • Up to 7 sample modules – Each of sample module 0~3 is configurable for ADC converter

	channel – EADC_CH0~15 and trigger source. – Configurable PDMA – Configured resolution for 12-bit or 16-bit result – Supports Left-adjusted result – Averaging and oversampling (2^n times, n=0~8) to support up to 16-bit result – Sample module 16~18 is fixed for ADC channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and battery power (V_{BAT}/4). – Configurable sampling time for each sample module. – Conversion results held in 19 data registers with valid and overrun indicators. • Supports digital comparator to monitor conversion result that can be under or over the compare register setting • Generate an interrupt when conversion result matches the compare register setting. • Internal reference voltage source: – 1.536V, 2.048V, 2.560V, 3.072V, or 4.096V • An A/D conversion can be started by: – Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18) – External pin EADC0_ST – Timer0~3 overflow pulse triggers – ADINT0/1 interrupt EOC (End of conversion) pulse triggers – BPWM triggers • Supports PDMA transfer • Auto turn on/off ADC power at power down or operation mode with wait state
DAC	• Up to two 12-bit 1 MSPS voltage type DAC • Analog output voltage: 0~V_{REF} (AV_{DD}) • Supports 8-bit and 12-bit mode • Rail to rail settle time 6us • Reference voltage selects from internal reference voltage, AV_{DD} or V_{REF} pin • Max. output voltage AV_{DD} -0.2V at buffer mode • Conversion started by software enable, Timer interrupt flag(TIF) or PDMA trigger • Voltage output buffer mode and bypass voltage output buffer mode

	• Supports PDMA mode
Analog Comparator (ACMP)	• Up to two rail-to-rail analog comparators • 4 multiplexed I/O pins at positive node • Negative node: – One I/O pin – Band-gap (VBG) – DAC0 output – Comparator Reference Voltage (CRV) • Programmable propagation speed and low power consumption • Interrupts generated when compare results change (Interrupt event condition programmable) • Supports Power-down Wake-up • Supports triggers for break events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: – 0 mV, 10 mV, 20 mV or 30 mV
Internal Reference Voltage	• Internal reference voltage select: 1.536V, 2.048V, 2.560V, 3.072V, 4.096V for EADC, DAC and CRV (comparator reference voltage) reference voltage
Capactitive Touch	• Supports up to 24 touch keys. • Supports flexible reference channel setting, at least 1 reference channel needed. • Programmable sensitivity levels for each channel • Programmable scanning speed for different applications. • Supports any touch key wake-up for low-power applications. • Supports single key-scan and programmable periodic key-scan. • Programmable interrupt options for key-scan complete with or without threshold control. • Supports independent reference capacitor bank (RefCB) registers for each channels • Supports Timer0~3 time-out interrupt signal(TIF) to trigger touch key scan
Com/Seg LCD	• Supports the following COM/SEG configurations: – Up to 352 dots (8-COM x 44-SEG) – Up to 276 dots (6-COM x 46-SEG) – Up to 192 dots (4-COM x 48-SEG)

	• Supports maximum 8 COM driving pins, multiplexed with GPIO pins • Supports maximum 48 SEG driving pins, multiplexed with GPIO pins • Supports 3 bias voltage levels 1/2, 1/3, and 1/4 • Supports 8 duty ratios 1, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, and 1/8 • Supports clock frequency divider from 0 to 1023 to configure the LCD operating frequency • Configurable frame counting event interrupt period • Supports LCD blinking display controlled by frame counting event • Supports LCD frame end interrupt • LCD keeps display or blinking even if in Power-down mode when LCD clock source is selected as LIRC or LXT • Supports both type A and type B driving waveforms • Programmable Charge Pump output voltage VLCD from 3.0V ~ 5.2V • Selectable VLCD source from Charge Pump output or external pin • Programmable buffer enable selection to enhance COM and SEG driving capability • With internal resistive series network to generate reference voltage for COM and SEG voltage • With big resistor series network to save power and small resistor series network to drive COM and SEG directly by software selection. • LCD panel loading detect feature
Communication Interfaces	
UART	• Supports up to 4 UARTs: UART0, UART1, UART2 and UART3 • UART baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode • Baud rate up to 10 Mbps • Full-duplex asynchronous communications • Supports one-wire half-duplex communications • Separates receive and transmit 16/16 bytes FIFO • Programmable receiver buffer trigger level • Hardware auto-flow control (CTS and RTS) • IrDA (SIR) function – Supports 3/16 bit duration for normal mode • RS-485 9-bit mode and direction control • UART0 supports LIN function

	– LIN master/slave mode – Programmable break generation function for transmitter – Break detection function for receiver • Programmable baud-rate generator up to 1/16 system clock • 8-bit receiver FIFO time-out detection function • Programmable transmitting data delay time between the last stop and the next start bit • Auto-Baud Rate measurement and baud rate compensation function • Break error, frame error, parity error and receive/transmit FIFO overflow detection function • Supports RS-485 mode: – RS-485 9-bit mode – Hardware or software enables to program nRTS pin to control RS-485 transmission direction – nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in Power-down mode. – Hardware or software enables to program nRTS pin to control RS-485 transmission direction • Fully programmable serial-interface: – Programmable number of data bit, 5-, 6-, 7-, 8- bit character – Programmable parity bit, even, odd, no parity or stick parity bit generation and detection – Programmable stop bit, 1, 1.5, or 2 stop bit generation • Supports PDMA mode
Smart Card Interface	**Smart card mode** • ISO 7816-3 T = 0, T = 1 compliant • EMV2000 compliant • One ISO 7816-3 port • Separates receive/transmit 4 byte entry FIFO for data payloads • Programmable transmission clock frequency • Programmable receiver buffer trigger level • Programmable guard time selection (11 ETU ~ 267 ETU) • One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing • Supports auto direct / inverse convention function • Supports transmitter and receiver error retry and error number limiting function • Supports hardware activation sequence process, and the time

	between PWR on and CLK start is configurable • Supports hardware warm reset sequence process • Supports hardware deactivation sequence process • Supports hardware auto deactivation sequence when the card removal is detected **UART mode** • Full duplex, asynchronous communications • Separates receiving / transmitting 4 bytes entry FIFO for data payloads • Supports programmable baud rate generator • Supports programmable receiver buffer trigger level • Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion • Programmable even, odd or no parity bit generation and detection • Programmable stop bit, 1- or 2- stop bit generation
SPI	• Supports Master or Slave mode operation • Master and slave mode up to 25 MHz (when chip works at V_{DD} = 3.0 ~ 5.5V) • Supports 2-bit Transfer mode • Supports Dual and Quad I/O Transfer mode • Configurable bit length of a transaction word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports Byte Reorder function • Supports Byte or Word Suspend mode • Supports PDMA transfer • Supports 3-Wire, no slave selection signal, bi-direction interface • Supports one data channel half-duplex transfer • Supports receive-only mode
I²C	• Up to 2 sets of I²C devices • Master/Slave mode • Bidirectional data transfer between masters and slaves • Multi-master bus (no central master) • 7-bit and 10-bit addressing mode • Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Arbitration between simultaneously transmitting masters without

	corruption of serial data on the bus • Serial clock synchronization allows devices with different bit rates to communicate via one serial bus • Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer • Supports 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows • Programmable clocks allow versatile rate control • Multiple address recognition (four slave address with mask option) • Supports setup/hold time programmable • Supports SMBus and PMBus • Multi-address Power-down wake-up function • Supports PDMA transfer
SPI/I^2S	**SPI Mode** • Up to 2 sets of SPI controllers • Master or Slave mode operation • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depended on SPI setting of data width • MSB first or LSB first transfer sequence • Supports byte reorder function • Byte or Word Suspend mode • Master and slave mode up to 25 MHz (V_{DD} = 3.0V ~5.5V) • Supports one data channel half-duplex transfer • Supports receive-only mode • Supports PDMA transfer **I^2S Mode** • Up to 2 sets of I^2S by SPI controllers • Interface with external audio CODEC • Supports Master and Slave mode • Capable of handling 8-, 16-, 24- and 32-bit word sizes • Mono and stereo audio data • PCM mode A, PCM mode B, I^2S and MSB justified data format • Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving • Generates interrupt requests when buffer levels cross a programmable boundary

	• Each supports two PDMA requests, one for transmitting and the other for receiving
Universal Serial Control Interface (USCI)	• Up to 2 sets of USCI • Supports UART, SPI and I²C function • Single byte TX and RX buffer mode **USCI_UART** • One transmit buffer and two receive buffer for data payload • Hardware auto flow control function and programmable flow control trigger level • Programmable baud-rate generator • Supports 9-bit data transfer • Baud rate detection by built-in capture event of baud rate generator • Supports Wake-up function (Data and nCTS Wakeup Only) • Supports PDMA transfer **USCI_SPI** • Master or Slave mode operation • Configurable bit length of a transfer word from 4 to 16-bit • One transmit buffer and two receive buffer for data payload • MSB first or LSB first transfer sequence • Word suspend function • Supports PDMA transfer • Supports 3-wire, no slave select signal, bi-direction interface • Wake-up function: input slave select transition • Supports one data channel half-duplex transfer **USCI_I2C** • Full master and slave device capability • 7-bit/10-bit addressing mode • Communication in Standard mode (100 kbps), Fast mode (up to 400 kbps) and Fast mode plus (1 Mbps) • Multi-master bus • One transmit buffer and two receive buffer for data payload • 10-bit bus time out capability • Supports Bus monitor mode • Wake-up by data toggle or address match in Power-down mode • Multiple address recognition • Setup/hold time programmable

GPIO	• Four I/O modes:
	  – Quasi bi-direction
	  – Push-Pull output
	  – Open-Drain output
	  – Input only with high impendence
	• TTL/Schmitt trigger input selectable
	• I/O pin configured as interrupt source with edge/level trigger setting
	• Independent pull-up/pull-down control
	• High driver and high sink current I/O (up to 16 mA at 5V, 25°C)
	• Minimum I/O Speed
	  – 25 MHz when V_{DD} = 2.7 ~ 5.5 V (-40°C ~ +105°C, CL=30p, high skew rate enabled)
	  – 10 MHz when V_{DD} = 1.75 ~ 5.5 V (-40°C ~ +105°C, CL=30p, high skew rate enabled)
	• Software selectable slew rate control
	• Supports wake-up function
	• Supports I/O de-bounce with LIRC at power down
	• I/O configurations of multi-function pin are controlled by module or MFOS register settings
	• Supports 5V tolerance except PF2, PF3, PF4 and PF5 pins

Advanced Connectivity	
USB 2.0 Full Speed	• Compliant with USB 2.0 Full-Speed specification • Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS) • Suspend function when no bus activity exists for 3 ms • Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1024 bytes buffer size • Provides remote wake-up capability • Start of Frame (SOF) locked clock pulse generation • Supports USB 2.0 Link Power Management (LPM) • Supports Crystal-less function • Supports Battery charging 1.2 (BC1.2)

3 PARTS INFORMATION

3.1 Package Type

Part No.	LQFP44	LQFP64	LQFP80	LQFP128
M254xD	M254MD2AE	M254SD2AE M254SD3AE		
M254xE		M254SE3AE	M254QE3AE	M254KE3AE
M254xG		M254SG6AE		M254KG6AE
M256xD	M256MD2AE	M256SD2AE		
M256xE		M256SE3AE	M256QE3AE	M256KE3AE
M256xG			M256QG6AE	
M258xE		M258SE3AE	M258QE3AE	M258KE3AE
M258xG		M258SG6AE	M258QG6AE	M258KG6AE

3.2 M254/M256/M258 Series Selection Guide

3.2.1 M254 LCD Series

PART NUMBER		M254MD2AE	M254SD2AE	M254SD3AE	M254SE3AE	M254SG6AE	M254QE3AE	M254KE3AE	M254KG6AE
Flash (KB)		64	64	64	128	256	128	128	256
SRAM (KB)		8	8	16	16	32	16	16	32
LDROM (KB)		4							
PLL (MHz)		-							
LXT		√							
I/O 5V tolerance		√							
I/O		37	54	53	53	53	70	86	86
32-bit Timer/PWM		4							
PWM		-							
BPWM		6	6	6	6	12	6	6	12
WDT/WWDT		√							
RTC		√							
Connectivity	USCI*	1	1	1	1	2	1	1	2
	UART	3	3	3	3	4	3	3	4
	SPI /I²S	1	1	1	1	2	1	1	2
	I²C	1	1	1	1	2	1	1	2
	SC/UART	1							
	PSIO	-							
12-bit ADC		12	16	16	16	16	16	16	16
12-bit DAC		-	-	-	-	2	-	-	2
ACMP		2							
PDMA		5	5	5	5	8	5	5	8
Capactitive Touch		-							
COM/SEG LCD Driver		4 x 20 6 x 18 8 x 16	4 x 32 6 x 30 8 x 28	4 x 32 6 x 30 8 x 28	4 x 32 6 x 30 8 x 28	4 x 32 6 x 30 8 x 28	4 x 48 6 x 46 8 x 44	4 x 48 6 x 46 8 x 44	4 x 48 6 x 46 8 x 44
V_{BAT} pin		-	-	√	√	√	-	√	√
Internal V_{REF}		-	√	√	√	√	√	√	√
Package		LQFP44	LQFP64				LQFP80	LQFP128	

USCI*: supports UART, SPI or I²C

3.2.2 M256 LCD + Touch Series

PART NUMBER		M256MD2AE	M256SD2AE	M256SE3AE	M256KE3AE	M256QE3AE	M256QG6AE
Flash (KB)		64	64	128	128	128	256
SRAM (KB)		8	8	16	16	16	32
LDROM (KB)		4					
PLL (MHz)		-					
LXT		√					
I/O 5V tolerance		√					
I/O		37	54	53	86	70	70
32-bit Timer/PWM		4					
PWM		-					
BPWM		6					12
WDT/WWDT		√					
RTC		√					
Connectivity	USCI*	1					2
	UART	3					4
	SPI /I²S	1					2
	I²C	1					2
	SC/UART	1					
	PSIO	-					
12-bit ADC		12	16	16	16	16	16
12-bit DAC		-					2
ACMP		2					
PDMA		5	5	5	5	5	8
Capactitive Touch		6	14	14	15	15	23
COM/SEG LCD Driver		4 x 20 6 x 18 8 x 16	4 x 32 6 x 30 8 x 28	4 x 32 6 x 30 8 x 28	4 x 48 6 x 46 8 x 44	4 x 48 6 x 46 8 x 44	4 x 48 6 x 46 8 x 44
V_{BAT} pin		-	-	√	√	-	-
Internal V_{REF}		-	√	√	√	√	√
Package		LQFP44	LQFP64		LQFP128	LQFP80	

USCI*: supports UART, SPI or I²C

3.2.3 M258 LCD + Touch + USB Series

PART NUMBER		M258SE3AE	M258SG6AE	M258KE3AE	M258KG6AE	M258QE3AE	M258QG6AE
Flash (KB)		128	256	128	256	128	256
SRAM (KB)		16	32	16	32	16	32
LDROM (KB)		4					
PLL (MHz)		-					
LXT		√					
I/O 5V tolerance		√					
I/O		49	49	82	82	66	66
32-bit Timer/PWM		4					
PWM		-					
BPWM		6	12	6	12	6	12
WDT/WWDT		√					
RTC		√					
Connectivity	USCI*	1	2	1	2	1	2
	UART	3	4	3	4	3	4
	SPI /I^{2}S	1	2	1	2	1	2
	I^{2}C	1	2	1	2	1	2
	SC/UART	1					
	PSIO	-					
	USB 2.0 FS	√	√	√	√	√	√
12-bit ADC		16					
12-bit DAC		-	2	-	2	-	2
ACMP		2					
PDMA		5	8	5	8	5	8
Capactitive Touch		14	20	15	24	15	23
COM/SEG LCD Driver		4 x 28 6 x 26 8 x 24	4 x 28 6 x 26 8 x 24	4 x 44 6 x 42 8 x 40	4 x 44 6 x 42 8 x 40	4 x 44 6 x 42 8 x 40	4 x 44 6 x 42 8 x 40
V_{BAT} pin		√	√	√	√	-	-
Internal V_{REF}		√	√	√	√	√	√
Package		LQFP64		LQFP128		LQFP80	

USCI*: supports UART, SPI or I^{2}C

3.2.4 Naming Rule

M2	51	S	E	3	A	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
Cortex®-M23	51: Control 52: USB 54: LCD 56: LCD, Touch 58: LCD, Touch, USB	F: TSSOP20 (4.4x6.5 mm) E: TSSOP28 (4.4x9.7 mm) Z: QFN33 (5x5 mm) M: LQFP44 (10x10 mm) L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm) Q: LQFP80 (14x14 mm) K: LQFP128 (14x14 mm)	C: 32 KB D: 64 KB E: 128 KB G: 256 KB	2: 8/12 KB 3: 16 KB 6: 32 KB		E: -40°C ~ +105°C

4 PIN CONFIGURATION

Users can find pin configuration information in chapter 4 or by using NuTool - PinConfig. The NuTool - PinConfigure contains all NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 M254 Series Pin Diagram

4.1.1.1 M254 Series LQFP 44-Pin Diagram

Corresponding Part Number: M254MD2AE

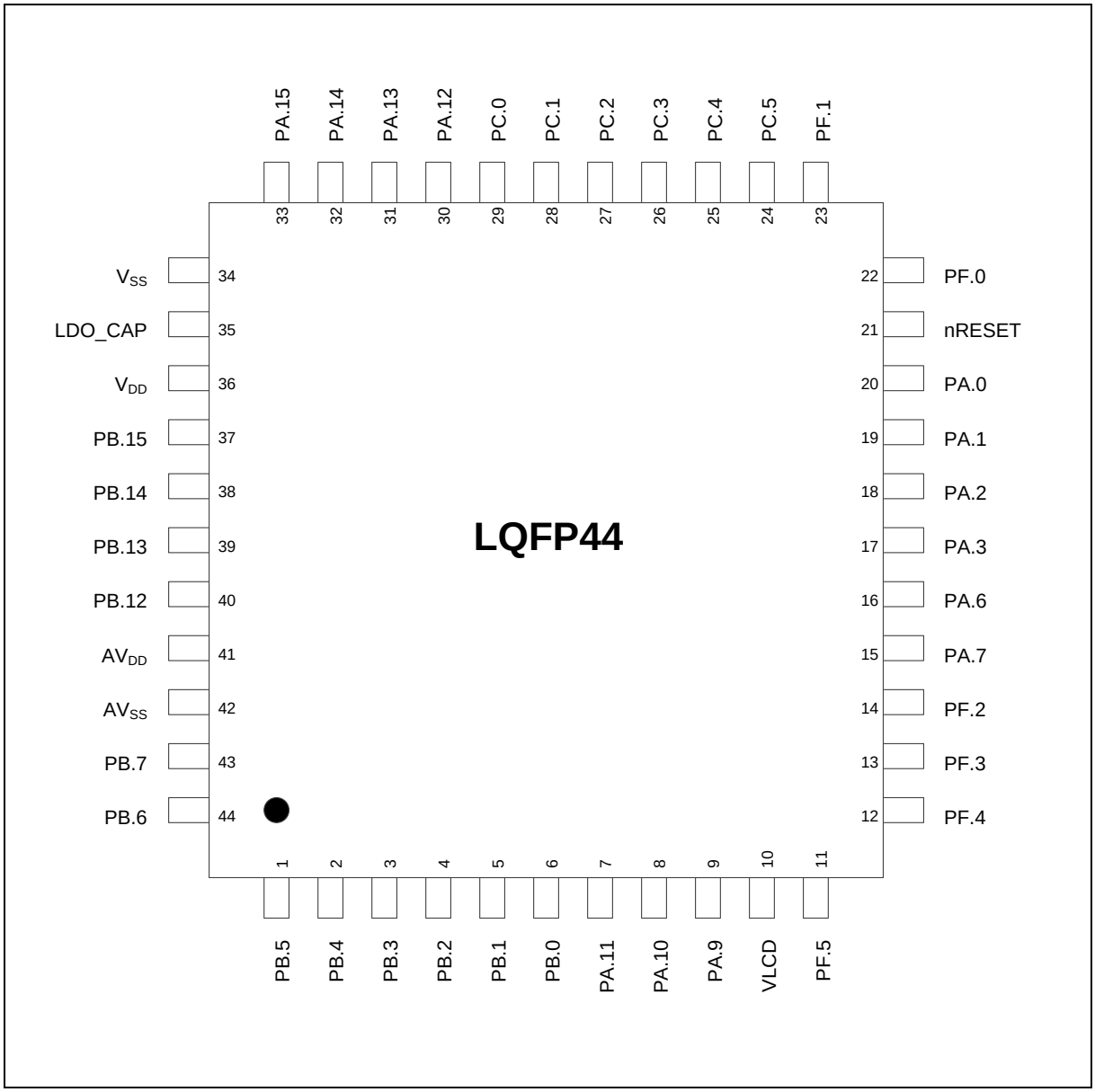


Figure 4.1-1 M254 Series LQFP 44-pin Diagram

4.1.1.2 M254 Series LQFP 64-Pin Diagram

Corresponding Part Number: M254SD2AE

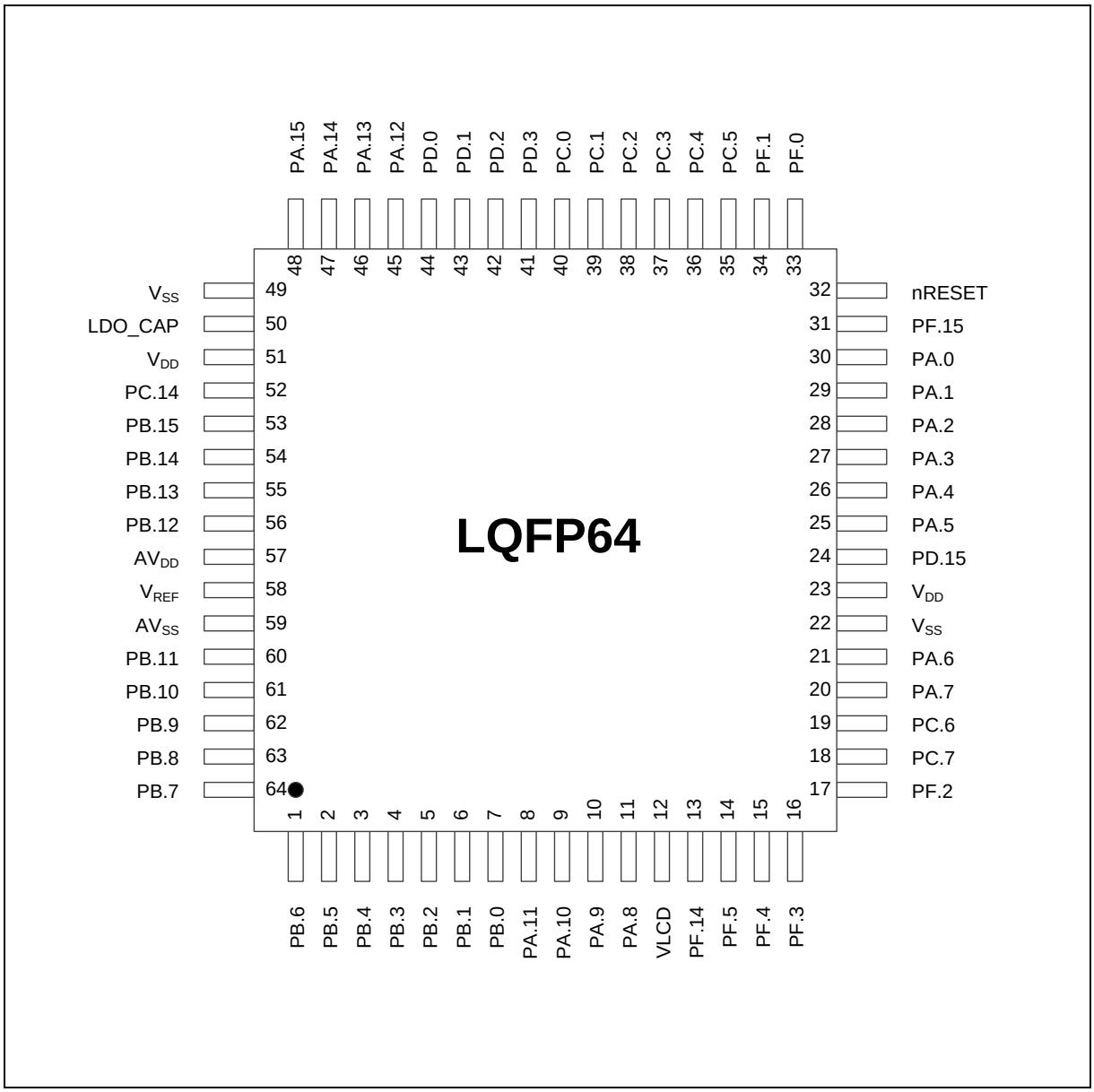


Figure 4.1-2 M254 Series LQFP 64-pin Diagram without V_{BAT}

Corresponding Part Number: M254SD3AE, M254SE3AE, M254SG6AE

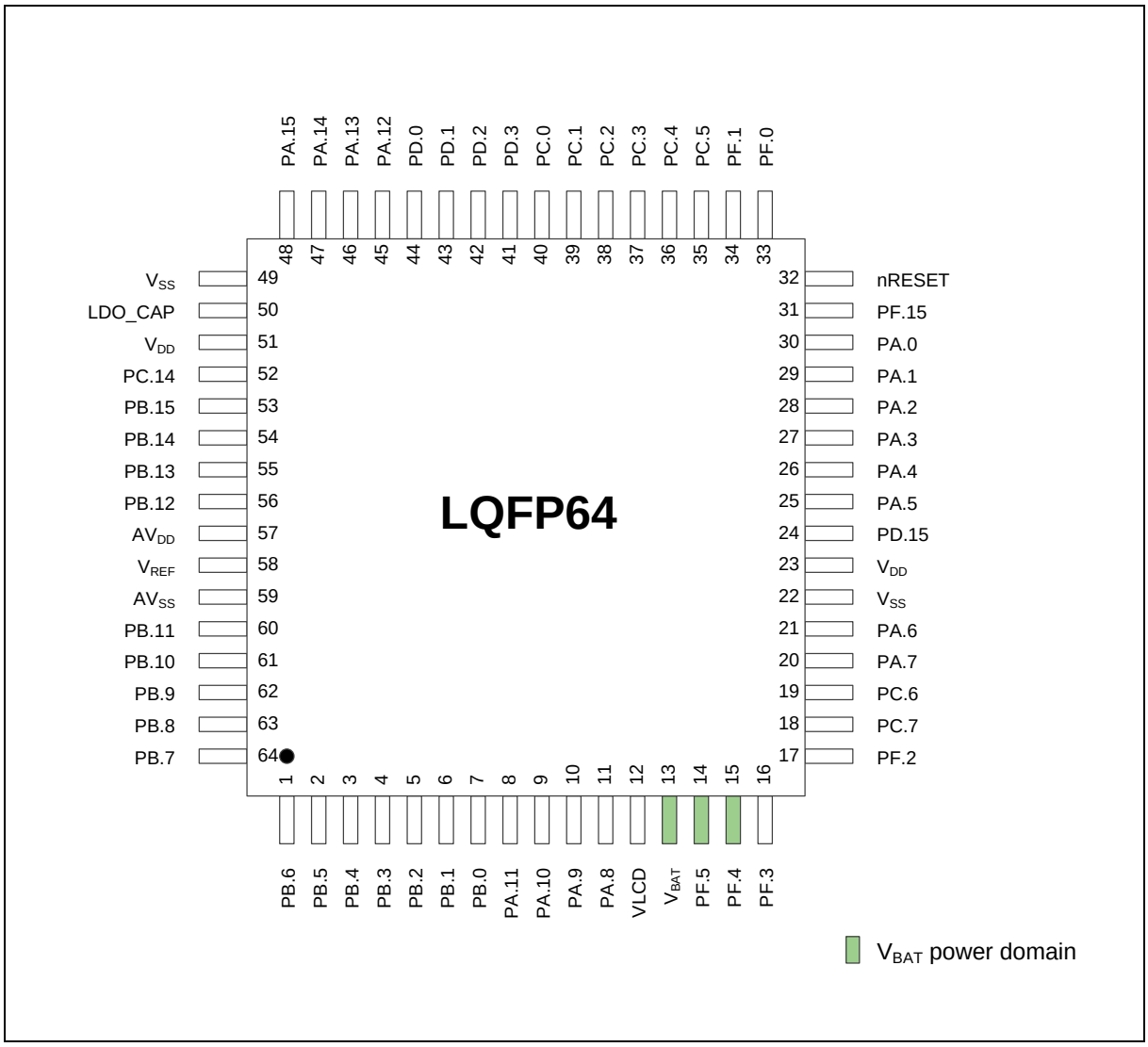


Figure 4.1-3 M254 Series LQFP 64-pin Diagram with V_{BAT}

4.1.1.3 M254 Series LQFP 80-Pin Diagram

Corresponding Part Number: M254QE3AE

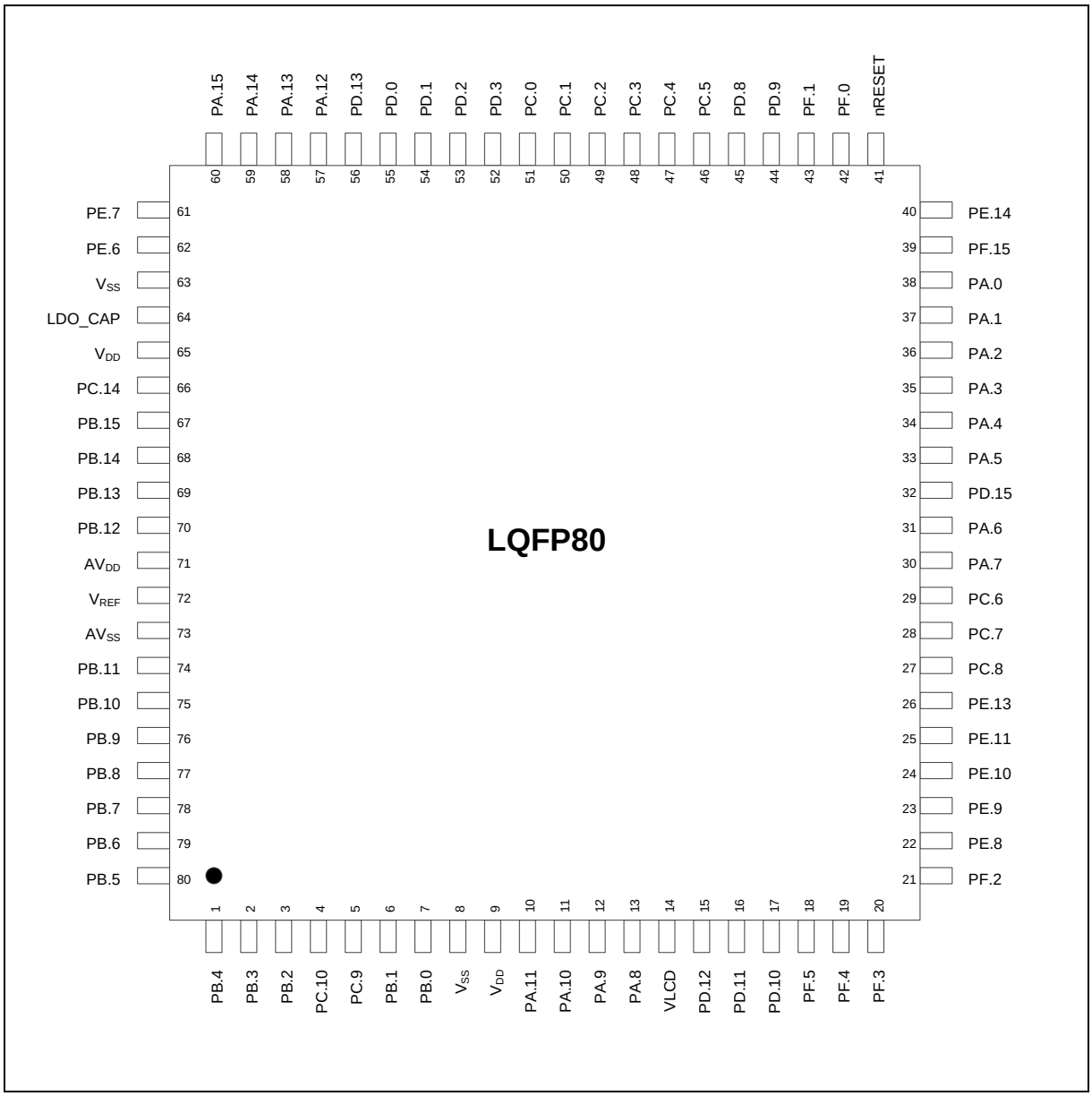


Figure 4.1-4 M254 Series LQFP 80-pin Diagram

4.1.1.4 M254 Series LQFP 128-Pin Diagram

Corresponding Part Number: M254KE3AE, M254KG6AE

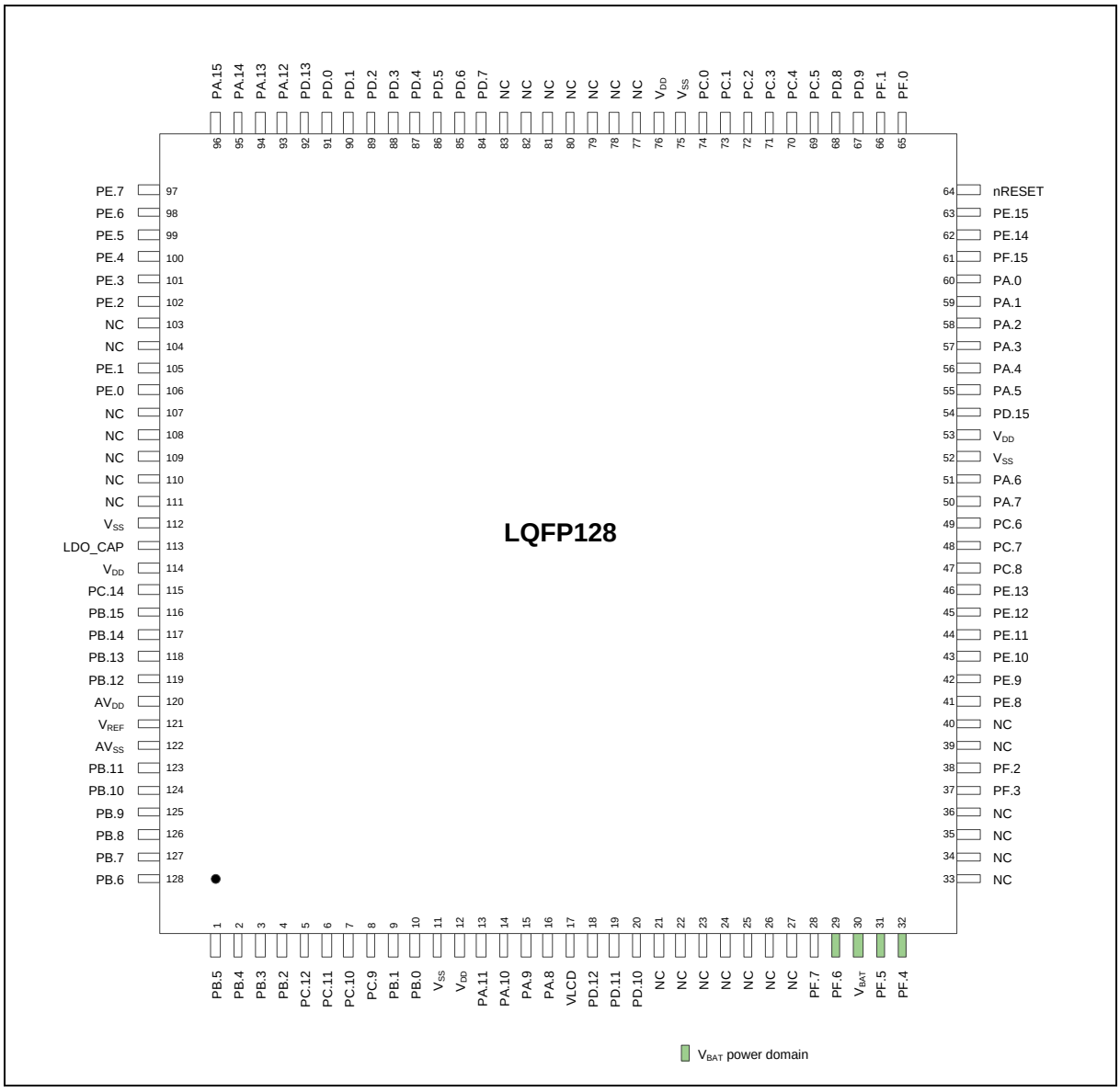


Figure 4.1-5 M254 Series LQFP 128-pin Diagram

4.1.2 M254 Series Multi-function Pin Diagram

4.1.2.1 M254 Series LQFP 44-Pin Multi-function Pin Diagram

Corresponding Part Number: M254MD2AE

M254MD2AE

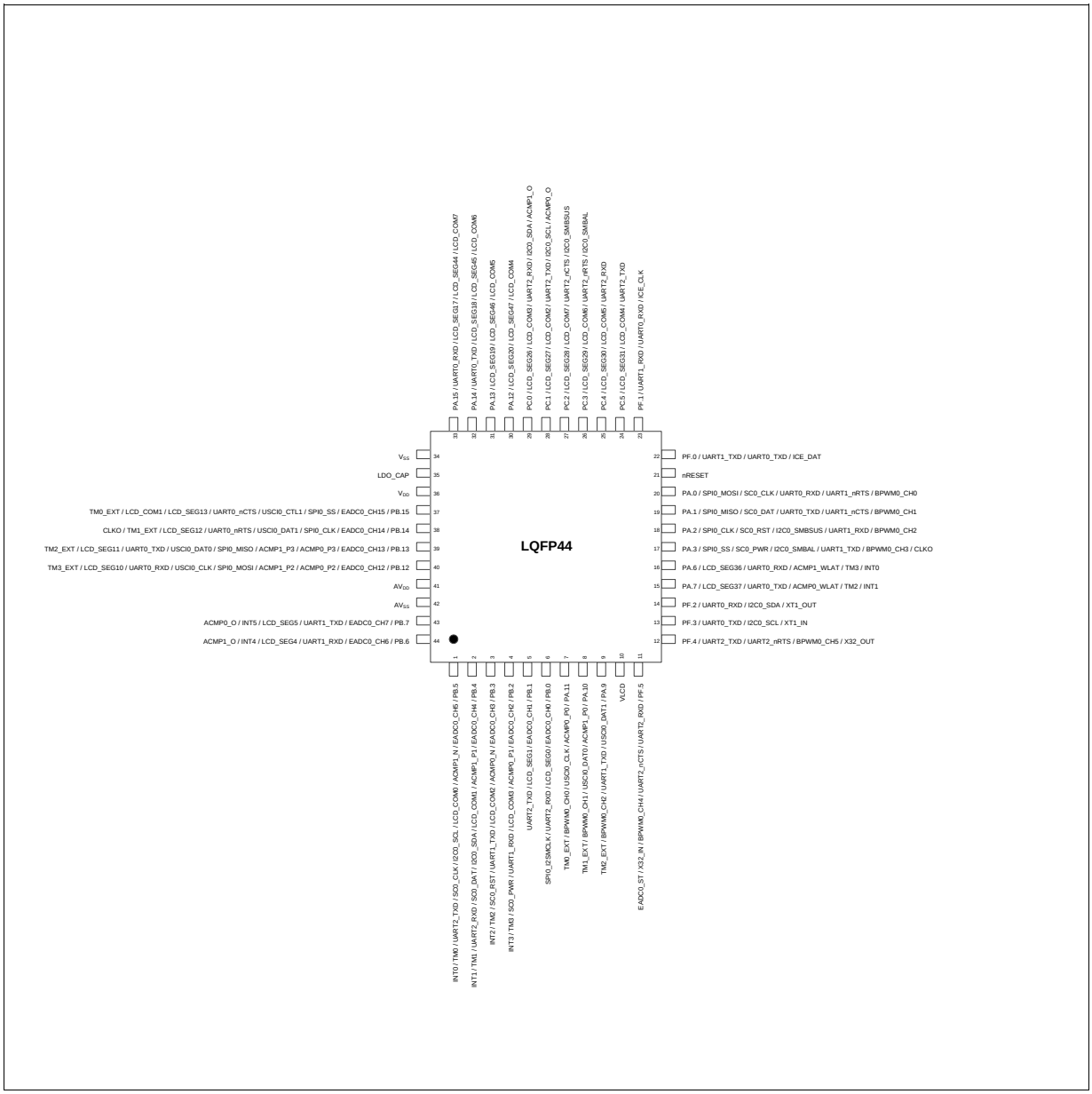


Figure 4.1-6 M254MD2AE Multi-function Pin Diagram

Pin	Type	M254MD2AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
5	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
6	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
7	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
9	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
10	P	V_{LCD}
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
15	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.3 / SPI0_SS / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
18	I/O	PA.2 / SPI0_CLK / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
19	I/O	PA.1 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
20	I/O	PA.0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
21	I	nRESET
22	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
23	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
24	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD
25	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD
26	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / UART2_nRTS / I2C0_SMBAL
27	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / UART2_nCTS / I2C0_SMBSUS
28	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
29	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
30	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
31	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
32	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
33	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
34	P	V_{SS}
35	A	LDO_CAP

Pin	Type	M254MD2AE Pin Function
36	P	V_{DD}
37	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
38	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO
39	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
40	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
41	P	AV_{DD}
42	P	AV_{SS}
43	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O
44	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O

Table 4.1-1 M254MD2AE Multi-function Pin Table

4.1.2.2 M254 Series LQFP 64-Pin Multi-function Pin Diagram

Corresponding Part Number: M254SD2AE, M254SD3AE, M254SE3AE, M254SG6AE

M254SD2AE

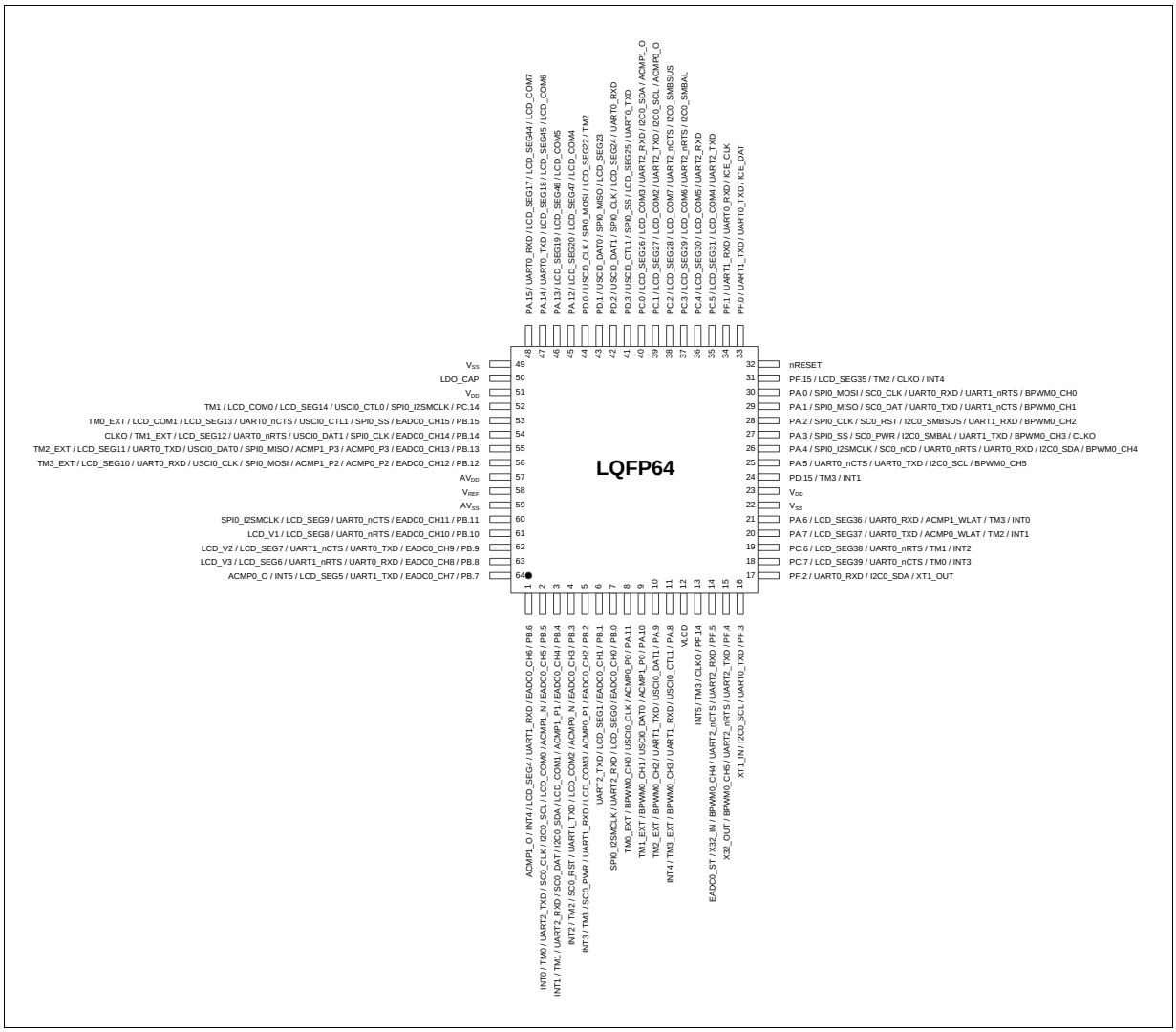


Figure 4.1-7 M254SD2AE Multi-function Pin Diagram

Pin	Type	M254SD2AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
8	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	P	V_{LCD}
13	I/O	PF.14 / CLKO / TM3 / INT5
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
18	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
19	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
20	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / TM3 / INT1
25	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
26	I/O	PA.4 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
27	I/O	PA.3 / SPI0_SS / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
28	I/O	PA.2 / SPI0_CLK / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
29	I/O	PA.1 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
30	I/O	PA.0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
31	I/O	PF.15 / LCD_SEG35 / TM2 / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
34	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
35	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD

Pin	Type	M254SD2AE Pin Function
36	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD
37	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / UART2_nRTS / I2C0_SMBAL
38	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / UART2_nCTS / I2C0_SMBSUS
39	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
40	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
41	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / UART0_TXD
42	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / UART0_RXD
43	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23
44	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TM2
45	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
46	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
47	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
48	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
53	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
54	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
61	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
62	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
63	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
64	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O

Table 4.1-2 M254SD2AE Multi-function Pin Table

M254SD3AE/M254SE3AE

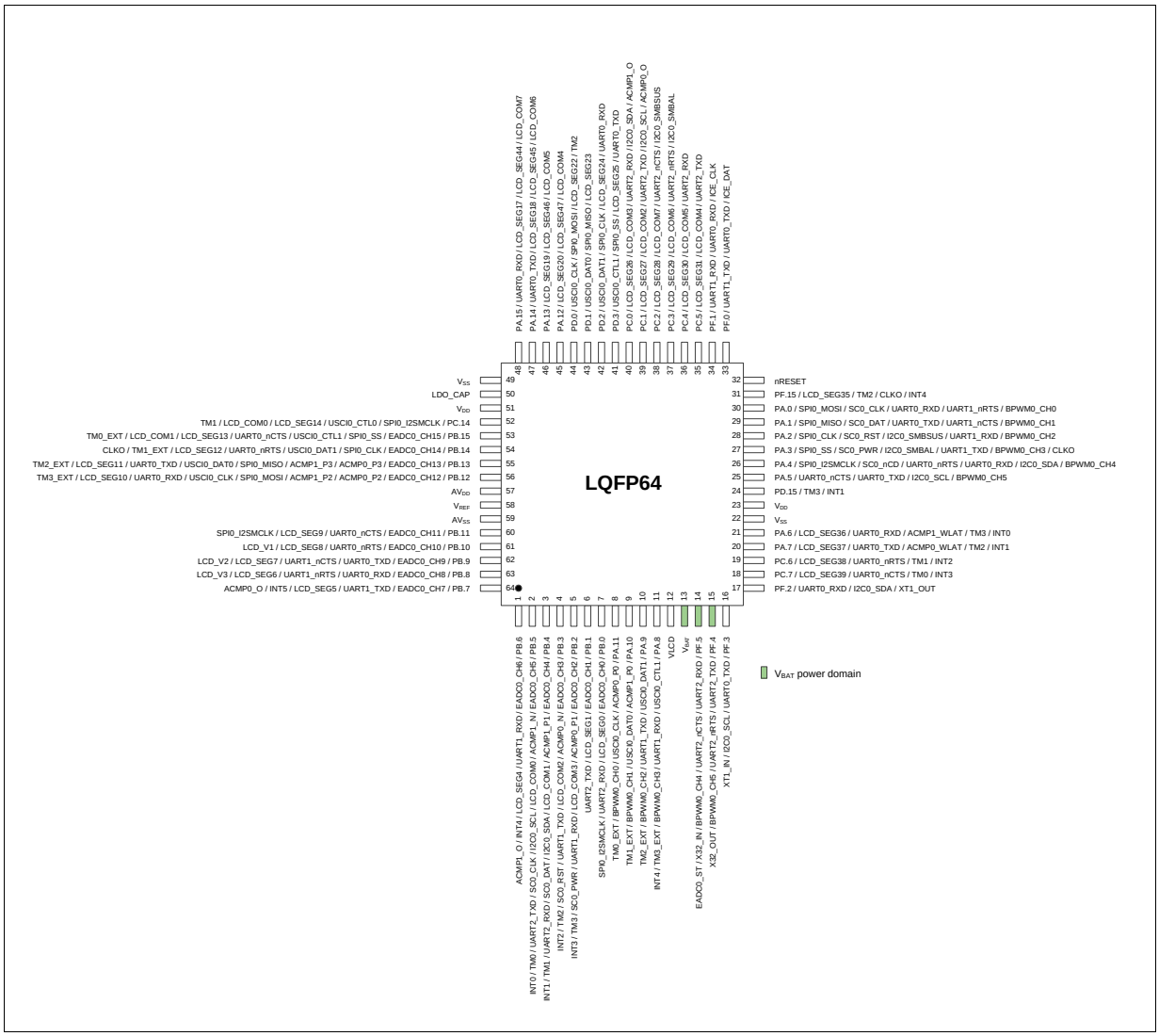


Figure 4.1-8 M254SD3AE/M254SE3AE Multi-function Pin Diagram

Pin	Type	M254SD3AE/M254SE3AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
8	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	P	V_{LCD}
13	P	V_{BAT}
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
18	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
19	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
20	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / TM3 / INT1
25	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
26	I/O	PA.4 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
27	I/O	PA.3 / SPI0_SS / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
28	I/O	PA.2 / SPI0_CLK / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
29	I/O	PA.1 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
30	I/O	PA.0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
31	I/O	PF.15 / LCD_SEG35 / TM2 / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
34	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
35	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD

Pin	Type	M254SD3AE/M254SE3AE Pin Function
36	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD
37	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / UART2_nRTS / I2C0_SMBAL
38	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / UART2_nCTS / I2C0_SMBSUS
39	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
40	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
41	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / UART0_TXD
42	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / UART0_RXD
43	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23
44	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TM2
45	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
46	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
47	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
48	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
53	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
54	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
61	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
62	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
63	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
64	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O

Table 4.1-3 M254SD3AE/M254SE3AE Multi-function Pin Table

M254SG6AE

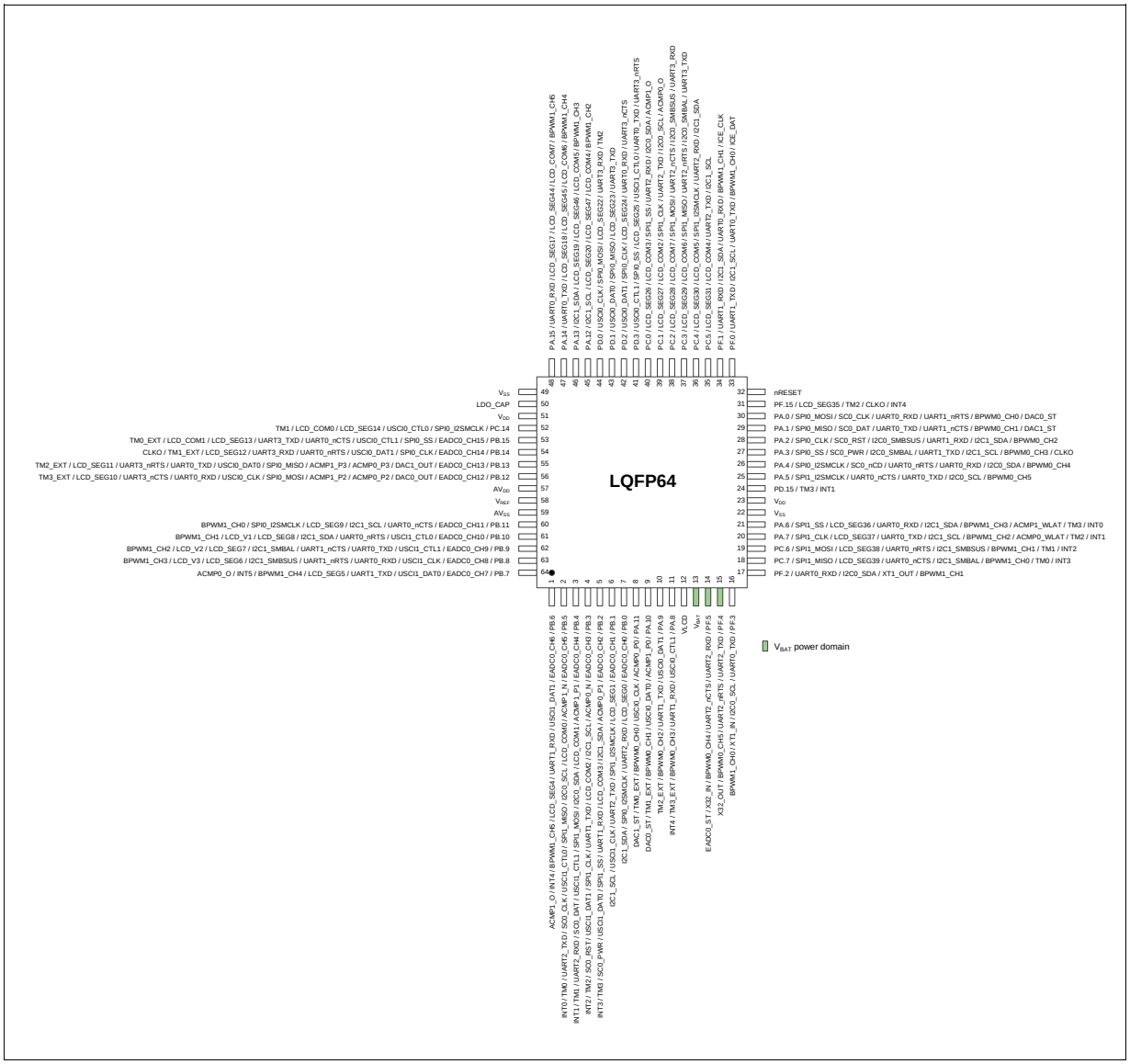


Figure 4.1-9 M254SG6AE Multi-function Pin Diagram

Pin	Type	M254SG6AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / UART1_RXD / LCD_SEG4 / BPWM1_CH5 / INT4 / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SPI1_MISO / USCI1_CTL0 / SC0_CLK / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SPI1_MOSI / USCI1_CTL1 / SC0_DAT / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / I2C1_SCL / LCD_COM2 / UART1_TXD / SPI1_CLK / USCI1_DAT1 / SC0_RST / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / I2C1_SDA / LCD_COM3 / UART1_RXD / SPI1_SS / USCI1_DAT0 / SC0_PWR / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA
8	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT / DAC1_ST
9	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT / DAC0_ST
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	P	V_{LCD}
13	P	V_{BAT}
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT / BPWM1_CH1
18	I/O	PC.7 / SPI1_MISO / LCD_SEG39 / UART0_nCTS / I2C1_SMBAL / BPWM1_CH0 / TM0 / INT3
19	I/O	PC.6 / SPI1_MOSI / LCD_SEG38 / UART0_nRTS / I2C1_SMBSUS / BPWM1_CH1 / TM1 / INT2
20	I/O	PA.7 / SPI1_CLK / LCD_SEG37 / UART0_TXD / I2C1_SCL / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / SPI1_SS / LCD_SEG36 / UART0_RXD / I2C1_SDA / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / TM3 / INT1
25	I/O	PA.5 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
26	I/O	PA.4 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
27	I/O	PA.3 / SPI0_SS / SC0_PWR / I2C0_SMBAL / UART1_TXD / I2C1_SCL / BPWM0_CH3 / CLKO
28	I/O	PA.2 / SPI0_CLK / SC0_RST / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / BPWM0_CH2
29	I/O	PA.1 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / DAC1_ST
30	I/O	PA.0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0 / DAC0_ST
31	I/O	PF.15 / LCD_SEG35 / TM2 / CLKO / INT4
32	I	nRESET

Pin	Type	M254SG6AE Pin Function
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
35	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD / I2C1_SCL
36	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA
37	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD
38	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD
39	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / SPI1_CLK / UART2_TXD / I2C0_SCL / ACMP0_O
40	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / SPI1_SS / UART2_RXD / I2C0_SDA / ACMP1_O
41	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / USCI1_CTL0 / UART0_TXD / UART3_nRTS
42	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / UART0_RXD / UART3_nCTS
43	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / UART3_TXD
44	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / UART3_RXD / TM2
45	I/O	PA.12 / I2C1_SCL / LCD_SEG20 / LCD_SEG47 / LCD_COM4 / BPWM1_CH2
46	I/O	PA.13 / I2C1_SDA / LCD_SEG19 / LCD_SEG46 / LCD_COM5 / BPWM1_CH3
47	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6 / BPWM1_CH4
48	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7 / BPWM1_CH5
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
53	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / LCD_SEG13 / LCD_COM1 / TM0_EXT
54	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / LCD_SEG12 / TM1_EXT / CLKO
55	I/O	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / LCD_SEG11 / TM2_EXT
56	I/O	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / LCD_SEG10 / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / I2C1_SCL / LCD_SEG9 / SPI0_I2SMCLK / BPWM1_CH0
61	I/O	PB.10 / EADC0_CH10 / USCI1_CTL0 / UART0_nRTS / I2C1_SDA / LCD_SEG8 / LCD_V1 / BPWM1_CH1
62	I/O	PB.9 / EADC0_CH9 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / LCD_SEG7 / LCD_V2 / BPWM1_CH2
63	I/O	PB.8 / EADC0_CH8 / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / LCD_SEG6 / LCD_V3 / BPWM1_CH3

Pin	Type	M254SG6AE Pin Function
64	I/O	PB.7 / EADC0_CH7 / USCI1_DAT0 / UART1_TXD / LCD_SEG5 / BPWM1_CH4 / INT5 / ACMP0_O

Table 4.1-4 M254SG6AE Multi-function Pin Table

4.1.2.3 M254 Series LQFP 80-Pin Multi-function Pin Diagram

Corresponding Part Number: M254QE3AE

M254QE3AE

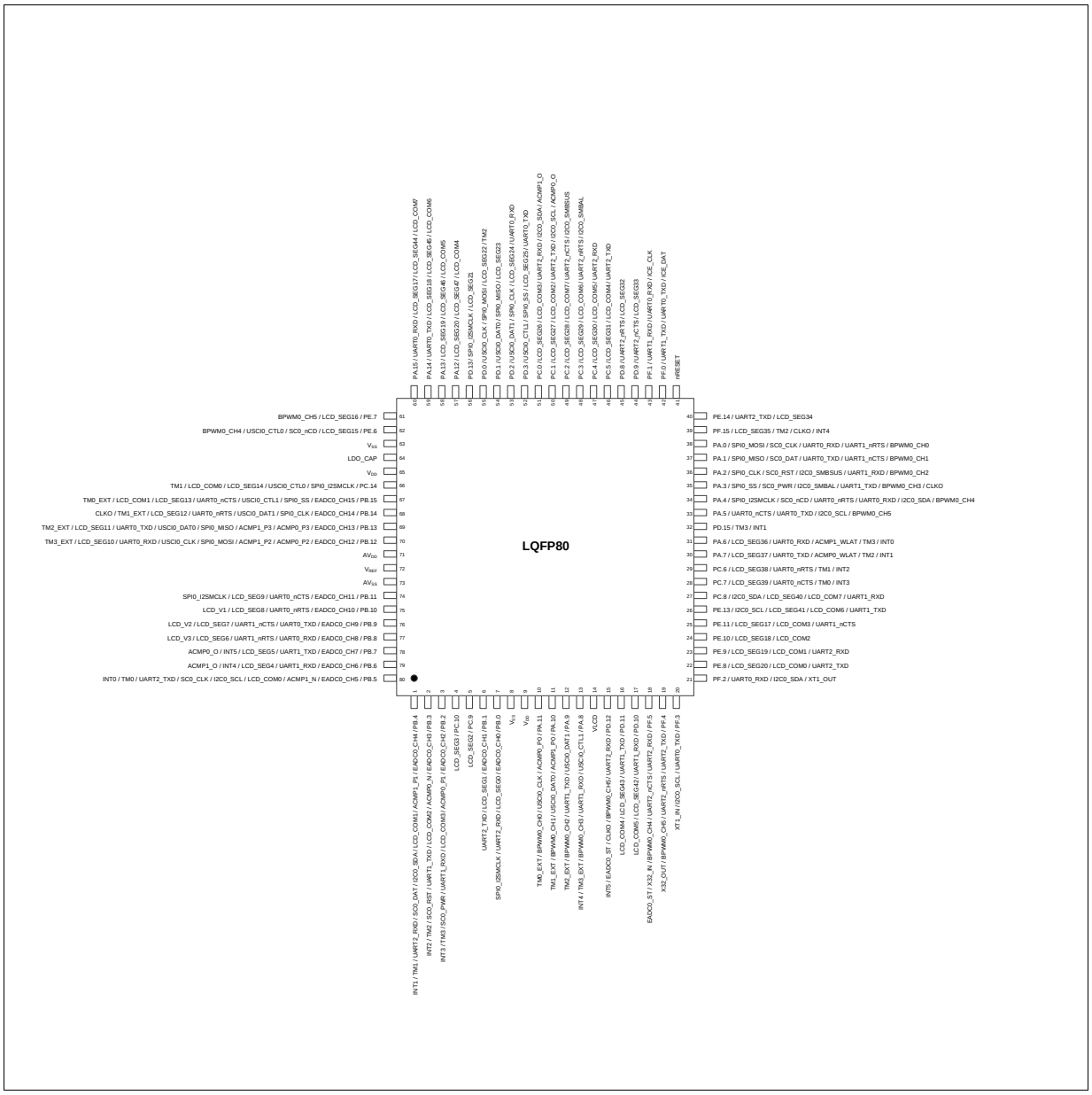


Figure 4.1-10 M254QE3AE Multi-function Pin Diagram

Pin	Type	M254QE3AE Pin Function
1	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
2	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
3	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
4	I/O	PC.10 / LCD_SEG3
5	I/O	PC.9 / LCD_SEG2
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
8	P	V_{SS}
9	P	V_{DD}
10	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
11	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
12	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
13	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
14	P	V_{LCD}
15	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / CLKO / EADC0_ST / INT5
16	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
17	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
18	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
19	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
20	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
21	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
22	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / UART2_TXD
23	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / UART2_RXD
24	I/O	PE.10 / LCD_SEG18 / LCD_COM2
25	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / UART1_nCTS
26	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD
27	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD
28	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
29	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
30	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
31	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
32	I/O	PD.15 / TM3 / INT1
33	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
34	I/O	PA.4 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
35	I/O	PA.3 / SPI0_SS / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO

Pin	Type	M254QE3AE Pin Function
36	I/O	PA.2 / SPI0_CLK / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
37	I/O	PA.1 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
38	I/O	PA.0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
39	I/O	PF.15 / LCD_SEG35 / TM2 / CLKO / INT4
40	I/O	PE.14 / UART2_TXD / LCD_SEG34
41	I	nRESET
42	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
43	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
44	I/O	PD.9 / UART2_nCTS / LCD_SEG33
45	I/O	PD.8 / UART2_nRTS / LCD_SEG32
46	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD
47	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD
48	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / UART2_nRTS / I2C0_SMBAL
49	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / UART2_nCTS / I2C0_SMBSUS
50	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
51	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
52	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / UART0_TXD
53	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / UART0_RXD
54	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23
55	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TM2
56	I/O	PD.13 / SPI0_I2SMCLK / LCD_SEG21
57	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
58	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
59	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
60	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
61	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
62	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
63	P	V_{SS}
64	A	LDO_CAP
65	P	V_{DD}
66	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
67	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
68	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO
69	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT

Pin	Type	M254QE3AE Pin Function
70	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
71	P	AV_{DD}
72	A	V_{REF}
73	P	AV_{SS}
74	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
75	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
76	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
77	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
78	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O
79	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O
80	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0

Table 4.1-5 M254QE3AE Multi-function Pin Table

4.1.2.4 M254 Series LQFP 128-Pin Multi-function Pin Diagram

Corresponding Part Number: M254KE3AE, M254KG6AE

M254KE3AE

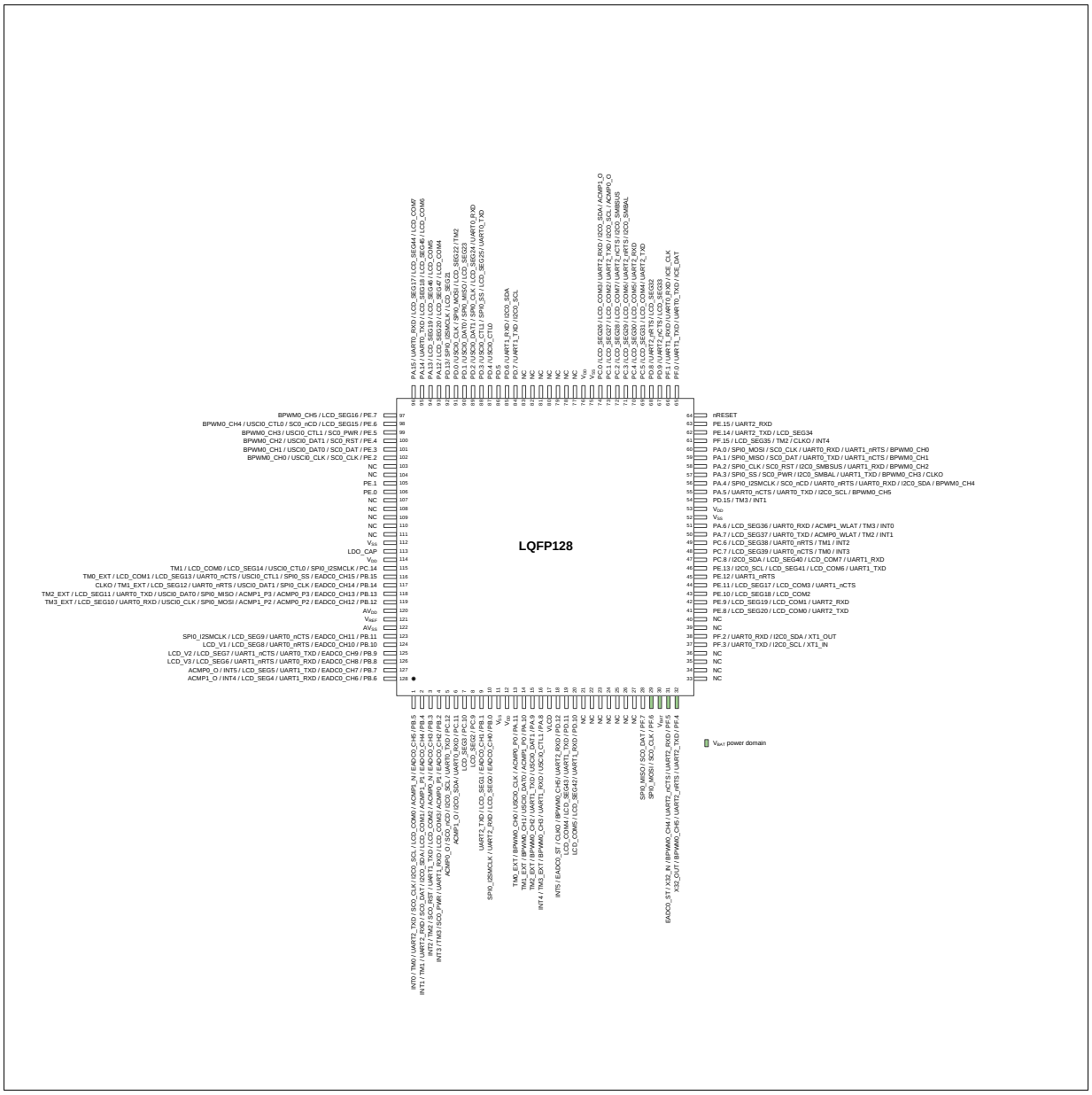


Figure 4.1-11 M254KE3AE Multi-function Pin Diagram

Pin	Type	M254KE3AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
5	I/O	PC.12 / UART0_TXD / I2C0_SCL / SC0_nCD / ACMP0_O
6	I/O	PC.11 / UART0_RXD / I2C0_SDA / ACMP1_O
7	I/O	PC.10 / LCD_SEG3
8	I/O	PC.9 / LCD_SEG2
9	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
10	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
14	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
15	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
16	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
17	P	V_{LCD}
18	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
20	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
21	-	NC
22	-	NC
23	-	NC
24	-	NC
25	-	NC
26	-	NC
27	-	NC
28	I/O	PF.7 / SC0_DAT / SPI0_MISO
29	I/O	PF.6 / SC0_CLK / SPI0_MOSI
30	P	V_{BAT}
31	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
33	-	NC
34	-	NC
35	-	NC

Pin	Type	M254KE3AE Pin Function
36	-	NC
37	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
38	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
39	-	NC
40	-	NC
41	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / UART2_TXD
42	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / UART2_RXD
43	I/O	PE.10 / LCD_SEG18 / LCD_COM2
44	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / UART1_nCTS
45	I/O	PE.12 / UART1_nRTS
46	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD
47	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD
48	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
49	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
50	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
51	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	I/O	PD.15 / TM3 / INT1
55	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
56	I/O	PA.4 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
57	I/O	PA.3 / SPI0_SS / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
58	I/O	PA.2 / SPI0_CLK / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
59	I/O	PA.1 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
60	I/O	PA.0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
61	I/O	PF.15 / LCD_SEG35 / TM2 / CLKO / INT4
62	I/O	PE.14 / UART2_TXD / LCD_SEG34
63	I/O	PE.15 / UART2_RXD
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
66	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
67	I/O	PD.9 / UART2_nCTS / LCD_SEG33
68	I/O	PD.8 / UART2_nRTS / LCD_SEG32
69	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD
70	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / UART2_RXD

Pin	Type	M254KE3AE Pin Function
71	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / UART2_nRTS / I2C0_SMBAL
72	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / UART2_nCTS / I2C0_SMBSUS
73	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
74	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
75	P	V_{SS}
76	P	V_{DD}
77	-	NC
78	-	NC
79	-	NC
80	-	NC
81	-	NC
82	-	NC
83	-	NC
84	I/O	PD.7 / UART1_TXD / I2C0_SCL
85	I/O	PD.6 / UART1_RXD / I2C0_SDA
86	I/O	PD.5
87	I/O	PD.4 / USCI0_CTL0
88	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / UART0_TXD
89	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / UART0_RXD
90	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23
91	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TM2
92	I/O	PD.13 / SPI0_I2SMCLK / LCD_SEG21
93	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
94	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
95	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
96	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
97	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
98	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
99	I/O	PE.5 / SC0_PWR / USCI0_CTL1 / BPWM0_CH3
100	I/O	PE.4 / SC0_RST / USCI0_DAT1 / BPWM0_CH2
101	I/O	PE.3 / SC0_DAT / USCI0_DAT0 / BPWM0_CH1
102	I/O	PE.2 / SC0_CLK / USCI0_CLK / BPWM0_CH0
103	-	NC
104	-	NC
105	I/O	PE.1

Pin	Type	M254KE3AE Pin Function
106	I/O	PE.0
107	-	NC
108	-	NC
109	-	NC
110	-	NC
111	-	NC
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
116	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
117	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO
118	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
119	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
124	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
125	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
126	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
127	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O

Table 4.1-6 M254KE3AE Multi-function Pin Table

M254KG6AE

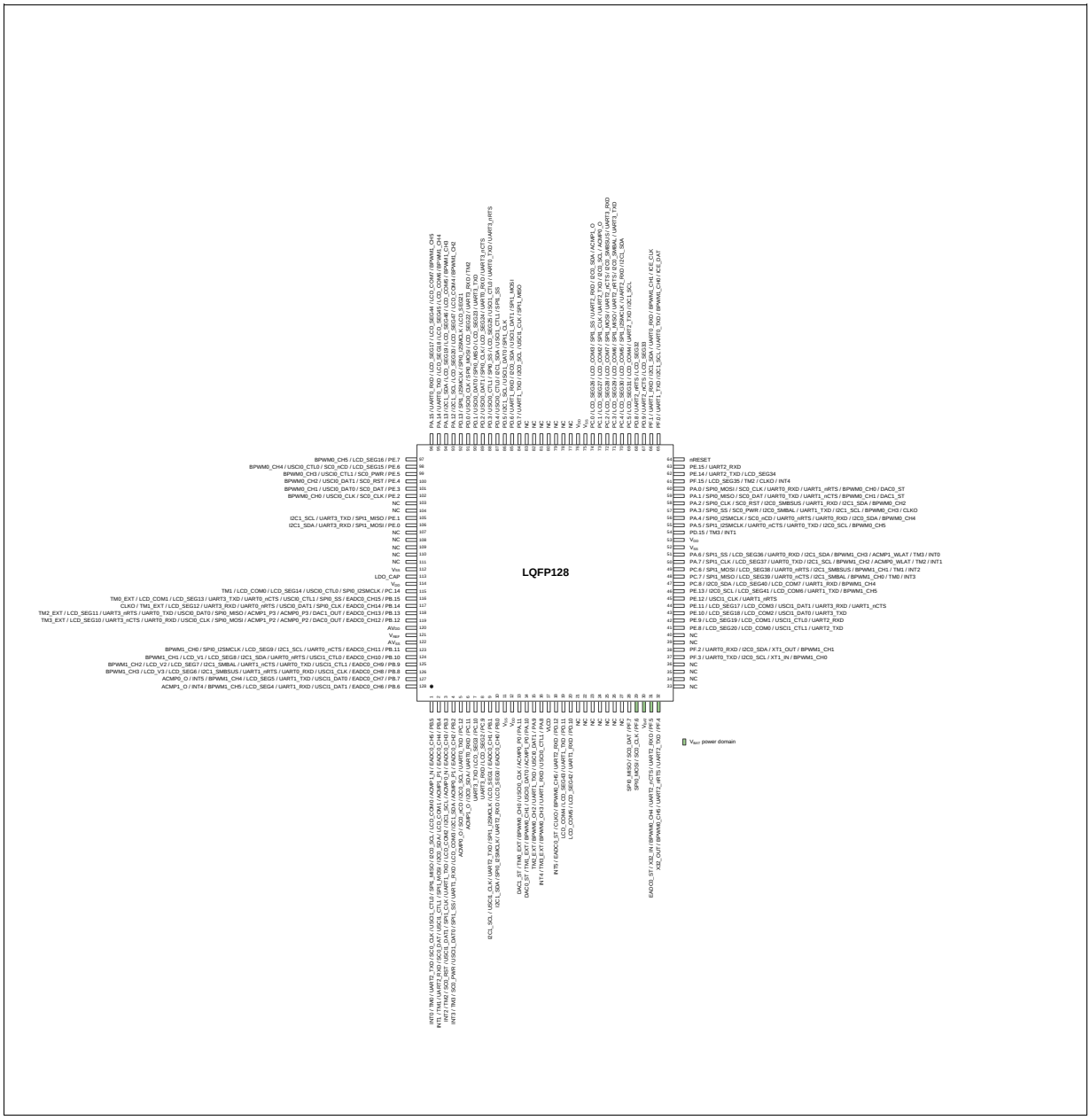


Figure 4.1-12 M254KG6AE Multi-function Pin Diagram

Pin	Type	M254KG6AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SPI1_MISO / USCI1_CTL0 / SC0_CLK / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SPI1_MOSI / USCI1_CTL1 / SC0_DAT / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / I2C1_SCL / LCD_COM2 / UART1_TXD / SPI1_CLK / USCI1_DAT1 / SC0_RST / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / I2C1_SDA / LCD_COM3 / UART1_RXD / SPI1_SS / USCI1_DAT0 / SC0_PWR / TM3 / INT3
5	I/O	PC.12 / UART0_TXD / I2C0_SCL / SC0_nCD / ACMP0_O
6	I/O	PC.11 / UART0_RXD / I2C0_SDA / ACMP1_O
7	I/O	PC.10 / LCD_SEG3 / UART3_TXD
8	I/O	PC.9 / LCD_SEG2 / UART3_RXD
9	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL
10	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT / DAC1_ST
14	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT / DAC0_ST
15	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
16	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
17	P	V_{LCD}
18	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
20	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
21	-	NC
22	-	NC
23	-	NC
24	-	NC
25	-	NC
26	-	NC
27	-	NC
28	I/O	PF.7 / SC0_DAT / SPI0_MISO
29	I/O	PF.6 / SC0_CLK / SPI0_MOSI
30	P	V_{BAT}
31	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
33	-	NC

Pin	Type	M254KG6AE Pin Function
34	-	NC
35	-	NC
36	-	NC
37	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
38	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT / BPWM1_CH1
39	-	NC
40	-	NC
41	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / USCI1_CTL1 / UART2_TXD
42	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / USCI1_CTL0 / UART2_RXD
43	I/O	PE.10 / LCD_SEG18 / LCD_COM2 / USCI1_DAT0 / UART3_TXD
44	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / USCI1_DAT1 / UART3_RXD / UART1_nCTS
45	I/O	PE.12 / USCI1_CLK / UART1_nRTS
46	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD / BPWM1_CH5
47	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD / BPWM1_CH4
48	I/O	PC.7 / SPI1_MISO / LCD_SEG39 / UART0_nCTS / I2C1_SMBAL / BPWM1_CH0 / TM0 / INT3
49	I/O	PC.6 / SPI1_MOSI / LCD_SEG38 / UART0_nRTS / I2C1_SMBSUS / BPWM1_CH1 / TM1 / INT2
50	I/O	PA.7 / SPI1_CLK / LCD_SEG37 / UART0_TXD / I2C1_SCL / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
51	I/O	PA.6 / SPI1_SS / LCD_SEG36 / UART0_RXD / I2C1_SDA / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	I/O	PD.15 / TM3 / INT1
55	I/O	PA.5 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
56	I/O	PA.4 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
57	I/O	PA.3 / SPI0_SS / SC0_PWR / I2C0_SMBAL / UART1_TXD / I2C1_SCL / BPWM0_CH3 / CLKO
58	I/O	PA.2 / SPI0_CLK / SC0_RST / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / BPWM0_CH2
59	I/O	PA.1 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / DAC1_ST
60	I/O	PA.0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0 / DAC0_ST
61	I/O	PF.15 / LCD_SEG35 / TM2 / CLKO / INT4
62	I/O	PE.14 / UART2_TXD / LCD_SEG34
63	I/O	PE.15 / UART2_RXD
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
67	I/O	PD.9 / UART2_nCTS / LCD_SEG33

Pin	Type	M254KG6AE Pin Function
68	I/O	PD.8 / UART2_nRTS / LCD_SEG32
69	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / UART2_TXD / I2C1_SCL
70	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA
71	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD
72	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD
73	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / SPI1_CLK / UART2_TXD / I2C0_SCL / ACMP0_O
74	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / SPI1_SS / UART2_RXD / I2C0_SDA / ACMP1_O
75	P	V_{SS}
76	P	V_{DD}
77	-	NC
78	-	NC
79	-	NC
80	-	NC
81	-	NC
82	-	NC
83	-	NC
84	I/O	PD.7 / UART1_TXD / I2C0_SCL / USCI1_CLK / SPI1_MISO
85	I/O	PD.6 / UART1_RXD / I2C0_SDA / USCI1_DAT1 / SPI1_MOSI
86	I/O	PD.5 / I2C1_SCL / USCI1_DAT0 / SPI1_CLK
87	I/O	PD.4 / USCI0_CTL0 / I2C1_SDA / USCI1_CTL1 / SPI1_SS
88	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / USCI1_CTL0 / UART0_TXD / UART3_nRTS
89	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / UART0_RXD / UART3_nCTS
90	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / UART3_TXD
91	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / UART3_RXD / TM2
92	I/O	PD.13 / SPI1_I2SMCLK / SPI0_I2SMCLK / LCD_SEG21
93	I/O	PA.12 / I2C1_SCL / LCD_SEG20 / LCD_SEG47 / LCD_COM4 / BPWM1_CH2
94	I/O	PA.13 / I2C1_SDA / LCD_SEG19 / LCD_SEG46 / LCD_COM5 / BPWM1_CH3
95	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6 / BPWM1_CH4
96	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7 / BPWM1_CH5
97	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
98	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
99	I/O	PE.5 / SC0_PWR / USCI0_CTL1 / BPWM0_CH3
100	I/O	PE.4 / SC0_RST / USCI0_DAT1 / BPWM0_CH2
101	I/O	PE.3 / SC0_DAT / USCI0_DAT0 / BPWM0_CH1
102	I/O	PE.2 / SC0_CLK / USCI0_CLK / BPWM0_CH0

Pin	Type	M254KG6AE Pin Function
103	-	NC
104	-	NC
105	I/O	PE.1 / SPI1_MISO / UART3_TXD / I2C1_SCL
106	I/O	PE.0 / SPI1_MOSI / UART3_RXD / I2C1_SDA
107	-	NC
108	-	NC
109	-	NC
110	-	NC
111	-	NC
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
116	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / LCD_SEG13 / LCD_COM1 / TM0_EXT
117	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / LCD_SEG12 / TM1_EXT / CLKO
118	I/O	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / LCD_SEG11 / TM2_EXT
119	I/O	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / LCD_SEG10 / TM3_EXT
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / I2C1_SCL / LCD_SEG9 / SPI0_I2SMCLK / BPWM1_CH0
124	I/O	PB.10 / EADC0_CH10 / USCI1_CTL0 / UART0_nRTS / I2C1_SDA / LCD_SEG8 / LCD_V1 / BPWM1_CH1
125	I/O	PB.9 / EADC0_CH9 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / LCD_SEG7 / LCD_V2 / BPWM1_CH2
126	I/O	PB.8 / EADC0_CH8 / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / LCD_SEG6 / LCD_V3 / BPWM1_CH3
127	I/O	PB.7 / EADC0_CH7 / USCI1_DAT0 / UART1_TXD / LCD_SEG5 / BPWM1_CH4 / INT5 / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / UART1_RXD / LCD_SEG4 / BPWM1_CH5 / INT4 / ACMP1_O

Table 4.1-7 M254KG6AE Multi-function Pin Table

4.1.3 M256 Series Pin Diagram

4.1.3.1 M256 Series LQFP 44-Pin Diagram

Corresponding Part Number: M256MD2AE

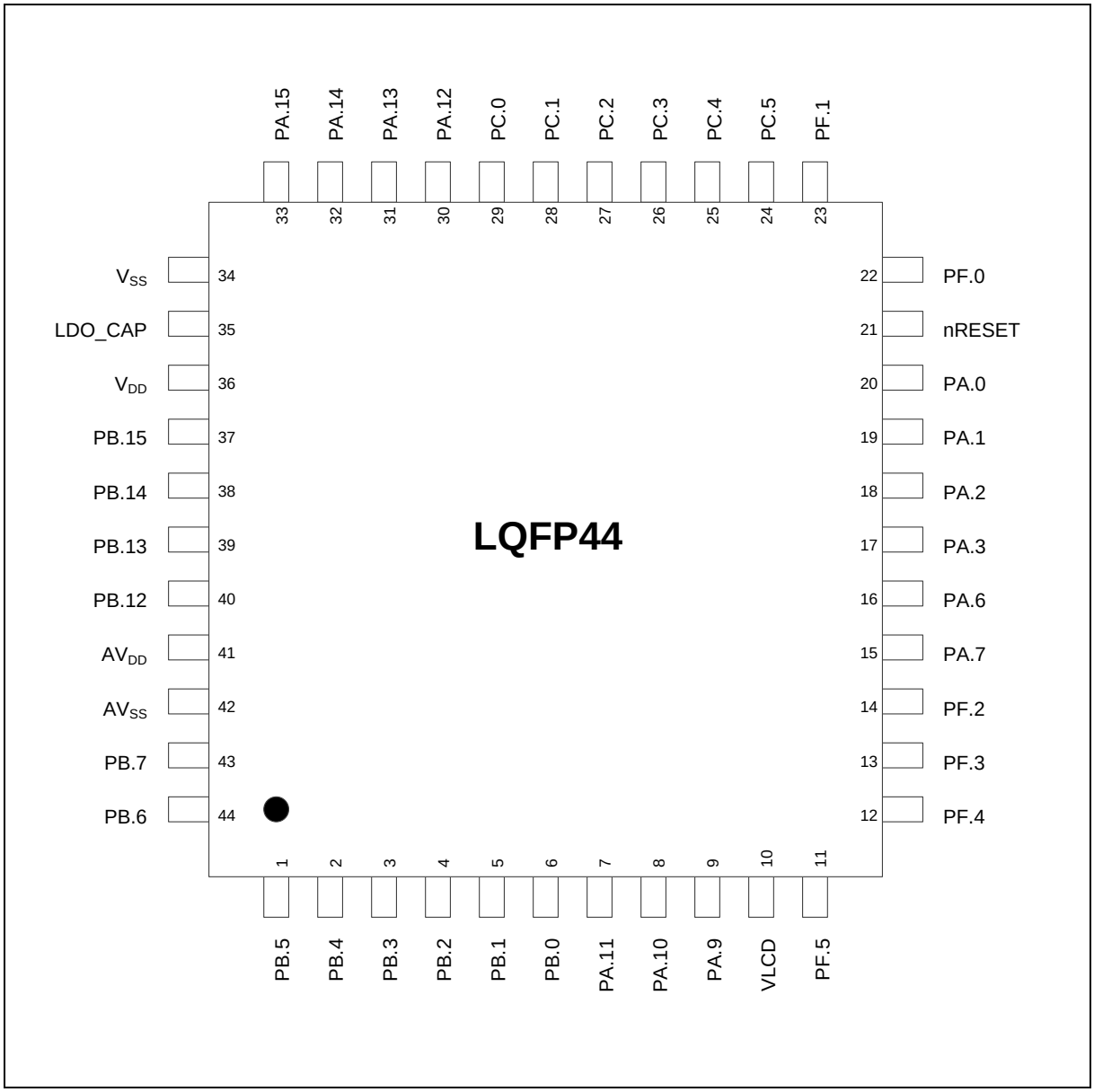


Figure 4.1-13 M256 Series LQFP 44-pin Diagram

4.1.3.2 M256 Series LQFP 64-Pin Diagram

Corresponding Part Number: M256SD2AE

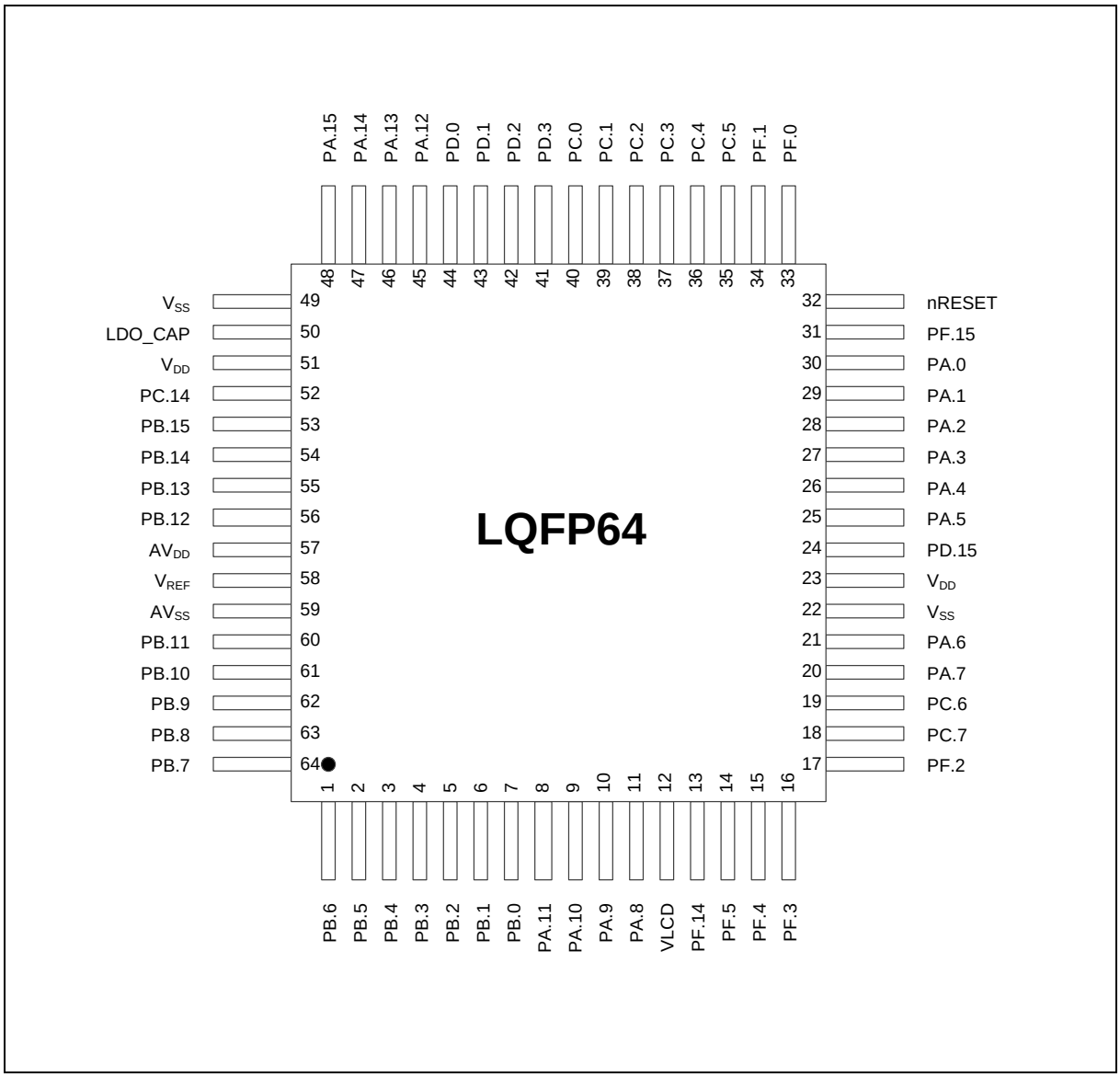


Figure 4.1-14 M256 Series LQFP 64-pin Diagram without V_{BAT}

Corresponding Part Number: M256SE3AE, M256SG6AE

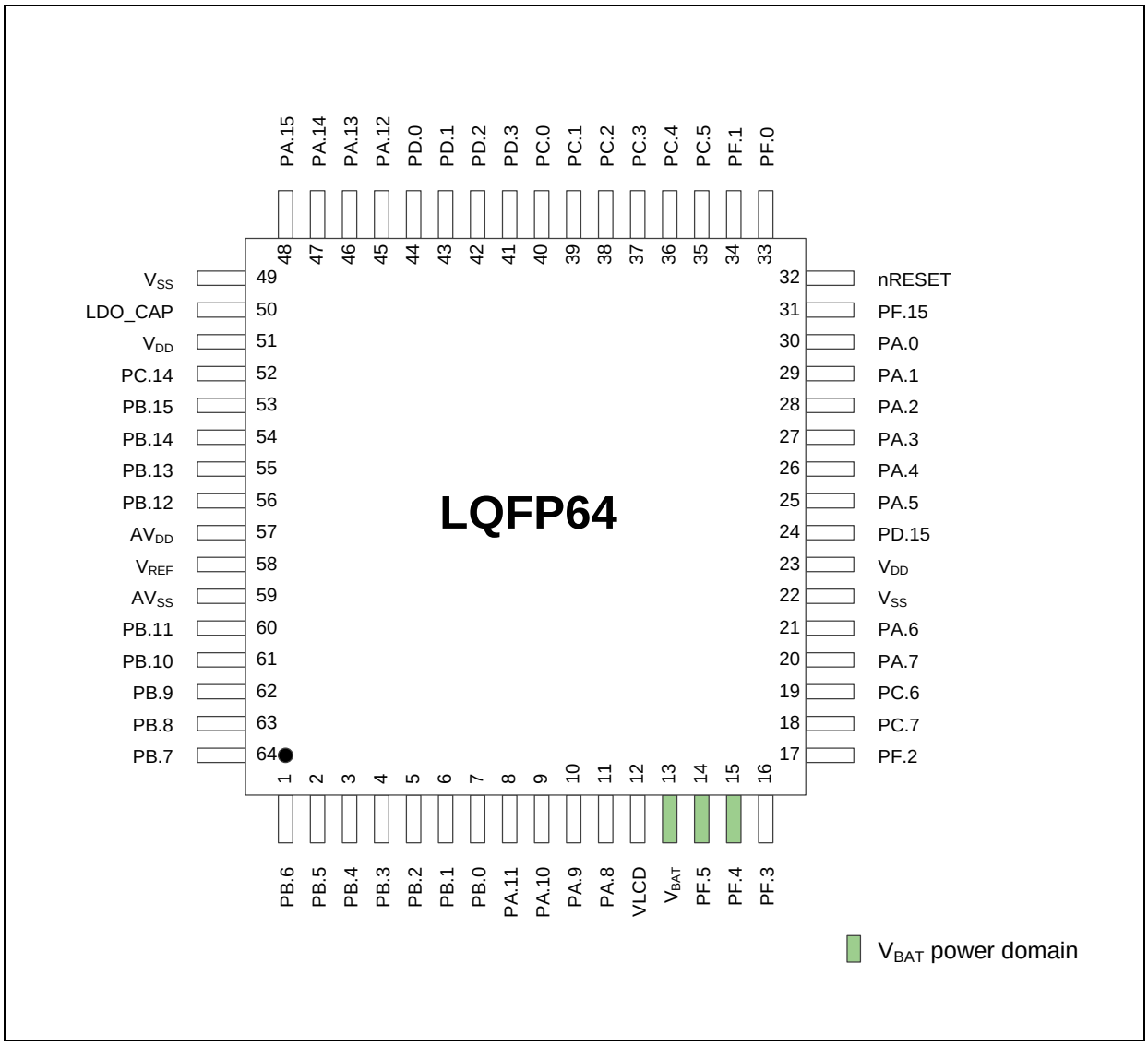


Figure 4.1-15 M256 Series LQFP 64-pin Diagram with V_{BAT}

4.1.3.3 M256 Series LQFP 80-Pin Diagram

Corresponding Part Number: M256QE3AE, M256QG6AE

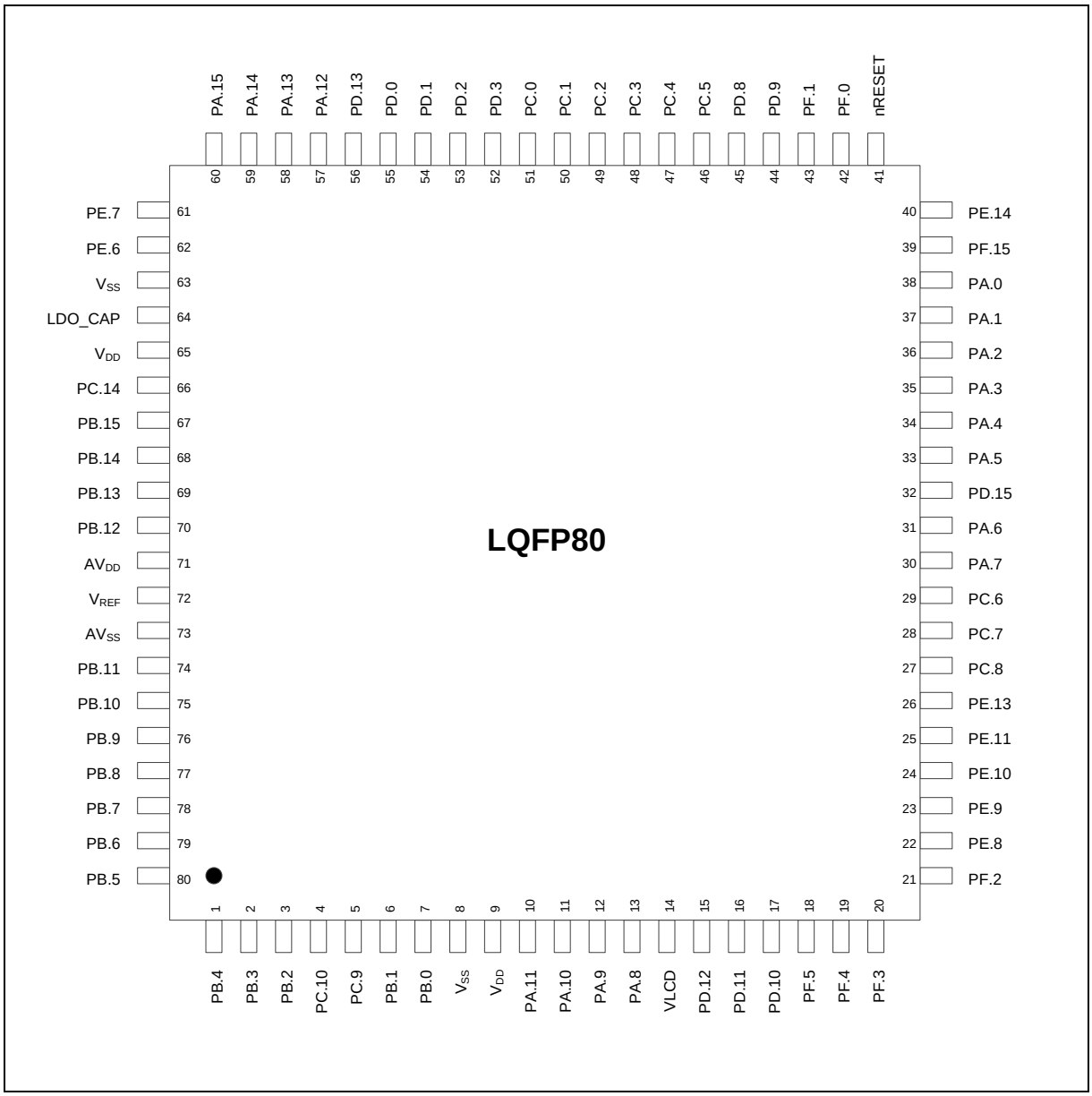


Figure 4.1-16 M256 Sereies LQFP 80-pin Diagram

4.1.3.4 M256 Series LQFP 128-Pin Diagram

Corresponding Part Number: M256KE3AE

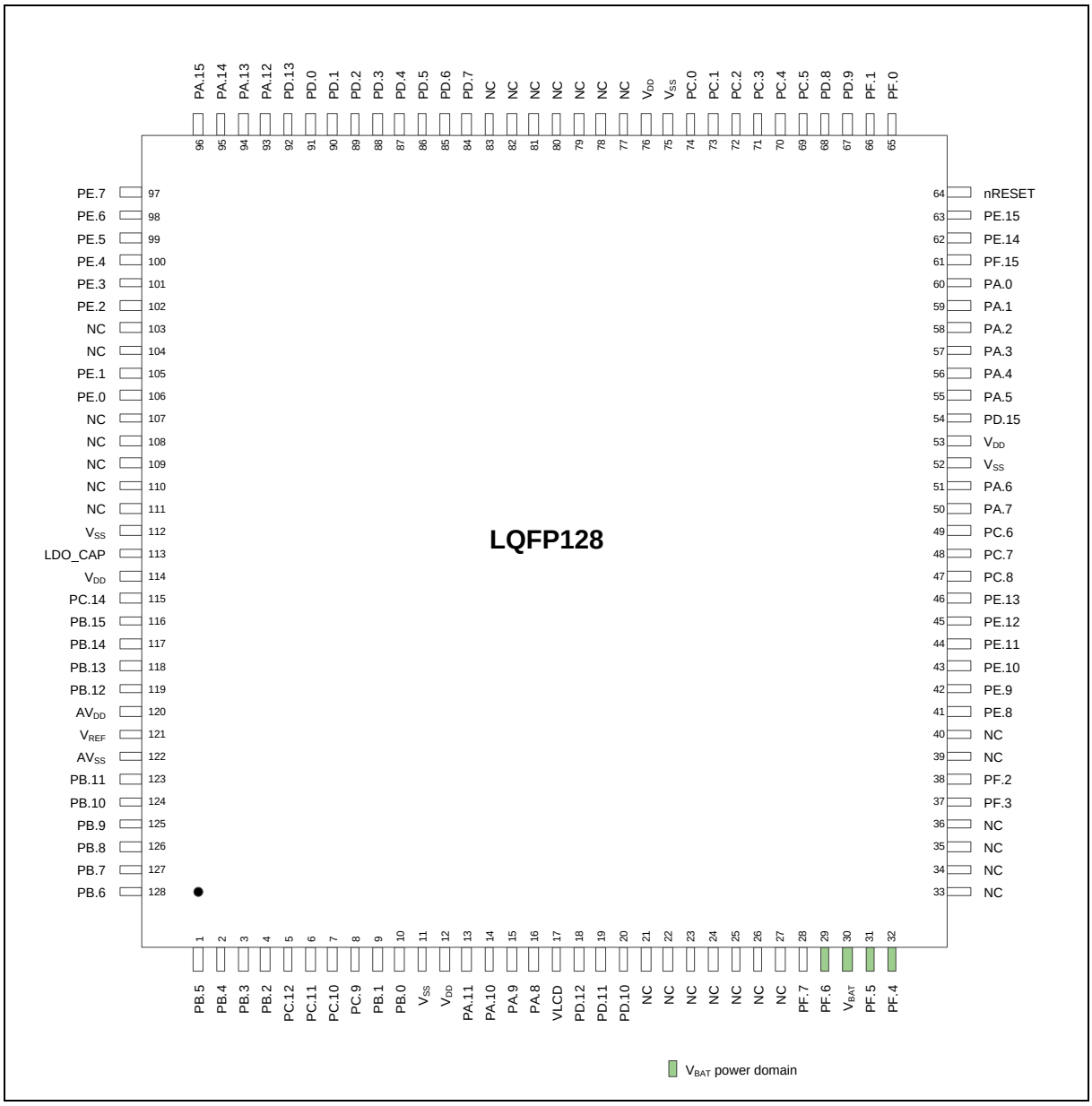


Figure 4.1-17 M256 Series LQFP 128-pin Diagram

4.1.4 M256 Series Multi-function Pin Diagram

4.1.4.1 M256 Series LQFP 44-Pin Multi-function Pin Diagram

Corresponding Part Number: M256MD2AE

M256MD2AE

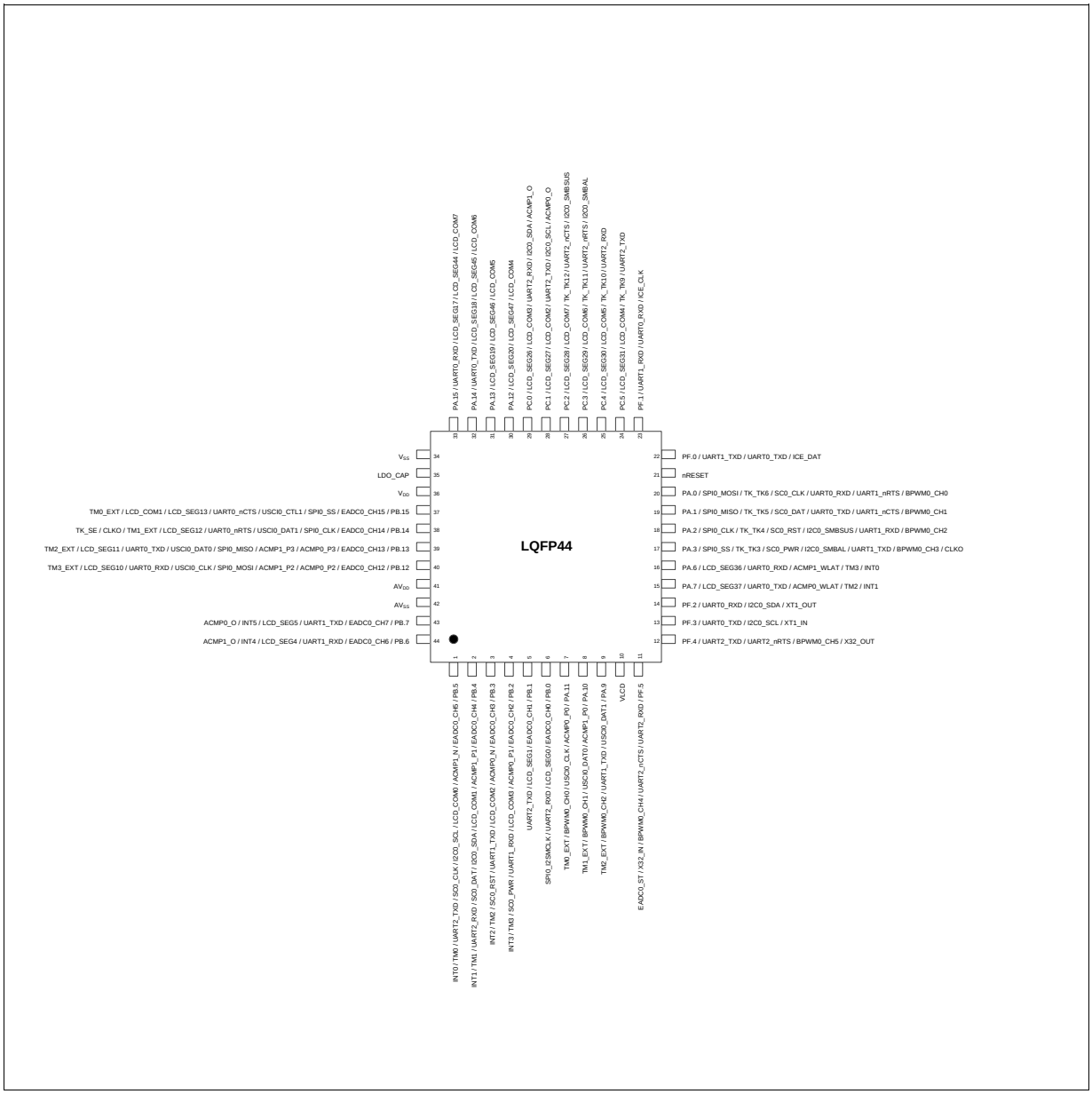


Figure 4.1-18 M256MD2AE Multi-function Pin Diagram

Pin	Type	M256MD2AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
5	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
6	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
7	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
9	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
10	P	V_{LCD}
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
15	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
18	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
19	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
20	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
21	I	nRESET
22	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
23	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
24	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD
25	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / UART2_RXD
26	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / UART2_nRTS / I2C0_SMBAL
27	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / UART2_nCTS / I2C0_SMBSUS
28	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
29	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
30	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
31	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
32	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
33	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
34	P	V_{SS}
35	A	LDO_CAP

36	P	V_{DD}
37	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
38	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
39	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
40	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
41	P	AV_{DD}
42	P	AV_{SS}
43	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O
44	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O

Table 4.1-8 M256MD2AE Multi-function Pin Table

4.1.4.2 M256 Series LQFP 64-Pin Multi-function *Pin Diagram*

Corresponding Part Number: M256SD2AE, M256SE3AE

M256SD2AE

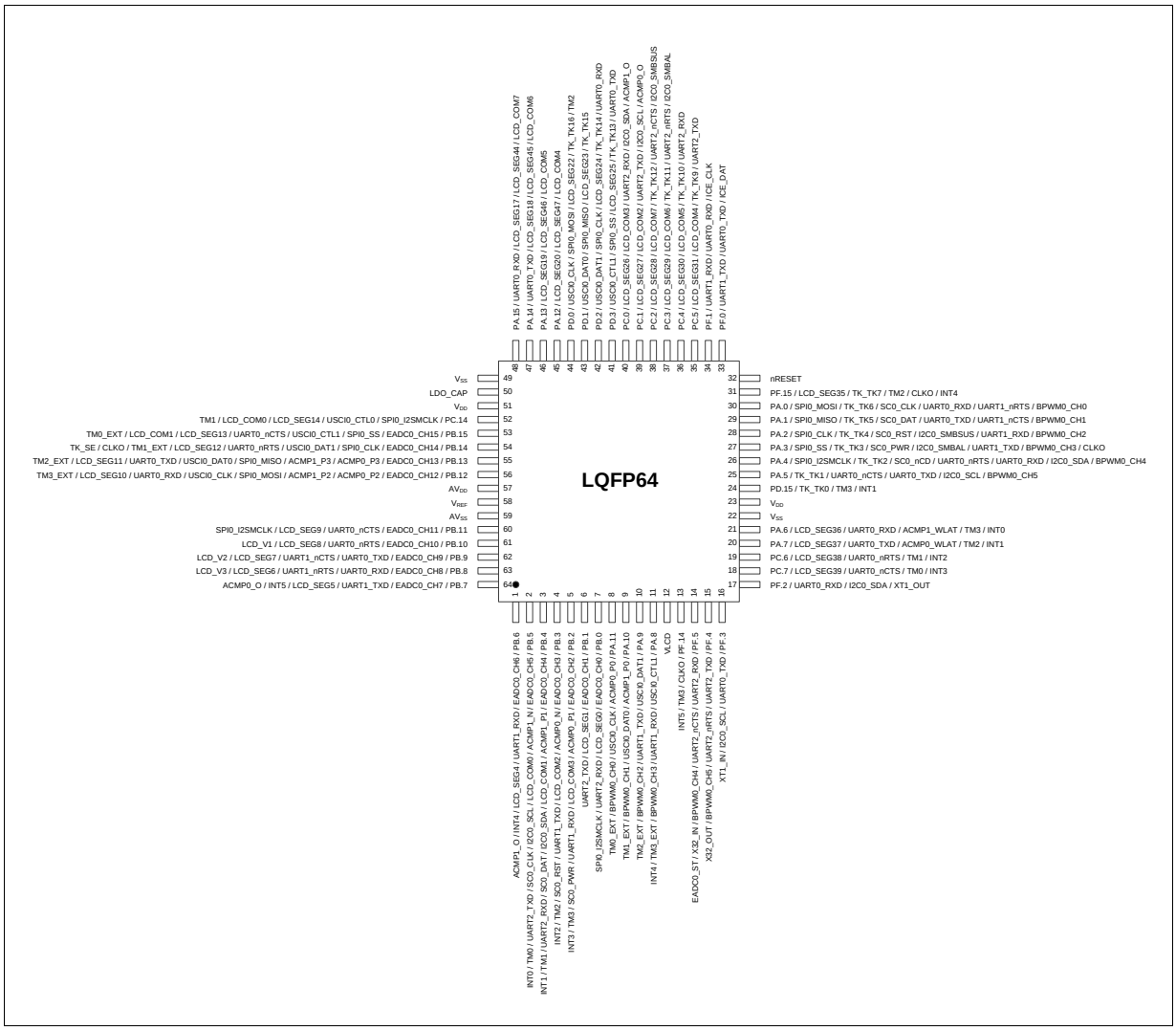


Figure 4.1-19 M256SD2AE Multi-function Pin Diagram

Pin	Type	M256SD2AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
8	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	P	V_{LCD}
13	I/O	PF.14 / CLKO / TM3 / INT5
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
18	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
19	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
20	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / TK_TK0 / TM3 / INT1
25	I/O	PA.5 / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
26	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
27	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
28	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
29	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
30	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
31	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
34	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK

Pin	Type	M256SD2AE Pin Function
35	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD
36	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / UART2_RXD
37	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / UART2_nRTS / I2C0_SMBAL
38	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / UART2_nCTS / I2C0_SMBSUS
39	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
40	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
41	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / UART0_TXD
42	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD
43	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15
44	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / TM2
45	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
46	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
47	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
48	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
53	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
54	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
61	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
62	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
63	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
64	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O

Table 4.1-9 M256SD2AE Multi-function Pin Table

M256SE3AE

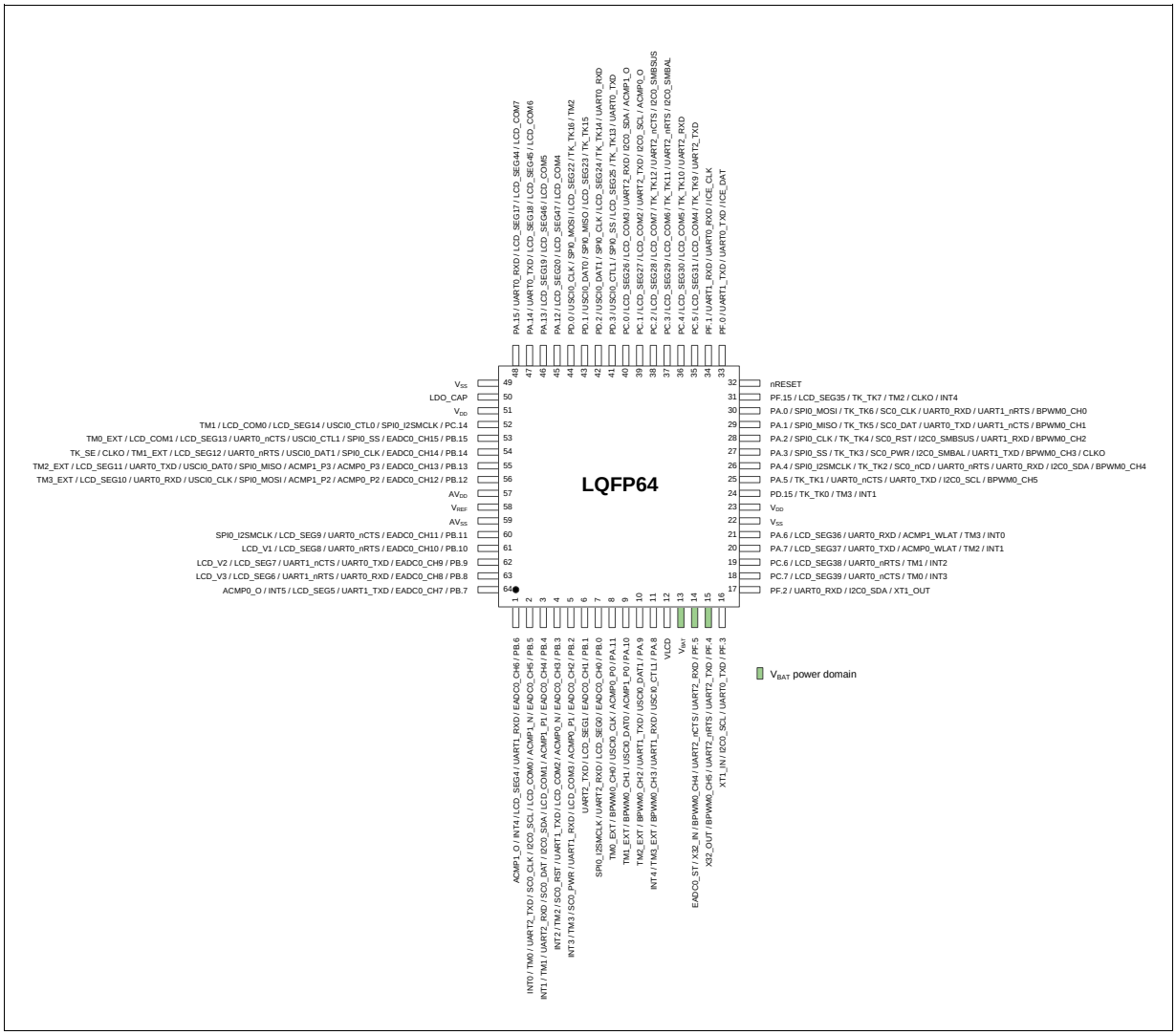


Figure 4.1-20 M256SE3AE Multi-function Pin Diagram

Pin	Type	M256SE3AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
8	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	P	V_{LCD}
13	P	V_{BAT}
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
18	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
19	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
20	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / TK_TK0 / TM3 / INT1
25	I/O	PA.5 / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
26	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
27	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
28	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
29	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
30	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
31	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
34	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK

Pin	Type	M256SE3AE Pin Function
35	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD
36	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / UART2_RXD
37	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / UART2_nRTS / I2C0_SMBAL
38	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / UART2_nCTS / I2C0_SMBSUS
39	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
40	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
41	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / UART0_TXD
42	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD
43	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15
44	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / TM2
45	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
46	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
47	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
48	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
53	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
54	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
61	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
62	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
63	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
64	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O

Table 4.1-10 M256SE3AE Multi-function Pin Table

4.1.4.3 M256 Series LQFP 80-Pin Multi-function Pin Diagram

Corresponding Part Number: M256QE3AE, M256QG6AE

M256QE3AE

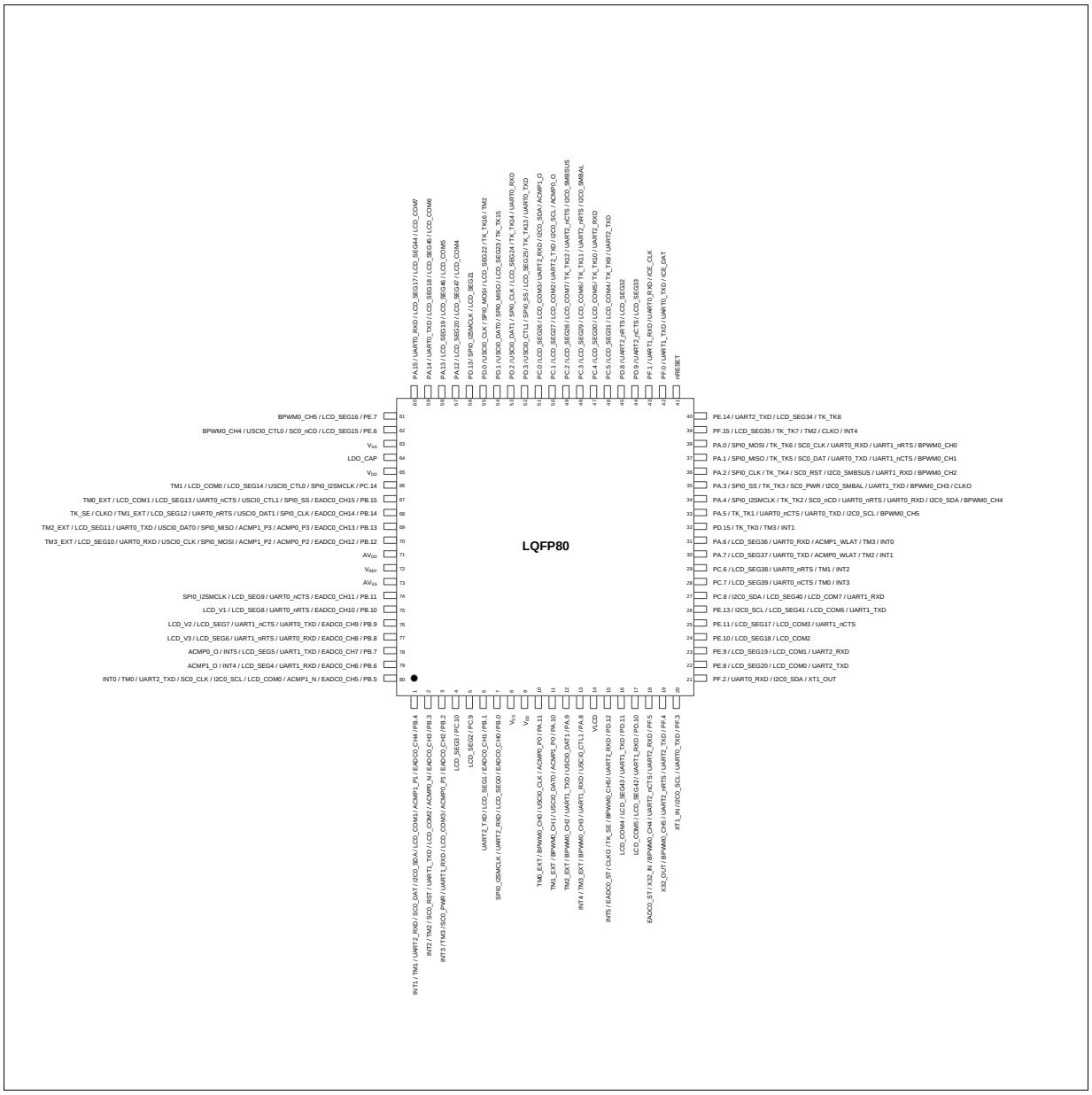


Figure 4.1-21 M256QE3AE Multi-function Pin Diagram

Pin	Type	M256QE3AE Pin Function
1	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
2	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
3	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
4	I/O	PC.10 / LCD_SEG3
5	I/O	PC.9 / LCD_SEG2
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
8	P	V_{SS}
9	P	V_{DD}
10	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
11	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
12	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
13	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
14	P	V_{LCD}
15	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / TK_SE / CLKO / EADC0_ST / INT5
16	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
17	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
18	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
19	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
20	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
21	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
22	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / UART2_TXD
23	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / UART2_RXD
24	I/O	PE.10 / LCD_SEG18 / LCD_COM2
25	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / UART1_nCTS
26	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD
27	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD
28	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
29	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
30	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
31	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
32	I/O	PD.15 / TK_TK0 / TM3 / INT1
33	I/O	PA.5 / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
34	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
35	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO

36	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
37	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
38	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
39	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
40	I/O	PE.14 / UART2_TXD / LCD_SEG34 / TK_TK8
41	I	nRESET
42	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
43	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
44	I/O	PD.9 / UART2_nCTS / LCD_SEG33
45	I/O	PD.8 / UART2_nRTS / LCD_SEG32
46	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD
47	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / UART2_RXD
48	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / UART2_nRTS / I2C0_SMBAL
49	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / UART2_nCTS / I2C0_SMBSUS
50	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
51	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
52	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / UART0_TXD
53	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD
54	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15
55	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / TM2
56	I/O	PD.13 / SPI0_I2SMCLK / LCD_SEG21
57	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
58	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
59	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
60	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
61	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
62	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
63	P	V_{SS}
64	A	LDO_CAP
65	P	V_{DD}
66	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
67	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
68	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
69	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT

70	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
71	P	AV_{DD}
72	A	V_{REF}
73	P	AV_{SS}
74	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
75	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
76	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
77	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
78	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O
79	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O
80	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0

Table 4.1-11 M256QE3AE Multi-function Pin Table

M256QG6AE

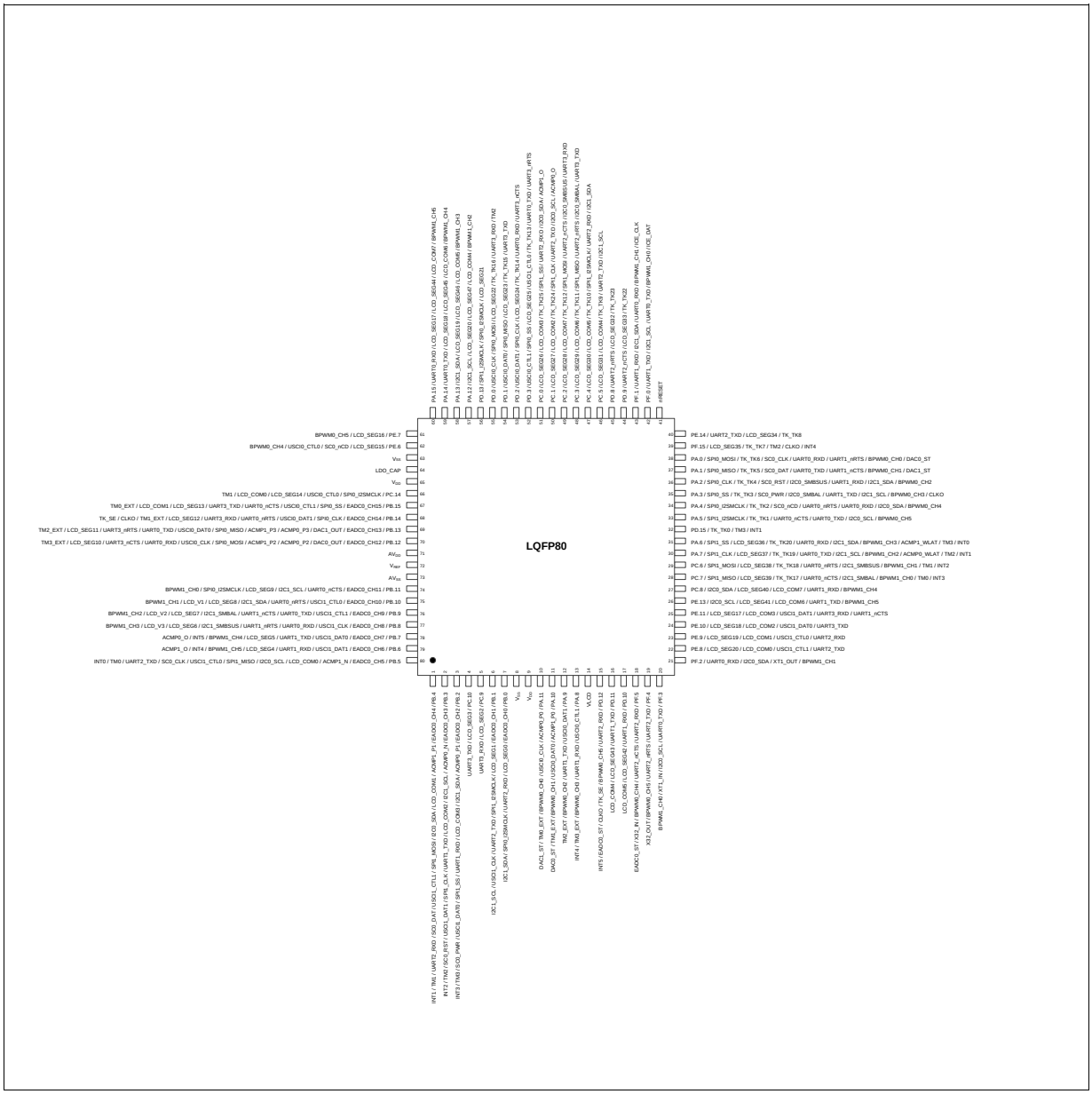


Figure 4.1-22 M256QG6AE Multi-function Pin Diagram

Pin	Type	M256QG6AE Pin Function
1	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SPI1_MOSI / USCI1_CTL1 / SC0_DAT / UART2_RXD / TM1 / INT1
2	I/O	PB.3 / EADC0_CH3 / ACMP0_N / I2C1_SCL / LCD_COM2 / UART1_TXD / SPI1_CLK / USCI1_DAT1 / SC0_RST / TM2 / INT2
3	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / I2C1_SDA / LCD_COM3 / UART1_RXD / SPI1_SS / USCI1_DAT0 / SC0_PWR / TM3 / INT3
4	I/O	PC.10 / LCD_SEG3 / UART3_TXD
5	I/O	PC.9 / LCD_SEG2 / UART3_RXD
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA
8	P	V_{SS}
9	P	V_{DD}
10	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT / DAC1_ST
11	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT / DAC0_ST
12	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
13	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
14	P	V_{LCD}
15	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / TK_SE / CLKO / EADC0_ST / INT5
16	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
17	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
18	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
19	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
20	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
21	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT / BPWM1_CH1
22	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / USCI1_CTL1 / UART2_TXD
23	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / USCI1_CTL0 / UART2_RXD
24	I/O	PE.10 / LCD_SEG18 / LCD_COM2 / USCI1_DAT0 / UART3_TXD
25	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / USCI1_DAT1 / UART3_RXD / UART1_nCTS
26	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD / BPWM1_CH5
27	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD / BPWM1_CH4
28	I/O	PC.7 / SPI1_MISO / LCD_SEG39 / TK_TK17 / UART0_nCTS / I2C1_SMBAL / BPWM1_CH0 / TM0 / INT3
29	I/O	PC.6 / SPI1_MOSI / LCD_SEG38 / TK_TK18 / UART0_nRTS / I2C1_SMBSUS / BPWM1_CH1 / TM1 / INT2
30	I/O	PA.7 / SPI1_CLK / LCD_SEG37 / TK_TK19 / UART0_TXD / I2C1_SCL / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
31	I/O	PA.6 / SPI1_SS / LCD_SEG36 / TK_TK20 / UART0_RXD / I2C1_SDA / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0

Pin	Type	M256QG6AE Pin Function
32	I/O	PD.15 / TK_TK0 / TM3 / INT1
33	I/O	PA.5 / SPI1_I2SMCLK / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
34	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
35	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / I2C1_SCL / BPWM0_CH3 / CLKO
36	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / BPWM0_CH2
37	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / DAC1_ST
38	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0 / DAC0_ST
39	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
40	I/O	PE.14 / UART2_TXD / LCD_SEG34 / TK_TK8
41	I	nRESET
42	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
43	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
44	I/O	PD.9 / UART2_nCTS / LCD_SEG33 / TK_TK22
45	I/O	PD.8 / UART2_nRTS / LCD_SEG32 / TK_TK23
46	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD / I2C1_SCL
47	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA
48	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD
49	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD
50	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / TK_TK24 / SPI1_CLK / UART2_TXD / I2C0_SCL / ACMP0_O
51	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / TK_TK25 / SPI1_SS / UART2_RXD / I2C0_SDA / ACMP1_O
52	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / USCI1_CTL0 / UART0_TXD / UART3_nRTS
53	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD / UART3_nCTS
54	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15 / UART3_TXD
55	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / UART3_RXD / TM2
56	I/O	PD.13 / SPI1_I2SMCLK / SPI0_I2SMCLK / LCD_SEG21
57	I/O	PA.12 / I2C1_SCL / LCD_SEG20 / LCD_SEG47 / LCD_COM4 / BPWM1_CH2
58	I/O	PA.13 / I2C1_SDA / LCD_SEG19 / LCD_SEG46 / LCD_COM5 / BPWM1_CH3
59	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6 / BPWM1_CH4
60	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7 / BPWM1_CH5
61	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
62	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
63	P	V_{SS}
64	A	LDO_CAP

Pin	Type	M256QG6AE Pin Function
65	P	V_{DD}
66	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
67	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / LCD_SEG13 / LCD_COM1 / TM0_EXT
68	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
69	I/O	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / LCD_SEG11 / TM2_EXT
70	I/O	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / LCD_SEG10 / TM3_EXT
71	P	AV_{DD}
72	A	V_{REF}
73	P	AV_{SS}
74	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / I2C1_SCL / LCD_SEG9 / SPI0_I2SMCLK / BPWM1_CH0
75	I/O	PB.10 / EADC0_CH10 / USCI1_CTL0 / UART0_nRTS / I2C1_SDA / LCD_SEG8 / LCD_V1 / BPWM1_CH1
76	I/O	PB.9 / EADC0_CH9 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / LCD_SEG7 / LCD_V2 / BPWM1_CH2
77	I/O	PB.8 / EADC0_CH8 / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / LCD_SEG6 / LCD_V3 / BPWM1_CH3
78	I/O	PB.7 / EADC0_CH7 / USCI1_DAT0 / UART1_TXD / LCD_SEG5 / BPWM1_CH4 / INT5 / ACMP0_O
79	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / UART1_RXD / LCD_SEG4 / BPWM1_CH5 / INT4 / ACMP1_O
80	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SPI1_MISO / USCI1_CTL0 / SC0_CLK / UART2_TXD / TM0 / INT0

Table 4.1-12 M256QG6AE Multi-function Pin Table

4.1.4.4 M256 Series LQFP 128-Pin Multi-function Pin Diagram

Corresponding Part Number: M256KE3AE

M256KE3AE

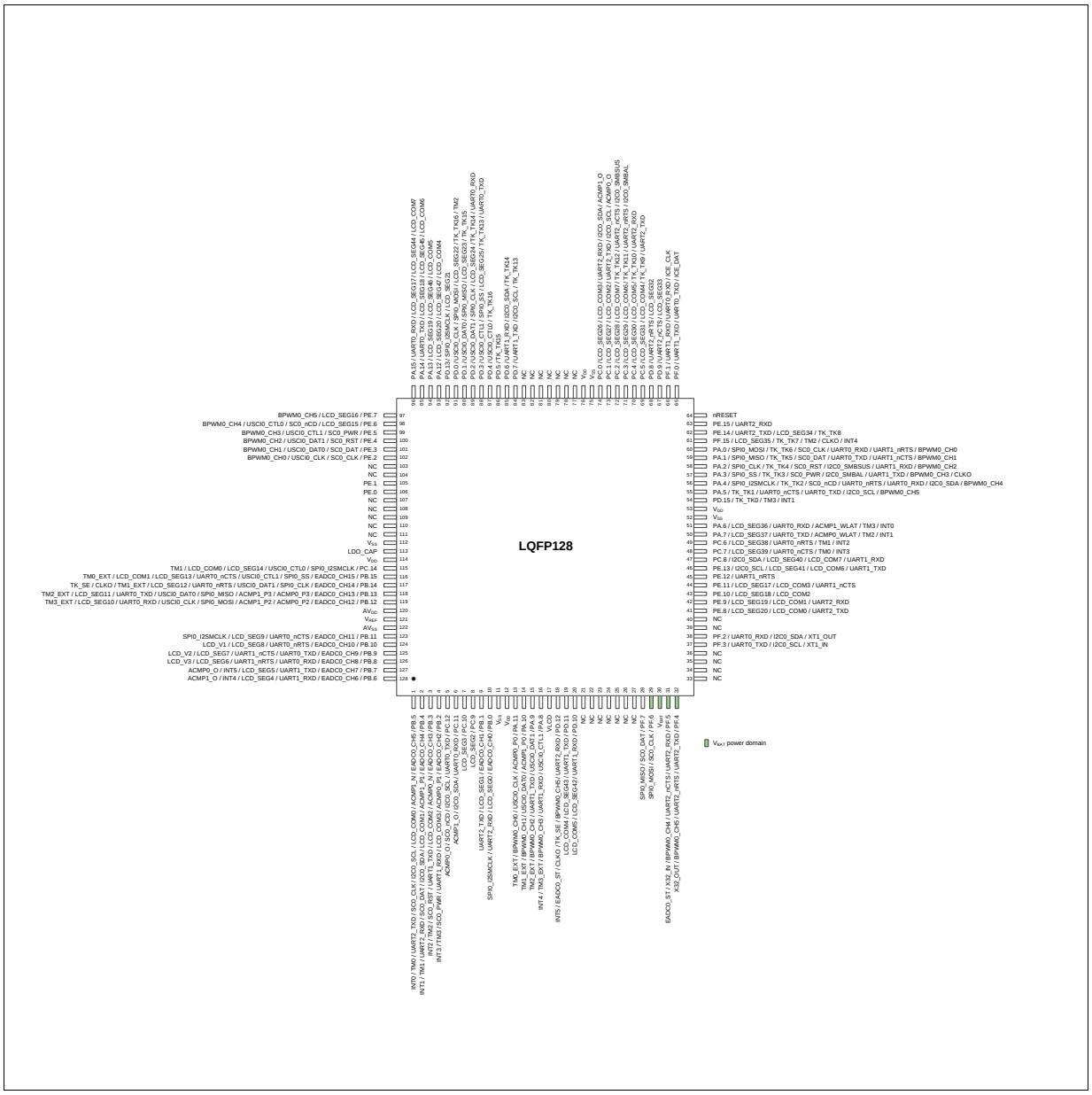


Figure 4.1-23 M256KE3AE Function Pin Diagram

Pin	Type	M256KE3AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
5	I/O	PC.12 / UART0_TXD / I2C0_SCL / SC0_nCD / ACMP0_O
6	I/O	PC.11 / UART0_RXD / I2C0_SDA / ACMP1_O
7	I/O	PC.10 / LCD_SEG3
8	I/O	PC.9 / LCD_SEG2
9	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
10	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
14	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
15	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
16	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
17	P	V_{LCD}
18	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / TK_SE / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
20	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
21	-	NC
22	-	NC
23	-	NC
24	-	NC
25	-	NC
26	-	NC
27	-	NC
28	I/O	PF.7 / SC0_DAT / SPI0_MISO
29	I/O	PF.6 / SC0_CLK / SPI0_MOSI
30	P	V_{BAT}
31	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
33	-	NC
34	-	NC
35	-	NC

36	-	NC
37	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
38	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
39	-	NC
40	-	NC
41	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / UART2_TXD
42	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / UART2_RXD
43	I/O	PE.10 / LCD_SEG18 / LCD_COM2
44	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / UART1_nCTS
45	I/O	PE.12 / UART1_nRTS
46	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD
47	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD
48	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
49	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
50	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
51	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	I/O	PD.15 / TK_TK0 / TM3 / INT1
55	I/O	PA.5 / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
56	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
57	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
58	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
59	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
60	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
61	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
62	I/O	PE.14 / UART2_TXD / LCD_SEG34 / TK_TK8
63	I/O	PE.15 / UART2_RXD
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
66	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
67	I/O	PD.9 / UART2_nCTS / LCD_SEG33
68	I/O	PD.8 / UART2_nRTS / LCD_SEG32
69	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD
70	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / UART2_RXD
71	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / UART2_nRTS / I2C0_SMBAL

72	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / UART2_nCTS / I2C0_SMBSUS
73	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
74	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
75	P	V_{SS}
76	P	V_{DD}
77	-	NC
78	-	NC
79	-	NC
80	-	NC
81	-	NC
82	-	NC
83	-	NC
84	I/O	PD.7 / UART1_TXD / I2C0_SCL / TK_TK13
85	I/O	PD.6 / UART1_RXD / I2C0_SDA / TK_TK14
86	I/O	PD.5 / TK_TK15
87	I/O	PD.4 / USCI0_CTL0 / TK_TK16
88	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / UART0_TXD
89	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD
90	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15
91	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / TM2
92	I/O	PD.13 / SPI0_I2SMCLK / LCD_SEG21
93	I/O	PA.12 / LCD_SEG20 / LCD_SEG47 / LCD_COM4
94	I/O	PA.13 / LCD_SEG19 / LCD_SEG46 / LCD_COM5
95	I/O	PA.14 / UART0_TXD / LCD_SEG18 / LCD_SEG45 / LCD_COM6
96	I/O	PA.15 / UART0_RXD / LCD_SEG17 / LCD_SEG44 / LCD_COM7
97	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
98	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
99	I/O	PE.5 / SC0_PWR / USCI0_CTL1 / BPWM0_CH3
100	I/O	PE.4 / SC0_RST / USCI0_DAT1 / BPWM0_CH2
101	I/O	PE.3 / SC0_DAT / USCI0_DAT0 / BPWM0_CH1
102	I/O	PE.2 / SC0_CLK / USCI0_CLK / BPWM0_CH0
103	-	NC
104	-	NC
105	I/O	PE.1
106	I/O	PE.0
107	-	NC

108	-	NC
109	-	NC
110	-	NC
111	-	NC
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
116	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
117	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
118	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
119	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
124	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
125	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
126	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
127	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O

Table 4.1-13 M256KE3AE Multi-function Pin Table

4.1.5 M258 Series Pin Diagram

4.1.5.1 M258 Series LQFP 64-Pin Diagram

Corresponding Part Number: M258SE3AE, M258SG6AE

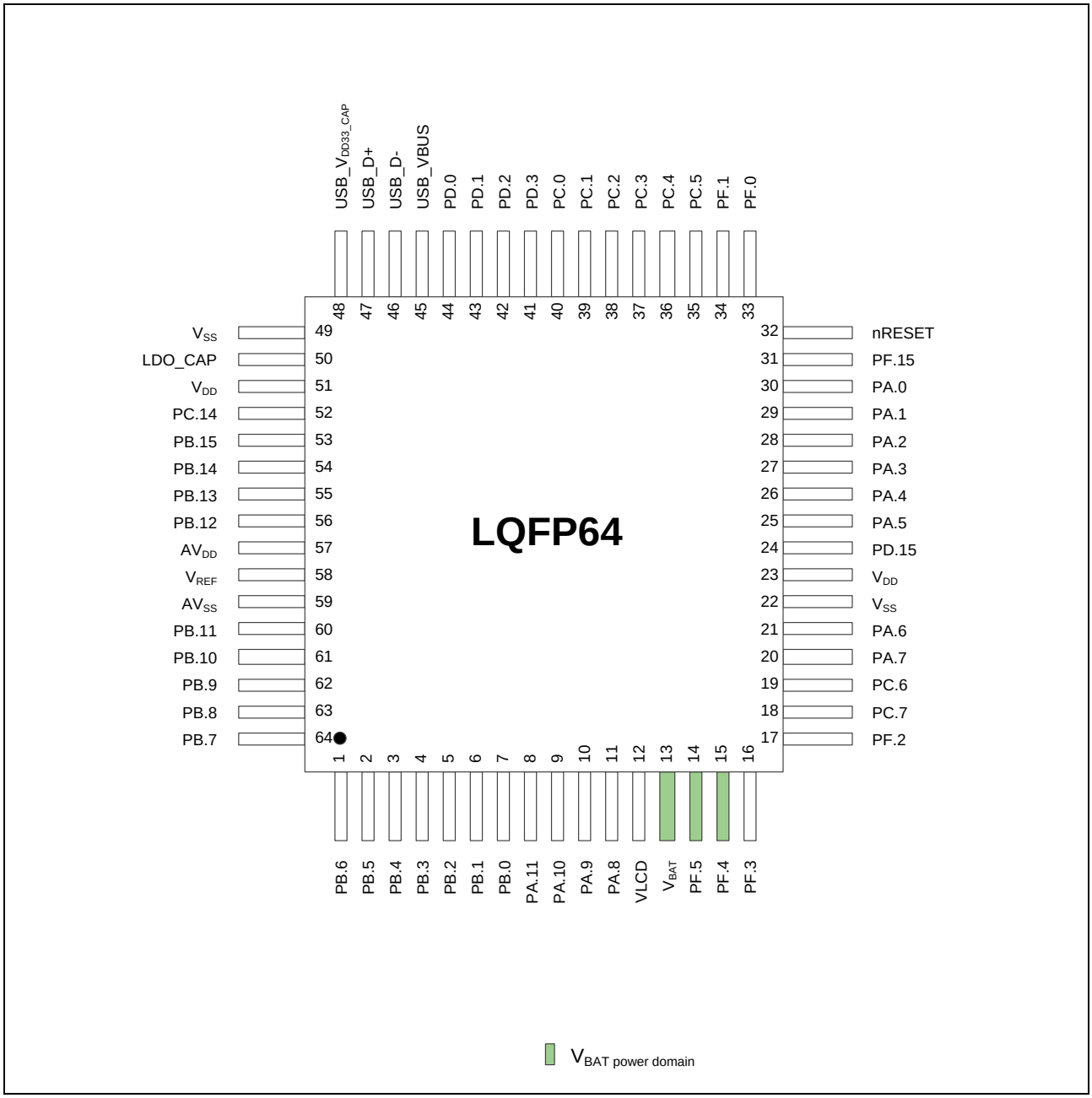


Figure 4.1-24 M258 Series LQFP 64-pin Diagram

4.1.5.2 M258 Series LQFP 80-Pin Diagram

Corresponding Part Number: M258QE3AE, M258QG6AE

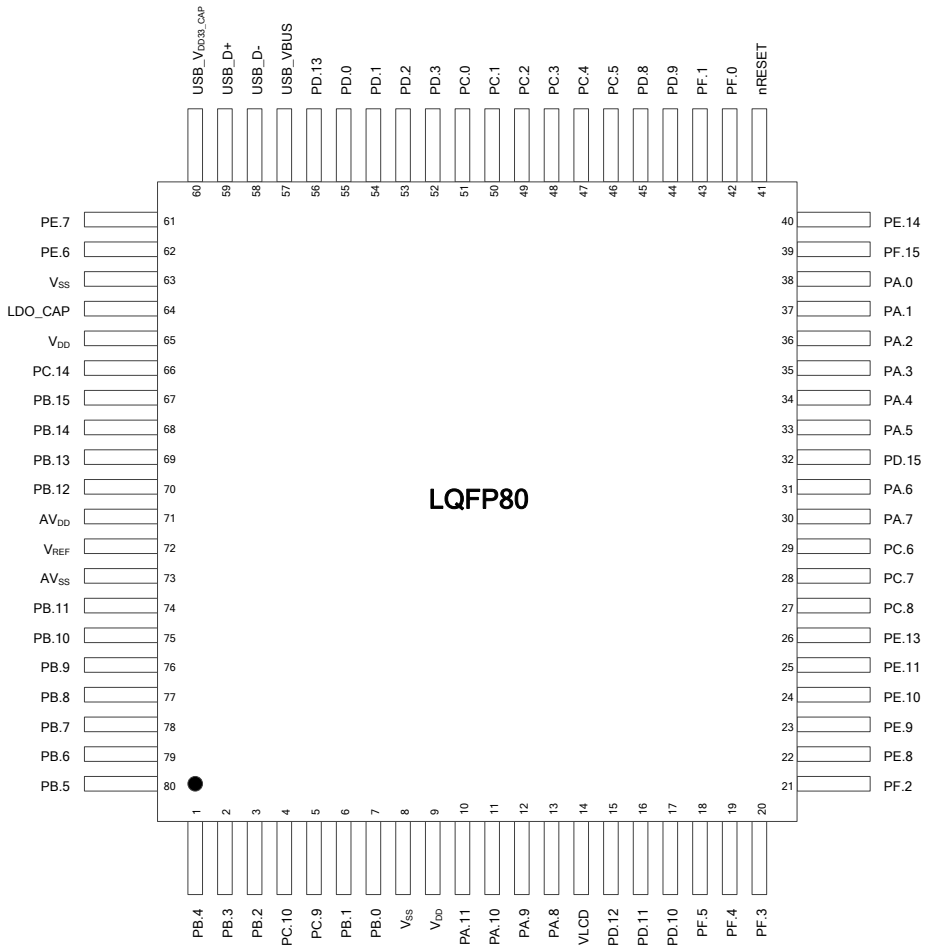


Figure 4.1-25 M258 Series LQFP 80-pin Diagram

4.1.5.3 M258 Series LQFP 128-Pin Diagram

Corresponding Part Number: M258KE3AE, M258KG6AE

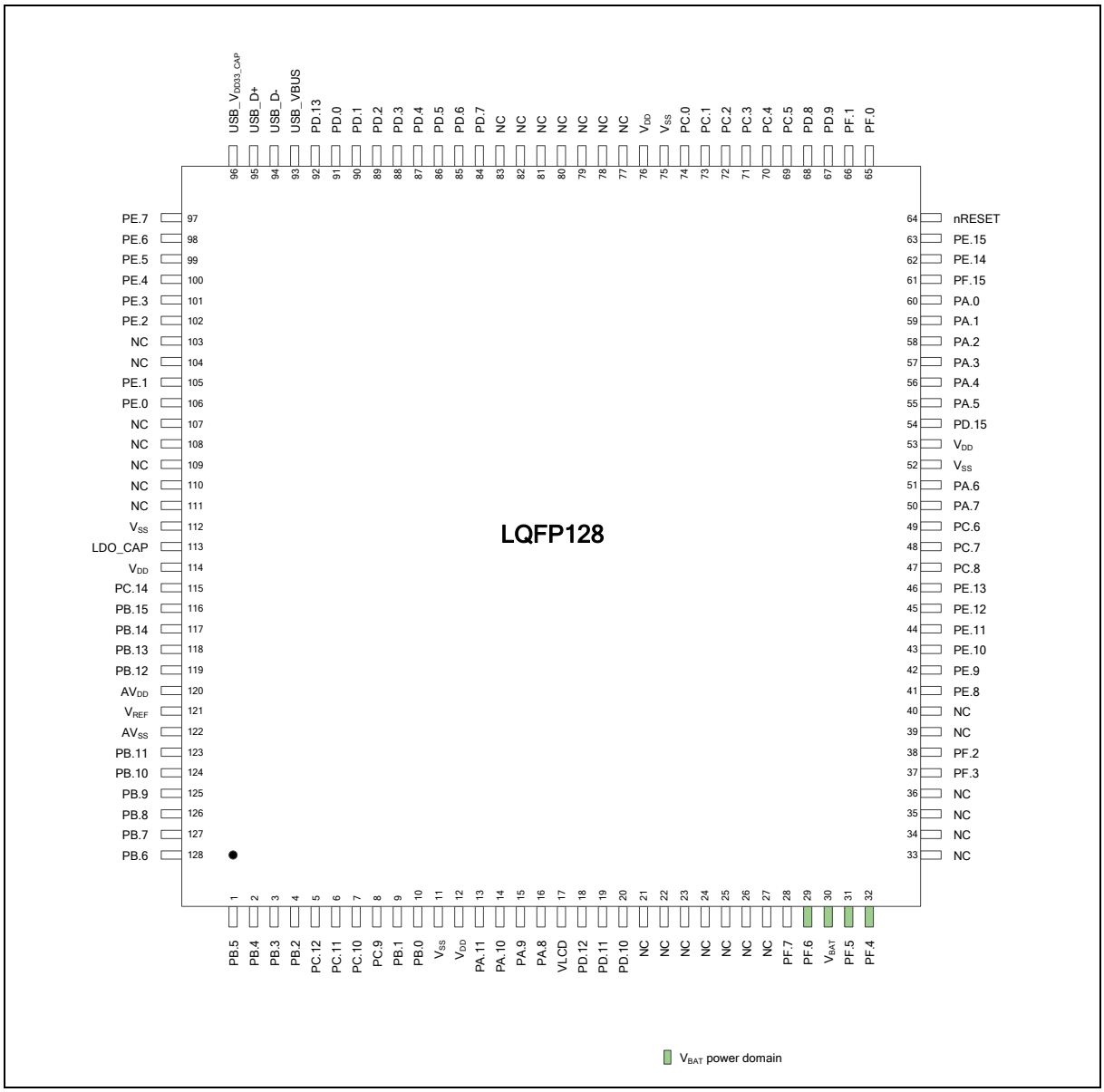


Figure 4.1-26 M258 Series LQFP 128-pin Diagram

4.1.6 M258 Series Multi-function Pin Diagram

4.1.6.1 M258 Series LQFP 64-Pin Multi-function Pin Diagram

Corresponding Part Number: M258SE3AE, M258SG6AE

M258SE3AE

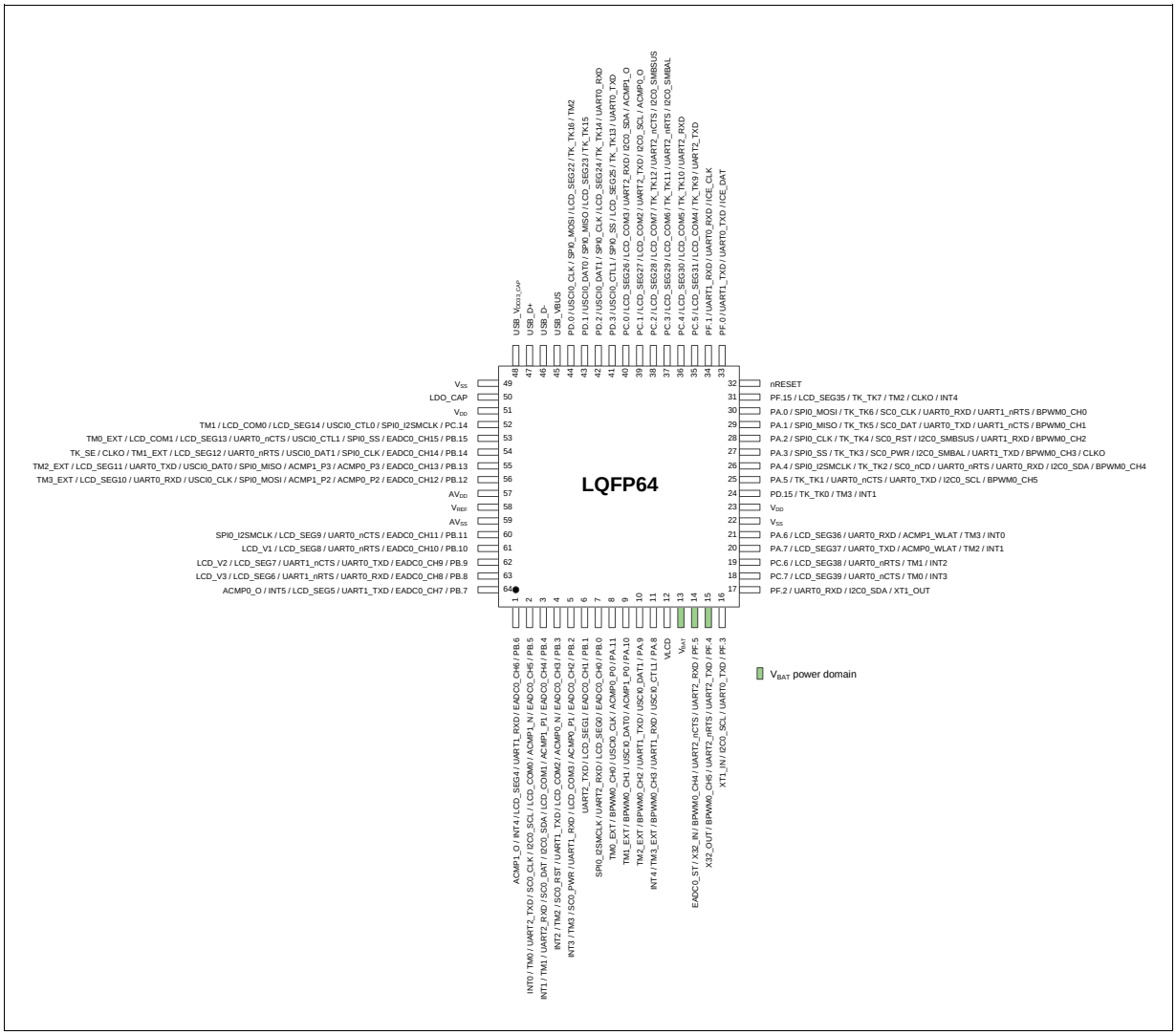


Figure 4.1-27 M258SE3AE Multi-function Pin Diagram

Pin	Type	M258SE3AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
8	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	P	V_{LCD}
13	P	V_{BAT}
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
18	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
19	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
20	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / TK_TK0 / TM3 / INT1
25	I/O	PA.5 / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
26	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
27	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
28	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
29	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
30	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
31	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
34	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
35	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD

36	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / UART2_RXD
37	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / UART2_nRTS / I2C0_SMBAL
38	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / UART2_nCTS / I2C0_SMBSUS
39	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
40	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
41	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / UART0_TXD
42	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD
43	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15
44	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / TM2
45	P	USB_VBUS
46	A	USB_D-
47	A	USB_D+
48	A	USB_VDD33_CAP
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
53	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
54	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
61	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
62	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
63	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
64	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O

Table 4.1-14 M258SE3AE Multi-function Pin Table

M258SG6AE

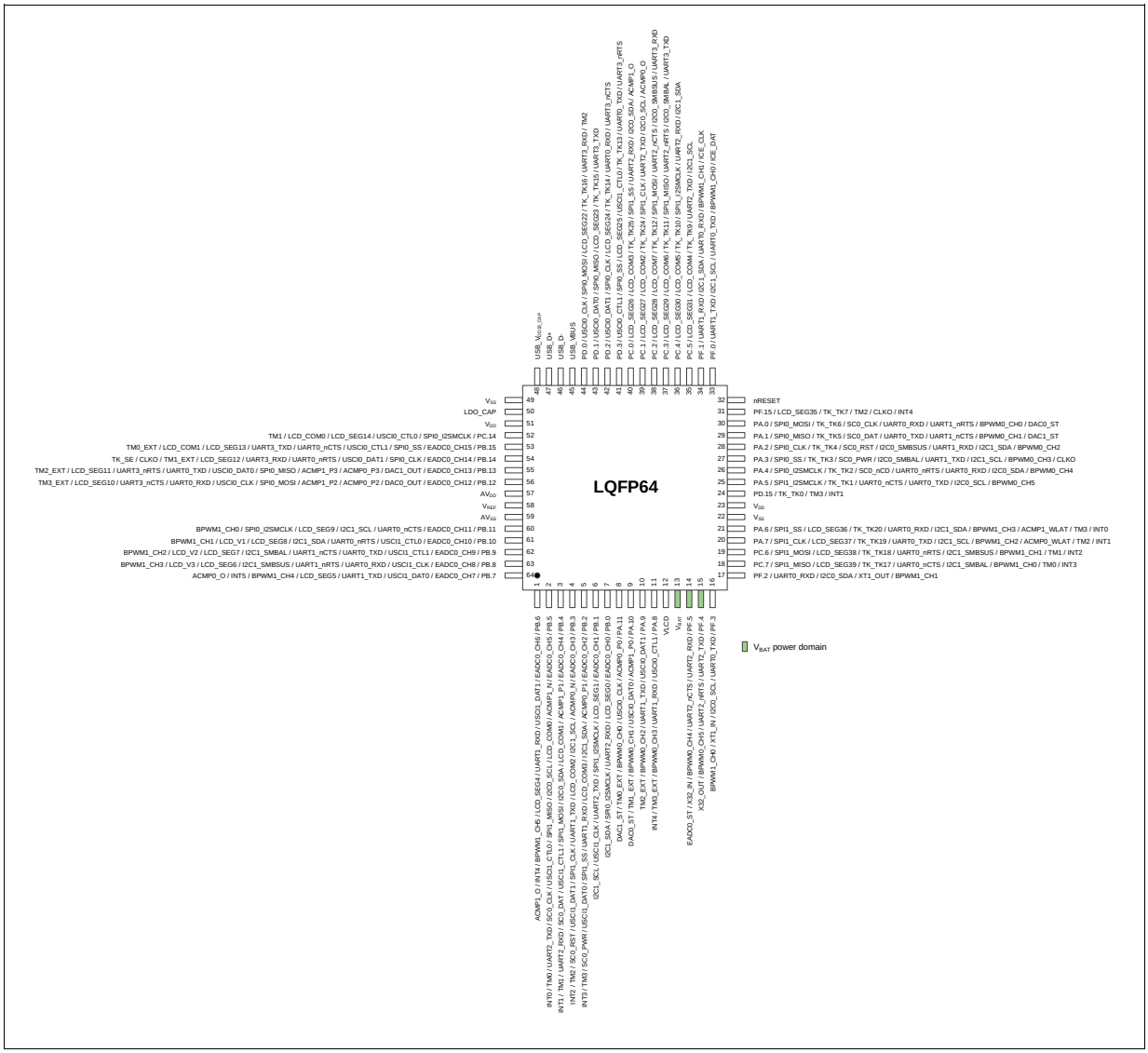


Figure 4.1-28 M258SG6AE Multi-function Pin Diagram

Pin	Type	M258SG6AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / UART1_RXD / LCD_SEG4 / BPWM1_CH5 / INT4 / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SPI1_MISO / USCI1_CTL0 / SC0_CLK / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SPI1_MOSI / USCI1_CTL1 / SC0_DAT / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / I2C1_SCL / LCD_COM2 / UART1_TXD / SPI1_CLK / USCI1_DAT1 / SC0_RST / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / I2C1_SDA / LCD_COM3 / UART1_RXD / SPI1_SS / USCI1_DAT0 / SC0_PWR / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA
8	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT / DAC1_ST
9	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT / DAC0_ST
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	P	V_{LCD}
13	P	V_{BAT}
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT / BPWM1_CH1
18	I/O	PC.7 / SPI1_MISO / LCD_SEG39 / TK_TK17 / UART0_nCTS / I2C1_SMBAL / BPWM1_CH0 / TM0 / INT3
19	I/O	PC.6 / SPI1_MOSI / LCD_SEG38 / TK_TK18 / UART0_nRTS / I2C1_SMBSUS / BPWM1_CH1 / TM1 / INT2
20	I/O	PA.7 / SPI1_CLK / LCD_SEG37 / TK_TK19 / UART0_TXD / I2C1_SCL / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / SPI1_SS / LCD_SEG36 / TK_TK20 / UART0_RXD / I2C1_SDA / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / TK_TK0 / TM3 / INT1
25	I/O	PA.5 / SPI1_I2SMCLK / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
26	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
27	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / I2C1_SCL / BPWM0_CH3 / CLKO
28	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / BPWM0_CH2
29	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / DAC1_ST
30	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0 / DAC0_ST

Pin	Type	M258SG6AE Pin Function
31	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
35	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD / I2C1_SCL
36	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA
37	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD
38	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD
39	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / TK_TK24 / SPI1_CLK / UART2_TXD / I2C0_SCL / ACMP0_O
40	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / TK_TK25 / SPI1_SS / UART2_RXD / I2C0_SDA / ACMP1_O
41	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / USCI1_CTL0 / UART0_TXD / UART3_nRTS
42	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD / UART3_nCTS
43	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15 / UART3_TXD
44	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / UART3_RXD / TM2
45	P	USB_VBUS
46	A	USB_D-
47	A	USB_D+
48	A	USB_VDD33_CAP
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
53	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / LCD_SEG13 / LCD_COM1 / TM0_EXT
54	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
55	I/O	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / LCD_SEG11 / TM2_EXT
56	I/O	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / LCD_SEG10 / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / I2C1_SCL / LCD_SEG9 / SPI0_I2SMCLK / BPWM1_CH0
61	I/O	PB.10 / EADC0_CH10 / USCI1_CTL0 / UART0_nRTS / I2C1_SDA / LCD_SEG8 / LCD_V1 / BPWM1_CH1

Pin	Type	M258SG6AE Pin Function
62	I/O	PB.9 / EADC0_CH9 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / LCD_SEG7 / LCD_V2 / BPWM1_CH2
63	I/O	PB.8 / EADC0_CH8 / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / LCD_SEG6 / LCD_V3 / BPWM1_CH3
64	I/O	PB.7 / EADC0_CH7 / USCI1_DAT0 / UART1_TXD / LCD_SEG5 / BPWM1_CH4 / INT5 / ACMP0_O

Table 4.1-15 M258SG6AE Multi-function Pin Table

4.1.6.2 M258 Series LQFP 80-Pin Multi-function Pin Diagram

Corresponding Part Number: M258QE3AE, M258QG6AE

M258QE3AE

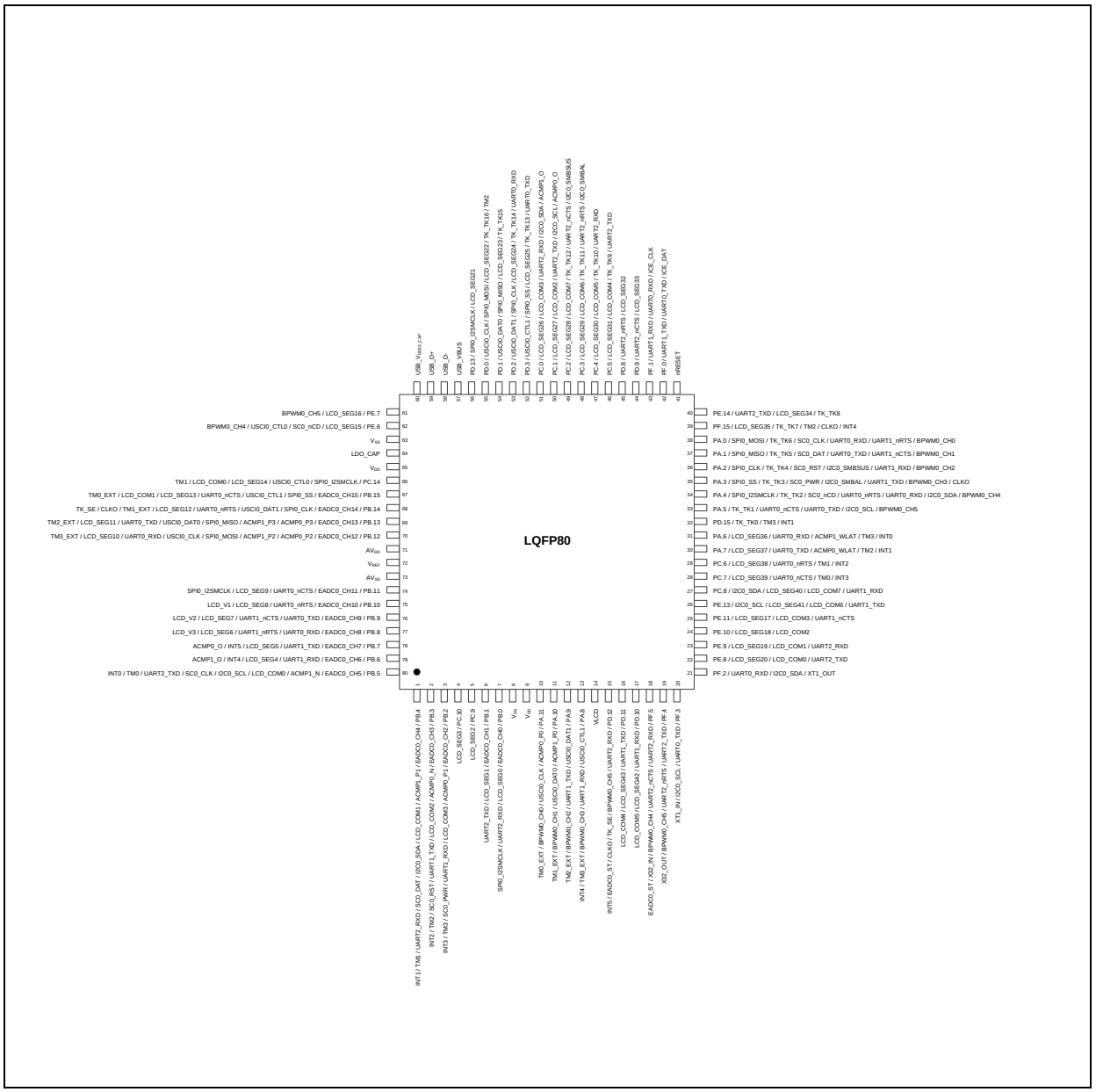


Figure 4.1-29 M258QE3AE Multi-Function Pin Diagram

Pin	Type	M258QE3AE Pin Function
1	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
2	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
3	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
4	I/O	PC.10 / LCD_SEG3
5	I/O	PC.9 / LCD_SEG2
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
8	P	V_{SS}
9	P	V_{DD}
10	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
11	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
12	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
13	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
14	P	V_{LCD}
15	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / TK_SE / CLKO / EADC0_ST / INT5
16	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
17	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
18	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
19	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
20	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
21	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
22	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / UART2_TXD
23	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / UART2_RXD
24	I/O	PE.10 / LCD_SEG18 / LCD_COM2
25	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / UART1_nCTS
26	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD
27	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD
28	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
29	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
30	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
31	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
32	I/O	PD.15 / TK_TK0 / TM3 / INT1
33	I/O	PA.5 / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
34	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
35	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO

36	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
37	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
38	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
39	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
40	I/O	PE.14 / UART2_TXD / LCD_SEG34 / TK_TK8
41	I	nRESET
42	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
43	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
44	I/O	PD.9 / UART2_nCTS / LCD_SEG33
45	I/O	PD.8 / UART2_nRTS / LCD_SEG32
46	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD
47	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / UART2_RXD
48	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / UART2_nRTS / I2C0_SMBAL
49	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / UART2_nCTS / I2C0_SMBSUS
50	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
51	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
52	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / UART0_TXD
53	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD
54	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15
55	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / TM2
56	I/O	PD.13 / SPI0_I2SMCLK / LCD_SEG21
57	P	USB_VBUS
58	A	USB_D-
59	A	USB_D+
60	A	USB_VDD33_CAP
61	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
62	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
63	P	V_{SS}
64	A	LDO_CAP
65	P	V_{DD}
66	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
67	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
68	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
69	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT

70	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
71	P	AV_{DD}
72	A	V_{REF}
73	P	AV_{SS}
74	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
75	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
76	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
77	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
78	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O
79	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O
80	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0

Table 4.1-16 M258QE3AE Multi-function Pin Table

M258QG6AE

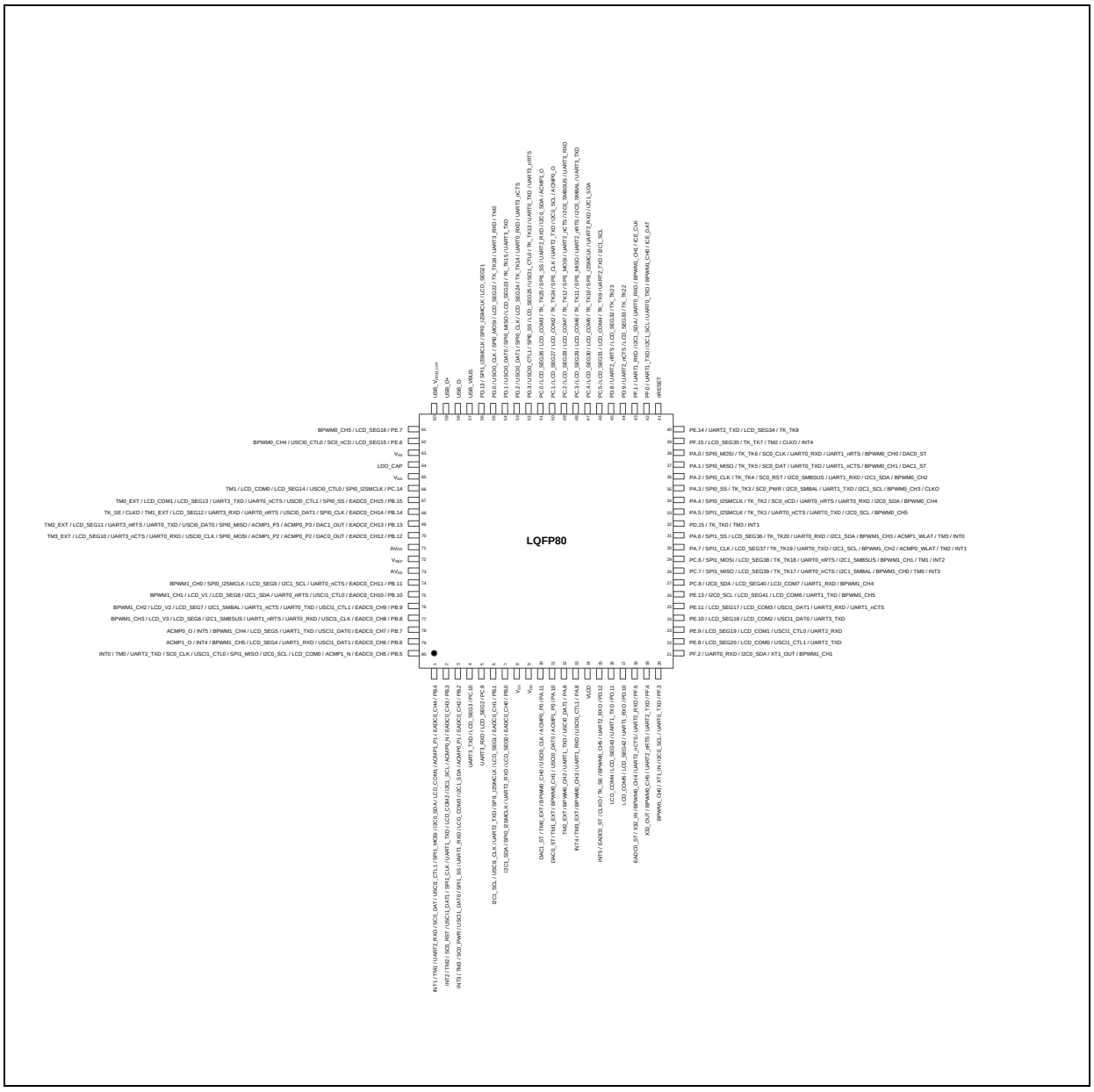


Figure 4.1-30 M258QG6AE Multi-Function Pin Diagram

Pin	Type	M258QG6AE Pin Function
1	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SPI1_MOSI / USCI1_CTL1 / SC0_DAT / UART2_RXD / TM1 / INT1
2	I/O	PB.3 / EADC0_CH3 / ACMP0_N / I2C1_SCL / LCD_COM2 / UART1_TXD / SPI1_CLK / USCI1_DAT1 / SC0_RST / TM2 / INT2
3	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / I2C1_SDA / LCD_COM3 / UART1_RXD / SPI1_SS / USCI1_DAT0 / SC0_PWR / TM3 / INT3
4	I/O	PC.10 / LCD_SEG3 / UART3_TXD
5	I/O	PC.9 / LCD_SEG2 / UART3_RXD
6	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL
7	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA
8	P	V_{SS}
9	P	V_{DD}
10	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT / DAC1_ST
11	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT / DAC0_ST
12	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
13	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
14	P	V_{LCD}
15	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / TK_SE / CLKO / EADC0_ST / INT5
16	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
17	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
18	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
19	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
20	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
21	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT / BPWM1_CH1
22	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / USCI1_CTL1 / UART2_TXD
23	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / USCI1_CTL0 / UART2_RXD
24	I/O	PE.10 / LCD_SEG18 / LCD_COM2 / USCI1_DAT0 / UART3_TXD
25	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / USCI1_DAT1 / UART3_RXD / UART1_nCTS
26	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD / BPWM1_CH5
27	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD / BPWM1_CH4
28	I/O	PC.7 / SPI1_MISO / LCD_SEG39 / TK_TK17 / UART0_nCTS / I2C1_SMBAL / BPWM1_CH0 / TM0 / INT3
29	I/O	PC.6 / SPI1_MOSI / LCD_SEG38 / TK_TK18 / UART0_nRTS / I2C1_SMBSUS / BPWM1_CH1 / TM1 / INT2
30	I/O	PA.7 / SPI1_CLK / LCD_SEG37 / TK_TK19 / UART0_TXD / I2C1_SCL / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
31	I/O	PA.6 / SPI1_SS / LCD_SEG36 / TK_TK20 / UART0_RXD / I2C1_SDA / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0

Pin	Type	M258QG6AE Pin Function
32	I/O	PD.15 / TK_TK0 / TM3 / INT1
33	I/O	PA.5 / SPI1_I2SMCLK / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
34	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
35	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / I2C1_SCL / BPWM0_CH3 / CLKO
36	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / BPWM0_CH2
37	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / DAC1_ST
38	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0 / DAC0_ST
39	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
40	I/O	PE.14 / UART2_TXD / LCD_SEG34 / TK_TK8
41	I	nRESET
42	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
43	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
44	I/O	PD.9 / UART2_nCTS / LCD_SEG33 / TK_TK22
45	I/O	PD.8 / UART2_nRTS / LCD_SEG32 / TK_TK23
46	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD / I2C1_SCL
47	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA
48	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD
49	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD
50	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / TK_TK24 / SPI1_CLK / UART2_TXD / I2C0_SCL / ACMP0_O
51	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / TK_TK25 / SPI1_SS / UART2_RXD / I2C0_SDA / ACMP1_O
52	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / USCI1_CTL0 / UART0_TXD / UART3_nRTS
53	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD / UART3_nCTS
54	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15 / UART3_TXD
55	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / UART3_RXD / TM2
56	I/O	PD.13 / SPI1_I2SMCLK / SPI0_I2SMCLK / LCD_SEG21
57	P	USB_VBUS
58	A	USB_D-
59	A	USB_D+
60	A	USB_VDD33_CAP
61	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
62	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
63	P	V_{SS}
64	A	LDO_CAP

Pin	Type	M258QG6AE Pin Function
65	P	V_{DD}
66	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
67	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / LCD_SEG13 / LCD_COM1 / TM0_EXT
68	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
69	I/O	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / LCD_SEG11 / TM2_EXT
70	I/O	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / LCD_SEG10 / TM3_EXT
71	P	AV_{DD}
72	A	V_{REF}
73	P	AV_{SS}
74	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / I2C1_SCL / LCD_SEG9 / SPI0_I2SMCLK / BPWM1_CH0
75	I/O	PB.10 / EADC0_CH10 / USCI1_CTL0 / UART0_nRTS / I2C1_SDA / LCD_SEG8 / LCD_V1 / BPWM1_CH1
76	I/O	PB.9 / EADC0_CH9 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / LCD_SEG7 / LCD_V2 / BPWM1_CH2
77	I/O	PB.8 / EADC0_CH8 / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / LCD_SEG6 / LCD_V3 / BPWM1_CH3
78	I/O	PB.7 / EADC0_CH7 / USCI1_DAT0 / UART1_TXD / LCD_SEG5 / BPWM1_CH4 / INT5 / ACMP0_O
79	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / UART1_RXD / LCD_SEG4 / BPWM1_CH5 / INT4 / ACMP1_O
80	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SPI1_MISO / USCI1_CTL0 / SC0_CLK / UART2_TXD / TM0 / INT0

Table 4.1-17 M258QG6AE Multi-function Pin Table

4.1.6.3 M258 Series LQFP 128-Pin Multi-function Pin Diagram

Corresponding Part Number: M258KE3AE, M258KG6AE

M258KE3AE

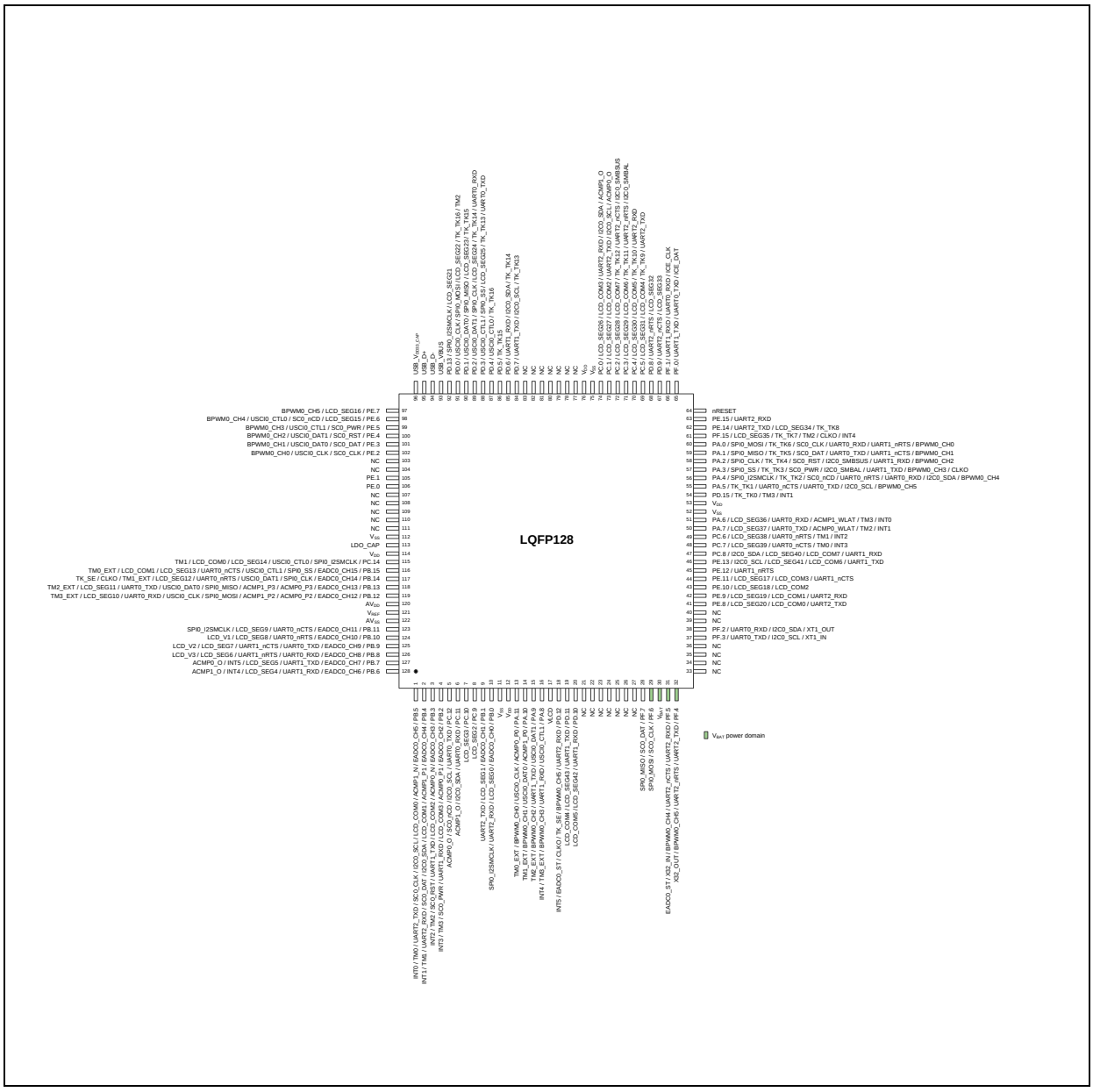


Figure 4.1-31 M258KE3AE Multi-Function Pin Diagram

Pin	Type	M258KE3AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SC0_CLK / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SC0_DAT / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LCD_COM2 / UART1_TXD / SC0_RST / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LCD_COM3 / UART1_RXD / SC0_PWR / TM3 / INT3
5	I/O	PC.12 / UART0_TXD / I2C0_SCL / SC0_nCD / ACMP0_O
6	I/O	PC.11 / UART0_RXD / I2C0_SDA / ACMP1_O
7	I/O	PC.10 / LCD_SEG3
8	I/O	PC.9 / LCD_SEG2
9	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / UART2_TXD
10	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
14	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
15	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
16	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
17	P	V_{LCD}
18	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / TK_SE / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
20	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
21	-	NC
22	-	NC
23	-	NC
24	-	NC
25	-	NC
26	-	NC
27	-	NC
28	I/O	PF.7 / SC0_DAT / SPI0_MISO
29	I/O	PF.6 / SC0_CLK / SPI0_MOSI
30	P	V_{BAT}
31	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
33	-	NC
34	-	NC
35	-	NC

36	-	NC
37	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
38	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
39	-	NC
40	-	NC
41	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / UART2_TXD
42	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / UART2_RXD
43	I/O	PE.10 / LCD_SEG18 / LCD_COM2
44	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / UART1_nCTS
45	I/O	PE.12 / UART1_nRTS
46	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD
47	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD
48	I/O	PC.7 / LCD_SEG39 / UART0_nCTS / TM0 / INT3
49	I/O	PC.6 / LCD_SEG38 / UART0_nRTS / TM1 / INT2
50	I/O	PA.7 / LCD_SEG37 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
51	I/O	PA.6 / LCD_SEG36 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	I/O	PD.15 / TK_TK0 / TM3 / INT1
55	I/O	PA.5 / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
56	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
57	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / BPWM0_CH3 / CLKO
58	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / BPWM0_CH2
59	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1
60	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0
61	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
62	I/O	PE.14 / UART2_TXD / LCD_SEG34 / TK_TK8
63	I/O	PE.15 / UART2_RXD
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / UART0_TXD / ICE_DAT
66	I/O	PF.1 / UART1_RXD / UART0_RXD / ICE_CLK
67	I/O	PD.9 / UART2_nCTS / LCD_SEG33
68	I/O	PD.8 / UART2_nRTS / LCD_SEG32
69	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD
70	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / UART2_RXD
71	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / UART2_nRTS / I2C0_SMBAL

72	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / UART2_nCTS / I2C0_SMBSUS
73	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / UART2_TXD / I2C0_SCL / ACMP0_O
74	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / UART2_RXD / I2C0_SDA / ACMP1_O
75	P	V_{SS}
76	P	V_{DD}
77	-	NC
78	-	NC
79	-	NC
80	-	NC
81	-	NC
82	-	NC
83	-	NC
84	I/O	PD.7 / UART1_TXD / I2C0_SCL / TK_TK13
85	I/O	PD.6 / UART1_RXD / I2C0_SDA / TK_TK14
86	I/O	PD.5 / TK_TK15
87	I/O	PD.4 / USCI0_CTL0 / TK_TK16
88	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / UART0_TXD
89	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD
90	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15
91	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / TM2
92	I/O	PD.13 / SPI0_I2SMCLK / LCD_SEG21
93	P	USB_VBUS
94	A	USB_D-
95	A	USB_D+
96	A	USB_VDD33_CAP
97	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
98	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
99	I/O	PE.5 / SC0_PWR / USCI0_CTL1 / BPWM0_CH3
100	I/O	PE.4 / SC0_RST / USCI0_DAT1 / BPWM0_CH2
101	I/O	PE.3 / SC0_DAT / USCI0_DAT0 / BPWM0_CH1
102	I/O	PE.2 / SC0_CLK / USCI0_CLK / BPWM0_CH0
103	-	NC
104	-	NC
105	I/O	PE.1
106	I/O	PE.0
107	-	NC

108	-	NC
109	-	NC
110	-	NC
111	-	NC
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
116	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / LCD_SEG13 / LCD_COM1 / TM0_EXT
117	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
118	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / LCD_SEG11 / TM2_EXT
119	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / LCD_SEG10 / TM3_EXT
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / LCD_SEG9 / SPI0_I2SMCLK
124	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / LCD_SEG8 / LCD_V1
125	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / LCD_SEG7 / LCD_V2
126	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / LCD_SEG6 / LCD_V3
127	I/O	PB.7 / EADC0_CH7 / UART1_TXD / LCD_SEG5 / INT5 / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / UART1_RXD / LCD_SEG4 / INT4 / ACMP1_O

Table 4.1-18 M258KE3AE Multi-function Pin Table

M258KG6AE

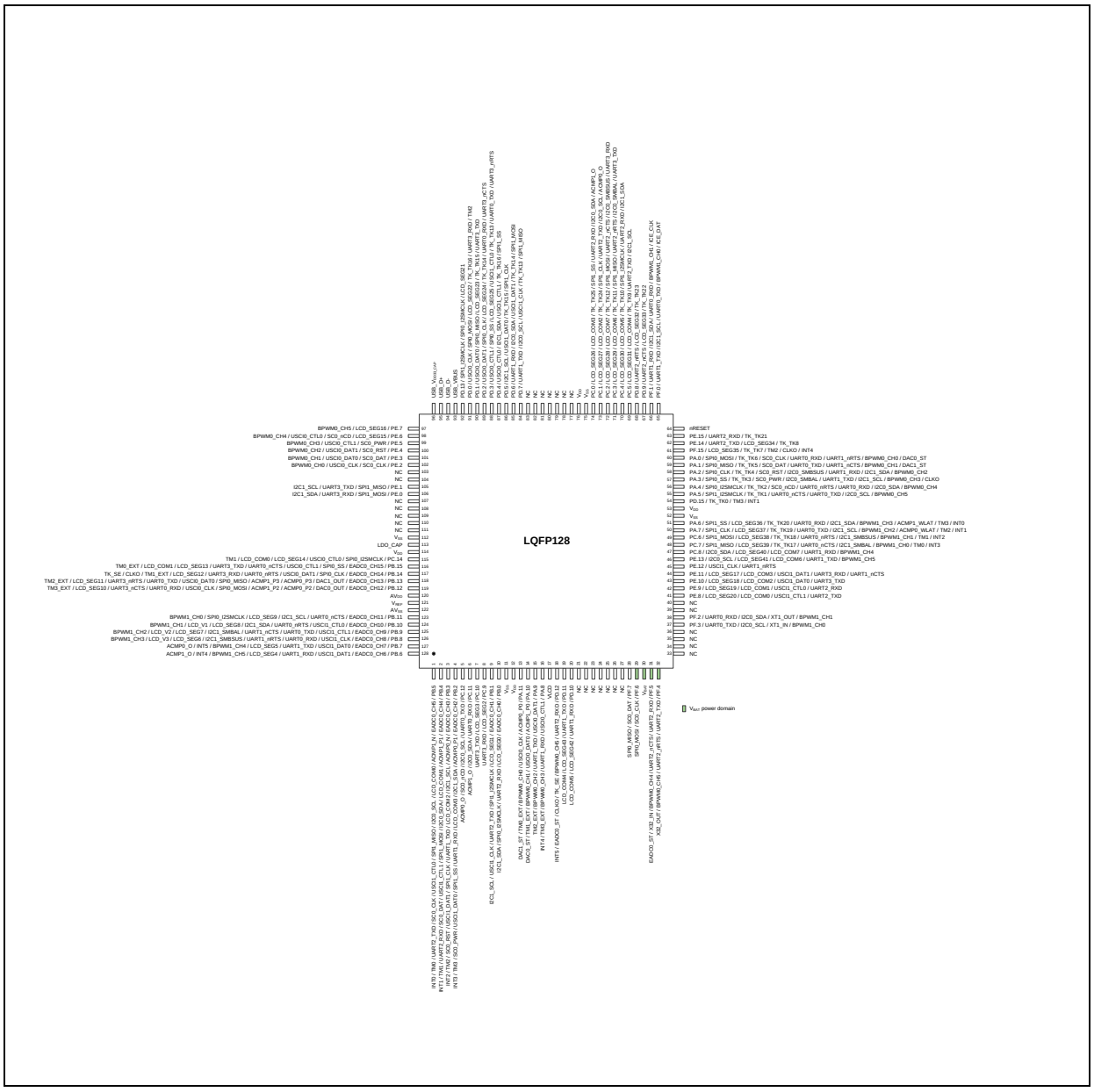


Figure 4.1-32 M258KG6AE Multi-Function Pin Diagram

Pin	Type	M258KG6AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LCD_COM0 / I2C0_SCL / SPI1_MISO / USCI1_CTL0 / SC0_CLK / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LCD_COM1 / I2C0_SDA / SPI1_MOSI / USCI1_CTL1 / SC0_DAT / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / I2C1_SCL / LCD_COM2 / UART1_TXD / SPI1_CLK / USCI1_DAT1 / SC0_RST / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / I2C1_SDA / LCD_COM3 / UART1_RXD / SPI1_SS / USCI1_DAT0 / SC0_PWR / TM3 / INT3
5	I/O	PC.12 / UART0_TXD / I2C0_SCL / SC0_nCD / ACMP0_O
6	I/O	PC.11 / UART0_RXD / I2C0_SDA / ACMP1_O
7	I/O	PC.10 / LCD_SEG3 / UART3_TXD
8	I/O	PC.9 / LCD_SEG2 / UART3_RXD
9	I/O	PB.1 / EADC0_CH1 / LCD_SEG1 / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL
10	I/O	PB.0 / EADC0_CH0 / LCD_SEG0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / ACMP0_P0 / USCI0_CLK / BPWM0_CH0 / TM0_EXT / DAC1_ST
14	I/O	PA.10 / ACMP1_P0 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT / DAC0_ST
15	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
16	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
17	P	V_{LCD}
18	I/O	PD.12 / UART2_RXD / BPWM0_CH5 / TK_SE / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / UART1_TXD / LCD_SEG43 / LCD_COM4
20	I/O	PD.10 / UART1_RXD / LCD_SEG42 / LCD_COM5
21	-	NC
22	-	NC
23	-	NC
24	-	NC
25	-	NC
26	-	NC
27	-	NC
28	I/O	PF.7 / SC0_DAT / SPI0_MISO
29	I/O	PF.6 / SC0_CLK / SPI0_MOSI
30	P	V_{BAT}
31	I/O	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
33	-	NC

34	-	NC
35	-	NC
36	-	NC
37	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
38	I/O	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT / BPWM1_CH1
39	-	NC
40	-	NC
41	I/O	PE.8 / LCD_SEG20 / LCD_COM0 / USCI1_CTL1 / UART2_TXD
42	I/O	PE.9 / LCD_SEG19 / LCD_COM1 / USCI1_CTL0 / UART2_RXD
43	I/O	PE.10 / LCD_SEG18 / LCD_COM2 / USCI1_DAT0 / UART3_TXD
44	I/O	PE.11 / LCD_SEG17 / LCD_COM3 / USCI1_DAT1 / UART3_RXD / UART1_nCTS
45	I/O	PE.12 / USCI1_CLK / UART1_nRTS
46	I/O	PE.13 / I2C0_SCL / LCD_SEG41 / LCD_COM6 / UART1_TXD / BPWM1_CH5
47	I/O	PC.8 / I2C0_SDA / LCD_SEG40 / LCD_COM7 / UART1_RXD / BPWM1_CH4
48	I/O	PC.7 / SPI1_MISO / LCD_SEG39 / TK_TK17 / UART0_nCTS / I2C1_SMBAL / BPWM1_CH0 / TM0 / INT3
49	I/O	PC.6 / SPI1_MOSI / LCD_SEG38 / TK_TK18 / UART0_nRTS / I2C1_SMBSUS / BPWM1_CH1 / TM1 / INT2
50	I/O	PA.7 / SPI1_CLK / LCD_SEG37 / TK_TK19 / UART0_TXD / I2C1_SCL / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
51	I/O	PA.6 / SPI1_SS / LCD_SEG36 / TK_TK20 / UART0_RXD / I2C1_SDA / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	I/O	PD.15 / TK_TK0 / TM3 / INT1
55	I/O	PA.5 / SPI1_I2SMCLK / TK_TK1 / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
56	I/O	PA.4 / SPI0_I2SMCLK / TK_TK2 / SC0_nCD / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
57	I/O	PA.3 / SPI0_SS / TK_TK3 / SC0_PWR / I2C0_SMBAL / UART1_TXD / I2C1_SCL / BPWM0_CH3 / CLKO
58	I/O	PA.2 / SPI0_CLK / TK_TK4 / SC0_RST / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / BPWM0_CH2
59	I/O	PA.1 / SPI0_MISO / TK_TK5 / SC0_DAT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / DAC1_ST
60	I/O	PA.0 / SPI0_MOSI / TK_TK6 / SC0_CLK / UART0_RXD / UART1_nRTS / BPWM0_CH0 / DAC0_ST
61	I/O	PF.15 / LCD_SEG35 / TK_TK7 / TM2 / CLKO / INT4
62	I/O	PE.14 / UART2_TXD / LCD_SEG34 / TK_TK8
63	I/O	PE.15 / UART2_RXD / TK_TK21
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK

67	I/O	PD.9 / UART2_nCTS / LCD_SEG33 / TK_TK22
68	I/O	PD.8 / UART2_nRTS / LCD_SEG32 / TK_TK23
69	I/O	PC.5 / LCD_SEG31 / LCD_COM4 / TK_TK9 / UART2_TXD / I2C1_SCL
70	I/O	PC.4 / LCD_SEG30 / LCD_COM5 / TK_TK10 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA
71	I/O	PC.3 / LCD_SEG29 / LCD_COM6 / TK_TK11 / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD
72	I/O	PC.2 / LCD_SEG28 / LCD_COM7 / TK_TK12 / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD
73	I/O	PC.1 / LCD_SEG27 / LCD_COM2 / TK_TK24 / SPI1_CLK / UART2_TXD / I2C0_SCL / ACMP0_O
74	I/O	PC.0 / LCD_SEG26 / LCD_COM3 / TK_TK25 / SPI1_SS / UART2_RXD / I2C0_SDA / ACMP1_O
75	P	V_{SS}
76	P	V_{DD}
77	-	NC
78	-	NC
79	-	NC
80	-	NC
81	-	NC
82	-	NC
83	-	NC
84	I/O	PD.7 / UART1_TXD / I2C0_SCL / USCI1_CLK / TK_TK13 / SPI1_MISO
85	I/O	PD.6 / UART1_RXD / I2C0_SDA / USCI1_DAT1 / TK_TK14 / SPI1_MOSI
86	I/O	PD.5 / I2C1_SCL / USCI1_DAT0 / TK_TK15 / SPI1_CLK
87	I/O	PD.4 / USCI0_CTL0 / I2C1_SDA / USCI1_CTL1 / TK_TK16 / SPI1_SS
88	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / LCD_SEG25 / TK_TK13 / USCI1_CTL0 / UART0_TXD / UART3_nRTS
89	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / LCD_SEG24 / TK_TK14 / UART0_RXD / UART3_nCTS
90	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / LCD_SEG23 / TK_TK15 / UART3_TXD
91	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / LCD_SEG22 / TK_TK16 / UART3_RXD / TM2
92	I/O	PD.13 / SPI1_I2SMCLK / SPI0_I2SMCLK / LCD_SEG21
93	P	USB_VBUS
94	A	USB_D-
95	A	USB_D+
96	A	USB_VDD33_CAP
97	I/O	PE.7 / LCD_SEG16 / BPWM0_CH5
98	I/O	PE.6 / LCD_SEG15 / SC0_nCD / USCI0_CTL0 / BPWM0_CH4
99	I/O	PE.5 / SC0_PWR / USCI0_CTL1 / BPWM0_CH3
100	I/O	PE.4 / SC0_RST / USCI0_DAT1 / BPWM0_CH2
101	I/O	PE.3 / SC0_DAT / USCI0_DAT0 / BPWM0_CH1

102	I/O	PE.2 / SC0_CLK / USCI0_CLK / BPWM0_CH0
103	-	NC
104	-	NC
105	I/O	PE.1 / SPI1_MISO / UART3_TXD / I2C1_SCL
106	I/O	PE.0 / SPI1_MOSI / UART3_RXD / I2C1_SDA
107	-	NC
108	-	NC
109	-	NC
110	-	NC
111	-	NC
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / LCD_SEG14 / LCD_COM0 / TM1
116	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / LCD_SEG13 / LCD_COM1 / TM0_EXT
117	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / LCD_SEG12 / TM1_EXT / CLKO / TK_SE
118	I/O	PB.13 / EADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / LCD_SEG11 / TM2_EXT
119	I/O	PB.12 / EADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / LCD_SEG10 / TM3_EXT
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / I2C1_SCL / LCD_SEG9 / SPI0_I2SMCLK / BPWM1_CH0
124	I/O	PB.10 / EADC0_CH10 / USCI1_CTL0 / UART0_nRTS / I2C1_SDA / LCD_SEG8 / LCD_V1 / BPWM1_CH1
125	I/O	PB.9 / EADC0_CH9 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / LCD_SEG7 / LCD_V2 / BPWM1_CH2
126	I/O	PB.8 / EADC0_CH8 / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / LCD_SEG6 / LCD_V3 / BPWM1_CH3
127	I/O	PB.7 / EADC0_CH7 / USCI1_DAT0 / UART1_TXD / LCD_SEG5 / BPWM1_CH4 / INT5 / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / UART1_RXD / LCD_SEG4 / BPWM1_CH5 / INT4 / ACMP1_O

Table 4.1-19 M258KG6AE Multi-function Pin Table

4.2 Pin Mapping

Different part number with same package might has different function. Please refer to the selection guide in section 3.2, Pin Configuration in section 4.1 or NuTool - PinConfig.

Corresponding Part Number: M254/M256/M258

M254/M256/M258 Series Pin Mapping

	M254 Series				M256 Series				M258 Series		
Pin Name	**44 Pin**	**64 Pin**	**80 Pin**	**128 Pin**	**44 Pin**	**64 Pin**	**80 Pin**	**128 Pin**	**64 Pin**	**80 Pin**	**128 Pin**
PB.5	1	2	80	1	1	2	80	1	2	80	1
PB.4	2	3	1	2	2	3	1	2	3	1	2
PB.3	3	4	2	3	3	4	2	3	4	2	3
PB.2	4	5	3	4	4	5	3	4	5	3	4
PC.12				5				5			5
PC.11				6				6			6
PC.10			4	7			4	7		4	7
PC.9			5	8			5	8		5	8
PB.1	5	6	6	9	5	6	6	9	6	6	9
PB.0	6	7	7	10	6	7	7	10	7	7	10
V_{SS}			8	11			8	11		8	11
V_{DD}			9	12			9	12		9	12
PA.11	7	8	10	13	7	8	10	13	8	10	13
PA.10	8	9	11	14	8	9	11	14	9	11	14
PA.9	9	10	12	15	9	10	12	15	10	12	15
PA.8		11	13	16		11	13	16	11	13	16
V_{LCD}	10	12	14	17	10	12	14	17	12	14	17
PD.12			15	18			15	18		15	18
PD.11			16	19			16	19		16	19
PD.10			17	20			17	20		17	20
NC				21				21			21
NC				22				22			22
NC				23				23			23
NC				24				24			24
NC				25				25			25
NC				26				26			26
NC				27				27			27
PF.7				28				28			28

PF.6				29				29			29
PF.14 or V_{BAT}		13				13					
V_{BAT}				30				30	13		30
PF.5	11	14	18	31	11	14	18	31	14	18	31
PF.4	12	15	19	32	12	15	19	32	15	19	32
NC				33				33			33
NC				34				34			34
NC				35				35			35
NC				36				36			36
PF.3	13	16	20	37	13	16	20	37	16	20	37
PF.2	14	17	21	38	14	17	21	38	17	21	38
NC				39				39			39
NC				40				40			40
PE.8			22	41			22	41		22	41
PE.9			23	42			23	42		23	42
PE.10			24	43			24	43		24	43
PE.11			25	44			25	44		25	44
PE.12				45				45			45
PE.13			26	46			26	46		26	46
PC.8			27	47			27	47		27	47
PC.7		18	28	48		18	28	48	18	28	48
PC.6		19	29	49		19	29	49	19	29	49
PA.7	15	20	30	50	15	20	30	50	20	30	50
PA.6	16	21	31	51	16	21	31	51	21	31	51
V_{SS}		22		52		22		52	22		52
V_{DD}		23		53		23		53	23		53
PD.15		24	32	54		24	32	54	24	32	54
PA.5		25	33	55		25	33	55	25	33	55
PA.4		26	34	56		26	34	56	26	34	56
PA.3	17	27	35	57	17	27	35	57	27	35	57
PA.2	18	28	36	58	18	28	36	58	28	36	58
PA.1	19	29	37	59	19	29	37	59	29	37	59
PA.0	20	30	38	60	20	30	38	60	30	38	60
PF.15		31	39	61		31	39	61	31	39	61
PE.14			40	62			40	62		40	62

PE.15				63				63			63
nRESET	21	32	41	64	21	32	41	64	32	41	64
PF.0	22	33	42	65	22	33	42	65	33	42	65
PF.1	23	34	43	66	23	34	43	66	34	43	66
PD.9			44	67			44	67		44	67
PD.8			45	68			45	68		45	68
PC.5	24	35	46	69	24	35	46	69	35	46	69
PC.4	25	36	47	70	25	36	47	70	36	47	70
PC.3	26	37	48	71	26	37	48	71	37	48	71
PC.2	27	38	49	72	27	38	49	72	38	49	72
PC.1	28	39	50	73	28	39	50	73	39	50	73
PC.0	29	40	51	74	29	40	51	74	40	51	74
V_{SS}				75				75			75
V_{DD}				76				76			76
NC				77				77			77
NC				78				78			78
NC				79				79			79
NC				80				80			80
NC				81				81			81
NC				82				82			82
NC				83				83			83
PD.7				84				84			84
PD.6				85				85			85
PD.5				86				86			86
PD.4				87				87			87
PD.3		41	52	88		41	52	88	41	52	88
PD.2		42	53	89		42	53	89	42	53	89
PD.1		43	54	90		43	54	90	43	54	90
PD.0		44	55	91		44	55	91	44	55	91
PD.13			56	92			56	92		56	92
PA.12	30	45	57	93	30	45	57	93			
PA.13	31	46	58	94	31	46	58	94			
PA.14	32	47	59	95	32	47	59	95			
PA.15	33	48	60	96	33	48	60	96			
USB_VBUS									45	57	93

USB_D-									46	58	94
USB_D+									47	59	95
USB_VDD33_CAP									48	60	96
PE.7			61	97			61	97		61	97
PE.6			62	98			62	98		62	98
PE.5				99				99			99
PE.4				100				100			100
PE.3				101				101			101
PE.2				102				102			102
NC				103				103			103
NC				104				104			104
PE.1				105				105			105
PE.0				106				106			106
NC				107				107			107
NC				108				108			108
NC				109				109			109
NC				110				110			110
NC				111				111			111
V_{SS}	34	49	63	112	34	49	63	112	49	63	112
LDO_CAP	35	50	64	113	35	50	64	113	50	64	113
V_{DD}	36	51	65	114	36	51	65	114	51	65	114
PC.14		52	66	115		52	66	115	52	66	115
PB.15	37	53	67	116	37	53	67	116	53	67	116
PB.14	38	54	68	117	38	54	68	117	54	68	117
PB.13	39	55	69	118	39	55	69	118	55	69	118
PB.12	40	56	70	119	40	56	70	119	56	70	119
AV_{DD}	41	57	71	120	41	57	71	120	57	71	120
V_{REF}		58	72	121		58	72	121	58	72	121
AV_{SS}	42	59	73	122	42	59	73	122	59	73	122
PB.11		60	74	123		60	74	123	60	74	123
PB.10		61	75	124		61	75	124	61	75	124
PB.9		62	76	125		62	76	125	62	76	125
PB.8		63	77	126		63	77	126	63	77	126
PB.7	43	64	78	127	43	64	78	127	64	78	127
PB.6	44	1	79	128	44	1	79	128	1	79	128

4.3 Pin Functional Description

M254/M256/M258 Series Pin Functional Description

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
CLKO	CLKO	O	Clock Out
DAC0	DAC0_OUT	A	DAC0 channel analog output.
	DAC0_ST	I	DAC0 external trigger input.
DAC1	DAC1_OUT	A	DAC1 channel analog output.
	DAC1_ST	I	DAC1 external trigger input.

Group	Pin Name	Type	Description
EADC0	EADC0_CH0	A	EADC0 channel 0 analog input.
	EADC0_CH1	A	EADC0 channel 1 analog input.
	EADC0_CH2	A	EADC0 channel 2 analog input.
	EADC0_CH3	A	EADC0 channel 3 analog input.
	EADC0_CH4	A	EADC0 channel 4 analog input.
	EADC0_CH5	A	EADC0 channel 5 analog input.
	EADC0_CH6	A	EADC0 channel 6 analog input.
	EADC0_CH7	A	EADC0 channel 7 analog input.
	EADC0_CH8	A	EADC0 channel 8 analog input.
	EADC0_CH9	A	EADC0 channel 9 analog input.
	EADC0_CH10	A	EADC0 channel 10 analog input.
	EADC0_CH11	A	EADC0 channel 11 analog input.
	EADC0_CH12	A	EADC0 channel 12 analog input.
	EADC0_CH13	A	EADC0 channel 13 analog input.
	EADC0_CH14	A	EADC0 channel 14 analog input.
	EADC0_CH15	A	EADC0 channel 15 analog input.
	EADC0_ST	I	EADC0 external trigger input.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
	I2C1_SMBAL	O	I2C1 SMBus SMBALTER pin
	I2C1_SMBSUS	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
ICE	ICE_CLK	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.

Group	Pin Name	Type	Description
INT5	INT5	I	External interrupt 5 input pin.
LCD	LCD_COM0	A	LCD common 0 output pin
	LCD_COM1	A	LCD common 1 output pin
	LCD_COM2	A	LCD common 2 output pin
	LCD_COM3	A	LCD common 3 output pin
	LCD_COM4	A	LCD common 4 output pin
	LCD_COM5	A	LCD common 5 output pin
	LCD_COM6	A	LCD common 6 output pin
	LCD_COM7	A	LCD common 7 output pin
	LCD_SEG0	A	LCD segment 0 output pin
	LCD_SEG1	A	LCD segment 1 output pin
	LCD_SEG2	A	LCD segment 2 output pin
	LCD_SEG3	A	LCD segment 3 output pin
	LCD_SEG4	A	LCD segment 4 output pin
	LCD_SEG5	A	LCD segment 5 output pin
	LCD_SEG6	A	LCD segment 6 output pin
	LCD_SEG7	A	LCD segment 7 output pin
	LCD_SEG8	A	LCD segment 8 output pin
	LCD_SEG9	A	LCD segment 9 output pin
	LCD_SEG10	A	LCD segment 10 output pin
	LCD_SEG11	A	LCD segment 11 output pin
	LCD_SEG12	A	LCD segment 12 output pin
	LCD_SEG13	A	LCD segment 13 output pin
	LCD_SEG14	A	LCD segment 14 output pin
	LCD_SEG15	A	LCD segment 15 output pin
	LCD_SEG16	A	LCD segment 16 output pin
	LCD_SEG17	A	LCD segment 17 output pin
	LCD_SEG18	A	LCD segment 18 output pin
	LCD_SEG19	A	LCD segment 19 output pin
	LCD_SEG20	A	LCD segment 20 output pin
	LCD_SEG21	A	LCD segment 21 output pin
	LCD_SEG22	A	LCD segment 22 output pin
	LCD_SEG23	A	LCD segment 23 output pin
	LCD_SEG24	A	LCD segment 24 output pin

Group	Pin Name	Type	Description
	LCD_SEG25	A	LCD segment 25 output pin
	LCD_SEG26	A	LCD segment 26 output pin
	LCD_SEG27	A	LCD segment 27 output pin
	LCD_SEG28	A	LCD segment 28 output pin
	LCD_SEG29	A	LCD segment 29 output pin
	LCD_SEG30	A	LCD segment 30 output pin
	LCD_SEG31	A	LCD segment 31 output pin
	LCD_SEG32	A	LCD segment 32 output pin
	LCD_SEG33	A	LCD segment 33 output pin
	LCD_SEG34	A	LCD segment 34 output pin
	LCD_SEG35	A	LCD segment 35 output pin
	LCD_SEG36	A	LCD segment 36 output pin
	LCD_SEG37	A	LCD segment 37 output pin
	LCD_SEG38	A	LCD segment 38 output pin
	LCD_SEG39	A	LCD segment 39 output pin
	LCD_SEG40	A	LCD segment 40 output pin
	LCD_SEG41	A	LCD segment 41 output pin
	LCD_SEG42	A	LCD segment 42 output pin
	LCD_SEG43	A	LCD segment 43 output pin
	LCD_SEG44	A	LCD segment 44 output pin
	LCD_SEG45	A	LCD segment 45 output pin
	LCD_SEG46	A	LCD segment 46 output pin
	LCD_SEG47	A	LCD segment 47 output pin
	LCD_V1	A	LCD Unit voltage for charge pump circuit.
	LCD_V2	A	LCD driver biasing voltage.
	LCD_V3	A	LCD driver biasing voltage.
Power	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	LDO_CAP	A	LDO output pin. Note: This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet.
	V_{BAT}	P	Power supply by batteries for RTC.
	V_{DD}	P	Power supply for I/O ports and LDO source for digital circuit.
	V_{LCD}	P	Power supply for LCD.

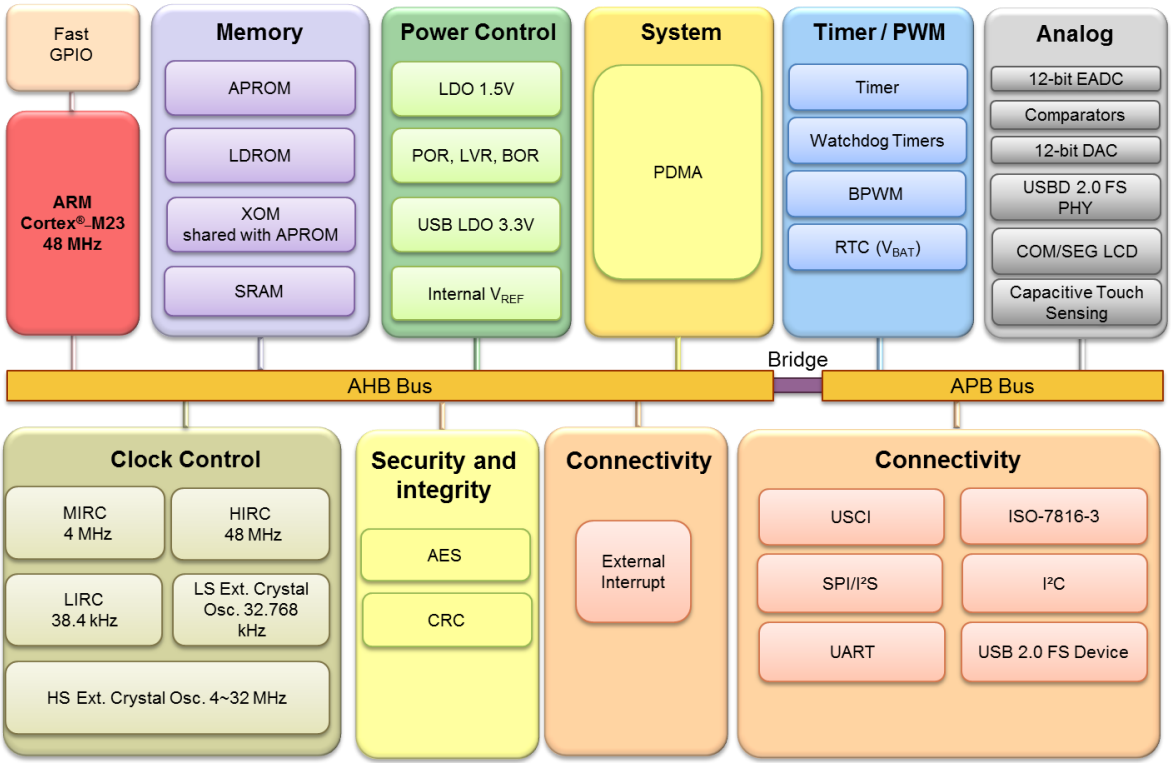
Group	Pin Name	Type	Description
	V_{REF}	A	ADC reference voltage input. Note: This pin needs to be connected with a 1uF capacitor.
	V_{SS}	P	Ground pin for digital circuit.
SC0	SC0_CLK	O	Smart Card 0 clock pin.
	SC0_DAT	I/O	Smart Card 0 data pin.
	SC0_PWR	O	Smart Card 0 power pin.
	SC0_RST	O	Smart Card 0 reset pin.
	SC0_nCD	I	Smart Card 0 card detect pin.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_I2SMCLK	I/O	SPI0 I2S master clock output pin
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_I2SMCLK	I/O	SPI1 I2S master clock output pin
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS	I/O	SPI1 slave select pin.
TK	TK_SE	I/O	Touch key (shielding electrode)
	TK_TK0	I/O	Touch key 0
	TK_TK1	I/O	Touch key 1
	TK_TK2	I/O	Touch key 2
	TK_TK3	I/O	Touch key 3
	TK_TK4	I/O	Touch key 4
	TK_TK5	I/O	Touch key 5
	TK_TK6	I/O	Touch key 6
	TK_TK7	I/O	Touch key 7
	TK_TK8	I/O	Touch key 8
	TK_TK9	I/O	Touch key 9
	TK_TK10	I/O	Touch key 10
	TK_TK11	I/O	Touch key 11
	TK_TK12	I/O	Touch key 12
	TK_TK13	I/O	Touch key 13
	TK_TK14	I/O	Touch key 14

Group	Pin Name	Type	Description
	TK_TK15	I/O	Touch key 15
	TK_TK16	I/O	Touch key 16
	TK_TK17	I/O	Touch key 17
	TK_TK18	I/O	Touch key 18
	TK_TK19	I/O	Touch key 19
	TK_TK20	I/O	Touch key 20
	TK_TK21	I/O	Touch key 21
	TK_TK22	I/O	Touch key 22
	TK_TK23	I/O	Touch key 23
	TK_TK24	I/O	Touch key 24
	TK_TK25	I/O	Touch key 25
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
	UART3_nCTS	I	UART3 clear to Send input pin.

Group	Pin Name	Type	Description
	UART3_nRTS	O	UART3 request to Send output pin.
USB	USB_D+	A	USB differential signal D+.
	USB_D-	A	USB differential signal D-.
	USB_VBUS	P	Power supply from USB host or HUB.
	USB_VDD33_CAP	A	Internal power regulator output 3.3V decoupling pin. Note: This pin needs to be connected with a 1uF capacitor.
USCI0	USCI0_CLK	I/O	USCI0 clock pin.
	USCI0_CTL0	I/O	USCI0 control 0 pin.
	USCI0_CTL1	I/O	USCI0 control 1 pin.
	USCI0_DAT0	I/O	USCI0 data 0 pin.
	USCI0_DAT1	I/O	USCI0 data 1 pin.
USCI1	USCI1_CLK	I/O	USCI1 clock pin.
	USCI1_CTL0	I/O	USCI1 control 0 pin.
	USCI1_CTL1	I/O	USCI1 control 1 pin.
	USCI1_DAT0	I/O	USCI1 data 0 pin.
	USCI1_DAT1	I/O	USCI1 data 1 pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.

5 BLOCK DIAGRAM

5.1 M254/256/M258 Block Diagram



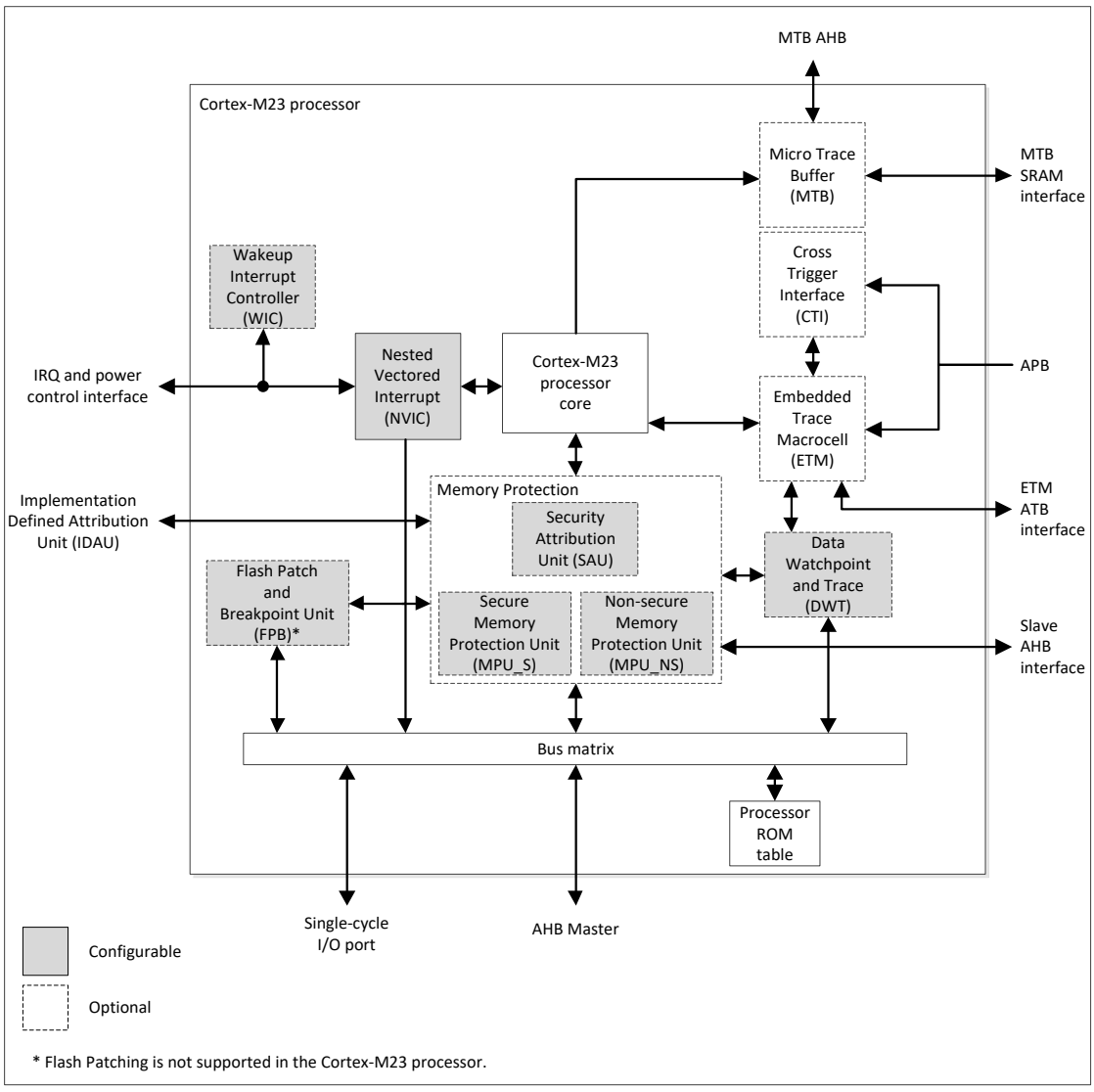
USB* : Only supported in M258 series.
Capacitive Touch Sensing* : Only supported in M256/M258 series.
Please refer to the selection guide in section 4.2 for detail information.

Figure 5.1-1 M254/M256/M258 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M23 Core

The Cortex®-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, which has an AMBA AHB5 interface supporting Arm® TrustZone® technology, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension. The NuMicro® M254/M256/M258 is embedded with Cortex®-M23 processor.Figure 6.1-1 shows the functional controller of the processor.



Note: M254/M256/M258 don't support security attribution unit, ETM, CTI and MTB function.

Figure 6.1-1 Cortex®-M23 Block Diagram

Cortex®-M23 processor features:

- Arm®v8-M Baseline architecture.
- Arm®v8-M Baseline Thumb®-2 instruction set that combines high code density with 32-bit performance.
- Support for single-cycle I/O access.
- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced Flash and ROM power consumption.
- A 32-bit Single cycle Hardware multiplier.
- A 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm® Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Protected Memory System Architecture (PMSAv8) Memory Protection Units (MPUs) for both Secure and Non-secure states.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin with glitch filter time 24us
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M23 core Only by writing 1 to CPURST (SYS_IPRST0[1])

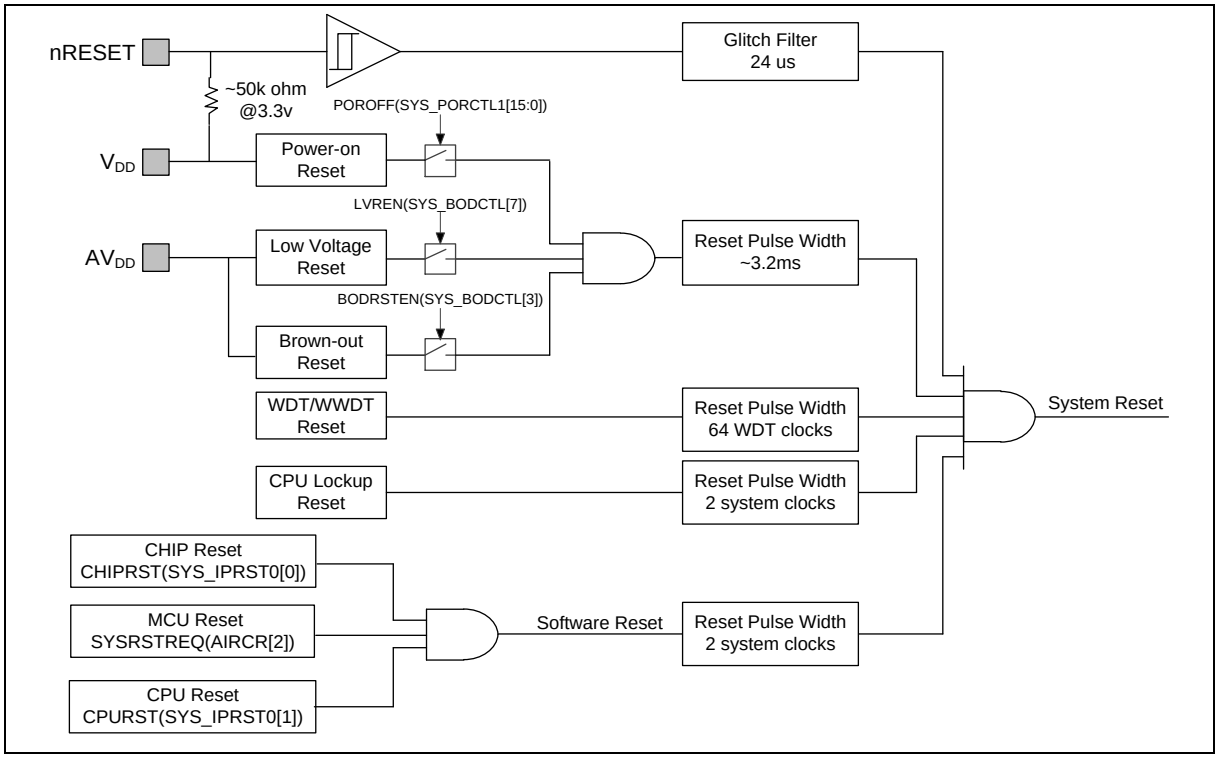


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M23 only; the other reset sources will reset Cortex®-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources **Register**	**POR**	**NRESET**	**WDT**	**LVR**	**BOD**	**Lockup**	**CHIP**	**MCU**	**CPU**
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[18:16])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	0x0	0x0	0x0	0x0	0x0	-	0x0	-	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL	0x5	0x5	0x5	0x5	0x5	-	0x5	0x5	-

(CLK_CLKSEL0[2:0])									
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	-	0x0800	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[29:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 24 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 24 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset

source is nRESET reset. Table 6.2-2 shows the nRESET reset waveform.

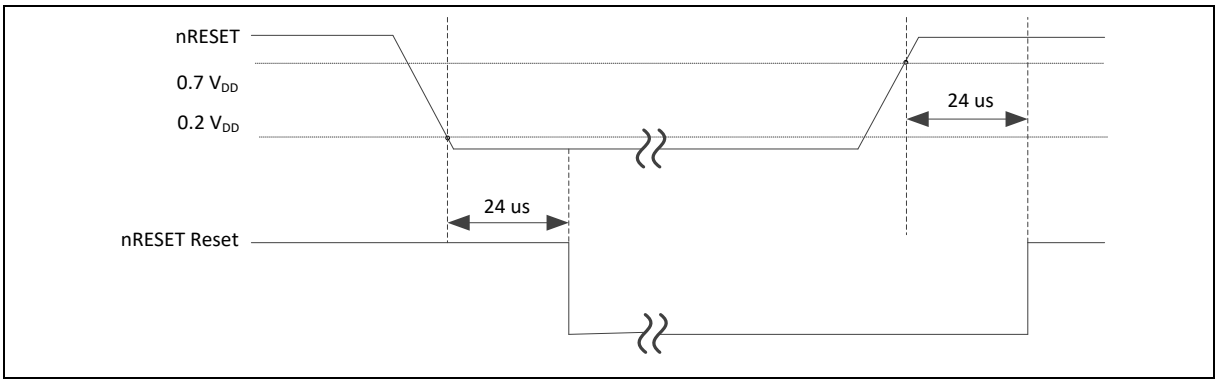


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

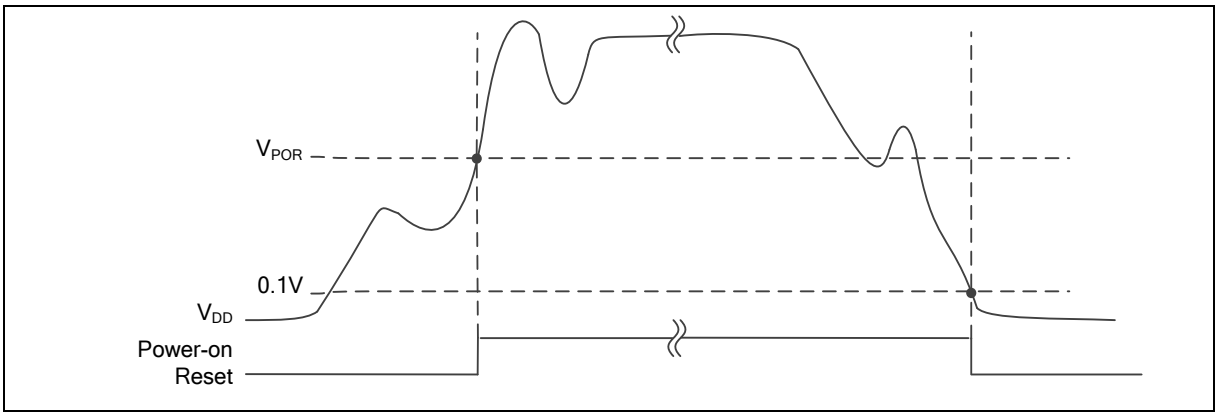


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

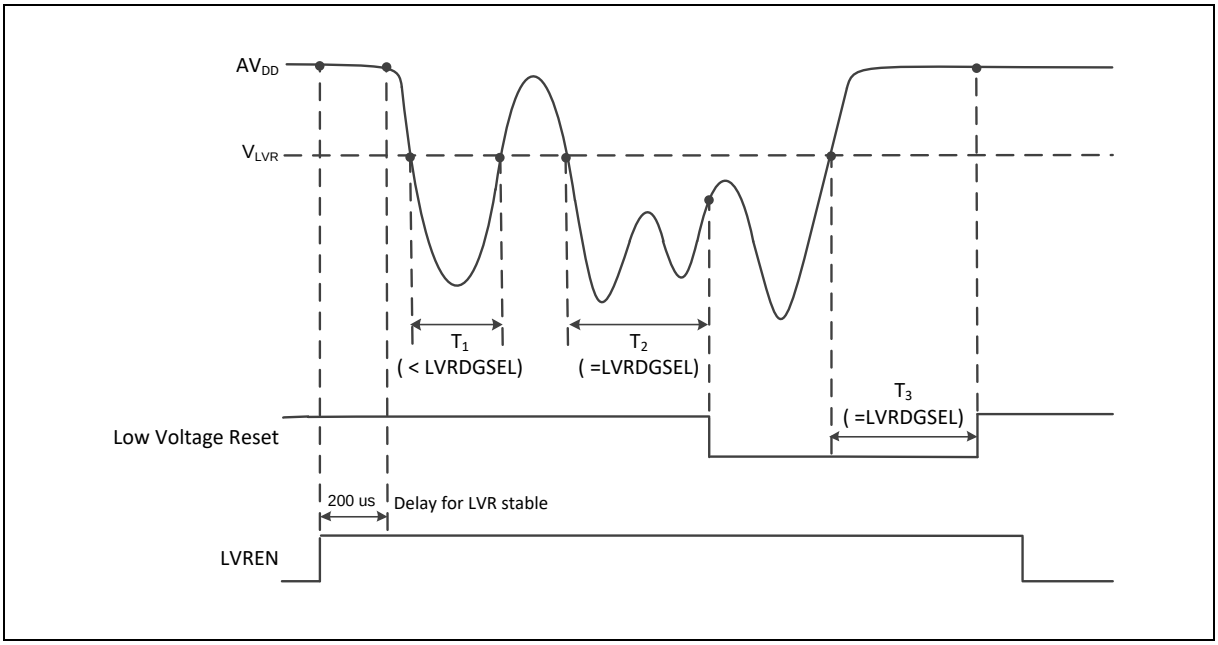


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

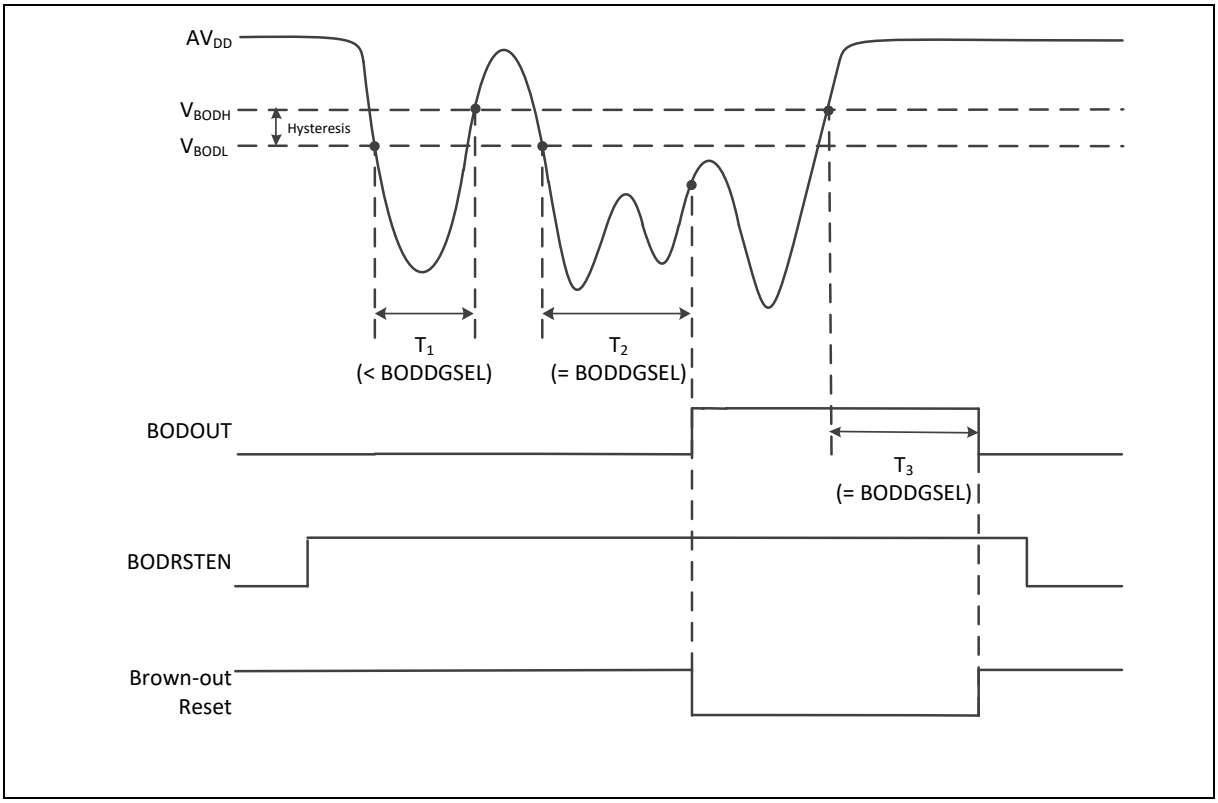


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M23 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.5V power for digital operation and I/O pins.
- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.
- RTC power from regulator uninterrupted power domain provides, the power for RTC.

Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-6 shows the ower distribution of the M254/M256/M258 series.

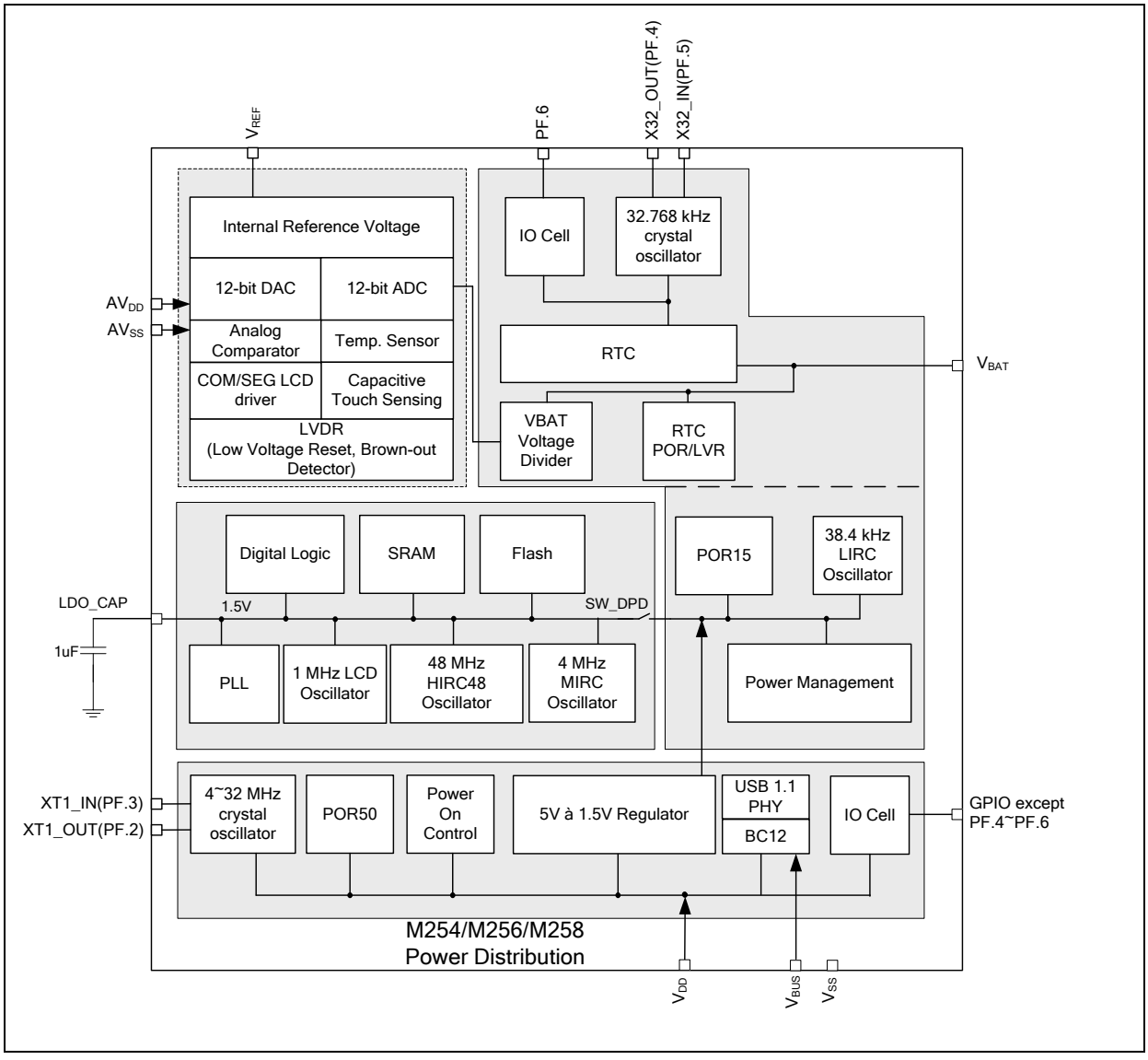


Figure 6.2-6 NuMicro® M254/M256/M258 Series Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The MM254/M256/M258 series has a power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power modes in the M254/M256/M258 series.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP(V)	Clock Disable
Normal mode	48	1.5	All clocks are disabled by control register.
Idle mode	CPU enters Sleep mode	1.5	Only CPU clock is disabled.
Power-down mode	CPU enters Deep Sleep mode	1.5	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Fast wake up Power-down mode (FWPD)	CPU enters Sleep mode	1.5	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Deep Power-down mode (DPD)	Power off	1.5	Only LIRC/LXT still enable for RTC function and wake-up timer usage

Table 6.2-2 Power Mode Table

There are different power mode entry settings. Each power mode has different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running ar normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCTL:[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode (CPU enters Sleep mode)	0	0	0	YES
Power-down mode (CPU enters Deep Sleep mode)	1	1	0	YES
Fast wake up Power-down mode (FWPD)	1	1	2	YES
Deep Power-down mode (CPU enters Sleep mode)	1	1	6	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, USBD and ACMP
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Difference Table

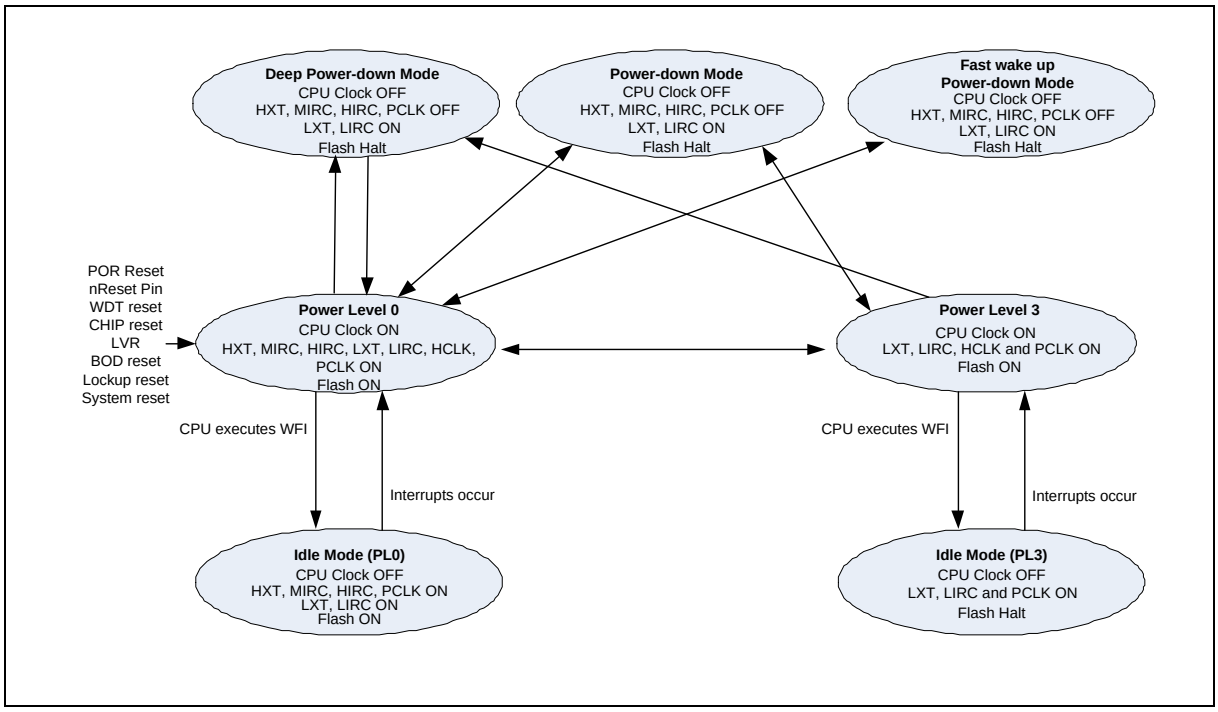


Figure 6.2-7 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (38.4 kHz OSC) ON or OFF depends on SOFTWARE setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode PD	DPD
HXT (4~32 MHz XTL)	ON	ON	Halt	Halt
MIRC (4 MHz OSC)	ON	ON	Halt	Halt
HIRC48 (48 MHz OSC)	ON	ON	Halt	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]	ON/OFF[1]
LIRC (38.4 kHz OSC)	ON	ON	ON/OFF[2]	ON/OFF[2]
OSCLCD (1.2 MHz OSC)	ON	ON	ON/OFF	Halt
LDO	ON	ON	ON	OFF
CPU	ON	Halt	Halt	Halt
HCLK/PCLK	ON	ON	Halt	Halt
SRAM retention	ON	ON	ON	OFF
FLASH	ON	ON	Halt	Halt
GPIO	ON	ON	Halt	Halt
PDMA	ON	ON	Halt	Halt
TIMER	ON	ON	ON/OFF[3]	Halt
PWM	ON	ON	Halt	Halt
WDT	ON	ON	ON/OFF[4]	Halt
WWDT	ON	ON	Halt	Halt
RTC	ON	ON	ON/OFF[5]	ON/OFF[5]
UART	ON	ON	ON/OFF[6]	Halt
SC	ON	ON	Halt	Halt
USCI	ON	ON	Halt	Halt
I^2C	ON	ON	Halt	Halt
SPI	ON	ON	Halt	Halt
USBD	ON	ON	Halt	Halt
ADC	ON	ON	Halt	Halt
ACMP	ON	ON	Halt	Halt
Touch Key	ON	ON	ON/OFF	OFF
LCD	ON	ON	ON/OFF	OFF

Table 6.2-5 Clocks in Power Modes

Wake-up sources in Power-down mode:

RTC, WDT, I²C, Timer, UART, USCI, BOD, GPIO, USBD, and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-5 ists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-Down Mode		System Can Enter Power-Down Mode Again Condition*
		PD FWKPD	DPD	
BOD	Brown-Out Detector Interrupt	Y	N	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
LVR	LVR Reset	Y	N	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		N	Y	After software writes 1 to CLRWK (CLK_PMUSTS[31] to clear LVRWK (CLK_PMUSTS[12]) when DPD mode is entered.
INT	External Interrupt	Y	N	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	Y	N	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PC.0) Wake-up pin	Rising or falling edge event, 1-pin	N	Y	PINWK0(CLK_PMUSTS[0]) is cleared when DPD mode is entered.
GPIO(PB.0) Wake-up pin	Rising or falling edge event, 1-pin	N	Y	PINWK1(CLK_PMUSTS[3]) is cleared when DPD mode is entered.
GPIO(PB.2) Wake-up pin	Rising or falling edge event, 1-pin	N	Y	PINWK2(CLK_PMUSTS[4]) is cleared when DPD mode is entered.
GPIO(PB.12) Wake-up pin	Rising or falling edge event, 1-pin	N	Y	PINWK3(CLK_PMUSTS[5]) is cleared when DPD mode is entered.
GPIO(PF.6) Wake-up pin	Rising or falling edge event, 1-pin	N	Y	PINWK4(CLK_PMUSTS[6]) is cleared when DPD mode is entered.
TIMER	Timer Interrupt	Y	N	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	N	Y	TMRWK (CLK_PMUSTS[1]) is cleared when SPD or DPD mode is entered.
WDT	WDT Interrupt	Y	N	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	Y	N	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	Y	N	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
RTC	Wakeup by RTC alarm	N	Y	RTCWK (CLK_PMUSTS[2]) is cleared when DPD mode is entered.
	Wakeup by RTC tick time	N	Y	RTCWK (CLK_PMUSTS[2]) is cleared when DPD mode is entered.
UART	nCTS wake-up	Y	N	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	Incoming Data wake-up	Y	N	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	Y	N	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode	Y	N	After software writes 1 to clear RS485WKF

	Wake-up			(UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	Y	N	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	Y	N	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	Y	N	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	Y	N	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	Y	N	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], and then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	Y	N	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	Y	N	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
USBD	Remote Wake-up	Y	N	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	Y	N	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
TK	Touch Key detect be touched Interrupt	Y	N	After software writes 1 to clear TKIFx,x=0~16 (TK_STA[24:8]) TKIF_ALL(TK_STA[7]) and TKIF(TK_STA[6]) and SCIF(TK_STA[1])

Table 6.2-6 Condition of Entering Power-down Mode Again

6.2.5 Chip Bus Matrix

The M254/M256/M258 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M254/M256/M258 series only supports little-endian data format.

6.2.6 System Memory Map

The MM254/M256/M258 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M254/M256/M258 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 Kbytes)
0x2000_0000 – 0x2000_7FFF	SRAM0_BA	SRAM Memory Space (32 Kbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4004_7000 – 0x4004_7FFF	DAC_BA	DAC Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers

0x4008_1000 – 0x4008_1FFF	I2C1_BA	I2C1 Control Registers
0x4009_0000 – 0x4009_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x400B_B000 – 0x400B_BFFF	SLCD_BA	SLCD Device Control Register
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400C_2000 – 0x400C_2FFF	TK_BA	TK Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.7 SRAM Memory Orginization

The M254/M256/M258 series supports embedded SRAM with up to 32 Kbytes size.

- Supports up to 32 Kbytes SRAM
- Supports byte /half word /word write
- Supports oversize response error

Table 6.2-9 shows the M254/M256/M258 series SRAM organization. The address between 0x2000_8000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

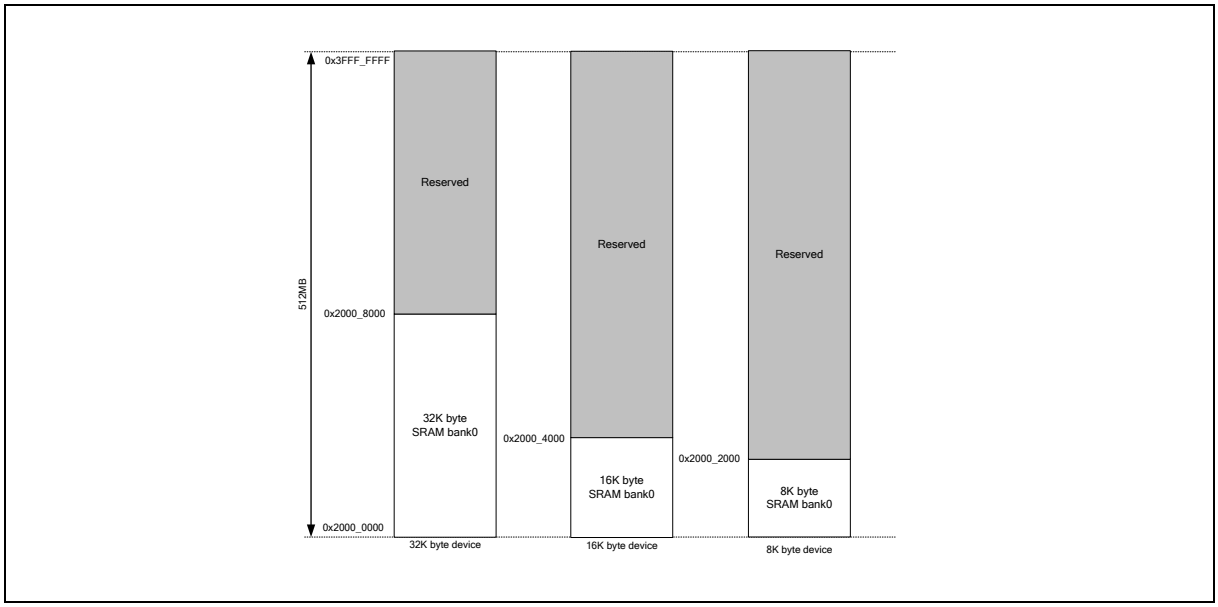


Figure 6.2-8 SRAM Memory Organization

6.2.8 IRC Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator) and MIRC trim (4.032 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 4.032 MHz clock. In such case, if neither uses HXT as the system clock source nor solders 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_MIRCTRIMCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_MIRCTRIMCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_MIRCTRIMSTS[0] MIRC frequency lock status) “1” indicates the MIRC output frequency is accurate within 0.25% deviation.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if neither uses HXT as the system clock source nor solders 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTRIMCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTRIMCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTRIMSTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

HIRC trim and MIRC trim can only work properly when the clock sources are stable. When the RC clock or the reference clock is not stable or the system goes into power down, HIRC trim and MIRC trim need to wait until the clock is stable or system wakes up, and then it can be enabled or will get a clock error flag.

6.2.9 System Timer (SysTick)

The Cortex®-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm® Cortex®-M23 Technical Reference Manual” and “Arm® v8-M Architecture Reference Manual”.

6.2.10 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-64 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.10.1 Exception Model and System Interrupt Map

Table 6.2-8 lists the exception model supported by the M254/M256/M258 series. Software can set 4 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xC0” (The 6-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80.

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Reserved	4~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Reserved	12~13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ63)	16 ~ 63	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	Reserved	Reserved
20	4	CLKFAIL	Clock fail detected interrupt
21	5	Reserved	Reserved
22	6	RTC_INT	Real time clock interrupt
23	7	Reserved	Reserved
24	8	WDT_INT	Watchdog Timer interrupt
25	9	WWDT_INT	Window Watchdog Timer interrupt
26	10	EINT0	External interrupt from PA.0, PD.2 or PE.4 pins
27	11	EINT1	External interrupt from PB.0, PD.3 or PE.5 pins
28	12	EINT2	External interrupt from PC.0 pin
29	13	EINT3	External interrupt from PD.0 pin
30	14	EINT4	External interrupt from PE.0 pin
31	15	EINT5	External interrupt from PF.0 pin
32	16	GPA_INT	External interrupt from PA[15:0] pin
33	17	GPB_INT	External interrupt from PB[15:0] pin

34	18	GPC_INT	External interrupt from PC[15:0] pin
35	19	GPD_INT	External interrupt from PD[15:0] pin
36	20	GPE_INT	External interrupt from PE[15:0] pin
37	21	GPF_INT	External interrupt from PF[15:0] pin
38	22	Reserved	Reserved
39	23	SPI0_INT	SPI0 interrupt
40	24	Reserved	Reserved
41	25	Reserved	Reserved
42	26	Reserved	Reserved
43	27	Reserved	Reserved
44	28	Reserved	Reserved
45	29	Reserved	Reserved
46	30	Reserved	Reserved
47	31	Reserved	Reserved
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	UART1_INT	UART1 interrupt
54	38	I2C0_INT	I2C0 interrupt
55	39	I2C1_INT	I2C1 interrupt
56	40	PDMA_INT	PDMA interrupt
57	41	DAC_INT	DAC interrupt
58	42	EADC_INT	EADC interrupt source 0
59	43	EADC1_INT	EADC interrupt source 1
60	44	ACMP01_INT	ACMP0 and ACMP1 interrupt
61	45	BPWM0	BPWM0 interrupt
62	46	EADC2_INT	EADC interrupt source 2
63	47	EADC3_INT	EADC interrupt source 3
64	48	UART2_INT	UART2 interrupt
65	49	Reserved	Reserved
66	50	USCI0	USCI0 interrupt
67	51	Reserved	Reserved
68	52	USCI1	USCI1 interrupt

69	53	USBD_INT	USB device interrupt
70	54	BPWM1	BPWM1
71	55	Reserved	Reserved
72	56	Reserved	Reserved
73	57	Reserved	Reserved
74	58	SC0_INT	Smart card host 0 interrupt
75	59	Reserved	Reserved
76	60	Reserved	Reserved
77	61	Reserved	Reserved
78	62	Reserved	Reserved
79	63	Reserved	Reserved

Table 6.2-9 Interrupt Number Table

6.2.10.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in the next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M23 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~32 MHz external high speed crystal (HXT), 48 MHz internal high speed RC oscillator (HIRC) and 4 MHz internal median speed RC oscillator (MIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

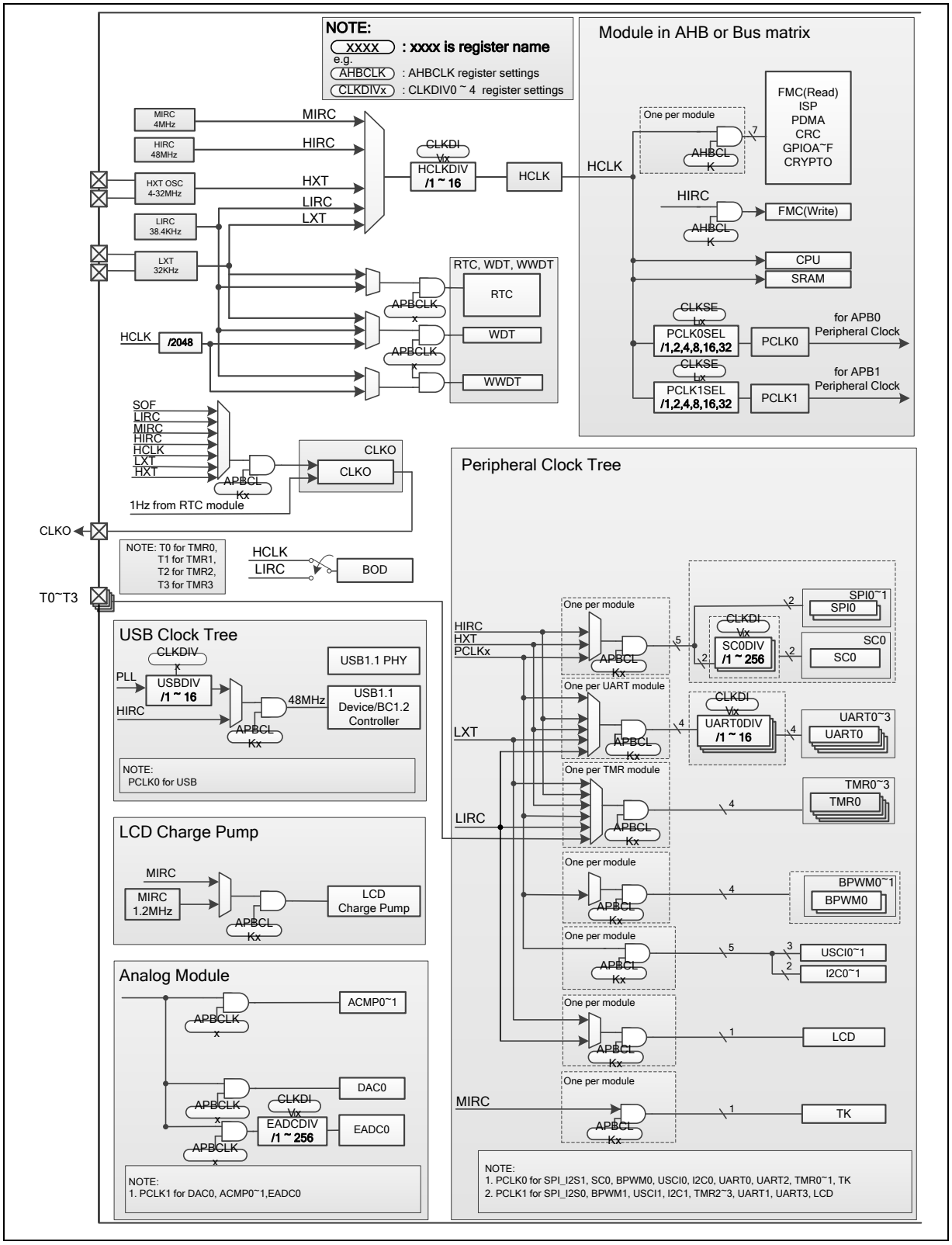


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 6 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~32 MHz external high speed crystal oscillator (HXT)
- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)
- 4 MHz internal medium speed oscillator (MIRC)

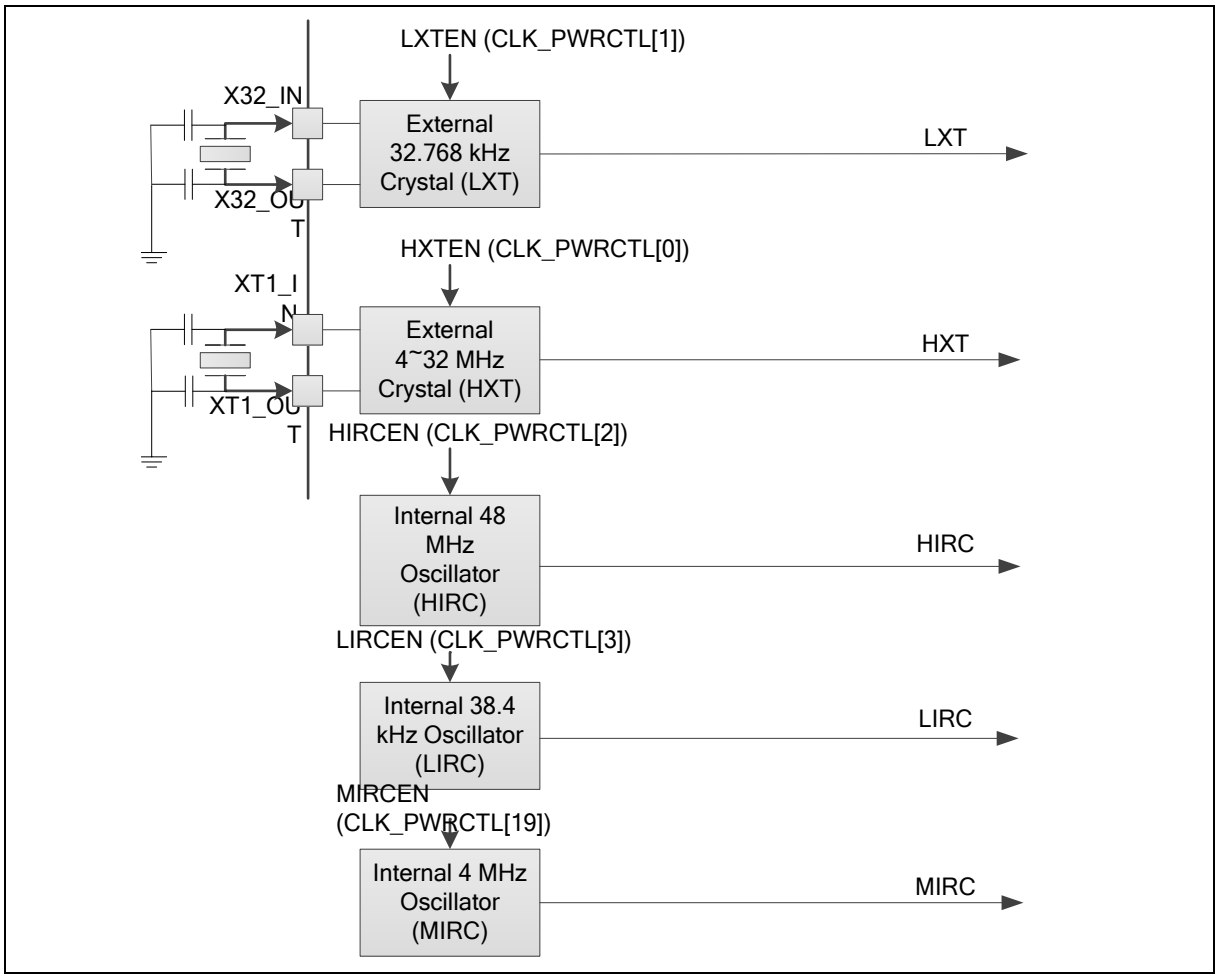


Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 6 clock sources, which are generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3

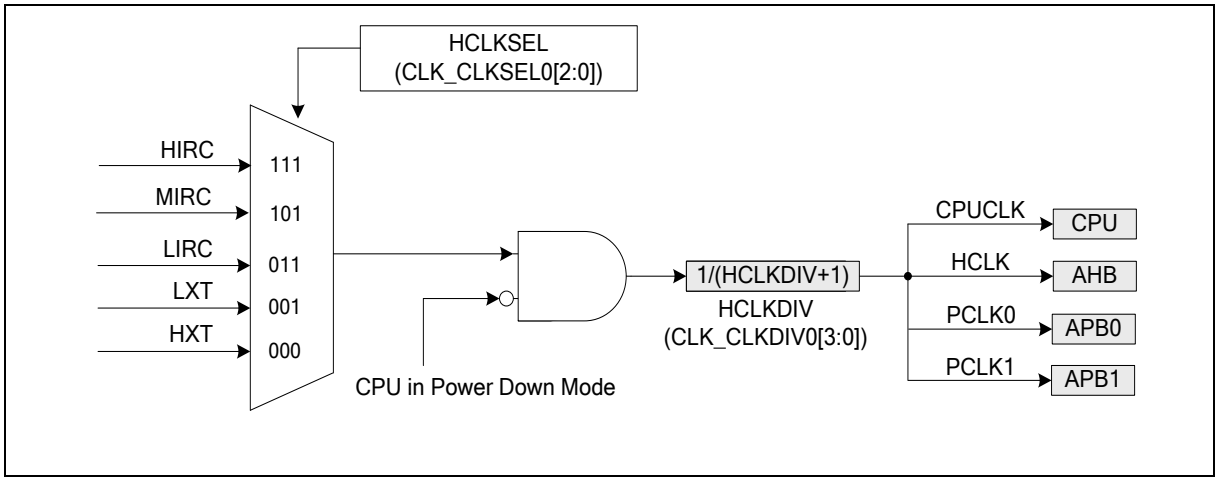


Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the MIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switched to MIRC if HXT clock stops being detected in the following condition: system clock source comes from HXT. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recovered to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to MIRC procedure is shown in Figure 6.3-4.

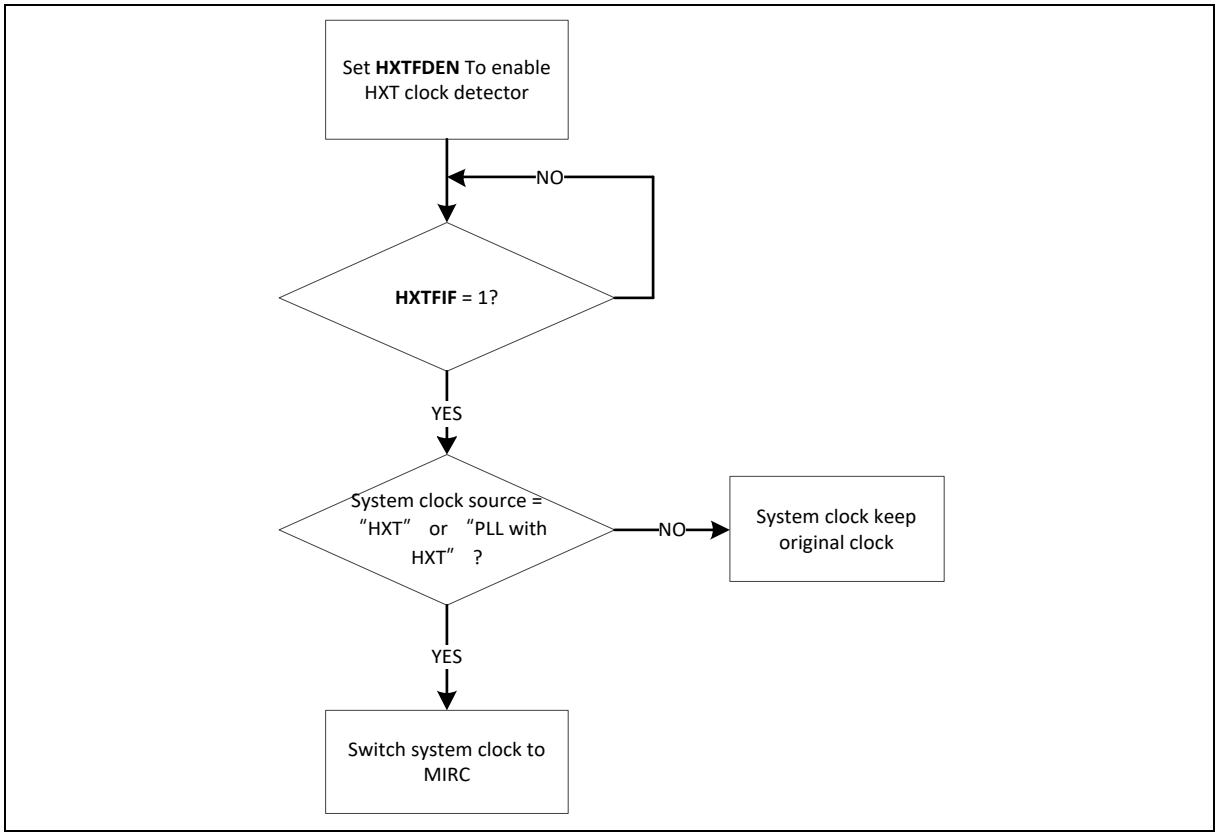


Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M23 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

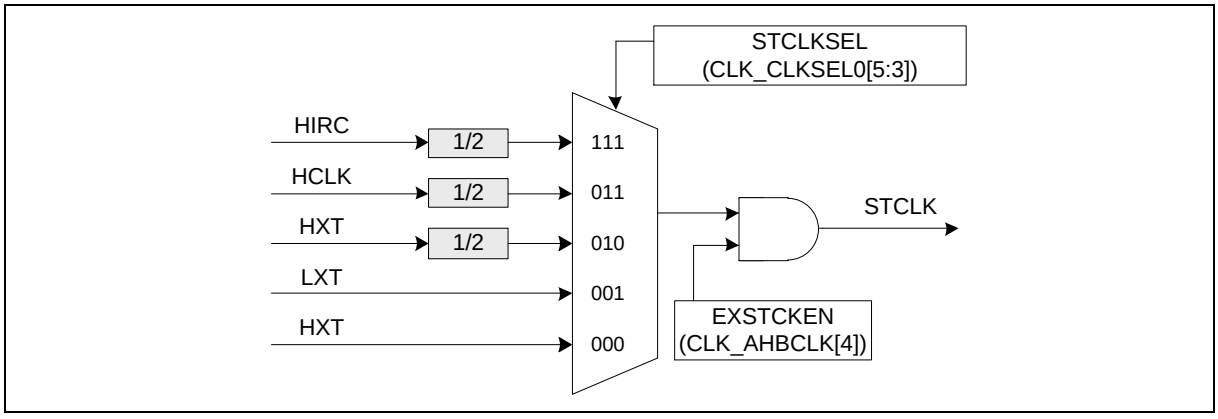


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock has different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSEL1 and CLK_CLKSEL2 register description in Register Description section.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
  - 4 MHz internal medium speed oscillator (MIRC) clock if LCD and TK enabled.
- Peripherals clock, except for HCLK, PCLK0 and PCLK1 (when the modules adopt LXT or LIRC as clock source).

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

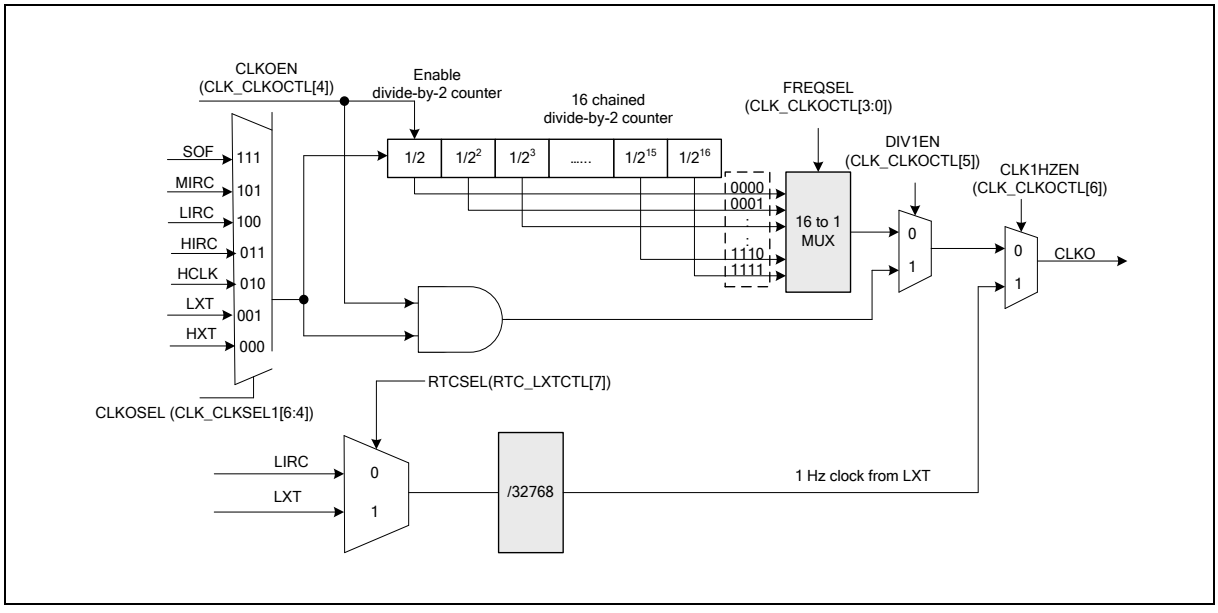


Figure 6.3-6 Clock Output Block Diagram

6.3.7 USB Clock Source

The clock source of USB 1.0 is generated from 48 MHz HIRC.

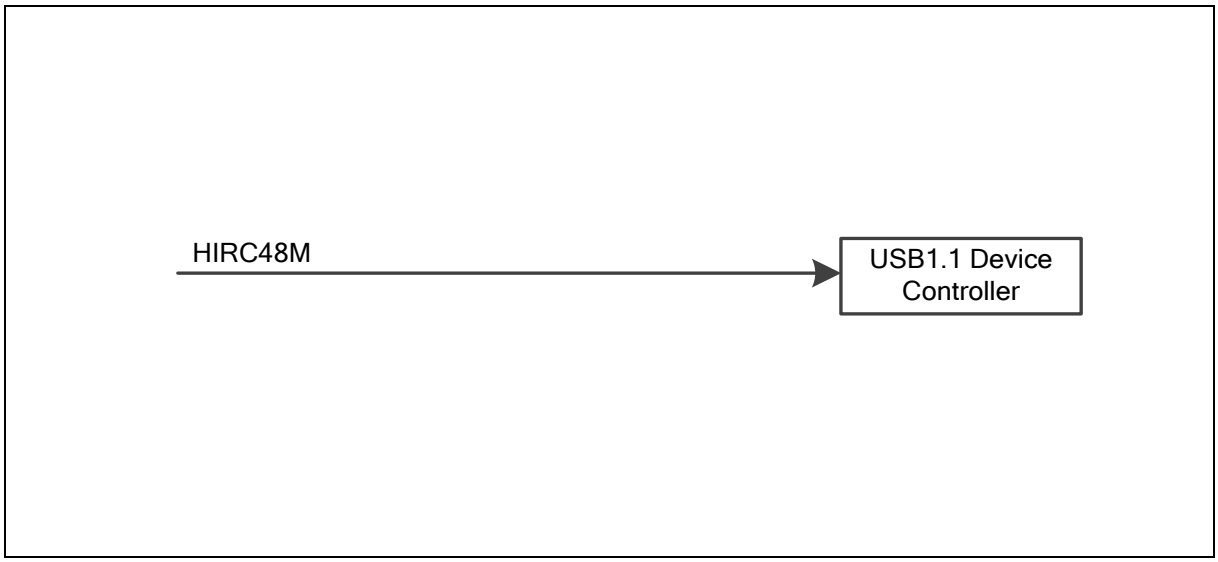


Figure 6.3-7 USB Clock Source

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The FMC is equipped with 64/128/256 Kbytes on-chip embedded Flash for application. A User Configuration block is provided for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. XOM (Execution Only Memory) setting block is used to conceal user program in XOM region. A 512/1024/2048 bytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.4.2 Features

- Supports 64/128/256 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 1 XOM (Execution Only Memory) region to conceal user program in APROM
- Supports 12 bytes User Configuration block to control system initiation.
- Supports 512 bytes page erase for all embedded Flash
- Supports 32-bit and multi-word Flash programming function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports embedded SRAM remap to system vector memory
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 86 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 86 pins are arranged in 6 ports named as PA, PB, PC, PD, PE, and PF. PA, PB and PE has 16 pins on port. PC has 14 pins on port, PD has 15 pins on port. PF has 9 pins on port. Each of the 86 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]). Each I/O pin has a very weakly individual pull-up/pull-down resistor which is about 50 kΩ. Please refer to the M254/M256/M258 Datasheet for detailed pin operation voltage information about V_{DD} and V_{BAT} electrical characteristics.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function
- Improves access efficiency by using single cycle I/O bus
- Support 5V tolerance except PF2, PF3, PF4 and PF5

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 8 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports up to 8 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Request source can be from software, SPI/I^{2}S, UART, USCI, EADC, DAC, PWM capture event and TIMER
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel 1

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports one PWM output and two selectable PWM output channels (TMx or TMx_EXT). The output state of PWM output pin can be control by polarity control, output enable control and output channel select.

6.7.2 Features

6.7.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin (TMx_EXT) event for interval measurement
- Supports external capture pin (TMx_EXT) event to reset 24-bit up counter
- Supports internal clock (HIRC, LIRC, MIRC) and external clock (HXT, LXT) for capture event
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger BPWM, PWM, EADC, DAC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode
- Supports event counting source from internal USB SOF signal
- Supports Timer0~3 time-out interrupts signal (TIF) to trigger Touch-Key scan.

6.7.2.2 PWM Function Features

- Supports PWM generator with two selectable output channels
- Supports 16-bit PWM counter
  - Up count operation type
  - One-shot or auto-reload counter operation mode
- Supports 8-bit prescale from 1 to 256
- Supports 16-bit compare register and period register and double buffer for period register and compare register
- Supports tri-state enable and polarity control for each PWM selectable output channels
- Supports interrupt on the following events:

  - PWM period point, up-count compared point events
- Supports wake-up when interrupt occurs when clock source is LXT or LIRC
- PWM can generate output in Power-down mode
- Supports trigger EADC, PDMA, and DAC on the following events:
  - PWM period point and up-count compared point events

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 417us ~ 27. 3 s if WDT_CLK = 38.4 kHz (LIRC).
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 38.4 kHz LIRC or LXT.

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.10 Real Time Clock (RTC)

6.10.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.10.2 Features

- Supports external power pin V_{BAT}.
- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.

6.11 Basic PWM Generator and Capture Timer (BPWM)

6.11.1 Overview

The chip provides up to two BPWM generators. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.11.2 Features

6.11.2.1 BPWM Function Features

- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.11.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.12 UART Interface Controller (UART)

6.12.1 Overview

The chip provides up to four channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.12.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0 with LIN function)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode.

UART Feature	UART0	UART1 ~ UART3	USCI-UART
FIFO	16 Bytes	16 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	√
IrDA	√	√	-
LIN	√	-	-
RS-485 Function Mode	√	√	√
nCTS Wake-up	√	√	√
Incoming Data Wake-up	√	√	√
Received Data FIFO reached threshold Wake-up	√	√	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-
Auto-Baud Rate Measurement	√	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√
Stick Bit	√	√	-

Table 6.12-1 NuMicro® M254/M256/M258 Series UART Features

6.13 Smart Card Host Interface (SC)

6.13.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.13.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- One ISO 7816-3 port
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.14 Serial Peripheral Interface (SPI)

6.14.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. The SPI controller also supports I^2S mode to connect external audio CODEC. Please refer to the M254/M256/M258 Datasheet for detailed information about maximum SPI clock frequency of SPI master mode and SPI slave mode and range of SPI operation voltage.

6.14.2 Features

- SPI Mode
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.15 I²C Serial Interface Controller (I²C)

6.15.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers that support Power-down wake-up function.

6.15.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

6.16 USCI - Universal Serial Control Interface Controller (USCI)

6.16.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.16.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.17 USCI – UART Mode

6.17.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

6.17.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Supports 9-bit Data Transfer (supports 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.18 USCI - SPI Mode

6.18.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

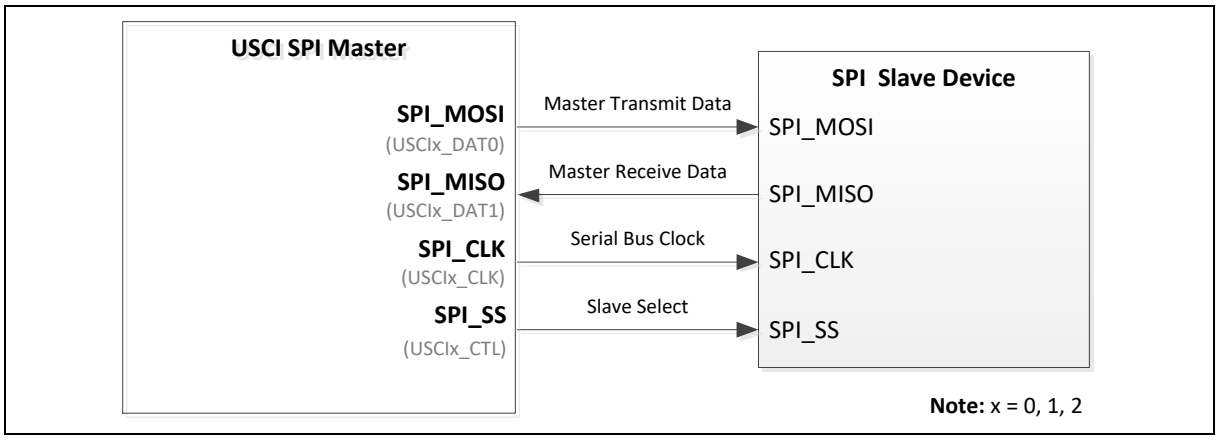


Figure 6.18-1 SPI Master Mode Application Block Diagram

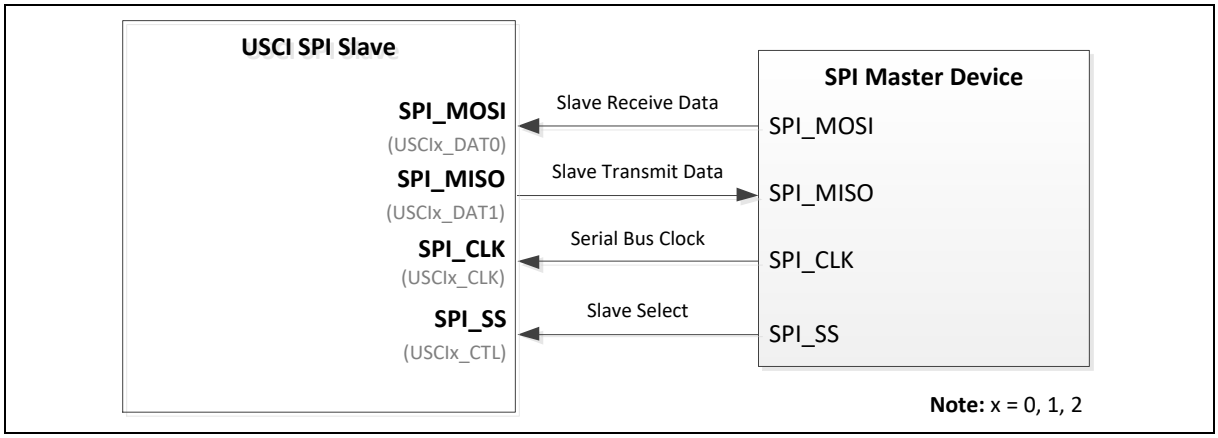


Figure 6.18-2 SPI Slave Mode Application Block Diagram

6.18.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master < f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence

- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.19 USCI - I²C Mode

6.19.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.19-1 for more detailed I²C BUS Timing.

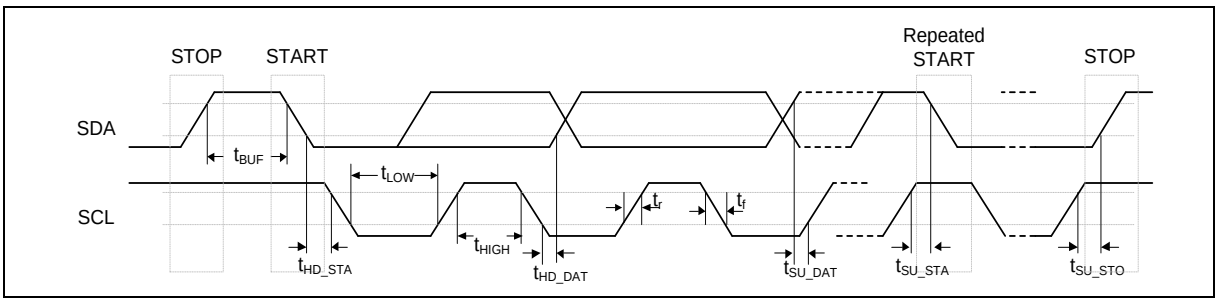


Figure 6.19-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: The external pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.19.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kbps) or in fast mode (up to 400 kbps)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.20 USB 2.0 Full-Speed Device Controller (USBD)

6.20.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver with BC1.2 in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SI.E. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are five different interrupt events in this controller. They are no-event-wake-up, device plug-in or plug-out event, USB events, such as IN ACK, OUT ACK, etc., and BUS events, such as suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurred, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurred in this endpoint.

A software-disconnect function is supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, the host will enumerate the USB device again.

Battery Charging 1.2 protocol is also supported in this USB controller. It executes V_{BUS} detect, DCD detect, PD (primary detect) and SD (secondary detect) through BCDC register. Status in BCDC will tell users what port is connected.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.20.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbytes buffer size
- Provides remote wake-up capability
- Supports Battery charging 1.2 (BC12) with interrupt event (BCD)

6.21 CRC Controller (CRC)

6.21.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.21.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.22 Cryptographic Accelerator (CRYPTO)

6.22.1 Overview

The Crypto (Cryptographic Accelerator) supports AES algorithms. The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

6.22.2 Features

- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode
  - Supports key expander

6.23 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.23.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR ADC converter) with 16 external input channels and 3 internal channels. The ADC converter can be started by software trigger, PWM0/1 triggers, BPWM0/1 triggers, Timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

6.23.2 Features

- Analog input voltage range: 0~V_{REF} (Max to AV_{DD})
- Reference voltage from V_{REF} pin or AV_{DD}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels
- 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and Battery power (V_{BAT}/4)
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses
- Maximum EADC clock frequency is 16 MHz
- Up to 730 KSPS conversion rate
- Configurable EADC internal sampling time.
- Up to 7 sample modules:
  - 4 sample modules that can be configurable for EADC converter channel EADC_CH0~15 and trigger source
  - Sample module 16~18 is fixed for EADC channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and battery power (V_{BAT}/4)
  - Configurable sampling time for each sample module
  - Support left-adjusted result
  - 12-bit resolution for conversion result and 16-bit resolution for accumulated conversion result
  - Conversion results are held in 7 data registers with valid and overrun indicators
  - Averaging (2^n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2^n times, n=0~8) to support up to 16-bit result
- An ADC conversion can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18)
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - BPWM0/1 triggers
- Supports configurable PDMA transfer
- Auto turn on/off EADC power at power off or operation mode with wait state(10us stable time)
- Supports digital comparator to monitor conversion result and user can select whether to generate an interrupt when conversion result matches the compare register setting

- Internal reference voltage source: 1.536V, 2.048V, 2.560V, 3.072V, 4.096V and V_{REF} pin

6.24 LCD Controller

6.24.1 Overview

The LCD controller controls the device's built-in voltage/current drivers, which can drive externally connected LCD panels with up to 8 common planes (or called common electrodes, COMs) and 48 segments (SEGs). Each COM or SEG output pin of the device can supply the necessary voltage waveform to the connected LCD panels.

The LCD controller provides several setting registers, by which users can effectively control a variety of LCD panels with specific considerations for display modes, driving capability, and power consumption.

6.24.2 Features

- Supports the following maximum COM/SEG combinations:
  - 352 pixels (8-COM x 44-SEG)
  - 276 pixels (6-COM x 46-SEG)
  - 192 pixels (4-COM x 48-SEG)

  (**Note:** The above numbers may differ for some devices with various package pinouts. Please refer to device datasheets for the exact numbers.)
- Supports up to 8 COM output pins, multiplexed with GPIO pins
- Supports up to 48 SEG output pins, multiplexed with GPIO pins
- Supports 3 bias levels: 1/2, 1/3, and 1/4
- Supports 8 duty ratios: 1, 1/2, 1/3, 1/4, 1/5, 1/6, 1/7, and 1/8
- Supports both types A and B waveforms
- Supports a clock frequency divider, programmable from 0 to 1023, to generate the LCD operating frequency (F_{LCD})
- Supports LCD operating voltage (V_{LCD}) from 3.0 V to 5.2 V
- Selectable LCD operating voltage sources:
  - V_{LCD} (External dedicated V_{DD} pin for LCD) power
  - AV_{DD} (Analog V_{DD}) power
  - Built-in charge pump
- A built-in resistive network to generate required bias voltages
  - Supports 2 drive modes: low-drive and high-drive modes
  - Supports voltage buffers which are active only in the low-drive mode
- Supports a programmable power-saving mode. During this mode,
  - the resistive network temporarily changes to the low-drive mode, or
  - the voltage buffers are temporarily turned off.
- At the end of every frame, a dedicated flag is set and an interrupt can be programmed to occur.
- Supports a frame counter. At the end of frame counting, a dedicated flag is set and an interrupt can be programmed to occur.
- Supports LCD blinking capability. By using the frame counter, users have more flexibility to adjust the blinking frequency.
- Selectable LCD clock sources: LIRC and LXT. LCD display or blinking can keep working

even when the chip is in Power-down mode, only if at least one of LIRC and LXT is active.

- Supports a charging timer for the charge pump, by which users can estimate the loading of the charge pump, and adjust, if necessary, its charging power.

6.25 Digital to Analog Converter (DAC)

6.25.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12-or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.25.2 Features

- Analog output voltage range: 0~AV_{DD}.
- Supports 12-or 8-bit output mode.
- Rail to rail settle time 8us.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

6.26 Analog Comparator Controller (ACMP)

6.26.1 Overview

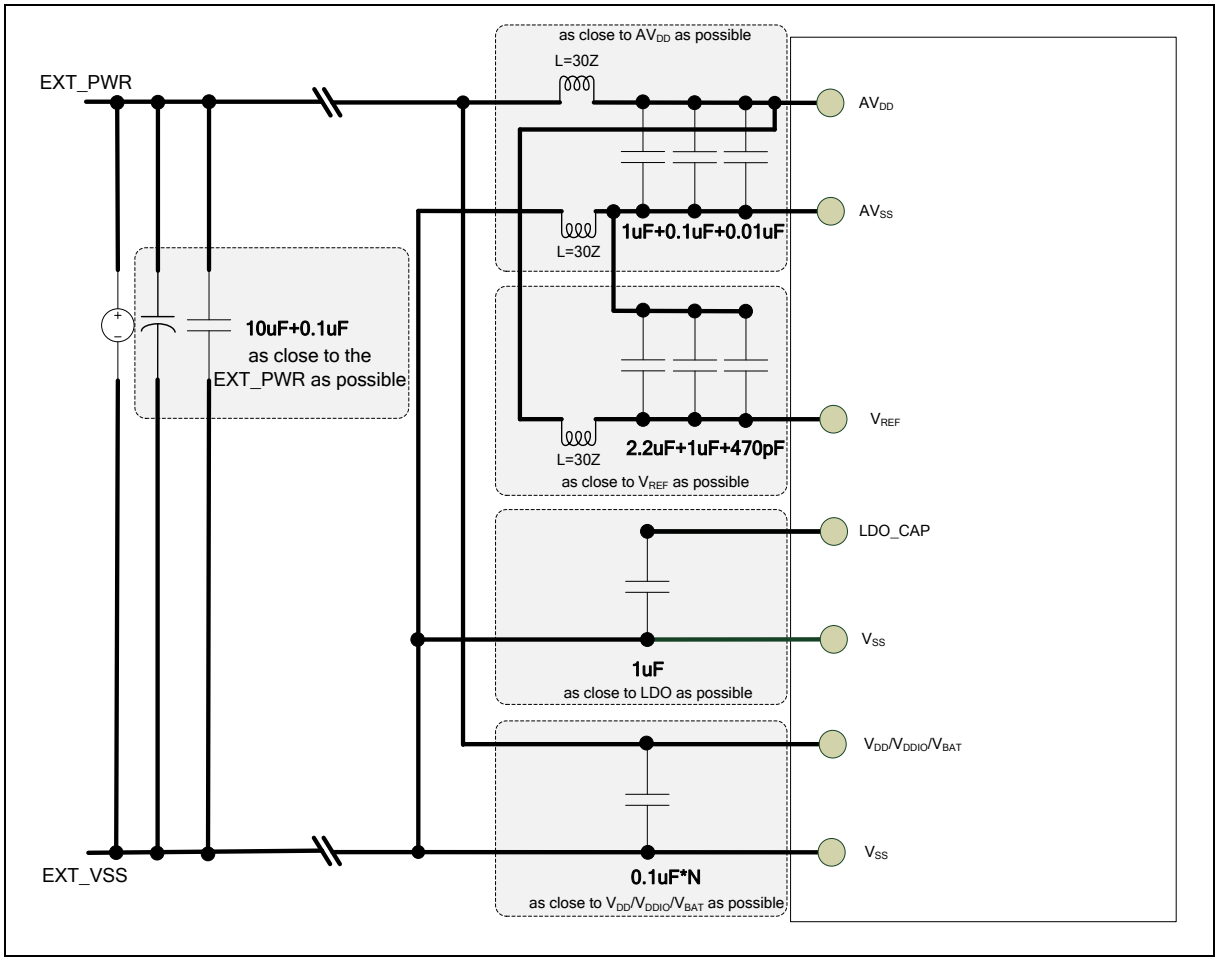
The chip provides up to two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.26.2 Features

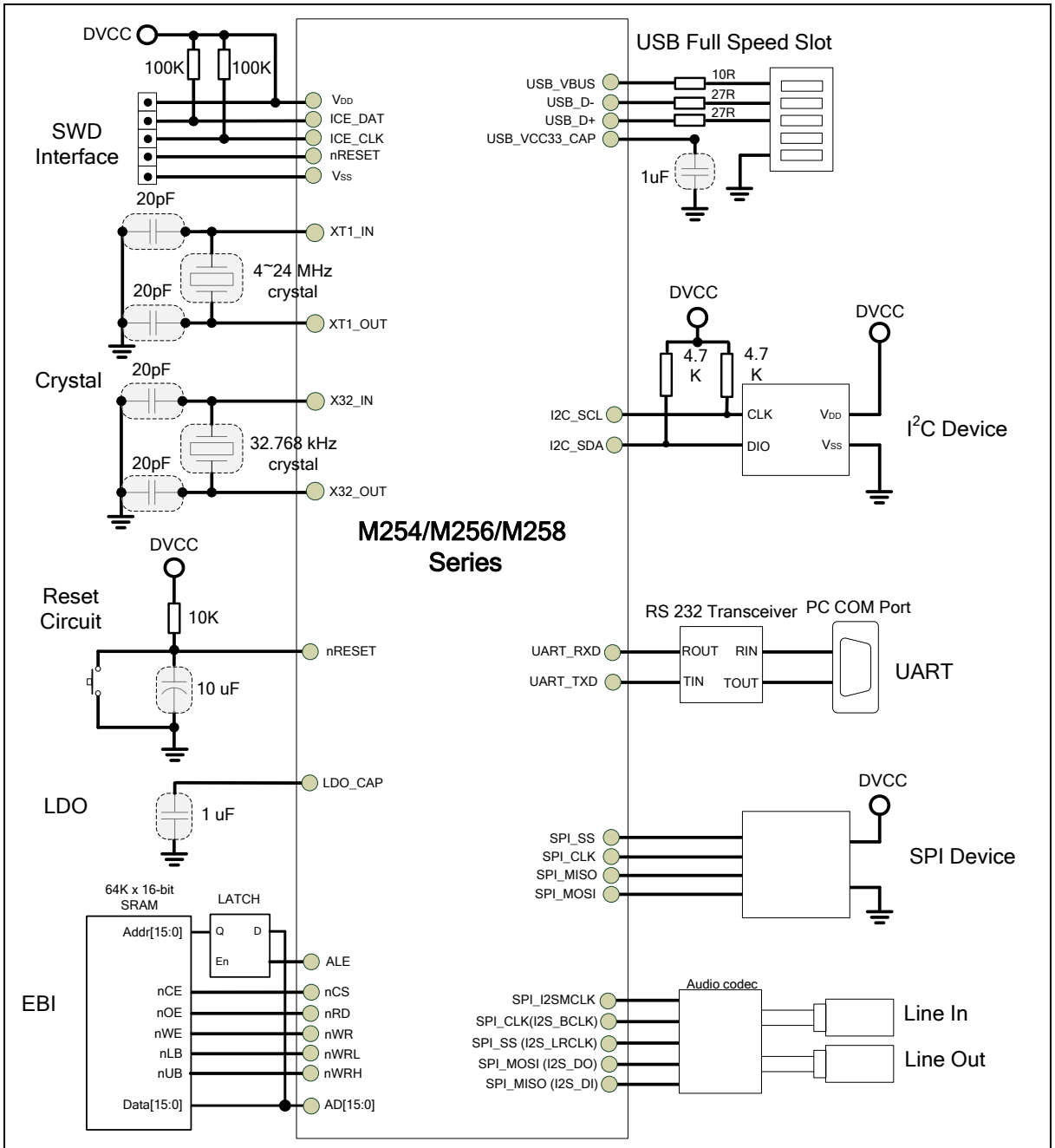
- Analog input voltage range: 0 ~ AV_{DD}
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
- Supports wake-up function
- Supports programmable propagaion speed and low power consumption
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for PWM
- Supports window compare mode and window latch mode

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



7.2 Peripheral Application Scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Note 3: It is recommended to use 10Ω series resistor on USB_VBUS pin.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
V_{BAT}-V_{SS}[*1]	V_{BAT} Power Supply	-0.3	6.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on any other pin[*2]	V_{SS}-0.3	6.5	V

Notes:

1. All main power (V_{DD}, V_{BAT}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
I_{BAT}	Maximum Current into V_{BAT}	-	100	
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 44-pin LQFP(10x10 mm)	-	48.4	-	℃/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	℃/Watt
	Thermal resistance junction-ambient 80-pin LQFP(14x14 mm)	-	63.1	-	℃/Watt
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	38.5	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-7000	-	+7000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-750	-	+750	
LU[*3]	Pin current for latch-up[*3]	-150 Class I	-	+150 Class I	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-4 EMC characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
44-pin LQFP(10x10 mm) [*1]	MSL 3
64-pin LQFP(7x7 mm) [*1]	MSL 3
80-pin LQFP(14x14 mm) [*1]	MSL 3
128-pin LQFP(14x14 mm) [*1]	MSL 3
Note: 1. Determined according to IPC/JEDEC J-STD-020	

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

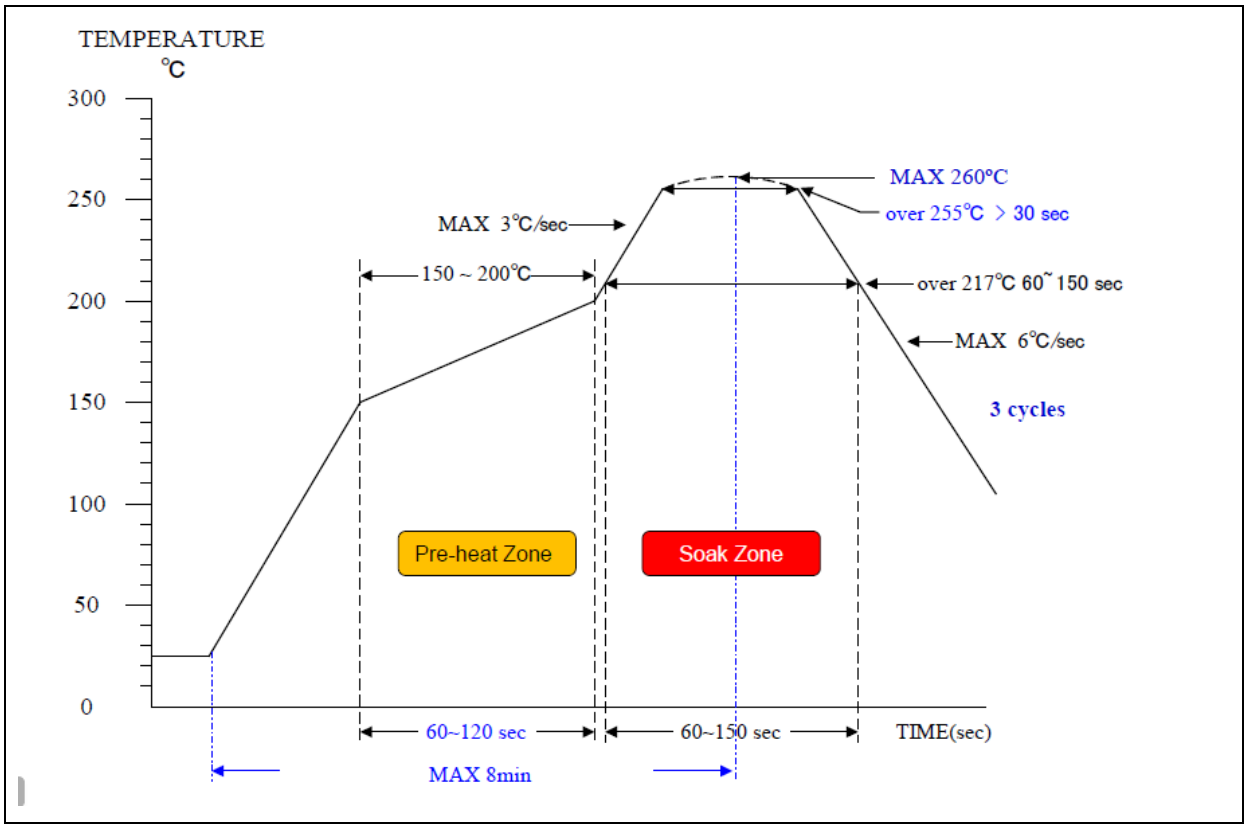


Figure 8.1-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.75 ~ 5.5V, T_A = 25°C, HCLK = 48 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz	
V_{DD}	Operation voltage	1.75	-	5.5	V	
V_{BAT}	V_{BAT} Operation voltage	1.75	-	5.5		
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	1.75	-	AV_{DD}		
V_{LDO}	LDO output voltage	-	1.5	-		
V_{BG}	Band-gap voltage	795	815	840	mV	
C_{LDO}[*2]	LDO output capacitor on each pin	1			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	60	150	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	1.8	-	µC	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 60 mA for 30 µs

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

Table 8.2-1 General operating conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics for M254xD/M256xD/M254xE/M256xE/M258xE

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1.75 ~ 5.5 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{BAT}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable. HCLK is set as HIRC or HXT clock.	48 MHz	5.36	6.0	6.2	6.4	mA
		32 MHz	3.92	4.4	4.8	5.0	
		24 MHz	3.20	3.65	3.85	4.05	
		12 MHz	2.10	2.4	2.6	2.8	
		4 MHz	1.35	1.55	1.75	1.95	
	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable. HCLK is set as MIRC clock.	4 MHz	0.64	0.85	1.05	1.25	
		2 MHz	0.45	0.65	0.85	1.05	
		1 MHz	0.35	0.55	0.75	0.95	
	Normal run mode with PL3 (PLSEL = 11), executed from Flash, all peripherals disable. HCLK is set as LIRC or LXT clock..	38.4 kHz	0.01	0.02	0.06	0.16	
		32.768 kHz	0.01	0.02	0.06	0.16	
	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable. HCLK is set as HIRC or HXT clock.	48 MHz	11.73	13.5	13.7	13.9	
		32 MHz	8.00	9.0	9.2	9.4	
		24 MHz	6.60	7.5	7.7	7.9	
		12 MHz	3.98	4.8	5.0	5.2	
		4 MHz	2.24	3.1	3.3	3.5	
	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable. HCLK is set as MIRC clock.	4 MHz	1.16	1.35	1.55	1.75	
		2 MHz	0.71	0.9	1.1	1.3	
		1 MHz	0.49	0.7	0.9	1.1	
	Normal run mode with PL3 (PLSEL = 11), executed from	38.4 kHz	0.05	0.06	0.08	0.18	

	Flash, all peripherals enable HCLK is set as LIRC or LXT clock..	32.768 kHz	0.05	0.06	0.08	0.18	

Note:

1. When analog peripheral blocks such as USB, ADC, ACMP, HIRC, MIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current consumption in Normal Run mode

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode with PL0 (PLSEL = 00), all peripherals disable. HCLK is set as HIRC or HXT clock.	48 MHz	1.38	1.75	1.95	2.05	mA
		32 MHz	1.25	1.6	1.8	2.0	
		24 MHz	1.20	1.5	1.7	1.9	
		12 MHz	1.10	1.35	1.55	1.75	
		4 MHz	1.02	1.15	1.35	1.55	
	Idle mode with PL0 (PLSEL = 00), all peripherals disable. HCLK is set as MIRC clock.	4 MHz	0.29	0.45	0.65	0.85	
		2 MHz	0.28	0.44	0.64	0.84	
		1 MHz	0.27	0.43	0.63	0.83	
	Idle mode with PL3 (PLSEL = 11), all peripherals disable HCLK is set as LIRC or LXT clock.	38.4 kHz	0.01	0.02	0.06	0.16	
		32.768 kHz	0.01	0.02	0.06	0.16	
	Idle mode with PL0 (PLSEL = 00), all peripherals enable. HCLK is set as HIRC or HXT clock.	48 MHz	6.56	7.35	7.55	7.75	
		32 MHz	4.58	5.15	5.35	5.55	
		24 MHz	3.96	4.5	4.7	4.9	
		12 MHz	2.63	3	3.2	3.4	
		4 MHz	1.74	2	2.2	2.4	
	Idle mode with PL0 (PLSEL = 00), all peripherals enable. HCLK is set as MIRC clock.	4 MHz	0.72	0.9	1.1	1.3	
		2 MHz	0.49	0.7	0.9	1.1	
		1 MHz	0.38	0.6	0.8	1.0	
	Idle mode with PL3 (PLSEL = 11), all peripherals enable HCLK is set as LIRC or LXT clock.	38.4 kHz	0.05	0.06	0.08	0.18	
		32.768 kHz	0.05	0.06	0.08	0.18	

Note:

1. When analog peripheral blocks such as USB, ADC, ACMP, HIRC, MIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current consumption in Idle mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 38.4 kHz	Typ[*2]	Max[*3][*4]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_DPD}	Deep Power-down mode, all peripherals disable	-	-	1.5	3.5	15.5	76	µA
	Deep Power-down mode, RTC enable and run	V	-	1.9	4.2	16.2	78	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	1.6	3.7	26	130	µA
	Power-down mode, RTC enable and run	V	-	2.5	4.9	27	131	
	Power-down mode, WDT/Timer/UART enable and run	-	V	4.4	6.6	28.5	132	
	Power-down mode, WDT/Timer/UART/RTC enable and run, WDT use LIRC, UART/Timer/RTC use LXT	V	V	5.2	7.5	29.5	133	
I_{DD_FWPD}	Fast wake up Power-down mode, all peripherals disable	-	-	102	142	175	295	µA
	Fast wake up Power-down mode, WDT/Timer/UART/RTC enable and run, WDT use LIRC, UART/Timer/RTC use LXT	V	V	105	145	180	300	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L1 gain level
2. V_{DD} = AV_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as USB, ADC and ACMP are ON, an additional power consumption should be considered.

Table 8.3-3 Chip Current Consumption in Power-down mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = V_{BAT} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 48 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA	165	uA
ISP	0	
EXST	175	
CRC	26	
FMCIDLE	194	
GPA	75	
GPB	60	
GPC	63	
GPD	58	
GPE	61	
GPF	57	
WDT	198	
RTC	164	
TMR0	402	
TMR1	399	
TMR2	373	
TMR3	393	
CLKO	200	
ACMP01[*3]	237	
I2C0	129	
SPI0	629	
UART0	679	
UART1	607	
UART2	556	
USBD[*4]	690	
EADC[*2]	449	
TK	194	
SC0	431	

USCI0	191	
LCD[*5]	175	
BPWM0	167	

Notes:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the USB is turned on, add an additional power consumption for the analog part.
5. When the LCD is turned on, add an additional power consumption for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_DPD}[*1][*2]	Wakeup from deep Power-down mode	190	250	µS
t_{WU_NPD}[*1][*2]	Wakeup from normal Power-down mode	19	30	
t_{WU_FWPD}[*1][*2]	Wakeup from fast wake up Power-down mode	12	15	

Notes:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-5 Low-power mode wakeup timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O current injection characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	0.3*V_{DD}	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 1.8 V
V_{IH}	Input high voltage (Schmitt trigger)	0.7*V_{DD}	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 5.5 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		0.8	-	V_{DD}		V_{DD} = 1.8 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[*2]	Input leakage current	-1	-	1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1	-	1		V_{DD} < V_{IN} < 5 V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor	45	50	57	kΩ	VDD=5.5V
R_{PD}[*1]	Pull down resistor	45	50	57	kΩ	VDD=5.5V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O input characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-7	-8.0	-9	μA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-7	-8.0	-9	μA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-7	-7.9	-9	μA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-5	-8	-11	mA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-3.2	-5.2	-7.2	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-2.1	-3.2	-4.2	mA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	13	20	27	mA	V_{DD} = 4.5 V V_{IN}= 0.4 V
		8.5	13	17.5	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		5.0	8	11	mA	V_{DD} = 1.8 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O output characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	$0.3*V_{DD}$	V	
V_{IHR}	Positive going threshold, nRESET	$0.7*V_{DD}$	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	45	52	57	kΩ	
t_{FR}[*1]	nRESET input filtered pulse time	-	24	-	µS	Normal run and Idle mode
		-	35	-		Fast wake up Power-down mode
		-	45	-		Power-down mode
		-	0.1	-		Deep Power-down mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.75	-	5.5	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3 V
		-2[*1]	-	2[*1]	%	T_A = -20 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V
		-2.5[*1]	-	2.5[*1]	%	T_A = -40 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V
I_{HRC}[*1]	Operating current	-	500	800	µA	
T_S[*2]	Stable time	-	14	16	µs	T_A = -40 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) characteristics

8.4.2 4 MHz Internal Median Speed RC Oscillator (MIRC)

The 4 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.75	-	5.5	V	
F_{MRC}	Oscillator frequnecy	3.951	4.032	4.112	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3V
		-10[*1]	-	10[*1]	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.75 ~ 5.5V
I_{MRC}[*1]	Operating current	-	-	30	µA	
T_S[*2]	Stable time	-	-	24	µs	T_A = -40 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-2 4 MHz Internal Median Speed RC Oscillator(MIRC) characteristics

8.4.3 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.75	-	5.5	V	
F_{LRC} [*2]	Oscillator frequnecy	-	38.4	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3V
		-15[*1]	-	15[*1]	%	T_A=-40~105°C V_{DD}=1.75V~5.5V
I_{LRC}	Operating current	-	0.85	1.3	µA	V_{DD} = 3.3 V
T_S	Stable time	-	-	70	µs	T_A = -40 °C ~ 105 °C V_{DD} = 1.75 V ~ 5.5 V

Notes:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 8.4-3 38.4 kHz Internal Low Speed RC Oscillator(LIRC) characteristics

8.4.4 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.75	-	5.5	V	
R_f	Internal feedback resister	-	1	-	MΩ	
f_{HXT}	Oscillator frequency	4	-	32	MHz	
I_{HXT}	Current consumption	-	55	150	µA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	100	250		8 MHz, Gain = L1, C_L = 12.5 pF
		-	165	430		12 MHz, Gain = L2, C_L = 12.5 pF
		-	250	600		16 Mhz, Gain = L3, C_L = 12.5 pF
		-	310	760		24 MHz, Gain = L4, C_L = 12.5 pF
		-	740	1500		32 MHz, Gain = L7, C_L = 12.5 pF
T_S	Stable time	-	2650	2950	µS	4 MHz, Gain = L0, C_L = 12.5 pF
		-	950	1250		8 MHz, Gain = L1, C_L = 12.5 pF
		-	550	850		12 MHz, Gain = L2, C_L = 12.5 pF
		-	400	700		16 Mhz, Gain = L3, C_L = 12.5 pF
		-	300	650		24 MHz, Gain = L4, C_L = 12.5 pF
		-	225	610		32 MHz, Gain = L7, C_L = 12.5 pF
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	-	1.6	-	V	

Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-4 External 4~32 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	120	Ω	Crystal @4 MHz, C_L = 12.5 pF, Gain = L0
		-	-	60		Crystal @8 MHz, C_L = 12.5 pF, Gain = L1
		-	-	25		Crystal @12 MHz, C_L = 12.5 pF, Gain = L2
		-	-	25		Crystal @16 MHz, C_L = 12.5 pF, Gain = L3
		-	-	25		Crystal @24 MHz, C_L = 12.5 pF, Gain = L4
		-	-	25		Crystal @32 MHz, C_L = 12.5 pF, Gain = L7

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

   $S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$

   R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

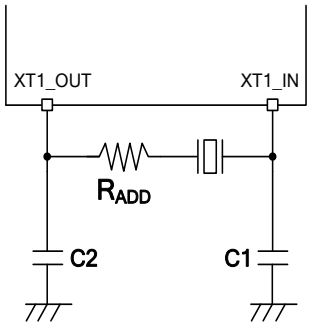


Table 8.4-5 External 4~32 MHz High Speed Crystal Characteristics

8.4.4.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 32 MHz	10 ~ 20 pF	10 ~ 20 pF	without

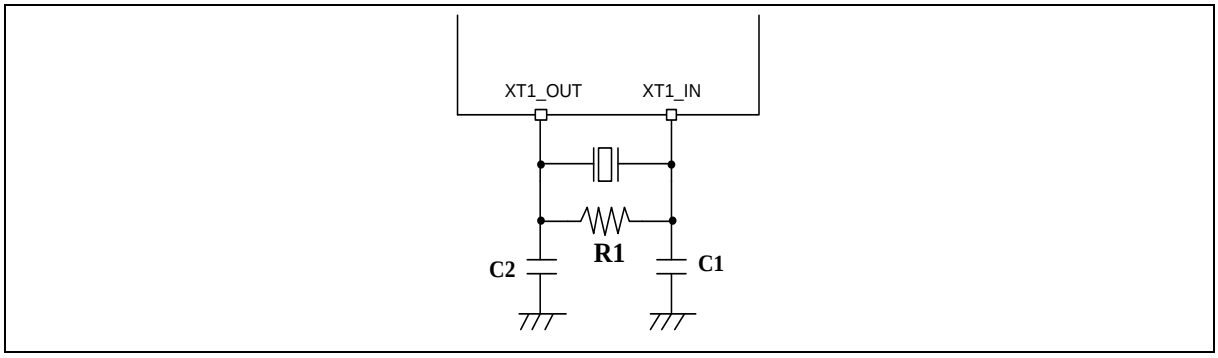
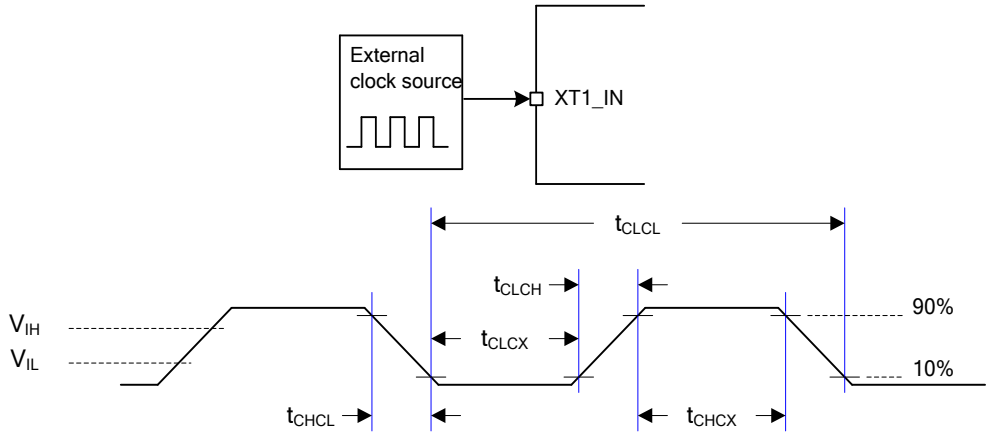


Figure 8.4-1 Typical Crystal Application Circuit

8.4.5 External 4~32 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	32	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 4~32 MHz High Speed Clock Input Signal

8.4.6 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics for M254MD2AE/M254SD2AE/M256xD

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BAT}	Operation voltage	1.75	-	5.5	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	15	-	MΩ	
F_{LXT}	Oscillator frequency	32.768			kHz	
I_{LXT}	Current consumption	-	0.6	2	µA	ESR=35 kΩ, C_L = 12.5 pF, Gain = L1
		-	0.74	2.5		ESR=70 kΩ, C_L = 12.5 pF, Gain = L2
		-	1.0	3.0		ESR=70 kΩ, C_L = 12.5 pF, Gain = L3
Ts_{LXT}	Stable time	-	2	-	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	-	0.4	-	V	

Notes:
1. Guaranteed by characterization, not tested in production.

Table 8.4-7 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-8 External 32.768 kHz Low Speed Crystal Characteristics

8.4.6.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

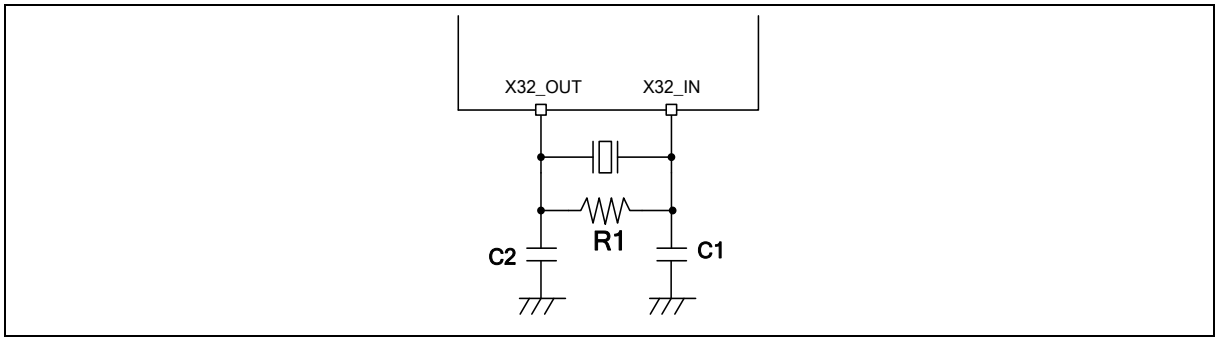


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.7 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics for M254SD3AE/M254xE/M256xE/M258xE/M254xG/M256xG/M258xG

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BAT}	Operation voltage	1.75	-	5.5	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	15	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	0.78	5	µA	ESR=35 kΩ, C_L = 12.5 pF, Gain = L3
		-	0.87	5.3		ESR=35 kΩ, C_L = 12.5 pF, Gain = L4
		-	0.97	5.55		ESR=35 kΩ, C_L = 12.5 pF, Gain = L5
		-	1.49	6.4		ESR=70 kΩ, C_L = 12.5 pF, Gain = L6
		-	1.9	7.5		ESR=70 kΩ, C_L = 12.5 pF, Gain = L7
Ts_{LXT}	Stable time	-	2	-	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	-	0.4	-	V	

Notes:
1. Guaranteed by characterization, not tested in production.

Table 8.4-9 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-10 External 32.768 kHz Low Speed Crystal Characteristics

8.4.7.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

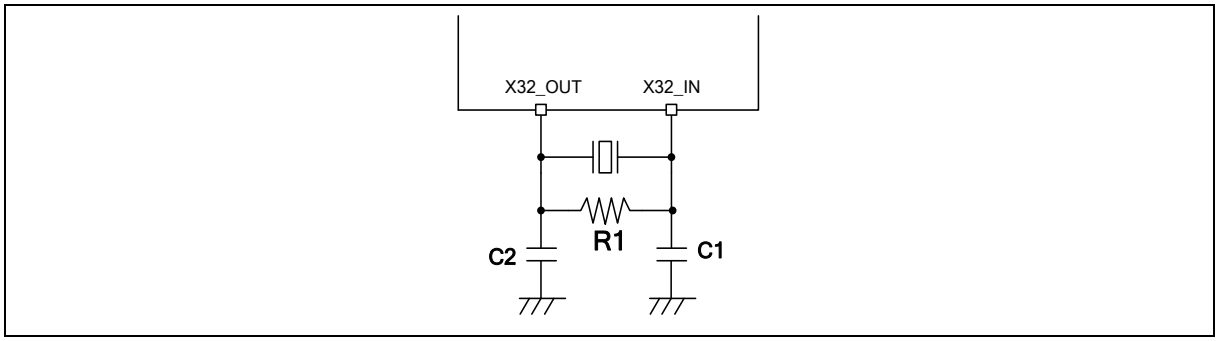
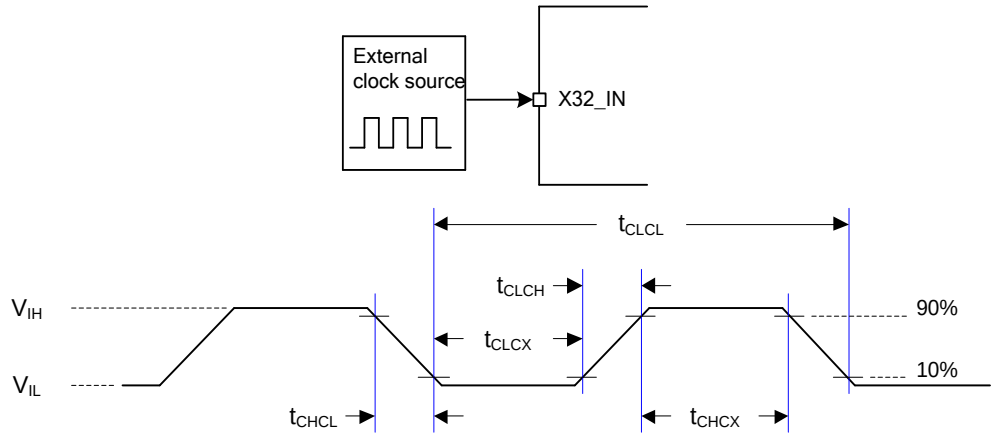


Figure 8.4-3 Typical 32.768 kHz Crystal Application Circuit

8.4.8 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	$V_{BAT} = V_{DD}$
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	$V_{BAT} = V_{DD}$



Notes:

1. Guaranteed by design, not tested in production

Table 8.4-11 External 32.768 kHz Low Speed Clock Input Signal

8.4.9 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	6.5	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		-	4.5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	10		C_L = 30 pF, V_{DD} >= 2.7 V
		-	7		C_L = 10 pF, V_{DD} >= 2.7 V
		-	16.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	11.5		C_L = 10 pF, V_{DD} >= 1.8 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	5		C_L = 30 pF, V_{DD} >= 4.5 V
		-	3.5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	8		C_L = 30 pF, V_{DD} >= 2.7 V
		-	5		C_L = 10 pF, V_{DD} >= 2.7 V
		-	12.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	8		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	-	7.5	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		-	5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	12		C_L = 30 pF, V_{DD} >= 2.7 V
		-	8		C_L = 10 pF, V_{DD} >= 2.7 V
		-	20.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	13.5		C_L = 10 pF, V_{DD} >= 1.8 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	-	6.5	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		-	4.5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	10		C_L = 30 pF, V_{DD} >= 2.7 V
		-	6.5		C_L = 10 pF, V_{DD} >= 2.7 V
		-	18		C_L = 30 pF, V_{DD} >= 1.8 V

		-	10.5		C_L = 10 pF, V_{DD} >= 1.8 V
$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	-	47	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		-	70		C_L = 10 pF, V_{DD} >= 4.5 V
		-	30		C_L = 30 pF, V_{DD} >= 2.7 V
		-	44		C_L = 10 pF, V_{DD} >= 2.7 V
		-	18		C_L = 30 pF, V_{DD} >= 1.8 V
		-	26		C_L = 10 pF, V_{DD} >= 1.8 V
	I/O maximum frequency (High Slew Rate)	-	55	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		-	80		C_L = 10 pF, V_{DD} >= 4.5 V
		-	36		C_L = 30 pF, V_{DD} >= 2.7 V
		-	56		C_L = 10 pF, V_{DD} >= 2.7 V
		-	21		C_L = 30 pF, V_{DD} >= 1.8 V
		-	35		C_L = 10 pF, V_{DD} >= 1.8 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-12 I/O AC characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	1.75	-	5.5	V	
V_{LDO}	Output voltage	-	1.5	-	V	
T_A	Temperature	-40	-	105	℃	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO_CAP pin and the closest VSS pin of the device.
3. V_{LDO} is only used to supply internal power.

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	70	100	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	-	0.3	3		AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	40	80		AV_{DD} = 5.5V, Normal mode
		-	3	6		AV_{DD} = 5.5V, Low Power mode
V_{POR}	POR reset voltage	1.40	1.5	1.65	V	
V_{LVR}	LVR reset voltage	1.55	1.6	1.7		
V_{BOD}	BOD brown-out detect voltage (Falling edge)	1.70	1.80	1.90		BODVL = 1
		1.90	2.00	2.10		BODVL = 2
		2.30	2.40	2.50		BODVL = 3
		2.60	2.70	2.80		BODVL = 4
		2.90	3.00	3.10		BODVL = 5
		3.60	3.70	3.80		BODVL = 6
		4.25	4.40	4.50		BODVL = 7
	BOD brown-out detect voltage (Rising edge)	1.76	1.88	2.00		BODVL = 1
		1.96	2.08	2.20		BODVL = 2
		2.36	2.48	2.60		BODVL = 3
		2.66	2.78	2.90		BODVL = 4
		2.96	3.08	3.20		BODVL = 5
		3.66	3.78	3.90		BODVL = 6
		4.31	4.48	4.60		BODVL = 7
T_{LVR_SU}[*1]	LVR startup time	-	200	2000	μS	-

T_{LVR_RE}[*1]	LVR respond time	-	20	100		-
T_{BOD_SU}[*1]	BOD startup time	-	1000	-		-
T_{BOD_RE}[*1]	BOD respond time	-	500	-		Normal mode BODDGSEL = 3
		-	10000	-		Low Power mode
R_{VDDR}[*1]	VDD rise time rate	10		-	µS/V	POR Enabled
R_{VDDF}[*1]	VDD fall time rate	10		-		POR Enabled
		-	1000	-		LVR Enabled
		-	333	-		BOD 1.8V Enabled, Normal mode
		-	200	-		BOD 2.0V Enabled, Normal mode
		-	111	-		BOD 2.4V Enabled, Normal mode
		-	83	-		BOD 2.7V Enabled, Normal mode
		-	66	-		BOD 3.0V Enabled, Normal mode
		-	45	-		BOD 3.7V Enabled, Normal mode
		-	35	-		BOD 4.4V Enabled, Normal mode
		-	50000	-		BOD 1.8V Enabled, Low Power mode
		-	30000	-		BOD 2.0V Enabled, Low Power mode
		-	16667	-		BOD 2.4V Enabled, Low Power mode
		-	12500	-		BOD 2.7V Enabled, Low Power mode
		-	10000	-		BOD 3.0V Enabled, Low Power mode
		-	6818	-		BOD 3.7V Enabled, Low Power mode
		-	5172	-		BOD 4.4V Enabled, Low Power mode

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and power control unit

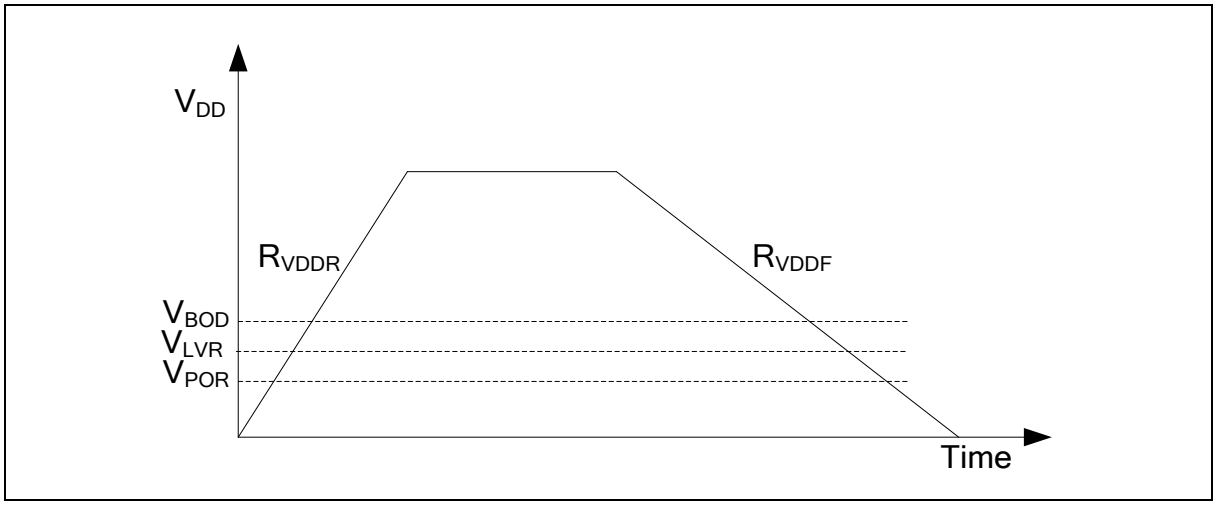


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog To Digital Converter (ADC)

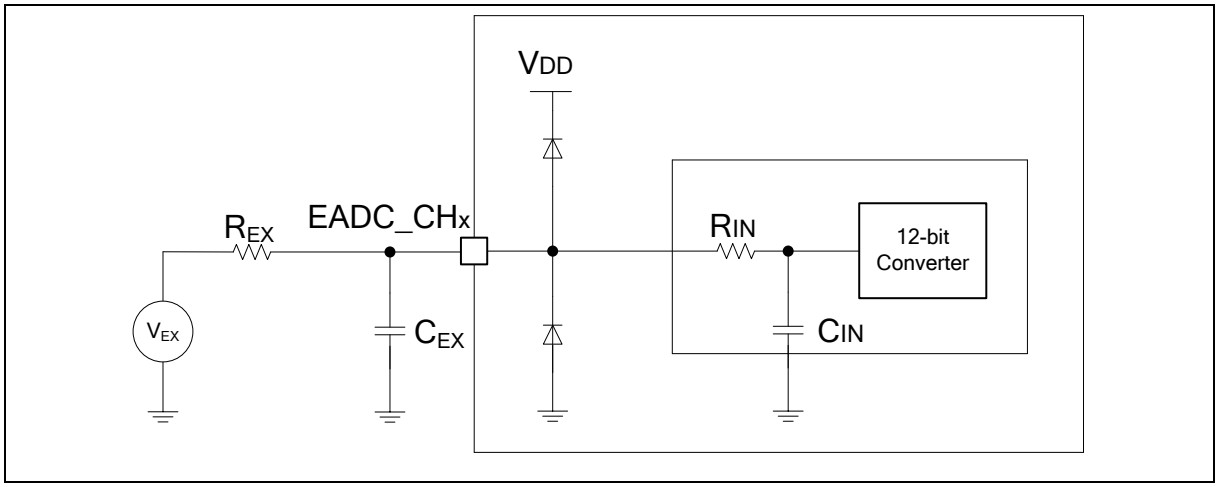
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	1.75	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.75	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	1000	-	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 16 MHz $T_{CONV} = 22 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	16	MHz	
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	22	-	277	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 21 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	30	-	730	kSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}	Enable to ready time	32	-	-	$1/F_{ADC}$	
INL[*1]	Integral Non-Linearity Error	-3	-	+3	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
DNL[*1]	Differential Non-Linearity Error	-1	-	+3	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
E_G[*1]	Gain error	-6	-	+7	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
E_O[*1]$_T$	Offset error	-3	-	+3	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
E_A[*1]	Absolute Error	-1.5	-	+8	LSB	$V_{REF} = AV_{DD}$, except TSSOP20 and TSSOP28
ENOB[*1]	Effective number of bits	10	-	-	bits	F_{ADC} = 16 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 10 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	64	-	dB	
SNR[*1]	Signal-to-noise ratio	-	64	-		
THD[*1]	Total harmonic distortion	-	-65	-		
C_{IN}[*1]	Internal Capacitance	-	26	30	pF	
R_{IN}[*1]	Internal Switch Resistance	-	0.5	-	kΩ	
R_{EX}[*1]	External input impedance	-	-	33	kΩ	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

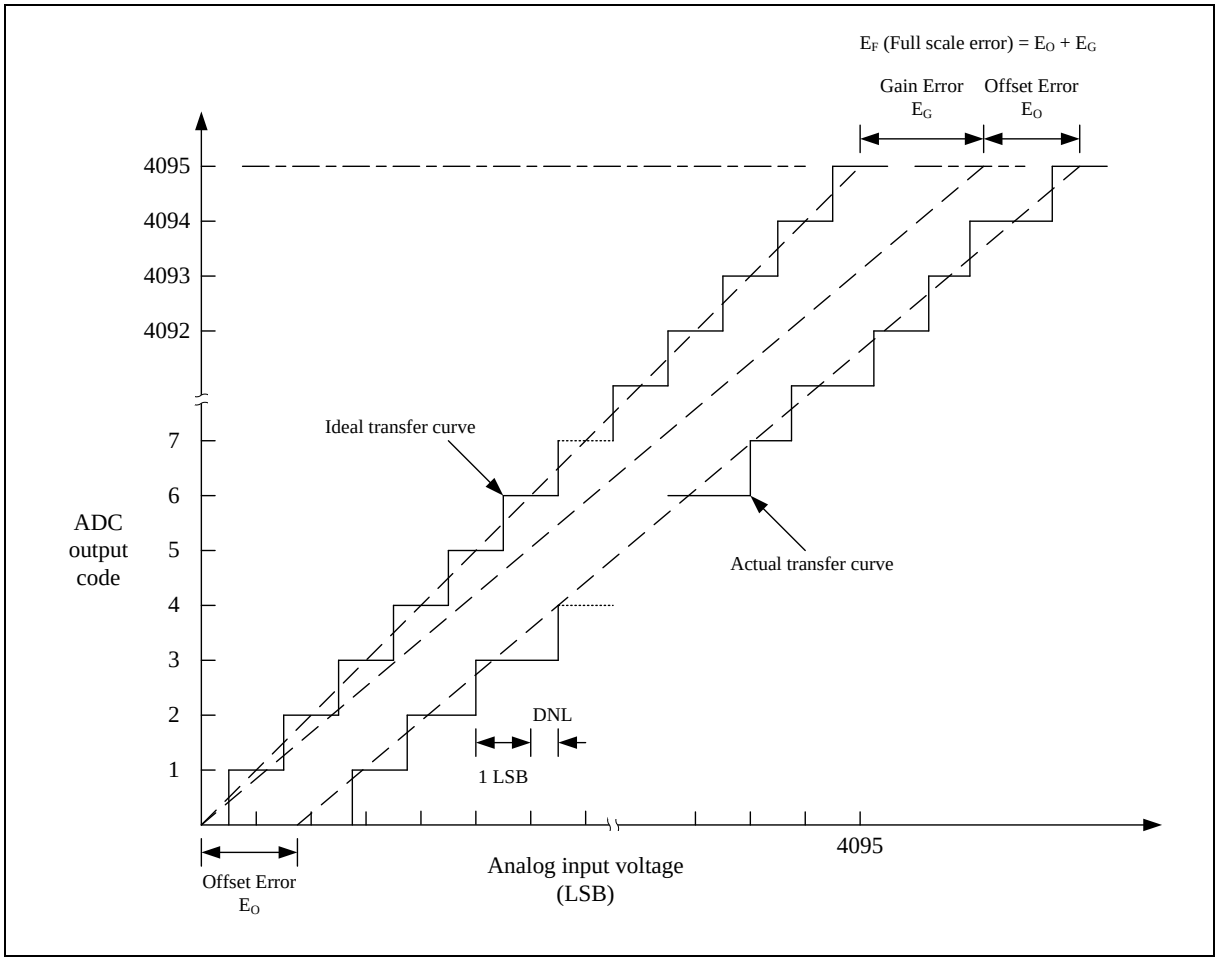
Notes:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	1.75	-	5.5	V	V_{DD} = AV_{DD}
T_A	Temperature	-40	-	105	℃	
I_{ACMP}[*2]	ACMP operating current	-	43	90	μA	MODESEL = 11
		-	12	30		MODESEL = 10
		-	4	10		MODESEL = 01
		-	1	6		MODESEL = 00
V_{CM}[*2]	Input common mode voltage range	0.1	1/2 AV_{DD}	AV_{DD} -0.1		
V_{offset}[*2]	Input offset voltage	-	±10	±20	mV	Hysteresis disable (HYSSEL = 00)
V_{hys}[*2]	Hysteresis window	-	10	20	mV	HYSSEL = 01
		-	20	40		HYSSEL = 10
		-	30	60		HYSSEL = 11
A_v[*1]	DC voltage Gain	43	70	-	dB	
T_d[*2]	Propagation delay	-	150	250	nS	MODESEL = 11
		-	300	600		MODESEL = 10
		-	650	2000		MODESEL = 01
		-	1300	4500		MODESEL = 00
T_{Setup}[*2]	Setup time	-	250 + T_d	450 + T_d	μS	
A_{CRV}[*2]	CRV output voltage	-5	-	5	%	AVDD x (1/6+CRVCTL/24)
R_{CRV}[*2]	Unit resistor value	-	4.2	-	kΩ	
T_{SETUP_CRV}[*1]	Setup time	280	350	440	nS	CRV output voltage settle to ±1%
I_{DD_CRV}[*2]	Operating current	-	107	120	μA	

Notes:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-2 ACMP characteristics

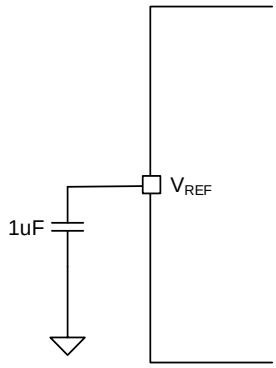
8.5.5 Internal Voltage Reference

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{REF_INT}	Internal reference voltage	1.49	1.536	1.59	V	AV_{DD} >= 2.0 V
		1.98	2.048	2.11		AV_{DD} >= 2.4 V
		2.48	2.560	2.64		AV_{DD} >= 2.9 V
		2.97	3.072	3.17		AV_{DD} >= 3.4 V
		3.97	4.096	4.22		AV_{DD} >= 4.5 V
T_S[*1]	Stable time	-	0.5	0.8	mS	C_L =4.7 uF, V_{REF} initial=0, Preload is enabled.
		-	9.3	13	mS	C_L =4.7 uF, V_{REF} initial=5.5, Preload is enabled.
		-	24	180	uS	C_L =1 uF, V_{REF} initial=0, Preload is enabled.
		-	2	2.6	mS	C_L =1 uF, V_{REF} initial=5.5, Preload is enabled.
I_{VREF_INT}[*1]	V_{REF_INT} operating current	-	50	70	uA	
I_{VREF_LOAD}[*1]	V_{REF_INT} output loading current	-	-	1	mA	

Note:

1. Guaranteed by characterization, not tested in production



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical connection with internal voltage reference

8.5.6 Temperature Sensor

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{TEMP_OS}[*1]	Temperature sensor offset voltage	690	720	750	mV	T_A = 0°C
T_C[*1]	Temperature Coefficient	-1.74	-1.83	-1.9	mV/°C	
I_{TEMP}[*1]	Temperature sensor operating current	-	16	30	μA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

8.5.7 LCD controller

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Supply voltage	1.75	-	5.5	V	
T_A	Temperature	-20	-	85	℃	
V_{LCD}[*2]	LCD external voltage	2.6	-	5.5	V	
	LCD internal voltage	2.9	3.06	3.1		VSEL = 0, V_{DD} > 1.75 V
		3.1	3.27	3.3		VSEL = 1, V_{DD} > 1.8 V
		3.3	3.47	3.5		VSEL = 2, V_{DD} > 1.9V
		3.5	3.64	3.7		VSEL = 3, V_{DD} > 2.1 V
		3.7	3.84	3.9		VSEL = 4, V_{DD} > 2.2 V
		3.9	4.05	4.1		VSEL = 5, V_{DD} > 2.3 V
		4.1	4.25	4.3		VSEL = 6, V_{DD} > 2.4 V
		4.3	4.46	4.5		VSEL = 7, V_{DD} > 2.5 V
		4.5	4.66	4.7		VSEL = 8, V_{DD} > 2.6 V
		4.7	4.83	4.9		VSEL = 9, V_{DD} > 2.7 V
		4.9	5.03	5.1		VSEL = 10, V_{DD} > 2.8 V
		5.1	5.24	5.3		VSEL = 11, V_{DD} > 2.9 V
$V_{3/4}$	COM/SEG 3/4 V_{LCD} (1/4 Bias)	-	3/4 V_{LCD}	-	V	
$V_{2/4}$	COM/SEG 2/4 V_{LCD} (1/4 Bias)	-	2/4 V_{LCD}	-	V	
$V_{1/4}$	COM/SEG 2/4 V_{LCD} (1/4 Bias)	-	1/4 V_{LCD}	-	V	
$V_{2/3}$	COM/SEG 2/3 V_{LCD} (1/3 Bias)	-	2/3 V_{LCD}	-	V	
$V_{1/3}$	COM/SEG 1/3 V_{LCD} (1/3 Bias)	-	1/3 V_{LCD}	-	V	
C_{LCD}	V_{LCD} external capacitance	1	-	10	μF	
I_{LCD}[*3]	Supply current from V_{DD} with built-in charge pump and buffer mode	-	77.36	-	μA	V_{LCD} = 3.2V, V_{DD} = 1.8V
		-	89.01	-		V_{LCD} = 3.2V, V_{DD} = 3.6V
		-	77.77	-		V_{LCD} = 3.2V, V_{DD} = 5.5V
		-	102.85	-		V_{LCD} = 5.2V, V_{DD} = 2.9V
		-	86.14	-		V_{LCD} = 5.2V, V_{DD} = 5.5V
I_{VLCD}[*3]	Supply current from V_{LCD} without Bulit-In Charge Pump	-	9.15	-	μA	V_{LCD} = 3.2V, buffer mode
		-	14.05	-		V_{LCD} = 5.2V, buffer mode
		-	4.78	-		V_{LCD} = 3.2V, low drive mode
		-	8.57	-		V_{LCD} = 5.2V, low drive mode
		-	19.83	-		V_{LCD} = 3.2V, high drive mode
		-	32.71	-		V_{LCD} = 5.2V, high drive mode
R_{LCD_INT}	Internal total LCD resistor value	-	5500	-	MΩ	Low drive

		-	240	-	kΩ	High drive

Note:

1. Guaranteed by design, not tested in production
2. $V_{LCD} < 1.8 * V_{DD}$
3. LCD COM/SEG is set to 1/8 duty, 1/4 bias, 64 Hz frame rate, all pixels active, type B waveform, no LCD panel loading.

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	24	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	24		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	16		1.8 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	7	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	11	nS	2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	18.5	nS	1.8 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-1 SPI Master Mode Characteristics

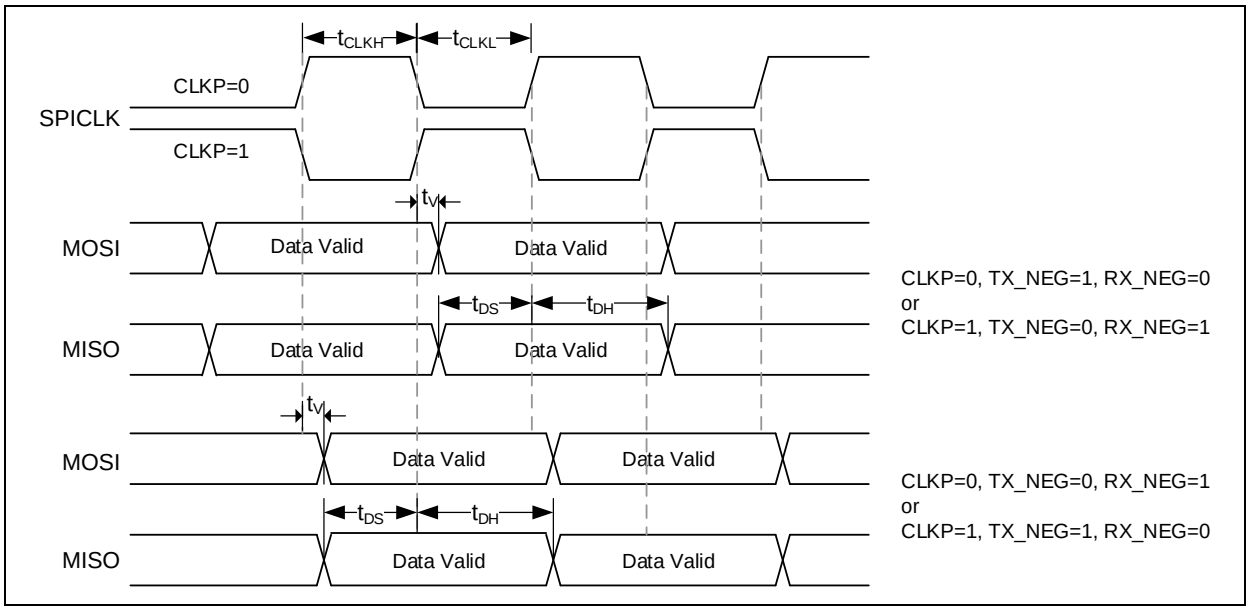


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	11.2	MHz	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	8.8		2.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	4.6		1.8 V ≤ VDD ≤ 5.5 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 2.5ns	-	-		2.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ VDD ≤ 5.5 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	1.5	-	-	nS	
t_{DH}	Data input hold time	3.5	-	-	nS	
t_V	Data output valid time	-	-	35	nS	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	42		2.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	74		1.8 V ≤ VDD ≤ 5.5 V, CL = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-2 SPI Slave Mode Characteristics

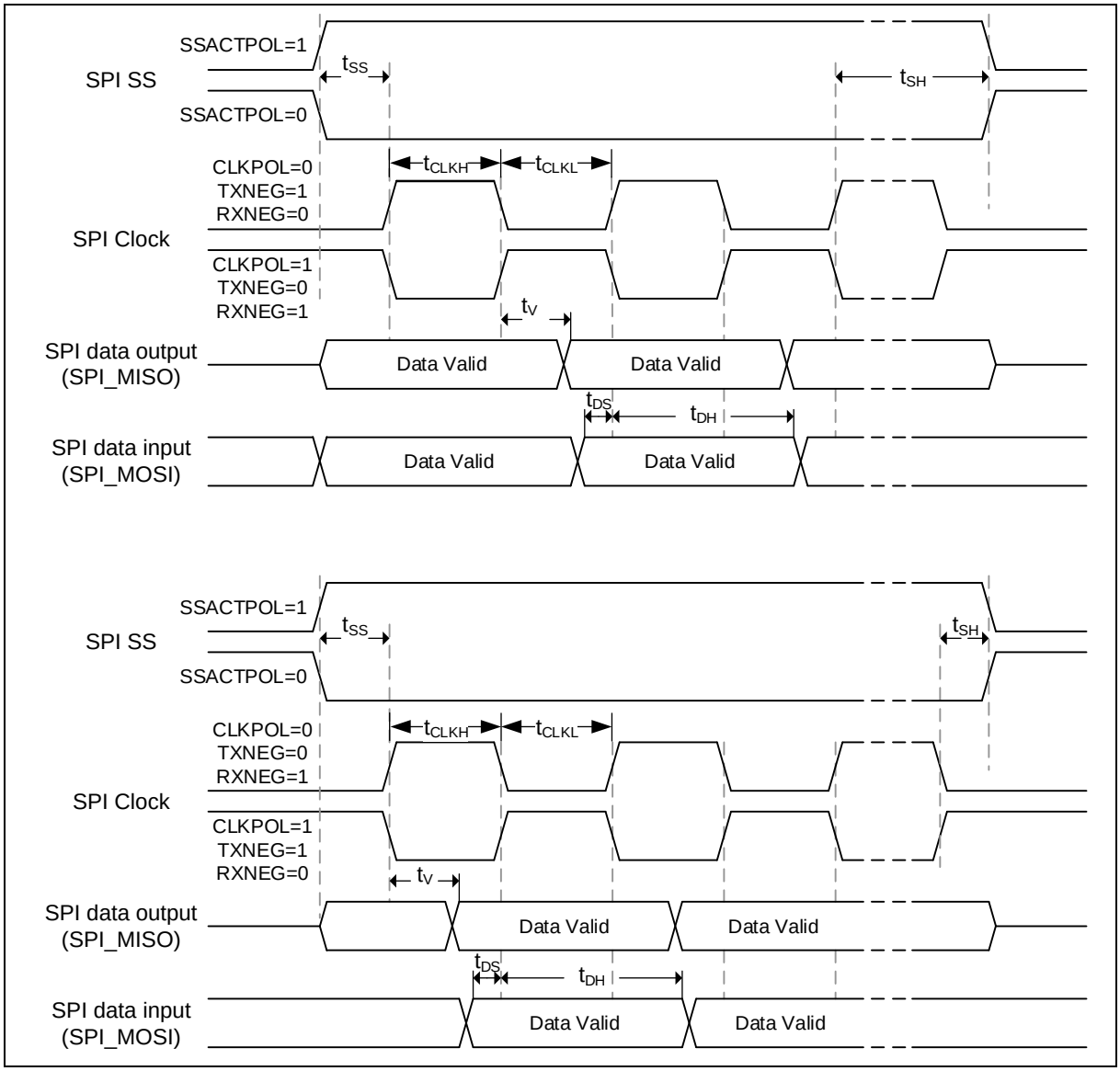


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [*1]	Max [*1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	80	-	nS	Master f_{PCLK} = 48 MHz, data: 24 bits, audio frequency = 128 kHz
$t_{w(CKL)}$	I²S clock low time	80	-		
$t_{v(WS)}$	WS valid time	2	6		Master mode
$t_{h(WS)}$	WS hold time	2	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	nS	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	25		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-3 I2S Characteristics

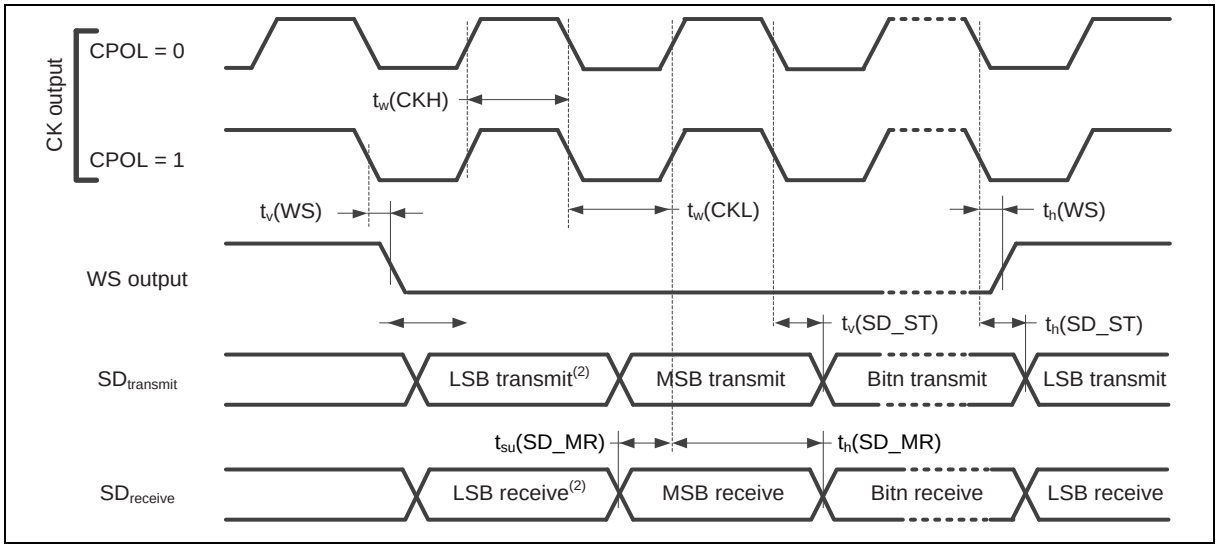


Figure 8.6-3 I2S Master Mode Timing Diagram

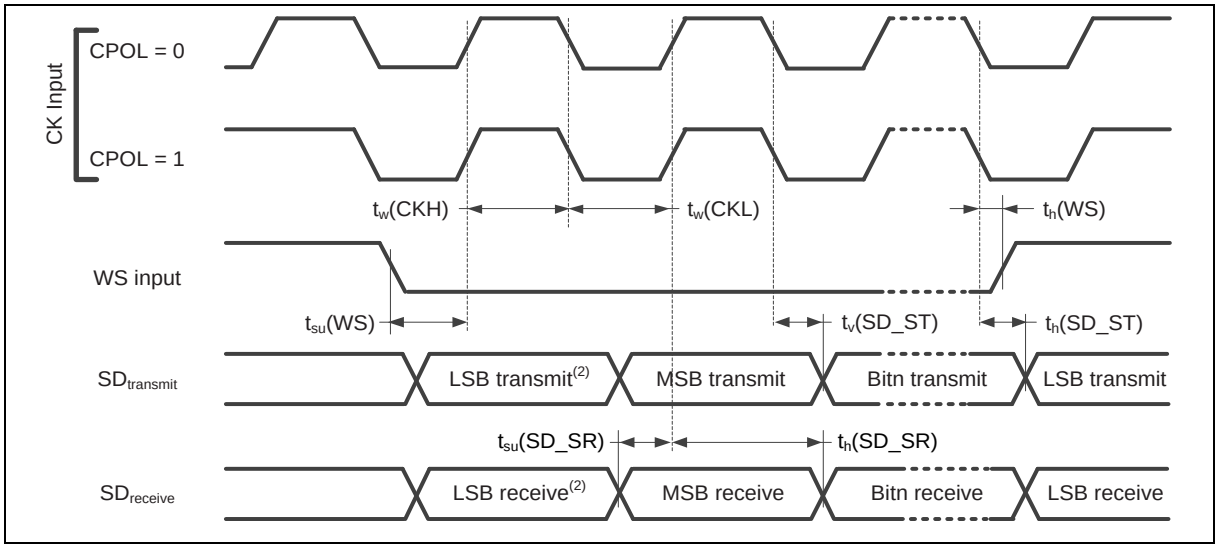


Figure 8.6-4 I²S Slave Mode Timing Diagram

8.6.3 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 I²C characteristics

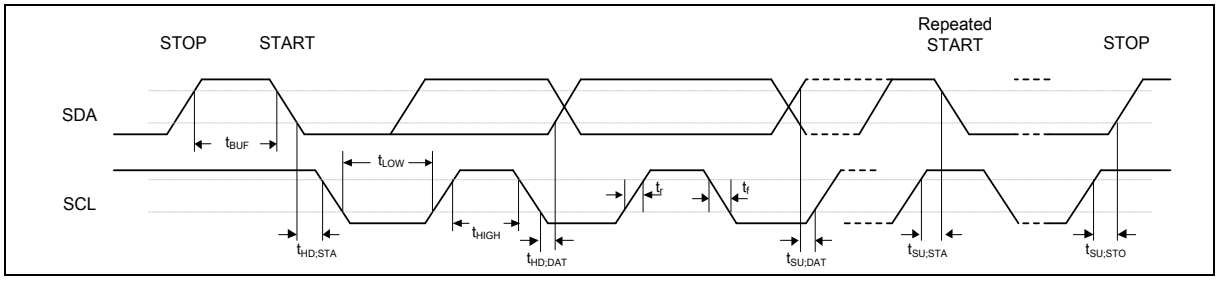


Figure 8.6-5 I²C Timing Diagram

8.6.4 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [*1]	Typ	Max[*1]	Unit	Test Conditions
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	24	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	24		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	16		1.8 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	7	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	11	nS	2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	18.5	nS	1.8 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-5 USCI-SPI Master Mode Characteristics

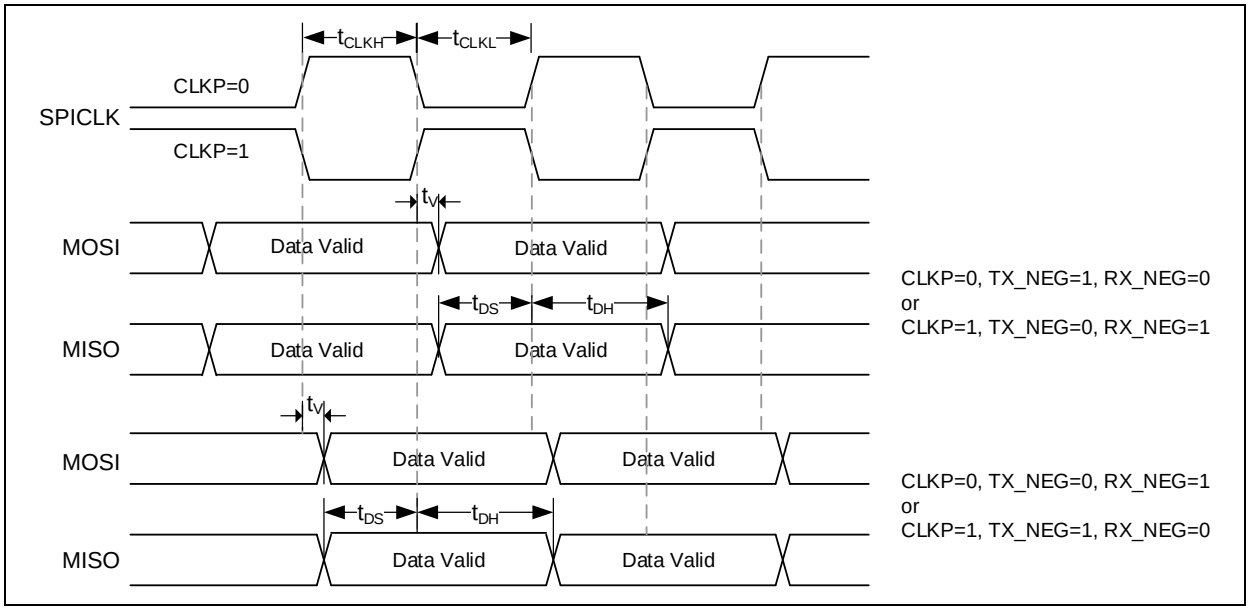


Figure 8.6-6 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	6.3	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	5.6		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	4.2		1.8 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		1 T_{SPICLK} + 2.5ns	-	-		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	79	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	88		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	117		1.8 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-6 USCI-SPI Slave Mode Characteristics

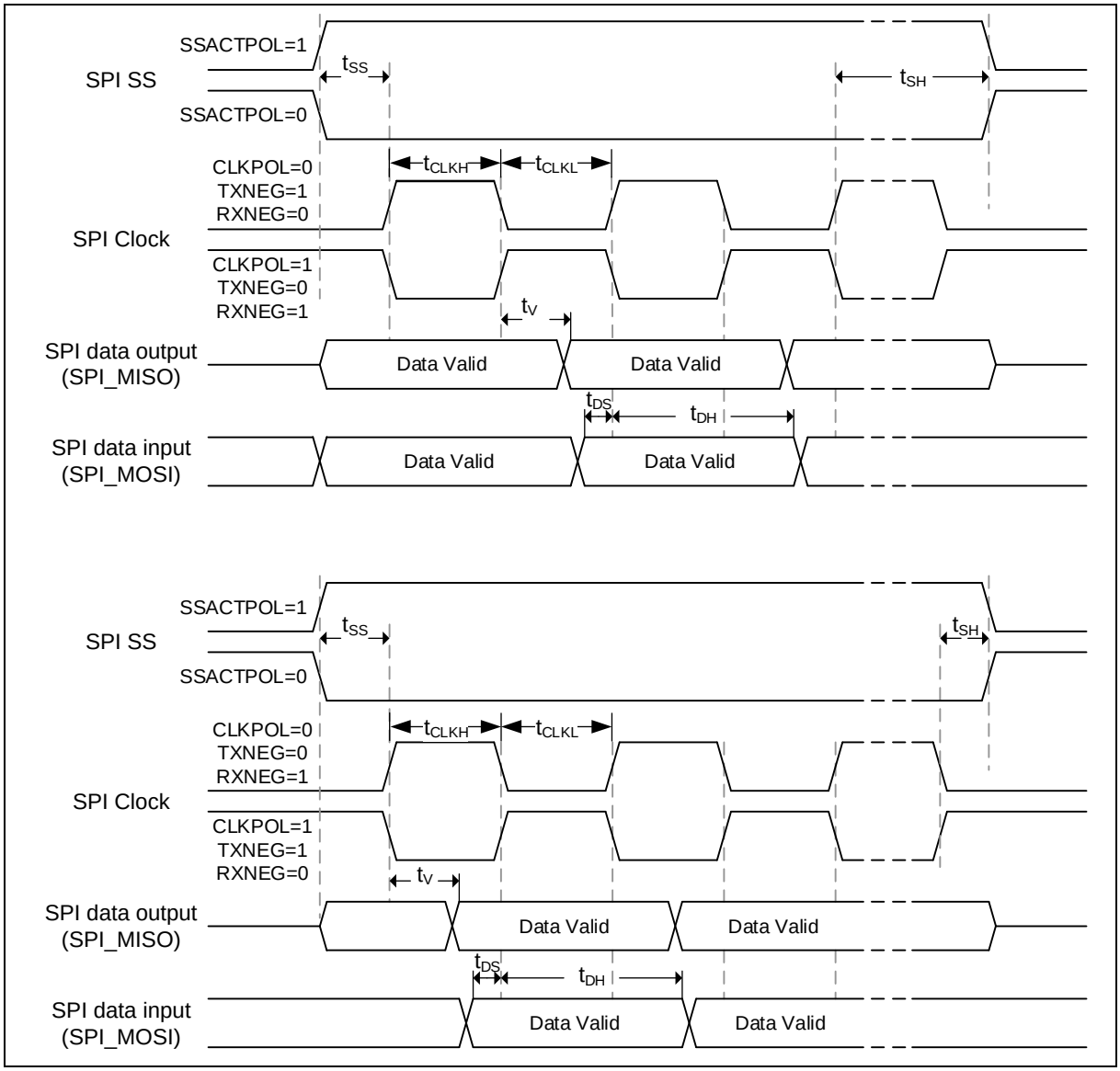


Figure 8.6-7 USCI-SPI Slave Mode Timing Diagram

8.6.5 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-7 USCI-I²C characteristics

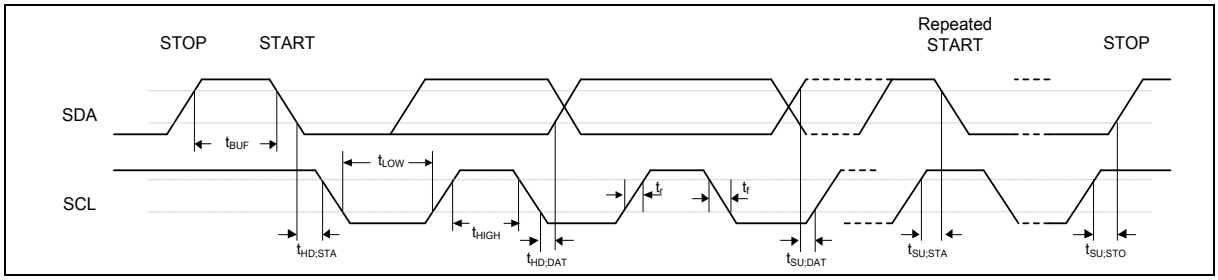


Figure 8.6-8 USCI-I²C Timing Diagram

8.6.6 USB Characteristics

8.6.6.1 USB Full-Speed Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BUS}	USB full speed transceiver operating voltage	4.4	-	5.25	V	
V_{DD33}[*2]	USB Internal power regulator output	3.0	3.3	3.6	V	
V_{IH}	Input high (driven)	2.0	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	0.2	-	-	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2.0	V	-
	Receiver hysteresis	-	200	-	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
V_{CRS}	Output signal cross voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up resistor	1.19	-	1.9	kΩ	-
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3.0	-	3.6	V	
Z_{DRV}[*3]	Driver output resistance	-	10	-	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	26	pF	Pin to GND

Notes:

1. Guaranteed by characterization result, not tested in production.
2. To ensure stability, an external 1 μF output capacitor, 1uF external capacitor must be connected between the USB_VDD33_CAP pin and the closest GND pin of the device.
3. USB_D+ and USB_D- must be connected with external series resistors to fit USB Full-speed spec request (28 ~ 44Ω).

Table 8.6-8 USB Full-Speed Characteristics

8.6.6.2 USB Full-Speed PHY characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	nS	C_L=50 pF
T_{FF}	fall time	4	-	20	nS	C_L=50 pF
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-9 USB Full-Speed PHY Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

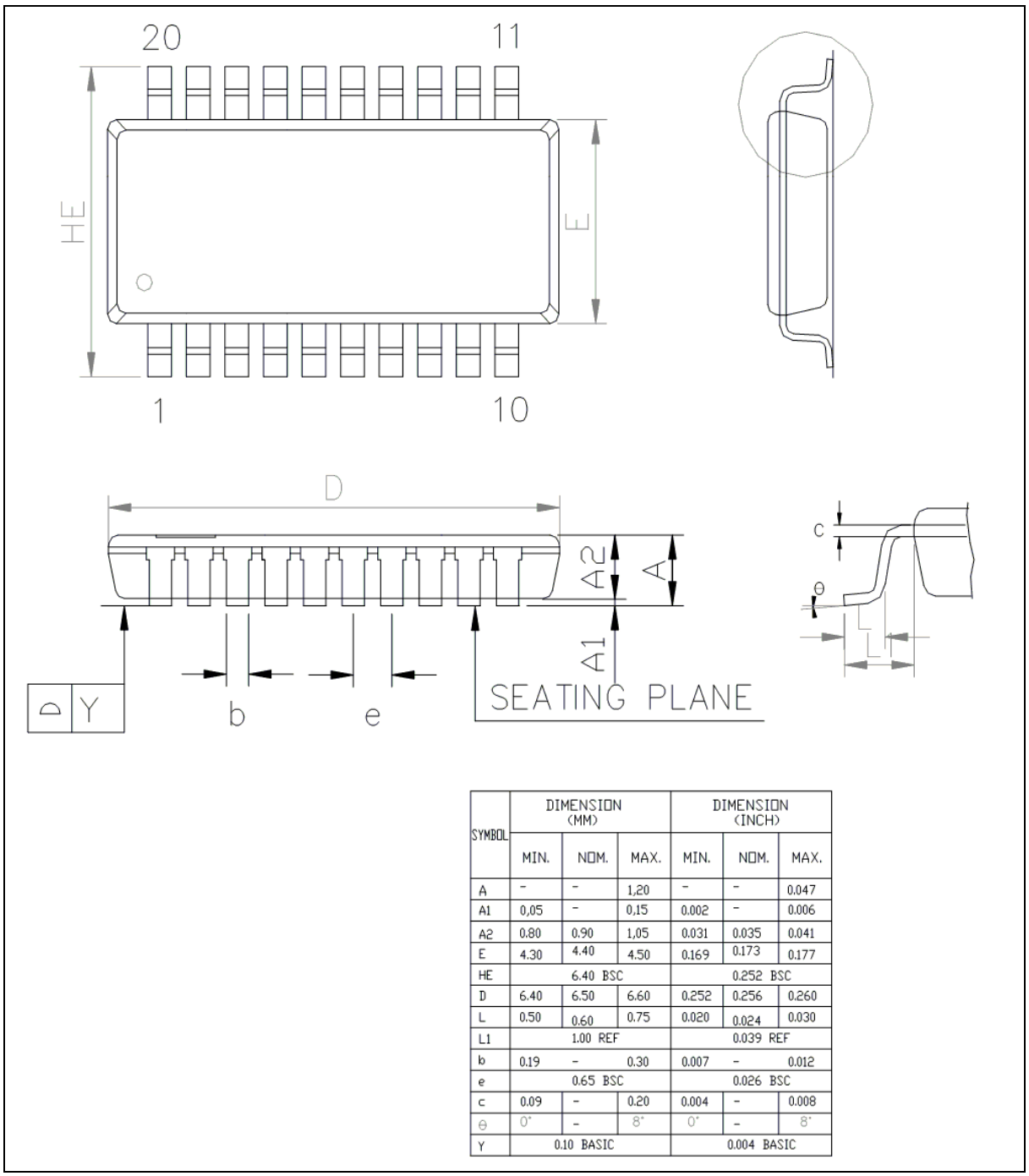
Symbol	Parameter	Min[2]	Typ	Max	Unit	Test Condition
T_{ERASE}	Page erase time	-	20	-	mS	T_A = 25℃
T_{PROG}	Program time	-	60	-	μS	
I_{DD1}	Read current	-	7	-	mA	
I_{DD2}	Program current	-	8	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Cycling Endurance	100,000	-	-	cycles[1]	T_A = 25℃
T_{RET}	Data retention	10	-	-	year	20 kcycle[1], T_J = 85℃
		100	-	-	year	20 kcycle[1], T_J = 25℃

Notes:

1. Number of program/erase cycles. The flash data can only be programmed once at the same address after flash erase.
2. Guaranteed by design.
3. The Erase/program command are only supported at power level 0

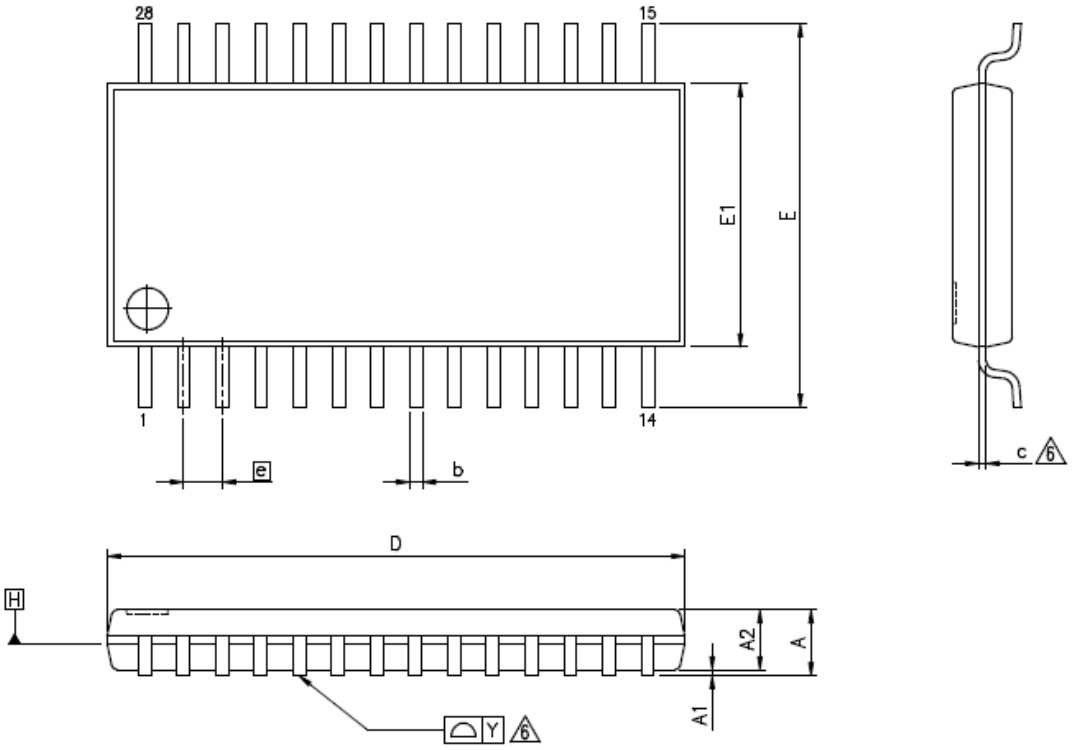
9 PACKAGE DIMENSIONS

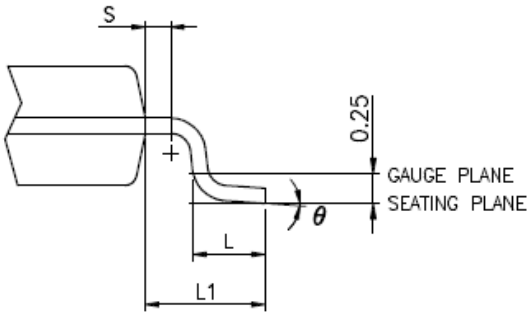
9.1 TSSOP20 (4.4x6.5x0.9 mm³)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1,20	-	-	0.047
A1	0,05	-	0,15	0.002	-	0.006
A2	0.80	0.90	1,05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

9.2 TSSOP28 (4.4x9.7x1.0 mm³)

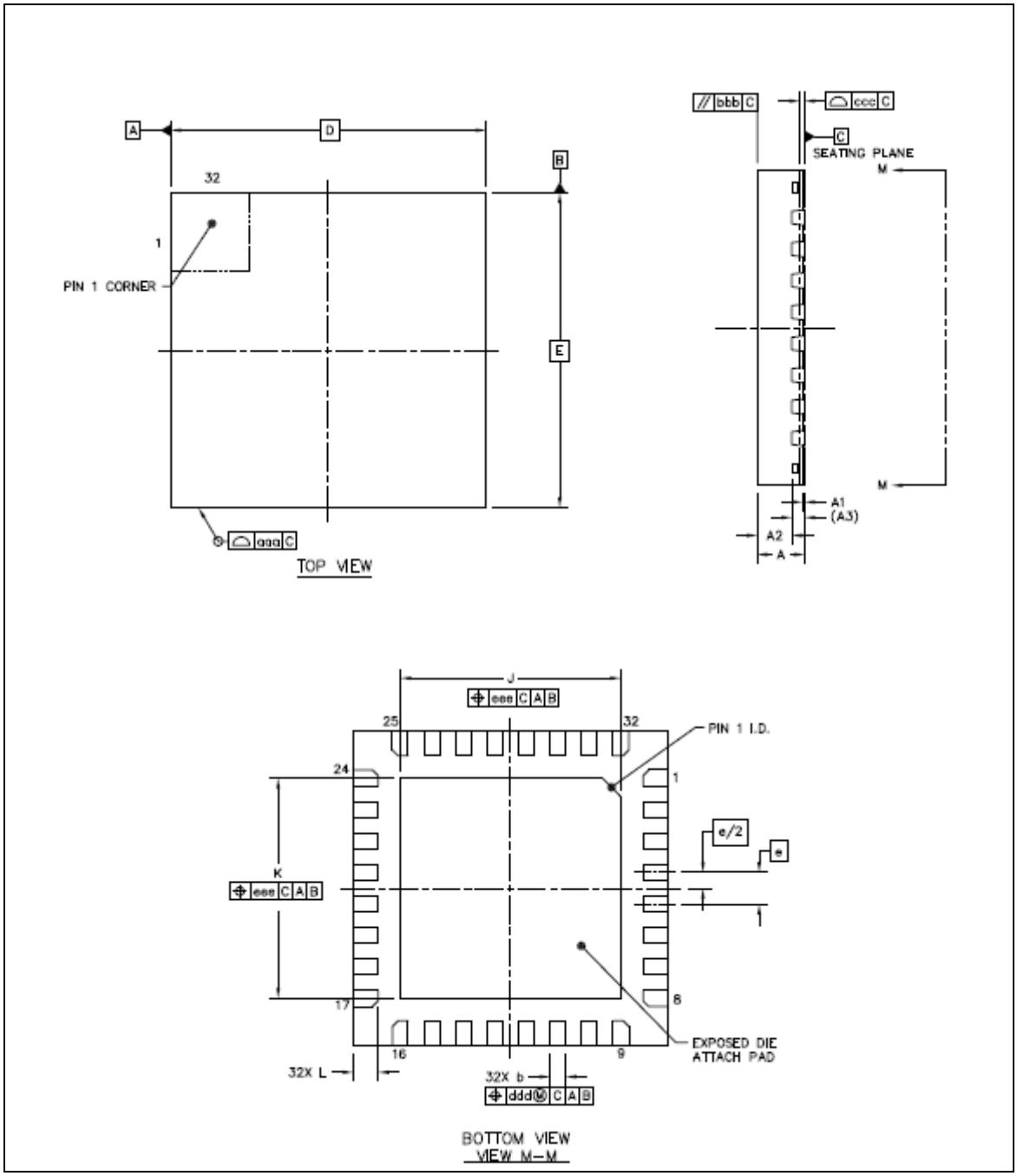




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

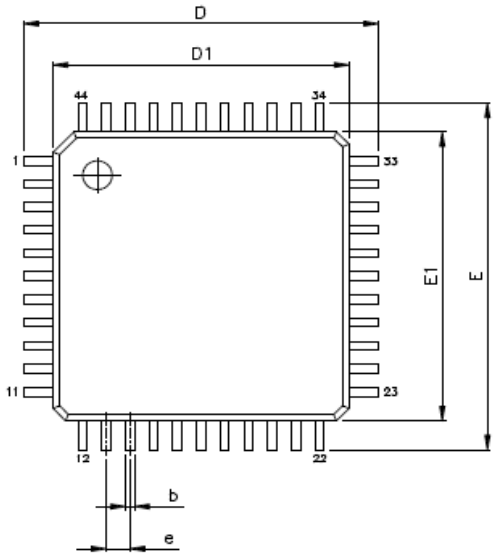
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

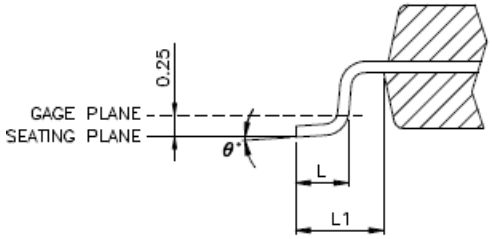
9.3 QFN 33L (5x5x0.8 mm³)

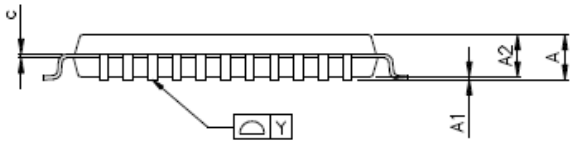


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

9.4 LQFP 44L (10x10x1.4 mm³ Footprint 2.0 mm)



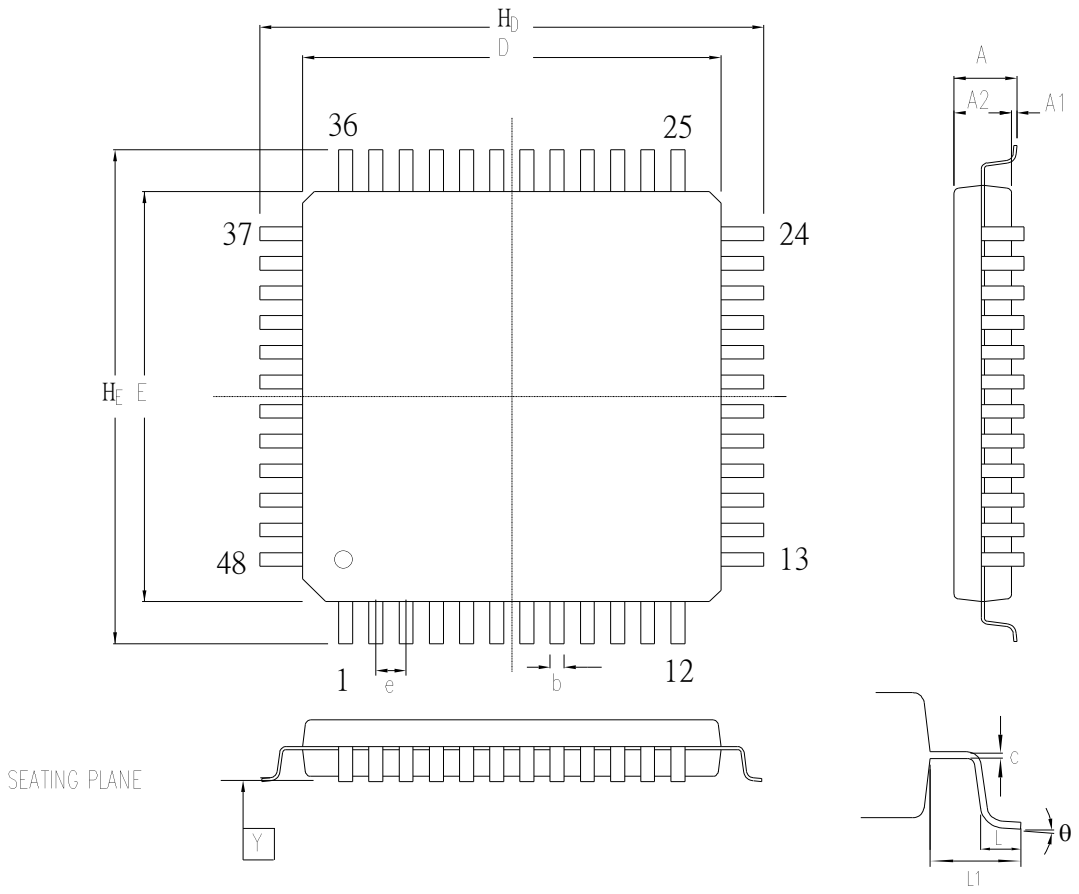




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	–	0.20
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
Y	0.10		

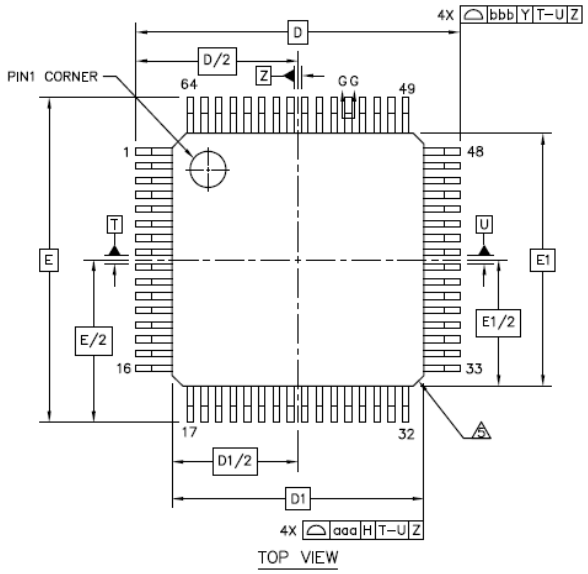
9.5 LQFP 48L (7x7x1.4 mm³ Footprint 2.0 mm)



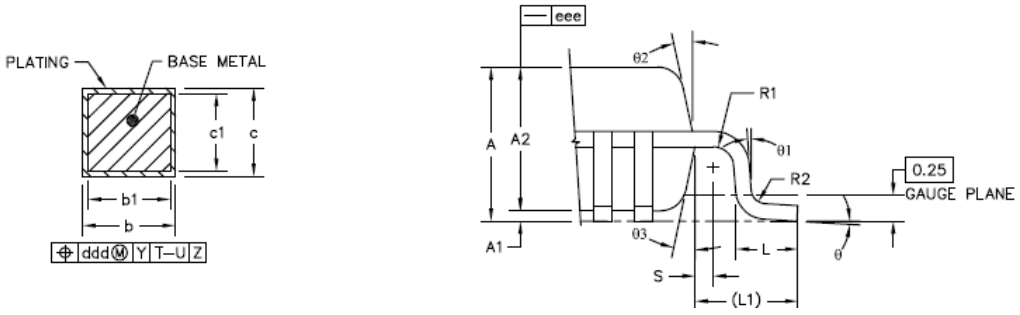
Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

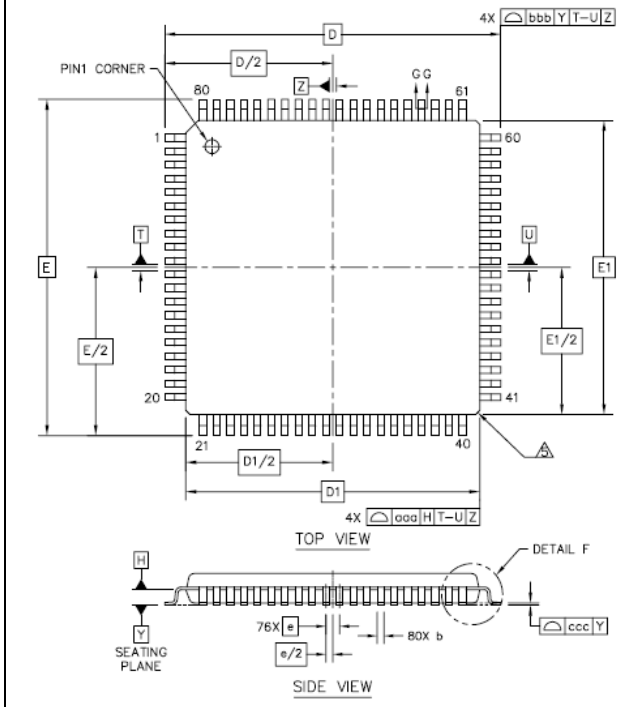
9.6 LQFP 64L (7x7x1.4 mm^3 Footprint 2.0 mm)



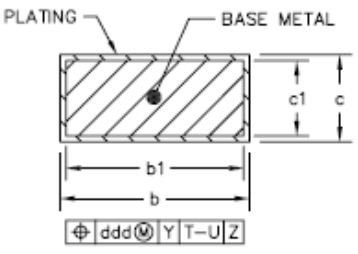
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

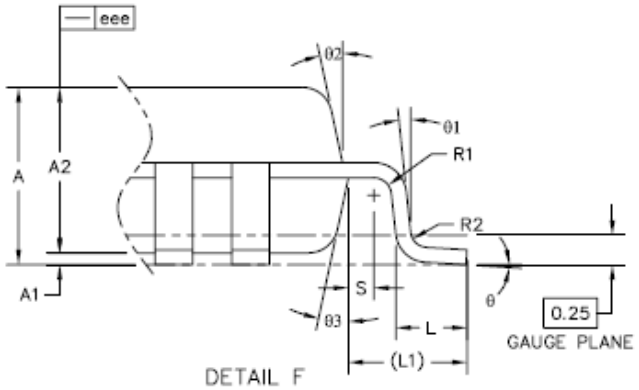


9.7 LQFP 80L (14x14x1.4 mm³ Footprint 2.0 mm)

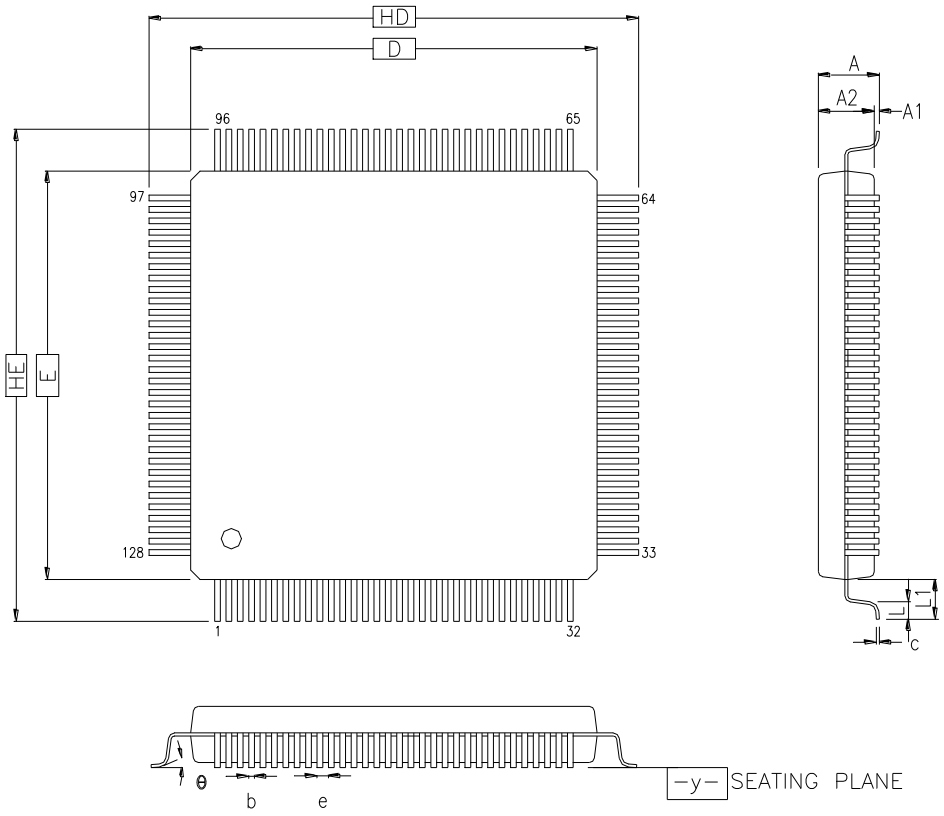


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.22	0.3	0.38
LEAD WIDTH		b1	0.22	---	0.34
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	16 BSC		
	Y	E	16 BSC		
	X	D1	14 BSC		
	Y	E1	14 BSC		
LEAD PITCH		e	0.65 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.1		
LEAD OFFSET		ddd	0.13		
MOLD FLATNESS		eee	0.05		





9.8 LQFP 128L (14x14x1.4 mm^3 Footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
HD		16.00 BSC.			0.630 BSC.	
D		14.00 BSC.			0.551 BSC.	
HE		16.00 BSC.			0.630 BSC.	
E		14.00 BSC.			0.551 BSC.	
b	0.13	0.16	0.23	0.005	0.006	0.009
e		0.40 BSC.			0.016 BSC.	
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 REF			0.039 REF	
y	–	–	0.1	–	–	0.004

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2021.07.30	1.00	Initial version.
2021.11.12	1.01	Added a new M254SD3AE part number in Chapter 3 and 4.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.