

Bridgetek Pte Ltd

FT81x

(Advanced Embedded Video Engine)



The FT81x is a series of easy to use graphic controllers targeted at embedded applications to generate high-quality Human Machine Interfaces (HMIs). It has the following features:

- Advanced Embedded Video Engine(EVE) with high resolution graphics and video playback
- FT81x functionality includes graphic control, audio control, and touch control interface.
- Pinout backward compatible with FT800 (FT810) and FT801 (FT811).
- Support multiple widgets for simplified design implementation
- Built-in graphics operations allow users with little expertise to create high-quality displays
- Support 4-wire resistive touch screen (FT810/FT812)
- Support capacitive touch screen with up to 5 touches detection (FT811/FT813)
- Hardware engine can recognize touch tags and track touch movement. Provides notification for up to 255 touch tags.
- Enhanced sketch processing
- Programmable interrupt controller provides interrupts to host MCU
- Built-in 12MHz crystal oscillator with PLL providing programmable system clock up to 60MHz
- Clock switch command for internal or external clock source. External 12MHz crystal or clock input can be used for higher accuracy.
- Video RGB parallel output; configurable to support PCLK up to 60MHz and R/G/B output of 1 to 8 bits
- Programmable timing to adjust HSYNC and VSYNC timing, enabling interface to numerous displays
- Support for LCD display with resolution up to SVGA (800x600) and formats with data enable (DE) mode or VSYNC/HSYNC mode
- Support landscape and portrait orientations
- Display enable control output to LCD panel
- Integrated 1MByte graphics RAM, no frame buffer RAM required
- Support playback of motion-JPEG encoded AVI videos
- Mono audio channel output with PWM output
- Built-in sound synthesizer
- Audio wave playback for mono 8-bit linear PCM, 4-bit ADPCM and μ -Law coding format at sampling frequencies from 8 kHz to 48 kHz. Built-in digital filter reduces the system design complexity of external filtering
- PWM output for display backlight dimming control
- Advanced object oriented architecture enables low cost MPU/MCU as system host using SPI interfaces
- Support SPI data lines in single, dual or quad mode; SPI clock up to 30MHz
- Power mode control allows the chip to be put in power down, sleep and standby states
- Supports I/O voltage from 1.8V to 3.3V
- Internal voltage regulator supplies 1.2V to the digital core
- Build-in Power-on-reset circuit
- -40°C to 85°C extended operating temperature range
- Available in a compact Pb-free, VQFN-48 and VQFN-56 package, RoHS compliant

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1 Typical Applications

- Point of Sales Machines
- Multi-function Printers
- Instrumentation
- Home Security Systems
- Graphic touch pad – remote, dial pad
- Tele / Video Conference Systems
- Phones and Switchboards
- Medical Appliances
- Blood Pressure displays
- Heart monitors
- Glucose level displays
- Breathalyzers
- Gas chromatographs
- Power meter
- Home appliance devices
- Set-top box
- Thermostats
- Sprinkler system displays
- Medical Appliances
- GPS / Satnav
- Vending Machine Control Panels
- Elevator Controls
-and many more

1.1 Part Numbers

| Part Number | Description | Package |
|-------------|---------------------------------------|---|
| FT810Q-x | EVE with 18 bit RGB, resistive touch | 48 Pin VQFN, body 7 x 7 mm, pitch 0.5mm |
| FT811Q-x | EVE with 18 bit RGB, capacitive touch | 48 Pin VQFN, body 7 x 7 mm, pitch 0.5mm |
| FT812Q-x | EVE with 24 bit RGB, resistive touch | 56 Pin VQFN, body 8 x 8 mm, pitch 0.5mm |
| FT813Q-x | EVE with 24 bit RGB, capacitive touch | 56 Pin VQFN, body 8 x 8 mm, pitch 0.5mm |

Table 1- FT81x Embedded Video Engine Part Numbers

Note: Packaging codes for x is:

-R: Taped and Reel (3000pcs per reel)

-T: Tray packing (260 pcs per tray for VQFN-48, 348 pcs per tray for VQFN-56)

For example: FT810Q-R is 3000 VQFN pieces in taped and reel packaging

2 Block Diagram

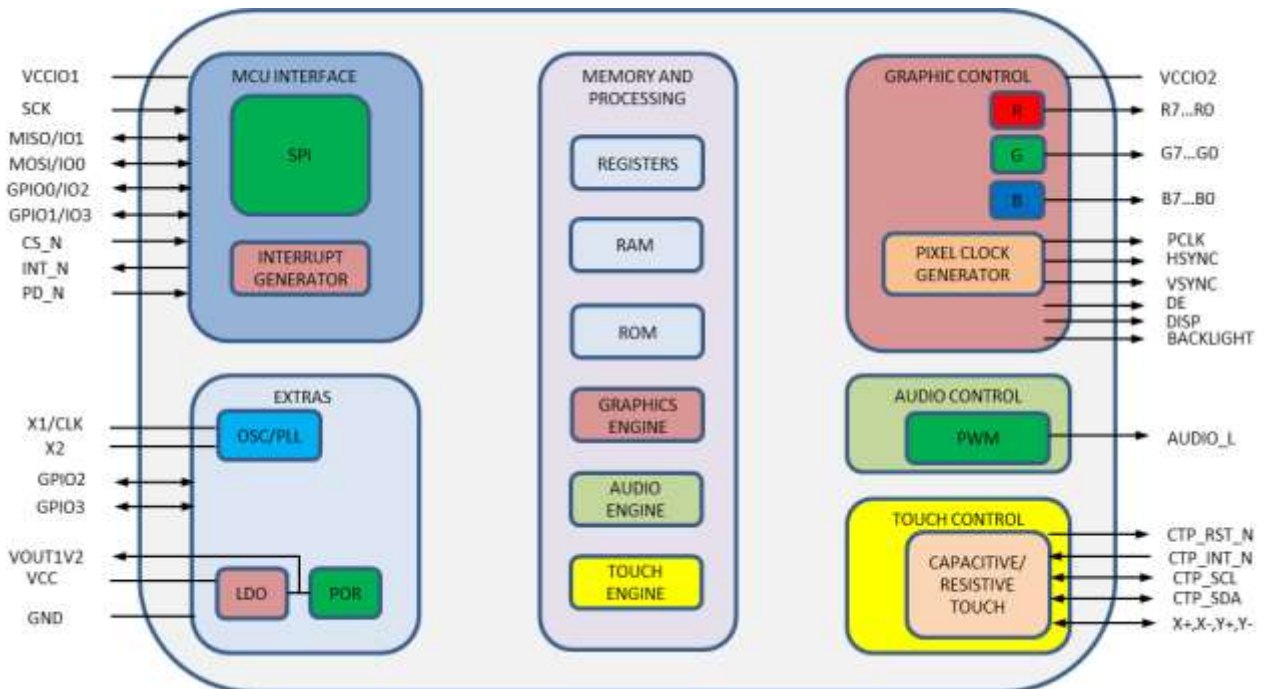


Figure 2-1 FT81x Block Diagram

For a description of each function please refer to Section 4.

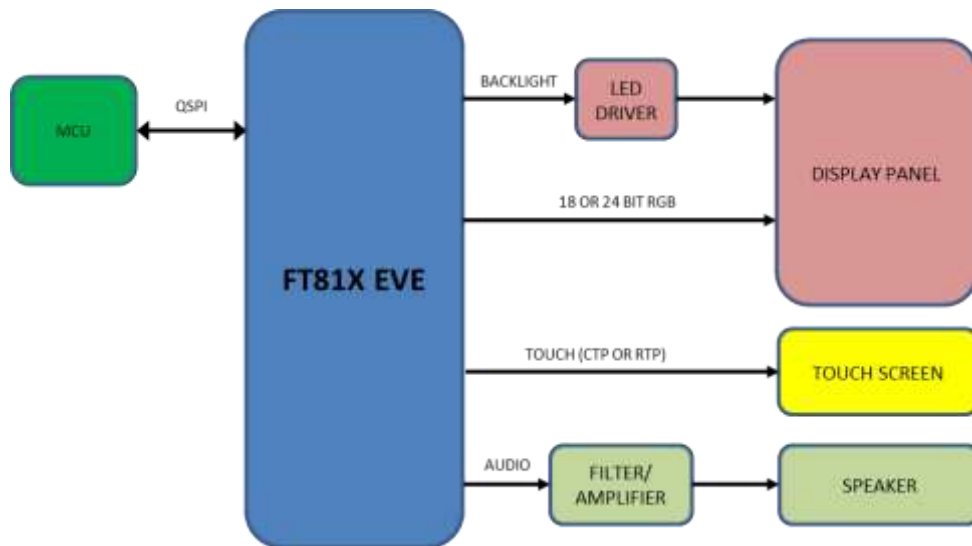


Figure 2-2 FT81x System Design Diagram

FT81x with EVE (Embedded Video Engine) technology simplifies the system architecture for advanced human machine interfaces (HMIs) by providing support for display, audio, and touch as well as an object oriented architecture approach that extends from display creation to the rendering of the graphics.

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3 Device Pin Out and Signal Description

3.1 FT810 VQFN-48 Package Pin Out

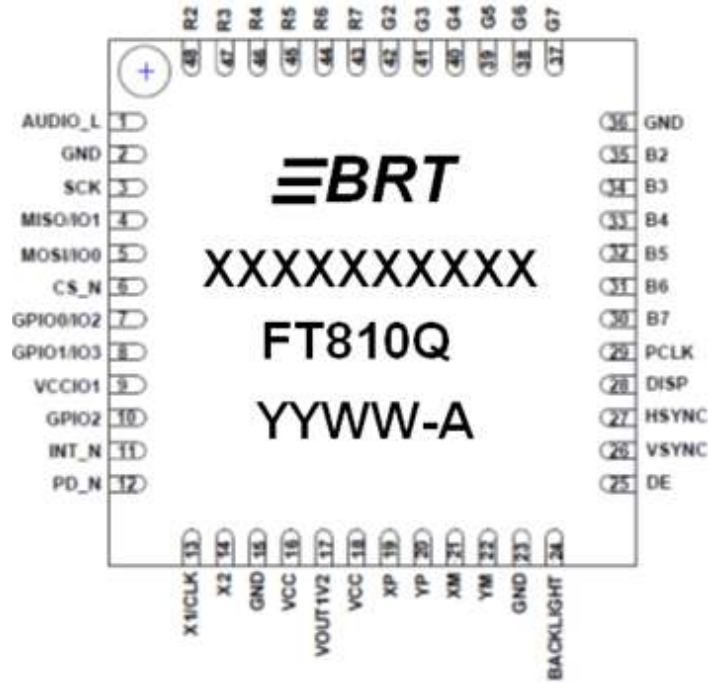


Figure 3-1 Pin Configuration FT810 VQFN-48 (top view)

3.2 FT811 VQFN-48 Package Pin Out

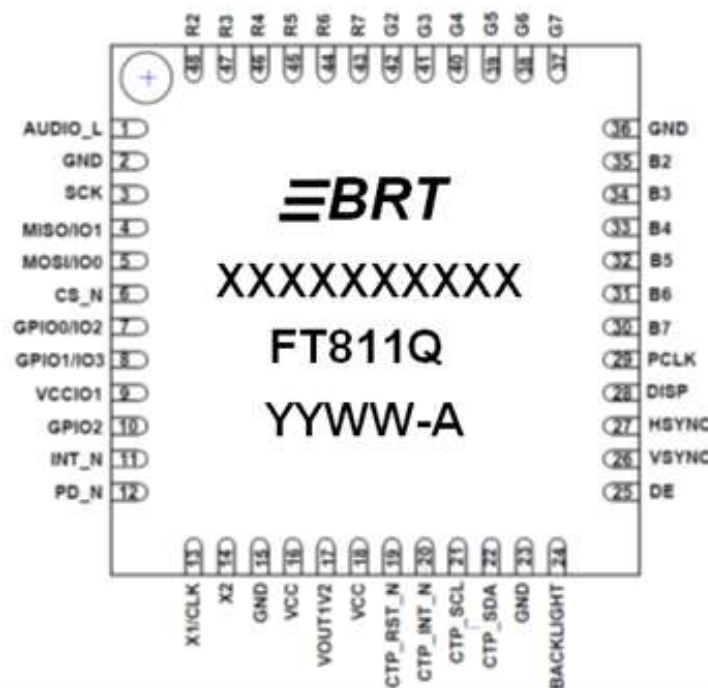


Figure 3-1 Pin Configuration FT811 VQFN-48 (top view)

3.3 FT812 VQFN-56 Package Pin Out

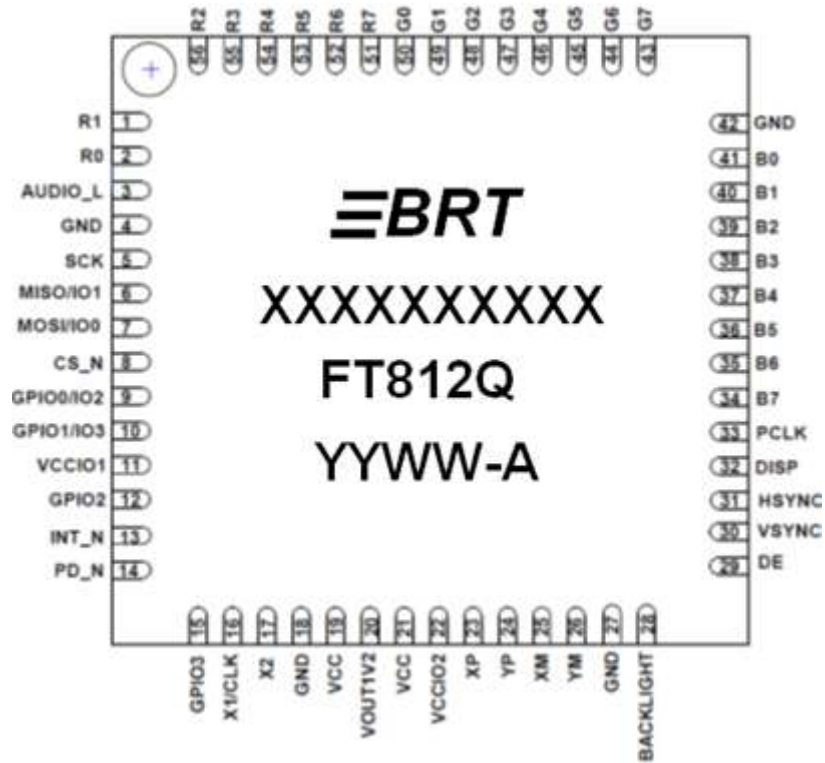


Figure 3-1 Pin Configuration FT812 VQFN-56 (top view)

3.4 FT813 VQFN-56 Package Pin Out

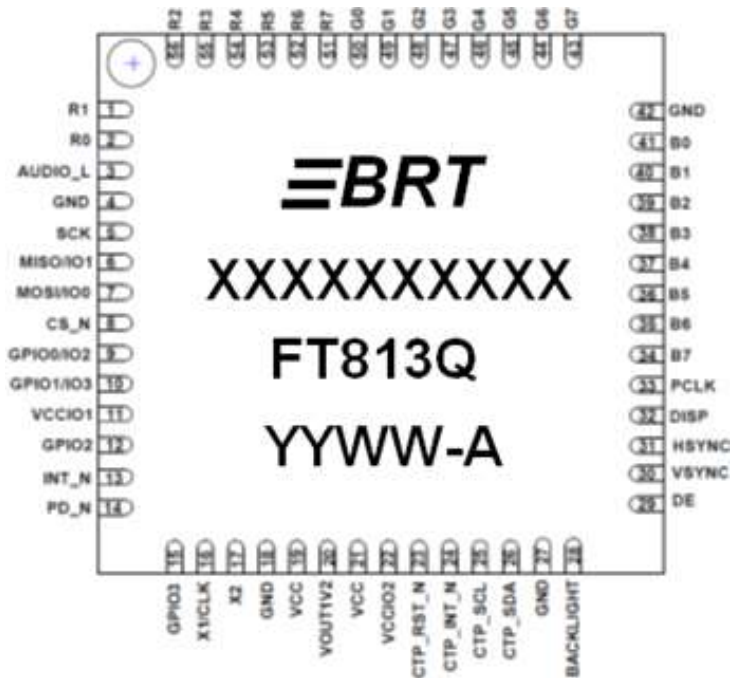


Figure 3-1 Pin Configuration FT813 VQFN-56 (top view)

3.5 Pin Description

| Pin Number | | | | Pin Name | Type | Description |
|------------|-------|-------|-------|-----------|------|---|
| FT810 | FT811 | FT812 | FT813 | | | |
| - | - | 1 | 1 | R1 | O | Bit 1 of Red RGB signals Powered from pin VCCIO2 |
| - | - | 2 | 2 | R0 | O | Bit 0 of Red RGB signals Powered from pin VCCIO2 |
| 1 | 1 | 3 | 3 | AUDIO_L | O | Audio PWM out Powered from pin VCC |
| 2 | 2 | 4 | 4 | GND | P | Ground |
| 3 | 3 | 5 | 5 | SCK | I | SPI clock input Powered from pin VCCIO1 |
| 4 | 4 | 6 | 6 | MISO/IO1 | I/O | SPI Single mode: SPI MISO output SPI Dual/Quad mode: SPI data line 1 Powered from pin VCCIO1 |
| 5 | 5 | 7 | 7 | MOSI/IO0 | I/O | SPI Single mode: SPI MOSI input SPI Dual/Quad mode: SPI data line 0 Powered from pin VCCIO1 |
| 6 | 6 | 8 | 8 | CS_N | I | SPI slave select input Powered from pin VCCIO1 |
| 7 | 7 | 9 | 9 | GPIO0/IO2 | I/O | SPI Single/Dual mode: General purpose IO 0 SPI Quad mode: SPI data line 2 Powered from pin VCCIO1 |
| 8 | 8 | 10 | 10 | GPIO1/IO3 | I/O | SPI Single/Dual mode: General purpose IO 1 SPI Quad mode: SPI data line 3 Powered from pin VCCIO1 |
| 9 | 9 | 11 | 11 | VCCIO1 | P | I/O power supply for host interface pins. Support 1.8V, 2.5V or 3.3V. |
| 10 | 10 | 12 | 12 | GPIO2 | I/O | General purpose IO 2 Powered from pin VCCIO1 |
| 11 | 11 | 13 | 13 | INT_N | OD/O | Interrupt to host, open drain output(default) or push-pull output, active low |
| 12 | 12 | 14 | 14 | PD_N | I | Chip power down mode control input, active low. Connect to MCU GPIO for power management or hardware reset function, or pulled up to VCCIO1 through 47kΩ resistor and 100nF to ground. Powered from pin VCCIO1 |
| - | - | 15 | 15 | GPIO3 | I/O | General purpose IO 3 Powered from pin VCCIO1 |
| 13 | 13 | 16 | 16 | X1/CLK | I | Crystal oscillator or clock input; Connect to GND if not used. 3.3V peak input allowed. |

| Pin Number | | | | Pin Name | Type | Description |
|------------|-------|-------|-------|-----------|------|---|
| FT810 | FT811 | FT812 | FT813 | | | |
| | | | | | | Powered from pin VCC. |
| 14 | 14 | 17 | 17 | X2 | O | Crystal oscillator output; leave open if not used. Powered from pin VCC. |
| 15 | 15 | 18 | 18 | GND | p | Ground |
| 16 | 16 | 19 | 19 | VCC | P | 3.3V power supply input. |
| 17 | 17 | 20 | 20 | VOOUT1V2 | O | 1.2V regulator output pin. Connect a 4.7uF decoupling capacitor to GND. |
| 18 | 18 | 21 | 21 | VCC | p | 3.3V power supply input. |
| | | 22 | 22 | VCCIO2 | P | I/O power supply for RGB and touch pins. For QFN-48 package, VCCIO2 is bonded together with VCC pin; For QFN-56 package, VCCIO2 is separate from VCC pin. VCCIO2 supports 1.8V, 2.5V or 3.3V. VCCIO2 can be connected to different voltage with VCCIO1. |
| 19 | | 23 | | XP | AI/O | Connect to X right electrode of 4-wire resistive touch-screen panel. Powered from pin VCCIO2. |
| 20 | | 24 | | YP | AI/O | Connect to Y top electrode of 4-wire resistive touch-screen panel. Powered from pin VCCIO2. |
| 21 | | 25 | | XM | AI/O | Connect to X left electrode of 4-wire resistive touch-screen panel. Powered from pin VCCIO2. |
| 22 | | 26 | | YM | AI/O | Connect to Y bottom electrode of 4-wire resistive touch-screen panel. Powered from pin VCCIO2. |
| - | 19 | - | 23 | CTP_RST_N | O | Connect to reset pin of the CTPM. Powered from pin VCCIO2. |
| - | 20 | - | 24 | CTP_INT_N | I | Connect to interrupt pin of the CTPM. Powered from pin VCCIO2. |
| - | 21 | - | 25 | CTP_SCL | I/OD | Connect to I2C SCL pin of the CTPM. Powered from pin VCCIO2. |
| - | 22 | - | 26 | CTP_SDA | I/OD | Connect to I2C SDA pin of the CTPM. Powered from pin VCCIO2. |
| 23 | 23 | 27 | 27 | GND | p | Ground |
| 24 | 24 | 28 | 28 | BACKLIGHT | O | LED Backlight brightness PWM control signal. Powered from pin VCCIO2. |
| 25 | 25 | 29 | 29 | DE | O | LCD Data Enable. Powered from pin VCCIO2. |
| 26 | 26 | 30 | 30 | VSYNC | O | LCD Vertical Sync. Powered from pin VCCIO2. |

| Pin Number | | | | Pin Name | Type | Description |
|------------|-------|-------|-------|----------|------|---|
| FT810 | FT811 | FT812 | FT813 | | | |
| 27 | 27 | 31 | 31 | HSYNC | O | LCD Horizontal Sync. Powered from pin VCCIO2. |
| 28 | 28 | 32 | 32 | DISP | O | LCD Display Enable. Powered from pin VCCIO2. |
| 29 | 29 | 33 | 33 | PCLK | O | LCD Pixel Clock. Powered from pin VCCIO2. |
| 30 | 30 | 34 | 34 | B7 | O | Bit 7 of Blue RGB signals. Powered from pin VCCIO2. |
| 31 | 31 | 35 | 35 | B6 | O | Bit 6 of Blue RGB signals. Powered from pin VCCIO2. |
| 32 | 32 | 36 | 36 | B5 | O | Bit 5 of Blue RGB signals. Powered from pin VCCIO2. |
| 33 | 33 | 37 | 37 | B4 | O | Bit 4 of Blue RGB signals. Powered from pin VCCIO2. |
| 34 | 34 | 38 | 38 | B3 | O | Bit 3 of Blue RGB signals. Powered from pin VCCIO2. |
| 35 | 35 | 39 | 39 | B2 | O | Bit 2 of Blue RGB signals. Powered from pin VCCIO2. |
| - | - | 40 | 40 | B1 | O | Bit 1 of Blue RGB signals. Powered from pin VCCIO2. |
| - | - | 41 | 41 | B0 | O | Bit 0 of Blue RGB signals. Powered from pin VCCIO2. |
| 36 | 36 | 42 | 42 | GND | p | Ground |
| 37 | 37 | 43 | 43 | G7 | O | Bit 7 of Green RGB signals. Powered from pin VCCIO2. |
| 38 | 38 | 44 | 44 | G6 | O | Bit 6 of Green RGB signals. Powered from pin VCCIO2. |
| 39 | 39 | 45 | 45 | G5 | O | Bit 5 of Green RGB signals. Powered from pin VCCIO2. |
| 40 | 40 | 46 | 46 | G4 | O | Bit 4 of Green RGB signals. Powered from pin VCCIO2. |
| 41 | 41 | 47 | 47 | G3 | O | Bit 3 of Green RGB signals. Powered from pin VCCIO2. |
| 42 | 42 | 48 | 48 | G2 | O | Bit 2 of Green RGB signals. Powered from pin VCCIO2. |
| - | - | 49 | 49 | G1 | O | Bit 1 of Green RGB signals. Powered from pin VCCIO2. |
| - | - | 50 | 50 | G0 | O | Bit 0 of Green RGB signals. Powered from pin VCCIO2. |

| Pin Number | | | | Pin Name | Type | Description |
|------------|-------|-------|-------|----------|------|---|
| FT810 | FT811 | FT812 | FT813 | | | |
| 43 | 43 | 51 | 51 | R7 | O | Bit 7 of Red RGB signals. Powered from pin VCCIO2. |
| 44 | 44 | 52 | 52 | R6 | O | Bit 6 of Red RGB signals. Powered from pin VCCIO2. |
| 45 | 45 | 53 | 53 | R5 | O | Bit 5 of Red RGB signals. Powered from pin VCCIO2. |
| 46 | 46 | 54 | 54 | R4 | O | Bit 4 of Red RGB signals. Powered from pin VCCIO2. |
| 47 | 47 | 55 | 55 | R3 | O | Bit 3 of Red RGB signals. Powered from pin VCCIO2. |
| 48 | 48 | 56 | 56 | R2 | O | Bit 2 of Red RGB signals. Powered from pin VCCIO2. |
| EP | EP | EP | EP | GND | p | Ground. Exposed thermal pad. |

Table 3-1 FT81x pin description

Note:

P : Power or ground

I : Input

O : Output

OD : Open drain output

I/O : Bi-direction Input and Output

AI/O: Analog Input and Output

4 Function Description

The FT81x is a single chip, embedded video controller with the following function blocks:

- Quad SPI Host Interface
- System Clock
- Graphics Engine
- Parallel RGB video interface
- Audio Engine
- Touch-screen support and interface
- Power Management

The functions for each block are briefly described in the following subsections.

4.1 Quad SPI Host Interface

The FT81x uses a quad serial parallel interface (QSPI) to communicate with host microcontrollers and microprocessors.

4.1.1 QSPI Interface

The QSPI slave interface operates up to 30MHz. Only SPI mode 0 is supported. Refer to section 6.4.2 for detailed timing specification. The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.

By default the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG_SPI_WIDTH. The table below depicts the setting.

| REG_SPI_WIDTH[1:0] | Channel Mode | Data pins | Max bus speed |
|--------------------|-----------------------|--------------------|---------------|
| 00 | SINGLE – default mode | MISO, MOSI | 30 MHz |
| 01 | DUAL | IO0, IO1 | 30 MHz |
| 10 | QUAD | IO0, IO1, IO2, IO3 | 25 MHz |
| 11 | Reserved | - | - |

Table 4-1 QSPI channel selection

With DUAL/QUAD channel modes, the SPI data ports are now unidirectional. In these modes, each SPI transaction (signified by CS_N going active low) will begin with the data ports set as inputs.

Hence, for writing to the FT81x, the protocol will operate as in FT800, with "WR-Command/Addr2, Addr1, Addr0, DataX, DataY, DataZ ..." The write operation is considered complete when CS_N goes inactive high.

For reading from the FT81x, the protocol will still operate as in FT800, with "RD-Command/Addr2, Addr1, Addr0, Dummy-Byte, DataX, DataY, DataZ". However as the data ports are now unidirectional, a change of port direction will occur before DataX is clocked out of the FT81x. Therefore it is important that the firmware controlling the SPI master changes the SPI master data port direction to "input" after transmitting Addr0. The FT81x will not change the port direction till it starts to clock out DataX. Hence, the Dummy-Byte cycles will be used as a change-over period when neither the SPI master nor slave will be driving the bus; the data paths thus must have pull-ups/pull-downs. The SPI slave from the FT81x will reset all its data ports' direction to input once CS_N goes inactive high (i.e. at the end of the current SPI master transaction).

The diagram depicts the behaviour of both the SPI master and slave in the master read case.

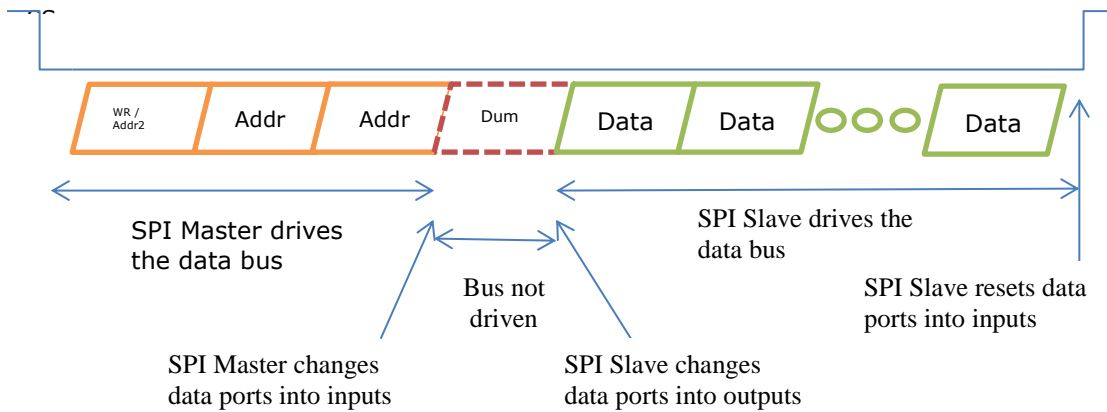


Figure 4-1 SPI master and slave in the master read case

In the DUAL channel mode, MISO (MSB) and MOSI are used while in the QUAD channel mode. IO3 (MSB), IO2, MISO and MOSI are used.

Figure 4-2 illustrates a direct connection to a 1.8-3.3V IO MPU/MCU with single or dual SPI interface.

Figure 4-3 illustrates a direct connection to a 1.8-3.3V IO MPU/MCU with Quad SPI interface.

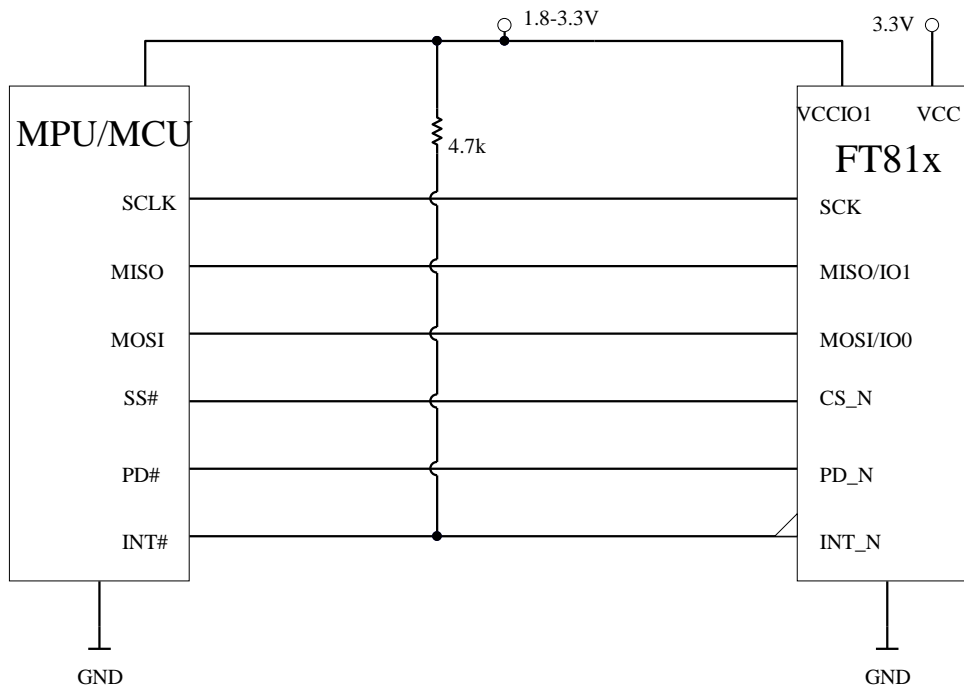


Figure 4-2 Single/Dual SPI Interface connection

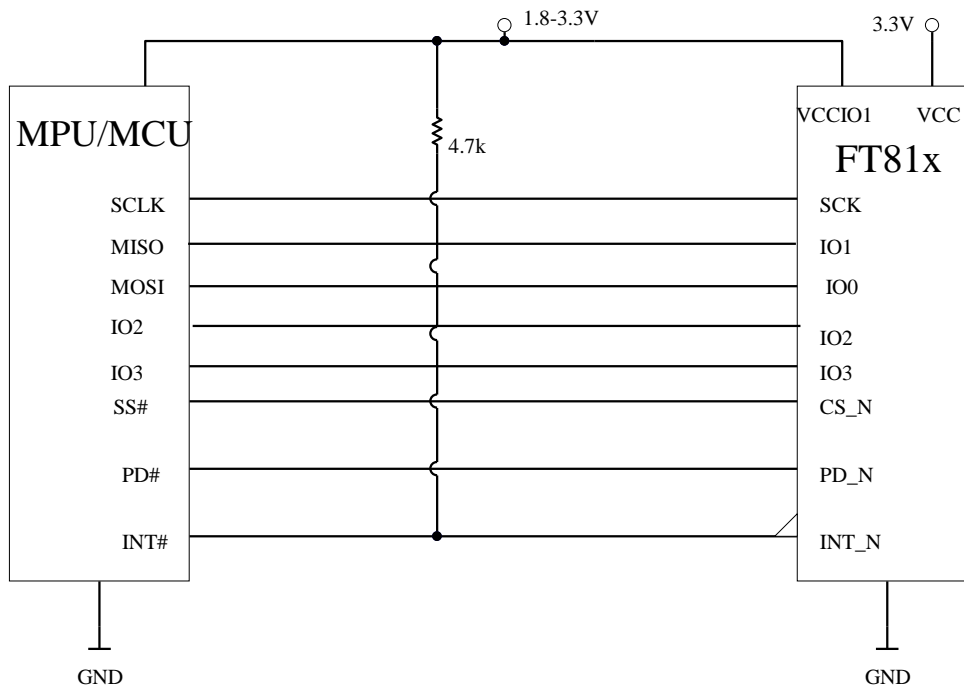


Figure 4-3 Quad SPI Interface connection

4.1.2 Serial Data Protocol

The FT81x appears to the host MPU/MCU as a memory-mapped SPI device. The host communicates with the FT81x using reads and writes to a large (4 megabyte) address space. Within this address space are dedicated areas for graphics, audio and touch control. Refer to section 5 for the detailed memory map.

The host reads and writes the FT81x address space using SPI transactions. These transactions are memory read, memory write and command write. Serial data is sent by the most significant bit first.

Each transaction starts with CS_N goes low, and ends when CS_N goes high. There's no limit on data length within one transaction, as long as the memory address is continuous.

4.1.3 Host Memory Read

For SPI memory read transactions, the host sends two zero bits, followed by the 22-bit address. This is followed by a dummy byte. After the dummy byte, the FT81x responds to each host byte with read data bytes.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|----------------|---|-----------------|---|---|---|---|---|---|---------------|
| 0 | 0 | Address [21:16] | | | | | | } | Write Address |
| Address [15:8] | | | | | | | | | |
| Address [7:0] | | | | | | | | | |
| Dummy byte | | | | | | | | } | Read Data |
| Byte 0 | | | | | | | | | |
| Byte n | | | | | | | | | |

Table 4-2 Host memory read transaction

4.1.4 Host Memory Write

For SPI memory write transactions, the host sends a '1' bit and '0' bit, followed by the 22-bit address. This is followed by the write data.

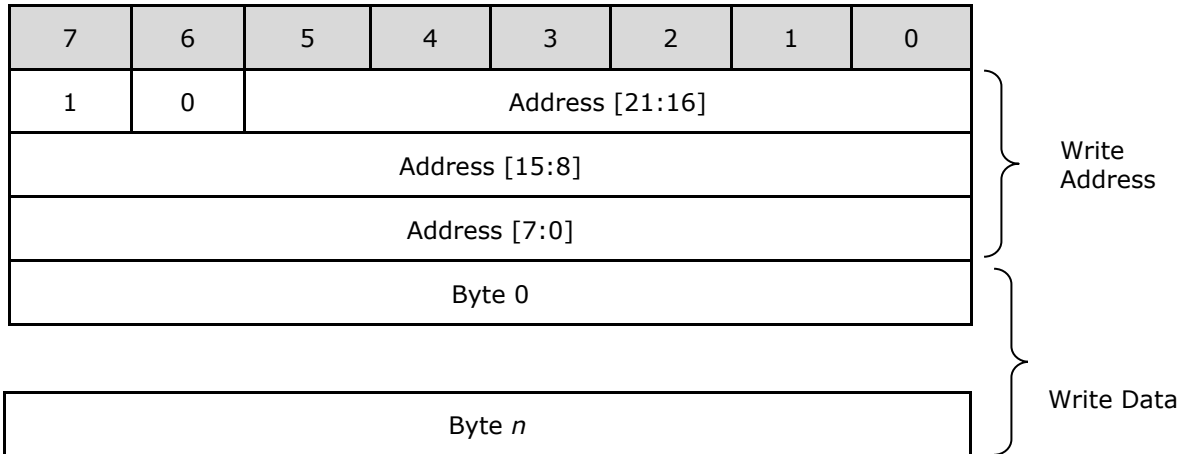


Table 4-3 Host memory write transaction

4.1.5 Host Command

When sending a command, the host transmits a 3 byte command. **Error! Reference source not found.** Lists all the host command functions.

For SPI command transactions, the host sends a '0' bit and '1' bit, followed by the 6-bit command code. The 2nd byte can be either 00h, or the parameter of that command. The 3rd byte is fixed at 00h.

All SPI commands except the system reset can only be executed when the SPI is in the Single channel mode. They will be ignored when the SPI is in either Dual or Quad channel mode.

Some commands are used to configure the device and these configurations will be reset upon receiving the SPI PWRDOWN command, except those that configure the pin state during power down. These commands will be sticky unless reconfigured or power-on-reset (POR) occurs.

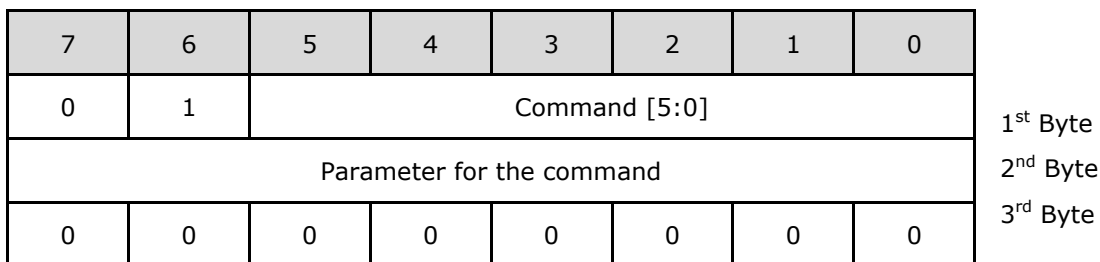


Table 4-4 Host command transaction

| 1st Byte | 2nd byte | 3rd byte | Command | Description |
|--------------------|----------|----------|---------------|--|
| Power Modes | | | | |
| 0000000b | 0000000b | 0000000b | 00h ACTIVE | Switch from Standby/Sleep/PWRDOWN modes to active mode. Dummy memory read from address 0(read twice) generates ACTIVE command. |

| 1st Byte | 2nd byte | 3rd byte | Command | Description | | | | | | | | | | | | |
|------------------------|---|-----------|--------------------|---|-------------|--------------------------|----------|----------------------------|----------|------------|----------|---|----------|------------|------------|----------|
| 01000001b | 00000000b | 00000000b | 41h STANDBY | Put FT81x core to standby mode. Clock gate off, PLL and Oscillator remain on (default). ACTIVE command to wake up. | | | | | | | | | | | | |
| 01000010b | 00000000b | 00000000b | 42h SLEEP | Put FT81x core to sleep mode. Clock gate off, PLL and Oscillator off. ACTIVE command to wake up. | | | | | | | | | | | | |
| 01000011b 01010000b | 00000000b | 00000000b | 43h/50h PWRDOWN | Switch off 1.2V core voltage to the digital core circuits. Clock, PLL and Oscillator off. SPI is alive. ACTIVE command to wake up. | | | | | | | | | | | | |
| 01000100b | xx | 00000000b | 49h PD_ROMS | <p>Select power down individual ROMs; Byte2 determines which ROM to power down or up. A 1 on a bit powers down the corresponding block; a 0 on a bit powers up the corresponding block. As these are not readable, the host must remember the setting on its own.</p> <table border="1"> <tr> <td>Byte2[7]</td> <td>ROM_MAIN</td> </tr> <tr> <td>Byte2[6]</td> <td>ROM_RCOSATAN</td> </tr> <tr> <td>Byte2[5]</td> <td>ROM_SAMPLE</td> </tr> <tr> <td>Byte2[4]</td> <td>ROM_JABOOT</td> </tr> <tr> <td>Byte2[3]</td> <td>ROM_J1BOOT</td> </tr> <tr> <td>Byte2[2-0]</td> <td>reserved</td> </tr> </table> | Byte2[7] | ROM_MAIN | Byte2[6] | ROM_RCOSATAN | Byte2[5] | ROM_SAMPLE | Byte2[4] | ROM_JABOOT | Byte2[3] | ROM_J1BOOT | Byte2[2-0] | reserved |
| Byte2[7] | ROM_MAIN | | | | | | | | | | | | | | | |
| Byte2[6] | ROM_RCOSATAN | | | | | | | | | | | | | | | |
| Byte2[5] | ROM_SAMPLE | | | | | | | | | | | | | | | |
| Byte2[4] | ROM_JABOOT | | | | | | | | | | | | | | | |
| Byte2[3] | ROM_J1BOOT | | | | | | | | | | | | | | | |
| Byte2[2-0] | reserved | | | | | | | | | | | | | | | |
| Clock and Reset | | | | | | | | | | | | | | | | |
| 01000100b | 00000000b | 00000000b | 44h CLKEXT | Select PLL input from external crystal oscillator or external input clock. No effect if external clock is already selected, otherwise a system reset will be generated | | | | | | | | | | | | |
| 01001000b | 00000000b | 00000000b | 48h CLKINT | Select PLL input from internal relaxation oscillator (default). No effect if internal clock is already selected, otherwise a system reset will be generated | | | | | | | | | | | | |
| 01100001b 01100010b | xx | 00000000b | 61h/62h CLKSEL | <p>This command will only be effective when the PLL is stopped (SLEEP mode).</p> <p>For compatibility to FT800/FT801, set Byte2 to 0x00. This will set the PLL clock back to default (60 MHz).</p> <table border="1"> <tr> <td>Byte2 [5:0]</td> <td>sets the clock frequency</td> </tr> <tr> <td>0</td> <td>Set to default clock speed</td> </tr> <tr> <td>1</td> <td>Reserved</td> </tr> <tr> <td>2 to 5</td> <td>2 to 5 times the osc frequency (i.e. 24 to 60MHz with 12MHz oscillator)</td> </tr> </table> | Byte2 [5:0] | sets the clock frequency | 0 | Set to default clock speed | 1 | Reserved | 2 to 5 | 2 to 5 times the osc frequency (i.e. 24 to 60MHz with 12MHz oscillator) | | | | |
| Byte2 [5:0] | sets the clock frequency | | | | | | | | | | | | | | | |
| 0 | Set to default clock speed | | | | | | | | | | | | | | | |
| 1 | Reserved | | | | | | | | | | | | | | | |
| 2 to 5 | 2 to 5 times the osc frequency (i.e. 24 to 60MHz with 12MHz oscillator) | | | | | | | | | | | | | | | |

| 1st Byte | 2nd byte | 3rd byte | Command | Description | | | | | | | | | | | | | | | | |
|----------------------|---------------------------|-----------|------------------|---|-------------|--------------------|----|---------------------------|----|------------------------|----|--------|----|--------|-------------|-----------------|-----|--------|-----|--------|
| | | | | <table border="1"> <tr> <td>Byte2 [7:6]</td> <td>sets the PLL range</td> </tr> <tr> <td>0</td> <td>When Byte2[5:0] = 0, 2, 3</td> </tr> <tr> <td>1</td> <td>When Byte2[5:0] = 4, 5</td> </tr> </table> | Byte2 [7:6] | sets the PLL range | 0 | When Byte2[5:0] = 0, 2, 3 | 1 | When Byte2[5:0] = 4, 5 | | | | | | | | | | |
| Byte2 [7:6] | sets the PLL range | | | | | | | | | | | | | | | | | | | |
| 0 | When Byte2[5:0] = 0, 2, 3 | | | | | | | | | | | | | | | | | | | |
| 1 | When Byte2[5:0] = 4, 5 | | | | | | | | | | | | | | | | | | | |
| 01101000b | 00000000b | 00000000b | 68h RST_PULSE | Send reset pulse to FT81x core. The behaviour is the same as POR except that settings done through SPI commands will not be affected | | | | | | | | | | | | | | | | |
| Configuration | | | | | | | | | | | | | | | | | | | | |
| 01110000b | xx | 00000000b | 70h PINDRIVE | <p>This will set the drive strength for various pins. For FT800/FT801 compatibility, by default those settings are from the GPIO registers. FT81x supports setting the drive strength via SPI command instead.</p> <p>When PINDRIVE for a pin from the SPI command is not updated, the drive strength will be determined by its corresponding GPIO register bits, if they exist. If they don't exist, a hard coded setting is used. Please refer to Error! Reference source not found. for default values.</p> <p>When PINDRIVE for a pin from the SPI command is updated, it will override the corresponding setting in the GPIO register bits.</p> <p>Byte2 determines which pin and the setting are to be updated.</p> <p>Byte2[1:0] determine the drive strength:</p> <table border="1"> <thead> <tr> <th>Byte2 [1:0]</th> <th>Drive Strength</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>5mA</td> </tr> <tr> <td>1h</td> <td>10.0mA</td> </tr> <tr> <td>2h</td> <td>15.0mA</td> </tr> <tr> <td>3h</td> <td>20.0mA</td> </tr> </tbody> </table> <p>Byte[7:2] determine which pin/pin group to set:</p> <table border="1"> <thead> <tr> <th>Byte2 [7:2]</th> <th>Pin / Pin Group</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>GPIO 0</td> </tr> <tr> <td>01h</td> <td>GPIO 1</td> </tr> </tbody> </table> | Byte2 [1:0] | Drive Strength | 0h | 5mA | 1h | 10.0mA | 2h | 15.0mA | 3h | 20.0mA | Byte2 [7:2] | Pin / Pin Group | 00h | GPIO 0 | 01h | GPIO 1 |
| Byte2 [1:0] | Drive Strength | | | | | | | | | | | | | | | | | | | |
| 0h | 5mA | | | | | | | | | | | | | | | | | | | |
| 1h | 10.0mA | | | | | | | | | | | | | | | | | | | |
| 2h | 15.0mA | | | | | | | | | | | | | | | | | | | |
| 3h | 20.0mA | | | | | | | | | | | | | | | | | | | |
| Byte2 [7:2] | Pin / Pin Group | | | | | | | | | | | | | | | | | | | |
| 00h | GPIO 0 | | | | | | | | | | | | | | | | | | | |
| 01h | GPIO 1 | | | | | | | | | | | | | | | | | | | |

| 1st Byte | 2nd byte | 3rd byte | Command | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------|------------------------|-----------|---------------------|--|-----|--------|-----|--------|--------|----------|-----|------|-----|----|-----|---------------|-----|------|-----|-----------|-----|------------------------|-----|---------|-----|-------|-----|-----------|-----|---------|-----|---------|-----|-----------------------|--------|----------|
| | | | | <table border="1"> <tr><td>02h</td><td>GPIO 2</td></tr> <tr><td>03h</td><td>GPIO 3</td></tr> <tr><td>04-07h</td><td>Reserved</td></tr> <tr><td>08h</td><td>DISP</td></tr> <tr><td>09h</td><td>DE</td></tr> <tr><td>0Ah</td><td>VSYNC / HSYNC</td></tr> <tr><td>0Bh</td><td>PCLK</td></tr> <tr><td>0Ch</td><td>BACKLIGHT</td></tr> <tr><td>0Dh</td><td>R[7:0], G[7:0], B[7:0]</td></tr> <tr><td>0Eh</td><td>AUDIO_L</td></tr> <tr><td>0Fh</td><td>INT_N</td></tr> <tr><td>10h</td><td>CTP_RST_N</td></tr> <tr><td>11h</td><td>CTP_SCL</td></tr> <tr><td>12h</td><td>CTP_SDA</td></tr> <tr><td>13h</td><td>SPI MISO/MOSI/IO2/IO3</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </table> <p>Note: GPIO0 shares the same pin as SPI IO2 and GPIO1 with SPI IO3. When SPI is set in Quad mode, IO2 and IO3 will inherit the drive strength set in GROUP 13h; otherwise GPIO0 and GPIO1 will inherit the drive strength from GROUP 00h and 01h respectively.</p> | 02h | GPIO 2 | 03h | GPIO 3 | 04-07h | Reserved | 08h | DISP | 09h | DE | 0Ah | VSYNC / HSYNC | 0Bh | PCLK | 0Ch | BACKLIGHT | 0Dh | R[7:0], G[7:0], B[7:0] | 0Eh | AUDIO_L | 0Fh | INT_N | 10h | CTP_RST_N | 11h | CTP_SCL | 12h | CTP_SDA | 13h | SPI MISO/MOSI/IO2/IO3 | Others | Reserved |
| 02h | GPIO 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 03h | GPIO 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 04-07h | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 08h | DISP | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 09h | DE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0Ah | VSYNC / HSYNC | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0Bh | PCLK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0Ch | BACKLIGHT | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0Dh | R[7:0], G[7:0], B[7:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0Eh | AUDIO_L | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0Fh | INT_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10h | CTP_RST_N | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11h | CTP_SCL | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12h | CTP_SDA | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13h | SPI MISO/MOSI/IO2/IO3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Others | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01110001b | xx | 00000000b | 71h PIN_PD_STATE | <p>During power down, all output and in/out pins will not be driven. Please refer to Error! Reference source not found. for their default power down state.</p> <p>These settings will only be effective during power down and will not affect normal operations. Also note that these configuration bits are sticky and, unlike other configuration bits, will not reset to default values upon exiting power down. Only POR will reset them.</p> <p>Byte2 determines which pin and the setting are to be updated.</p> <p>Byte2[1:0] determine the pin state.</p> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| 1st Byte | 2nd byte | 3rd byte | Command | Description | | | | | | | | | | |
|-------------|-------------|----------|---------|--|-------------|-------------|----|-------|----|-----------|----|---------|----|----------|
| | | | | <table border="1"> <tr> <td>Byte2 [1:0]</td> <td>Pin Setting</td> </tr> <tr> <td>0h</td> <td>Float</td> </tr> <tr> <td>1h</td> <td>Pull-Down</td> </tr> <tr> <td>2h</td> <td>Pull-Up</td> </tr> <tr> <td>3h</td> <td>Reserved</td> </tr> </table> <p>Byte2[7:2] determine which pin/pin group to set. Please refer to the table in command PINDRIVE entry.</p> | Byte2 [1:0] | Pin Setting | 0h | Float | 1h | Pull-Down | 2h | Pull-Up | 3h | Reserved |
| Byte2 [1:0] | Pin Setting | | | | | | | | | | | | | |
| 0h | Float | | | | | | | | | | | | | |
| 1h | Pull-Down | | | | | | | | | | | | | |
| 2h | Pull-Up | | | | | | | | | | | | | |
| 3h | Reserved | | | | | | | | | | | | | |

Table 4-5 Host command list

NOTE: Any command code not specified is reserved and should not be used by the software

4.1.6 Interrupts

The interrupt output pin is enabled by REG_INT_EN. When REG_INT_EN is 0, INT_N is tri-state (pulled to high by external pull-up resistor). When REG_INT_EN is 1, INT_N is driven low when any of the interrupt flags in REG_INT_FLAGS are high, after masking with REG_INT_MASK. Writing a '1' in any bit of REG_INT_MASK will enable the corresponding interrupt. Each bit in REG_INT_FLAGS is set by a corresponding interrupt source. REG_INT_FLAGS is readable by the host at any time, and clears when read.

The INT_N pin is open-drain (OD) output by default. It can be configured to push-pull output by register REG_GPIOX.

| | | | | |
|-------------------|------------------------------------|-------------------------------|--------------------|----------------------------|
| Bit | 7 | 6 | 5 | 4 |
| Interrupt Sources | CONVCOMPLETE | CMDFLAG | CMDEEMPTY | PLAYBACK |
| Conditions | Touch-screen conversions completed | Command FIFO flag | Command FIFO empty | Audio playback ended |
| Bit | 3 | 2 | 1 | 0 |
| Interrupt Sources | SOUND | TAG | TOUCH | SWAP |
| Conditions | Sound effect ended | Touch-screen tag value change | touch detected | Display list swap occurred |

Table 4-6 Interrupt Flags bit assignment

4.2 System Clock

4.2.1 Clock Source

The FT81x can be configured to use any of the three clock sources for system clock:

- Internal relaxation oscillator clock (default)
- External 12MHz crystal
- External 12MHz square wave clock

Figure 4-4, Figure 4-5 and Figure 4-6 show the pin connections for these clock options.

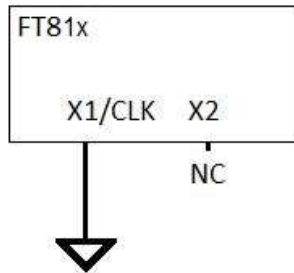


Figure 4-4 Internal relaxation oscillator connection

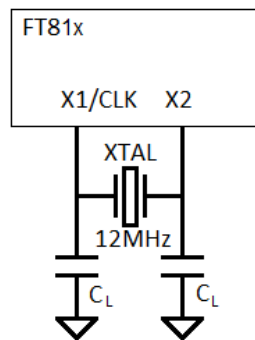


Figure 4-5 Crystal oscillator connection

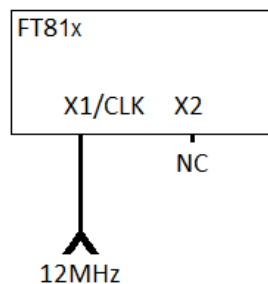


Figure 4-6 External clock input

4.2.2 Phase Locked Loop

The internal PLL takes an input clock from the oscillator, and generates clocks to all internal circuits, including the graphics engine, audio engine and touch engine.

4.2.3 Clock Enable

At power-on the FT81x enters sleep mode. The internal relaxation oscillator is selected for the PLL clock source. The system clock will be enabled when the following step is executed:

- Host sends an "ACTIVE" command

If the application chooses to use the external clock source (12MHz crystal or clock), the following steps shall be executed:

- Host sends a "CLKEXT" command
- Host sends an "ACTIVE" command

4.2.4 Clock Frequency

By default the system clock is 60MHz when the input clock is 12MHz. The host is allowed to switch the system clock to other frequencies (48MHz, 36MHz, and 24MHz) by the host command "CLKSEL". The clock switching command shall be sent in SLEEP mode only.

When using the internal relaxation oscillator, its clock frequency is trimmed to be 12MHz at factory. Software is allowed to change the frequency to a lower value by programming the register REG_TRIM. Note that software shall not change the internal oscillator frequency to be higher than 12MHz.

4.3 Graphics Engine

4.3.1 Introduction

The graphics engine executes the display list once for every horizontal line. It executes the primitive objects in the display list and constructs the display line buffer. The horizontal pixel content in the line buffer is updated if the object is visible at the horizontal line.

Main features of the graphics engine are:

- The primitive objects supported by the graphics processor are: lines, points, rectangles, bitmaps (comprehensive set of formats), text display, plotting bar graph, edge strips, and line strips, etc.
- Operations such as stencil test, alpha blending and masking are useful for creating a rich set of effects such as shadows, transitions, reveals, fades and wipes.
- Anti-aliasing of the primitive objects (except bitmaps) gives a smoothing effect to the viewer.
- Bitmap transformations enable operations such as translate, scale and rotate.
- Display pixels are plotted with 1/16th pixel precision.
- Four levels of graphics states
- Tag buffer detection

The graphics engine also supports customized built-in widgets and functionalities such as jpeg decode, screen saver, calibration etc. The graphics engine interprets commands from the MPU host via a 4 Kbyte FIFO in the FT81x memory at RAM_CMD. The MPU/MCU writes commands into the FIFO, and the graphics engine reads and executes the commands. The MPU/MCU updates the register REG_CMD_WRITE to indicate that there are new commands in the FIFO, and the graphics engine updates REG_CMD_READ after commands have been executed.

Main features supported are:

- Drawing of widgets such as buttons, clock, keys, gauges, text displays, progress bars, sliders, toggle switches, dials, gradients, etc.
- JPEG and motion-JPEG decode
- Inflate functionality (zlib inflate is supported)
- Timed interrupt (generate an interrupt to the host processor after a specified number of milliseconds)
- In-built animated functionalities such as displaying logo, calibration, spinner, screen saver and sketch
- Snapshot feature to capture the current graphics display

For a complete list of graphics engine display commands and widgets refer to [FT81x Series Programmer Guide](#), Chapter 4.

4.3.2 ROM and RAM Fonts

The FT81x has built in ROM character bitmaps as font metrics. The graphics engine can use these metrics when drawing text fonts. There are a total of 19 ROM fonts, numbered with font handle 16-34. The user can define and load customized font metrics into RAM_G, which can be used by display command with handle 0-15.

Each font metric block has a 148 byte font table which defines the parameters of the font and the pointer of font image. The font table format is shown in **Error! Reference source not found.**

| Address Offset | Size(byte) | Parameter Description |
|----------------|------------|--|
| 0 | 128 | width of each font character, in pixels |
| 128 | 4 | font bitmap format, for example L1, L4 or L8 |
| 132 | 4 | font line stride, in bytes |
| 136 | 4 | font width, in pixels |
| 140 | 4 | font height, in pixels |
| 144 | 4 | pointer to font image data in memory |

Table 4-7 Font table format

The ROM fonts are stored in the memory space ROM_FONT. The ROM font table is also stored in the ROM. The starting address of the ROM font table for font index 16 is stored at ROM_FONT_ADDR, with other font tables following. The ROM font table and individual character width (in pixel) are listed in **Error! Reference source not found.** through **Error! Reference source not found.** Font index 16, 18 and 20-31 are for basic ASCII characters (code 0-127), while font index 17 and 19 are for Extended ASCII characters (code 128-255). The character width for font index 16 through 19 is fixed at 8 pixels for any of the ASCII characters.

| Font Index | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
|-----------------------------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| Font format | L1 | L1 | L1 | L1 | L1 | L1 | L1 | L1 | L1 | L4 | L4 | L4 | L4 | L4 | L4 | L4 | L4 | L4 | L4 |
| Line stride | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 3 | 3 | 4 | 7 | 8 | 9 | 11 | 14 | 18 | 23 | 30 | 39 |
| Font width (max) | 8 | 8 | 8 | 8 | 11 | 13 | 17 | 18 | 25 | 34 | 11 | 15 | 19 | 22 | 28 | 37 | 49 | 64 | 83 |
| Font height | 8 | 8 | 16 | 16 | 13 | 17 | 20 | 22 | 29 | 38 | 16 | 20 | 25 | 28 | 36 | 49 | 64 | 83 | 108 |
| Image pointer start address (hex) | 2FF7FC | 2FFBFC | 2FE7FC | 2FEFFC | 2FDAFC | 2FCD3C | 2FBD7C | 2FA17C | 2F7E3C | 2F3D1C | 2F181C | 2ED61C | 2E799C | 2DFB9C | 2D263C | 2BAC3C | 2945FC | 251E1C | 1E1B5C |

Table 4-8 ROM font table

| Font Index => | 16/18 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
|---------------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0 | NULL | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | SOH | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2 | STX | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 3 | ETX | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4 | EOT | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 5 | ENQ | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 6 | ACK | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7 | BEL | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | BS | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Font Index => | 16/18 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | |
|---------------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 9 | HT | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 10 | LF | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 11 | VT | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 12 | FF | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 13 | CR | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 14 | SO | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 15 | SI | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 16 | DLE | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 17 | DC1 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 18 | DC2 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 19 | DC3 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 20 | DC4 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 21 | NAK | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 22 | SYN | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 23 | ETB | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 24 | CAN | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 25 | EM | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 26 | SUB | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 27 | ESC | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 28 | FS | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 29 | GS | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 30 | RS | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 31 | US | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 32 | space | 8 | 3 | 4 | 5 | 5 | 6 | 9 | 3 | 4 | 5 | 6 | 8 | 10 | 13 | 18 | 23 |
| 33 | ! | 8 | 3 | 4 | 5 | 6 | 6 | 9 | 3 | 4 | 6 | 6 | 9 | 11 | 15 | 19 | 25 |
| 34 | " | 8 | 4 | 5 | 6 | 5 | 8 | 12 | 5 | 6 | 7 | 8 | 12 | 15 | 19 | 25 | 33 |
| 35 | # | 8 | 6 | 8 | 9 | 10 | 14 | 19 | 10 | 11 | 14 | 15 | 19 | 26 | 33 | 44 | 57 |
| 36 | \$ | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 11 | 15 | 18 | 25 | 31 | 41 | 54 |
| 37 | % | 8 | 9 | 12 | 14 | 16 | 22 | 29 | 11 | 13 | 16 | 17 | 23 | 31 | 40 | 52 | 68 |
| 38 | & | 8 | 8 | 10 | 11 | 13 | 17 | 22 | 9 | 11 | 14 | 15 | 19 | 26 | 34 | 44 | 57 |
| 39 | ' | 8 | 2 | 3 | 3 | 3 | 6 | 6 | 3 | 4 | 4 | 5 | 7 | 10 | 11 | 15 | 20 |
| 40 | (| 8 | 4 | 5 | 6 | 6 | 8 | 11 | 5 | 6 | 7 | 9 | 11 | 15 | 18 | 24 | 31 |
| 41 |) | 8 | 4 | 5 | 6 | 6 | 8 | 11 | 5 | 6 | 8 | 8 | 10 | 14 | 18 | 24 | 31 |
| 42 | * | 8 | 4 | 7 | 6 | 7 | 10 | 13 | 7 | 8 | 10 | 11 | 14 | 18 | 24 | 31 | 40 |
| 43 | + | 8 | 6 | 9 | 10 | 10 | 14 | 19 | 9 | 10 | 12 | 14 | 17 | 24 | 30 | 41 | 52 |
| 44 | , | 8 | 3 | 3 | 4 | 5 | 6 | 9 | 3 | 4 | 4 | 5 | 7 | 9 | 12 | 16 | 20 |
| 45 | - | 8 | 4 | 4 | 5 | 6 | 8 | 11 | 6 | 7 | 10 | 11 | 15 | 18 | 24 | 32 | 41 |
| 46 | . | 8 | 3 | 3 | 4 | 5 | 6 | 9 | 3 | 4 | 6 | 7 | 8 | 11 | 14 | 19 | 24 |
| 47 | / | 8 | 3 | 4 | 5 | 5 | 7 | 9 | 6 | 7 | 9 | 10 | 13 | 17 | 22 | 29 | 38 |
| 48 | 0 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 49 | 1 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 50 | 2 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 51 | 3 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 52 | 4 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 53 | 5 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 54 | 6 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 55 | 7 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 56 | 8 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 57 | 9 | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 30 | 40 | 52 |
| 58 | : | 8 | 3 | 3 | 4 | 5 | 6 | 9 | 3 | 4 | 6 | 6 | 7 | 10 | 13 | 18 | 23 |
| 59 | ; | 8 | 3 | 4 | 4 | 5 | 6 | 9 | 3 | 4 | 6 | 6 | 8 | 10 | 14 | 18 | 23 |
| 60 | < | 8 | 6 | 8 | 10 | 10 | 15 | 19 | 8 | 9 | 11 | 12 | 16 | 21 | 28 | 36 | 46 |
| 61 | = | 8 | 5 | 9 | 10 | 11 | 15 | 19 | 8 | 9 | 13 | 14 | 18 | 23 | 30 | 40 | 52 |

| Font Index | => | 16/18 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 |
|------------|----|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 62 | > | 8 | 6 | 8 | 10 | 10 | 15 | 19 | 8 | 9 | 11 | 13 | 16 | 22 | 29 | 37 | 48 |
| 63 | ? | 8 | 6 | 8 | 9 | 10 | 12 | 18 | 7 | 9 | 10 | 12 | 15 | 20 | 26 | 34 | 44 |
| 64 | @ | 8 | 11 | 13 | 17 | 18 | 25 | 34 | 13 | 15 | 19 | 21 | 28 | 37 | 49 | 63 | 82 |
| 65 | A | 8 | 7 | 9 | 11 | 13 | 17 | 22 | 9 | 11 | 13 | 15 | 20 | 27 | 34 | 45 | 58 |
| 66 | B | 8 | 7 | 9 | 11 | 13 | 17 | 22 | 9 | 10 | 14 | 15 | 19 | 27 | 34 | 45 | 58 |
| 67 | C | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 13 | 15 | 20 | 26 | 34 | 45 | 58 |
| 68 | D | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 14 | 17 | 22 | 28 | 36 | 48 | 63 |
| 69 | E | 8 | 7 | 9 | 11 | 13 | 16 | 22 | 7 | 9 | 12 | 13 | 16 | 23 | 29 | 39 | 50 |
| 70 | F | 8 | 6 | 8 | 10 | 12 | 14 | 20 | 7 | 9 | 12 | 13 | 17 | 22 | 29 | 39 | 50 |
| 71 | G | 8 | 8 | 11 | 13 | 15 | 19 | 25 | 9 | 11 | 14 | 16 | 22 | 28 | 37 | 48 | 62 |
| 72 | H | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 15 | 17 | 23 | 29 | 37 | 50 | 65 |
| 73 | I | 8 | 3 | 4 | 4 | 6 | 8 | 9 | 4 | 5 | 6 | 7 | 9 | 12 | 15 | 20 | 26 |
| 74 | J | 8 | 5 | 7 | 8 | 10 | 13 | 16 | 8 | 9 | 12 | 13 | 17 | 23 | 30 | 40 | 50 |
| 75 | K | 8 | 7 | 9 | 11 | 13 | 18 | 22 | 9 | 11 | 14 | 16 | 19 | 26 | 34 | 45 | 58 |
| 76 | L | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 7 | 9 | 12 | 13 | 17 | 22 | 29 | 39 | 51 |
| 77 | M | 8 | 9 | 12 | 13 | 16 | 21 | 27 | 11 | 14 | 19 | 21 | 26 | 35 | 46 | 62 | 79 |
| 78 | N | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 15 | 17 | 23 | 29 | 37 | 50 | 65 |
| 79 | O | 8 | 8 | 11 | 13 | 15 | 18 | 25 | 10 | 12 | 14 | 16 | 22 | 28 | 37 | 49 | 63 |
| 80 | P | 8 | 7 | 9 | 11 | 13 | 16 | 22 | 9 | 10 | 14 | 15 | 19 | 26 | 34 | 45 | 58 |
| 81 | Q | 8 | 8 | 11 | 13 | 15 | 18 | 26 | 10 | 12 | 14 | 17 | 22 | 29 | 38 | 50 | 64 |
| 82 | R | 8 | 7 | 10 | 12 | 14 | 17 | 24 | 9 | 11 | 13 | 15 | 19 | 27 | 33 | 45 | 58 |
| 83 | S | 8 | 7 | 9 | 11 | 13 | 16 | 22 | 9 | 11 | 12 | 14 | 20 | 26 | 33 | 43 | 56 |
| 84 | T | 8 | 5 | 9 | 10 | 12 | 16 | 20 | 10 | 12 | 14 | 15 | 19 | 26 | 32 | 42 | 56 |
| 85 | U | 8 | 8 | 10 | 12 | 14 | 18 | 24 | 9 | 11 | 13 | 17 | 21 | 28 | 37 | 48 | 62 |
| 86 | V | 8 | 7 | 9 | 11 | 13 | 17 | 22 | 9 | 11 | 14 | 15 | 20 | 27 | 34 | 45 | 58 |
| 87 | W | 8 | 9 | 13 | 15 | 18 | 22 | 31 | 12 | 15 | 18 | 21 | 27 | 36 | 46 | 61 | 79 |
| 88 | X | 8 | 7 | 9 | 11 | 13 | 17 | 22 | 9 | 11 | 13 | 15 | 20 | 27 | 34 | 45 | 58 |
| 89 | Y | 8 | 7 | 9 | 11 | 13 | 16 | 22 | 9 | 10 | 14 | 15 | 19 | 26 | 34 | 45 | 58 |
| 90 | Z | 8 | 7 | 9 | 10 | 12 | 15 | 20 | 9 | 11 | 13 | 14 | 18 | 25 | 32 | 42 | 55 |
| 91 | [| 8 | 3 | 4 | 5 | 5 | 7 | 9 | 4 | 5 | 6 | 7 | 9 | 12 | 15 | 19 | 25 |
| 92 | \ | 8 | 3 | 4 | 5 | 5 | 7 | 9 | 6 | 7 | 9 | 10 | 13 | 18 | 22 | 29 | 38 |
| 93 |] | 8 | 3 | 4 | 5 | 5 | 7 | 9 | 4 | 5 | 7 | 7 | 9 | 12 | 15 | 19 | 25 |
| 94 | ^ | 8 | 6 | 7 | 8 | 9 | 12 | 16 | 6 | 7 | 9 | 10 | 13 | 18 | 23 | 30 | 38 |
| 95 | _ | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 10 | 11 | 13 | 16 | 21 | 26 | 34 | 43 |
| 96 | ` | 8 | 3 | 5 | 6 | 4 | 7 | 11 | 4 | 5 | 7 | 8 | 10 | 13 | 17 | 22 | 29 |
| 97 | a | 8 | 5 | 8 | 9 | 11 | 13 | 18 | 8 | 9 | 11 | 13 | 17 | 23 | 30 | 39 | 50 |
| 98 | b | 8 | 6 | 7 | 9 | 11 | 14 | 18 | 8 | 9 | 11 | 14 | 17 | 24 | 31 | 40 | 52 |
| 99 | c | 8 | 5 | 7 | 8 | 10 | 12 | 16 | 8 | 9 | 11 | 12 | 16 | 22 | 28 | 37 | 48 |
| 100 | d | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 10 | 12 | 14 | 17 | 24 | 31 | 40 | 52 |
| 101 | e | 8 | 5 | 8 | 9 | 10 | 13 | 18 | 8 | 9 | 11 | 12 | 16 | 22 | 29 | 37 | 48 |
| 102 | f | 8 | 4 | 4 | 5 | 6 | 8 | 9 | 6 | 7 | 8 | 10 | 12 | 15 | 19 | 25 | 31 |
| 103 | g | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 10 | 11 | 14 | 18 | 24 | 31 | 41 | 52 |
| 104 | h | 8 | 6 | 8 | 9 | 10 | 13 | 18 | 8 | 9 | 11 | 14 | 17 | 24 | 31 | 41 | 52 |
| 105 | i | 8 | 2 | 3 | 3 | 4 | 6 | 7 | 3 | 4 | 6 | 6 | 7 | 10 | 13 | 18 | 23 |
| 106 | j | 8 | 2 | 3 | 4 | 4 | 6 | 7 | 3 | 4 | 6 | 6 | 8 | 11 | 14 | 18 | 23 |
| 107 | k | 8 | 5 | 7 | 8 | 9 | 12 | 16 | 7 | 9 | 11 | 13 | 16 | 22 | 28 | 36 | 47 |
| 108 | l | 8 | 2 | 3 | 3 | 4 | 6 | 7 | 3 | 4 | 6 | 6 | 7 | 10 | 13 | 18 | 23 |
| 109 | m | 8 | 8 | 11 | 14 | 16 | 20 | 27 | 11 | 15 | 18 | 21 | 27 | 36 | 47 | 63 | 80 |
| 110 | n | 8 | 6 | 8 | 9 | 10 | 14 | 18 | 8 | 9 | 11 | 14 | 17 | 24 | 31 | 41 | 52 |
| 111 | o | 8 | 6 | 8 | 9 | 11 | 13 | 18 | 8 | 10 | 12 | 13 | 17 | 24 | 31 | 40 | 52 |
| 112 | p | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 9 | 11 | 14 | 17 | 24 | 31 | 40 | 51 |
| 113 | q | 8 | 6 | 8 | 9 | 11 | 14 | 18 | 8 | 10 | 12 | 13 | 17 | 24 | 31 | 40 | 52 |
| 114 | r | 8 | 4 | 5 | 5 | 6 | 9 | 11 | 5 | 6 | 7 | 9 | 11 | 15 | 19 | 25 | 32 |
| 115 | s | 8 | 5 | 7 | 8 | 9 | 12 | 16 | 7 | 9 | 11 | 12 | 17 | 22 | 29 | 38 | 48 |

| Font Index => | 16/18 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | |
|---------------|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 116 | t | 8 | 4 | 4 | 5 | 6 | 8 | 9 | 6 | 7 | 8 | 9 | 11 | 14 | 17 | 23 | 29 |
| 117 | u | 8 | 5 | 7 | 9 | 10 | 14 | 18 | 8 | 9 | 12 | 14 | 17 | 24 | 31 | 41 | 52 |
| 118 | v | 8 | 6 | 7 | 8 | 10 | 13 | 16 | 7 | 9 | 11 | 12 | 16 | 21 | 27 | 36 | 46 |
| 119 | w | 8 | 8 | 10 | 12 | 14 | 18 | 23 | 11 | 13 | 16 | 18 | 23 | 32 | 41 | 54 | 70 |
| 120 | x | 8 | 6 | 7 | 8 | 10 | 12 | 16 | 7 | 9 | 11 | 12 | 16 | 21 | 27 | 36 | 46 |
| 121 | y | 8 | 5 | 7 | 8 | 10 | 13 | 16 | 7 | 9 | 11 | 12 | 16 | 21 | 27 | 36 | 46 |
| 122 | z | 8 | 5 | 7 | 8 | 9 | 12 | 16 | 8 | 9 | 11 | 12 | 15 | 22 | 27 | 36 | 46 |
| 123 | { | 8 | 3 | 5 | 6 | 6 | 8 | 11 | 5 | 6 | 8 | 8 | 11 | 15 | 18 | 24 | 31 |
| 124 | | 8 | 3 | 3 | 4 | 5 | 6 | 9 | 3 | 4 | 5 | 6 | 7 | 10 | 14 | 18 | 23 |
| 125 | } | 8 | 3 | 5 | 6 | 6 | 8 | 11 | 5 | 6 | 7 | 9 | 10 | 15 | 18 | 24 | 31 |
| 126 | ~ | 8 | 7 | 8 | 10 | 10 | 14 | 19 | 10 | 11 | 14 | 15 | 21 | 29 | 36 | 47 | 63 |
| 127 | DEL | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 4 | 5 | 6 | 5 | 10 | 13 | 18 | 23 |

Table 4-9 ROM font ASCII character width in pixels

| Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol | Decimal | Symbol |
|---------|--------|---------|--------|---------|--------|---------|--------|---------|--------|---------|--------|---------|--------|---------|--------|
| 128 | ç | 144 | é | 160 | á | 176 | ☐ | 192 | └ | 208 | ┌ | 224 | α | 240 | ≡ |
| 129 | ü | 145 | æ | 161 | í | 177 | ☐ | 193 | ┘ | 209 | ┐ | 225 | β | 241 | ± |
| 130 | é | 146 | Æ | 162 | ó | 178 | ☐ | 194 | ┘ | 210 | ┘ | 226 | γ | 242 | ≥ |
| 131 | â | 147 | ô | 163 | ú | 179 | | 195 | ┘ | 211 | ┘ | 227 | π | 243 | ≤ |
| 132 | ä | 148 | ö | 164 | ñ | 180 | ┘ | 196 | — | 212 | ┘ | 228 | Σ | 244 | ∫ |
| 133 | à | 149 | ò | 165 | Ñ | 181 | ┘ | 197 | + | 213 | ┘ | 229 | σ | 245 | ∫ |
| 134 | â | 150 | û | 166 | ë | 182 | ┘ | 198 | ┘ | 214 | ┘ | 230 | μ | 246 | ÷ |
| 135 | ç | 151 | ù | 167 | ø | 183 | ┘ | 199 | ┘ | 215 | + | 231 | τ | 247 | ≈ |
| 136 | ê | 152 | ÿ | 168 | ç | 184 | ┘ | 200 | ┘ | 216 | + | 232 | φ | 248 | ° |
| 137 | ë | 153 | ö | 169 | — | 185 | ┘ | 201 | ┘ | 217 | ┘ | 233 | θ | 249 | • |
| 138 | è | 154 | Ü | 170 | — | 186 | | 202 | ┘ | 218 | ┘ | 234 | Ω | 250 | · |
| 139 | ï | 155 | ¢ | 171 | ½ | 187 | ┘ | 203 | ┘ | 219 | ■ | 235 | δ | 251 | √ |
| 140 | î | 156 | £ | 172 | ¼ | 188 | ┘ | 204 | ┘ | 220 | ■ | 236 | ω | 252 | ⁿ |
| 141 | ì | 157 | ¥ | 173 | ¡ | 189 | ┘ | 205 | — | 221 | ■ | 237 | φ | 253 | ² |
| 142 | Ä | 158 | ₣ | 174 | « | 190 | ┘ | 206 | + | 222 | ■ | 238 | ε | 254 | ■ |
| 143 | Å | 159 | ₣ | 175 | » | 191 | ┘ | 207 | ┘ | 223 | ■ | 239 | π | 255 | nbsp |

Table 4-10 ROM font Extended ASCII characters

Note: Font 17 and 19 are extended ASCII characters, with width fixed at 8 pixels for all characters.

Note: All fonts included in the FT81x ROM are widely available to the market-place for general usage. See section nine for specific copyright data and links to the corresponding license agreements.

4.4 Parallel RGB Interface

The RGB parallel interface consists of 23 or 29 signals - DISP, PCLK, VSYNC, HSYNC, DE, 6 or 8 signals each for R, G and B.

A set of RGB registers configure the LCD operation and timing parameters.

REG_PCLK is the PCLK divisor. The default value is 0, which means the PCLK output is disabled. When REG_PCLK is none 0 (1-1023), the PCLK frequency can be calculated as:

PCLK frequency = System Clock frequency / REG_PCLK

The FT81x system clock frequency is programmable. Some of the possible PCLK frequencies that FT81x supports are listed in **Error! Reference source not found.**

| REG_PCLK | System Clock Frequency (MHz) | | | |
|----------|------------------------------|-----|-----|-----|
| | 60(default) | 48 | 36 | 24 |
| 1 | 60 | 48 | 36 | 24 |
| 2 | 30 | 24 | 18 | 12 |
| 3 | 20 | 16 | 12 | 8.0 |
| 4 | 15 | 12 | 9.0 | 6.0 |
| 5 | 12 | 9.6 | 7.2 | 4.8 |
| 6 | 10 | 8.0 | 6.0 | 4.0 |
| 7 | 8.6 | 6.9 | 5.1 | 3.4 |
| 8 | 7.5 | 6.0 | 4.5 | 3.0 |
| 9 | 6.7 | 5.3 | 4.0 | 2.7 |
| 10 | 6.0 | 4.8 | 3.6 | 2.4 |

Table 4-11 RGB PCLK frequency

REG_PCLK_POL defines the clock polarity, with 0 for positive active clock edge, and 1 for negative clock edge.

REG_CSPREAD controls the transition of RGB signals with respect to the PCLK active clock edge. When REG_CSPREAD=0, R[7:0], G[7:0] and B[7:0] signals change following the active edge of PCLK. When REG_CSPREAD=1, R[7:0] changes a PCLK clock early and B[7:0] a PCLK clock later, which helps reduce the switching noise.

REG_DITHER enables colour dither. This option improves the half-tone appearance on displays. Internally, the graphics engine computes the colour values at an 8 bit precision; however, the LCD colour at a lower precision is sufficient. The FT810/FT811 output is only 6 bits per colour in 6:6:6 formats and a 2X2 dither matrix allow the truncated bits to contribute to the final colour values.

REG_OUTBITS gives the bit width of each colour channel, the default is 6/6/6(for FT810/FT811) or 8/8/8(for FT812/FT813) bits for each R/G/B colour. A lower value means fewer bits are output for each channel allowing dithering on lower precision LCD displays.

REG_SWIZZLE controls the arrangement of the output colour pins, to help the PCB route different LCD panel arrangements. Bit 0 of the register causes the order of bits in each colour channel to be reversed. Bits 1-3 control the RGB order. Setting Bit 1 causes R and B channels to be swapped. Setting Bit 3 allows rotation to be enabled. If Bit 3 is set, then (R,G,B) is rotated right if bit 2 is one, or left if bit 2 is zero.

| REG_SWIZZLE | | | | PINS (FT810/FT811, 6 bits) | | | PINS (FT812/FT813, 8 bits) | | |
|-------------|----|----|----|----------------------------|---------------------------|---------------------------|---|---|---|
| b3 | b2 | b1 | b0 | R7, R6, R5, R4, R3, R2 | G7, G6, G5, G4, G3, G2 | B7, B6, B5, B4, B3, B2 | R7, R6, R5, R4, R3, R2, R1, R0 | G7, G6, G5, G4, G3, G2, G1, G0 | B7, B6, B5, B4, B3, B2, B1, B0 |
| 0 | X | 0 | 0 | R[7:2] | G[7:2] | B[7:2] | R[7:0] | G[7:0] | B[7:0] |
| 0 | X | 0 | 1 | R[2:7] | G[2:7] | B[2:7] | R[0:7] | G[0:7] | B[0:7] |
| 0 | X | 1 | 0 | B[7:2] | G[7:2] | R[7:2] | B[7:0] | G[7:0] | R[7:0] |
| 0 | X | 1 | 1 | B[2:7] | G[2:7] | R[2:7] | B[0:7] | G[0:7] | R[0:7] |

| | | | | | | | | | |
|---|---|---|---|--------|--------|--------|--------|--------|--------|
| 1 | 0 | 0 | 0 | B[7:2] | R[7:2] | G[7:2] | B[7:0] | R[7:0] | G[7:0] |
| 1 | 0 | 0 | 1 | B[2:7] | R[2:7] | G[2:7] | B[0:7] | R[0:7] | G[0:7] |
| 1 | 0 | 1 | 0 | G[7:2] | R[7:2] | B[7:2] | G[7:0] | R[7:0] | B[7:0] |
| 1 | 0 | 1 | 1 | G[2:7] | R[2:7] | B[2:7] | G[0:7] | R[0:7] | B[0:7] |
| 1 | 1 | 0 | 0 | G[7:2] | B[7:2] | R[7:2] | G[7:0] | B[7:0] | R[7:0] |
| 1 | 1 | 0 | 1 | G[2:7] | B[2:7] | R[2:7] | G[0:7] | B[0:7] | R[0:7] |
| 1 | 1 | 1 | 0 | R[7:2] | B[7:2] | G[7:2] | R[7:0] | B[7:0] | G[7:0] |
| 1 | 1 | 1 | 1 | R[2:7] | B[2:7] | G[2:7] | R[0:7] | B[0:7] | G[0:7] |

Table 4-12 REG_SWIZZLE RGB Pins Mapping

REG_HCYCLE, REG_HSIZE, REG_HOFFSET, REG_HSYNC0 and REG_HSYNC1 define the LCD horizontal timings. Each register has 12 bits to allow programmable range of 0-4095 PCLK cycles. REG_VCYCLE, REG_VSIZE, REG_VOFFSET, REG_VSYNC0 and REG_VSYNC1 define the LCD vertical timings. Each register has 12 bits to allow programmable range of 0-4095 lines.

| | Register | Display Parameter | Description |
|------------|-----------------|----------------------------|---|
| Horizontal | REG_HCYCLE | T_H | Total length of line (visible and non-visible) (in PCLKs) |
| | REG_HSIZE | T_{HD} | Length of visible part of line (in PCLKs) |
| | REG_HOFFSET | $T_{HF} + T_{HP} + T_{HB}$ | Length of non-visible part of line (in PCLK cycles) |
| | REG_HSYNC0 | T_{HF} | Horizontal Front Porch (in PCLK cycles) |
| | REG_HSYNC1 | $T_{HF} + T_{HP}$ | Horizontal Front Porch plus Hsync Pulse width (in PCLK cycles) |
| Vertical | REG_VCYCLE | T_V | Total number of lines (visible and non-visible) (in lines) |
| | REG_VSIZE | T_{VD} | Number of visible lines (in lines) |
| | REG_VOFFSET | $T_{VF} + T_{VP} + T_{VB}$ | Number of non-visible lines (in lines) |
| | REG_VSYNC0 | T_{VF} | Vertical Front Porch (in lines) |
| | REG_VSYNC1 | $T_{VF} + T_{VP}$ | Vertical Front Porch plus Vsync Pulse width (in lines) |

Table 4-13 Registers for RGB horizontal and vertical timings

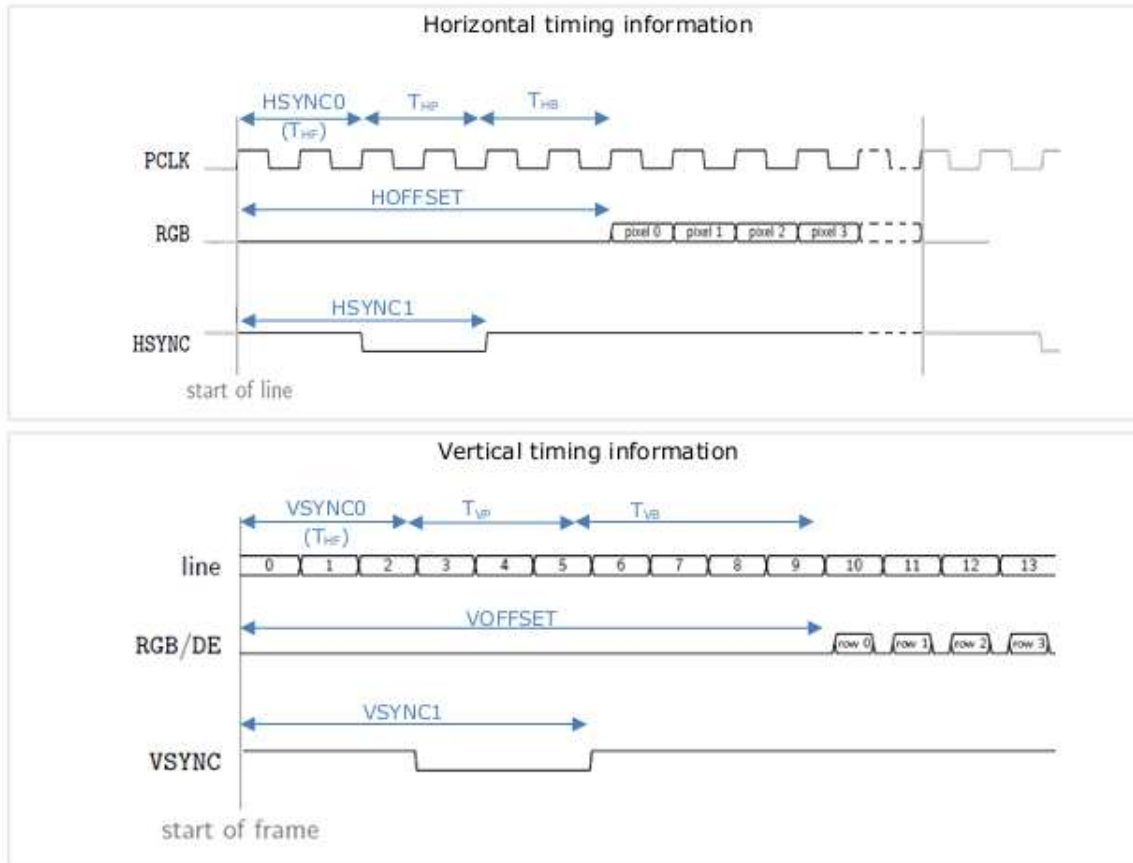


Figure 4-7 RGB timing waveforms

4.5 Miscellaneous Control

4.5.1 Backlight Control Pin

The backlight dimming control pin (BACKLIGHT) is a pulse width modulated (PWM) signal controlled by two registers: *REG_PWM_HZ* and *REG_PWM_DUTY*. *REG_PWM_HZ* specifies the PWM output frequency, the range is 250-10000 Hz. *REG_PWM_DUTY* specifies the duty cycle; the range is 0-128. A value of 0 means that the PWM is completely off and 128 means completely on.

The BACKLIGHT pin will output low when the DISP pin is not enabled (i.e. logic 0).

4.5.2 DISP Control Pin

The DISP pin is a general purpose output that can be used to enable, or reset the LCD display panel. The pin is controlled by writing to Bit 7 of the *REG_GPIO* register, or bit 15 of *REG_GPIOX*.

4.5.3 General Purpose IO pins

Depending on the package, the FT81x can be configured to use up to 4 GPIO pins. These GPIO pins are controlled by the *REG_GPIOX_DIR* and *REG_GPIOX* registers. Alternatively the GPIO0 and GPIO1 pins can also be controlled by *REG_GPIO_DIR* and *REG_GPIO* to maintain backward compatibility with the FT800/FT801.

When the QSPI is enabled in Quad mode, GPIO0/IO2 and GPIO1/IO3 pins are used as data lines of the QSPI.

4.5.4 Pins Drive Current Control

The output drive current of output pins can be changed as per the following table by writing to bit[6:2] of REG_GPIO register or bit[14:10] of REG_GPIOX register. Alternatively, use the SPI command PINDRIVE to change the individual pin drive strength.

| REG_GPIO | Bit[6:5] | | | | Bit[4] | | Bit[3:2] | | | |
|---------------|---|------|------|------|---|------|-------------------------------------|------|------|------|
| REG_GPIOX | Bit[14:13] | | | | Bit[12] | | Bit[11:10] | | | |
| Value | 00b# | 01b | 10b | 11b | 0b# | 1b | 00b# | 01b | 10b | 11b |
| Drive Current | 5mA | 10mA | 15mA | 20mA | 5mA | 10mA | 5mA | 10mA | 15mA | 20mA |
| Pins | GPIO0 GPIO1 GPIO2 GPIO3 CTP_RST_N | | | | PCLK DISP VSYNC HSYNC DE R7..R0 G7..G0 B7..B0 BACKLIGHT | | MISO MOSI IO2 IO3 INT_N | | | |

Table 4-14 Output drive current selection

Note: #Default value

4.6 Audio Engine

FT81x provides mono audio output through a PWM output pin, AUDIO_L. It outputs two audio sources, the sound synthesizer and audio file playback.

4.6.1 Sound Synthesizer

A sound processor, AUDIO ENGINE, generates the sound effects from a small ROM library of waves table. To play a sound effect listed in Table 4.3, load the REG_SOUND register with a code value and write 1 to the REG_PLAY register. The REG_PLAY register reads 1 while the effect is playing and returns a '0' when the effect ends. Some sound effects play continuously until interrupted or instructed to play the next sound effect. To interrupt an effect, write a new value to REG_SOUND and REG_PLAY registers; e.g. write 0 (Silence) to REG_SOUND and 1 to PEG_PLAY to stop the sound effect.

The sound volume is controlled by register REG_VOL_SOUND. The 16-bit REG_SOUND register takes an 8-bit sound in the low byte. For some sounds, marked "pitch adjust" in the table below, the high 8 bits contain a MIDI note value. For these sounds, a note value of zero indicates middle C. For other sounds the high byte of REG_SOUND is ignored.

| Value | Effect | Continuous | Pitch adjust |
|-------|---------|------------|--------------|
| 00h | Silence | Y | N |

| Value | Effect | Continuous | Pitch adjust |
|-------|--------|------------|--------------|
| 32h | DTMF 2 | Y | N |

| | | | | | | | |
|-----|---------------|---|---|-----|--------------|---|---|
| 01h | square wave | Y | Y | 33h | DTMF 3 | Y | N |
| 02h | sine wave | Y | Y | 34h | DTMF 4 | Y | N |
| 03h | sawtooth wave | Y | Y | 35h | DTMF 5 | Y | N |
| 04h | triangle wave | Y | Y | 36h | DTMF 6 | Y | N |
| 05h | Beeping | Y | Y | 37h | DTMF 7 | Y | N |
| 06h | Alarm | Y | Y | 38h | DTMF 8 | Y | N |
| 07h | Warble | Y | Y | 39h | DTMF 9 | Y | N |
| 08h | Carousel | Y | Y | 40h | harp | N | Y |
| 10h | 1 short pip | N | Y | 41h | xylophone | N | Y |
| 11h | 2 short pips | N | Y | 42h | tuba | N | Y |
| 12h | 3 short pips | N | Y | 43h | glockenspiel | N | Y |
| 13h | 4 short pips | N | Y | 44h | organ | N | Y |
| 14h | 5 short pips | N | Y | 45h | trumpet | N | Y |
| 15h | 6 short pips | N | Y | 46h | piano | N | Y |
| 16h | 7 short pips | N | Y | 47h | chimes | N | Y |
| 17h | 8 short pips | N | Y | 48h | music box | N | Y |
| 18h | 9 short pips | N | Y | 49h | bell | N | Y |
| 19h | 10 short pips | N | Y | 50h | click | N | N |
| 1Ah | 11 short pips | N | Y | 51h | switch | N | N |
| 1Bh | 12 short pips | N | Y | 52h | cowbell | N | N |
| 1Ch | 13 short pips | N | Y | 53h | notch | N | N |
| 1Dh | 14 short pips | N | Y | 54h | hihat | N | N |
| 1Eh | 15 short pips | N | Y | 55h | kickdrum | N | N |
| 1Fh | 16 short pips | N | Y | 56h | pop | N | N |
| 23h | DTMF # | Y | N | 57h | clack | N | N |
| 2Ch | DTMF * | Y | N | 58h | chack | N | N |
| 30h | DTMF 0 | Y | N | 60h | mute | N | N |
| 31h | DTMF 1 | Y | N | 61h | unmute | N | N |

Table 4-15 Sound Effect

| MIDI note | ANSI note | Freq (Hz) |
|-----------|-----------|-----------|
| 21 | A0 | 27.5 |
| 22 | A#0 | 29.1 |
| 23 | B0 | 30.9 |
| 24 | C1 | 32.7 |
| 25 | C#1 | 34.6 |
| 26 | D1 | 36.7 |
| 27 | D#1 | 38.9 |
| 28 | E1 | 41.2 |
| 29 | F1 | 43.7 |
| 30 | F#1 | 46.2 |
| 31 | G1 | 49.0 |
| 32 | G#1 | 51.9 |
| 33 | A1 | 55.0 |
| 34 | A#1 | 58.3 |
| 35 | B1 | 61.7 |
| 36 | C2 | 65.4 |
| 37 | C#2 | 69.3 |
| 38 | D2 | 73.4 |

| MIDI note | ANSI note | Freq (Hz) |
|-----------|-----------|-----------|
| 65 | F4 | 349.2 |
| 66 | F#4 | 370.0 |
| 67 | G4 | 392.0 |
| 68 | G#4 | 415.3 |
| 69 | A4 | 440.0 |
| 70 | A#4 | 466.2 |
| 71 | B4 | 493.9 |
| 72 | C5 | 523.3 |
| 73 | C#5 | 554.4 |
| 74 | D5 | 587.3 |
| 75 | D#5 | 622.3 |
| 76 | E5 | 659.3 |
| 77 | F5 | 698.5 |
| 78 | F#5 | 740.0 |
| 79 | G5 | 784.0 |
| 80 | G#5 | 830.6 |
| 81 | A5 | 880.0 |
| 82 | A#5 | 932.3 |

| | | | | | |
|----|-----|-------|-----|-----|--------|
| 39 | D#2 | 77.8 | 83 | B5 | 987.8 |
| 40 | E2 | 82.4 | 84 | C6 | 1046.5 |
| 41 | F2 | 87.3 | 85 | C#6 | 1108.7 |
| 42 | F#2 | 92.5 | 86 | D6 | 1174.7 |
| 43 | G2 | 98.0 | 87 | D#6 | 1244.5 |
| 44 | G#2 | 103.8 | 88 | E6 | 1318.5 |
| 45 | A2 | 110.0 | 89 | F6 | 1396.9 |
| 46 | A#2 | 116.5 | 90 | F#6 | 1480.0 |
| 47 | B2 | 123.5 | 91 | G6 | 1568.0 |
| 48 | C3 | 130.8 | 92 | G#6 | 1661.2 |
| 49 | C#3 | 138.6 | 93 | A6 | 1760.0 |
| 50 | D3 | 146.8 | 94 | A#6 | 1864.7 |
| 51 | D#3 | 155.6 | 95 | B6 | 1975.5 |
| 52 | E3 | 164.8 | 96 | C7 | 2093.0 |
| 53 | F3 | 174.6 | 97 | C#7 | 2217.5 |
| 54 | F#3 | 185.0 | 98 | D7 | 2349.3 |
| 55 | G3 | 196.0 | 99 | D#7 | 2489.0 |
| 56 | G#3 | 207.7 | 100 | E7 | 2637.0 |
| 57 | A3 | 220.0 | 101 | F7 | 2793.8 |
| 58 | A#3 | 233.1 | 102 | F#7 | 2960.0 |
| 59 | B3 | 246.9 | 103 | G7 | 3136.0 |
| 60 | C4 | 261.6 | 104 | G#7 | 3322.4 |
| 61 | C#4 | 277.2 | 105 | A7 | 3520.0 |
| 62 | D4 | 293.7 | 106 | A#7 | 3729.3 |
| 63 | D#4 | 311.1 | 107 | B7 | 3951.1 |
| 64 | E4 | 329.6 | 108 | C8 | 4186.0 |

Table 4-16 MIDI Note Effect

4.6.2 Audio Playback

The FT81x can play back recorded sound through its audio output. To do this, load the original sound data into the FT81x's RAM, and set registers to start the playback.

The registers controlling audio playback are:

| | |
|----------------------|---|
| REG_PLAYBACK_START: | the start address of the audio data |
| REG_PLAYBACK_LENGTH: | the length of the audio data, in bytes |
| REG_PLAYBACK_FREQ: | the playback sampling frequency, in Hz |
| REG_PLAYBACK_FORMAT: | the playback format, one of LINEAR SAMPLES, uLAW SAMPLES, or ADPCM SAMPLES |
| REG_PLAYBACK_LOOP: | if zero, the sample is played once. If one, the sample is repeated indefinitely |
| REG_PLAYBACK_PLAY: | a write to this location triggers the start of audio playback, regardless of writing '0' or '1'. Read back '1' when playback is ongoing, and '0' when playback finishes |
| REG_VOL_PB: | playback volume, 0-255 |

The mono audio formats supported are 8-bits PCM, 8-bits uLAW and 4-bits IMA-ADPCM. For ADPCM_SAMPLES, each sample is 4 bits, so two samples are packed per byte, the first sample is in bits 0-3 and the second is in bits 4-7.

The current audio playback read pointer can be queried by reading the REG_PLAYBACK_READPTR. Using a large sample buffer, looping, and this read pointer, the host MPU/MCU can supply a continuous stream of audio.

4.7 Touch-Screen Engine

The FT81x touch-screen engine supports both resistive and capacitive touch panels. FT810 and FT812 support resistive touch, while FT811 and FT813 support capacitive touch.

4.7.1 Resistive Touch Control

The resistive touch-screen consists of a touch screen engine, ADC, Axis-switches, and ADC input multiplexer. The touch screen engine reads commands from the memory map register and generates the required control signals to the axis-switches and inputs mux and ADC. The ADC data are acquired, processed and updated in the respective register for the MPU/MCU to read.

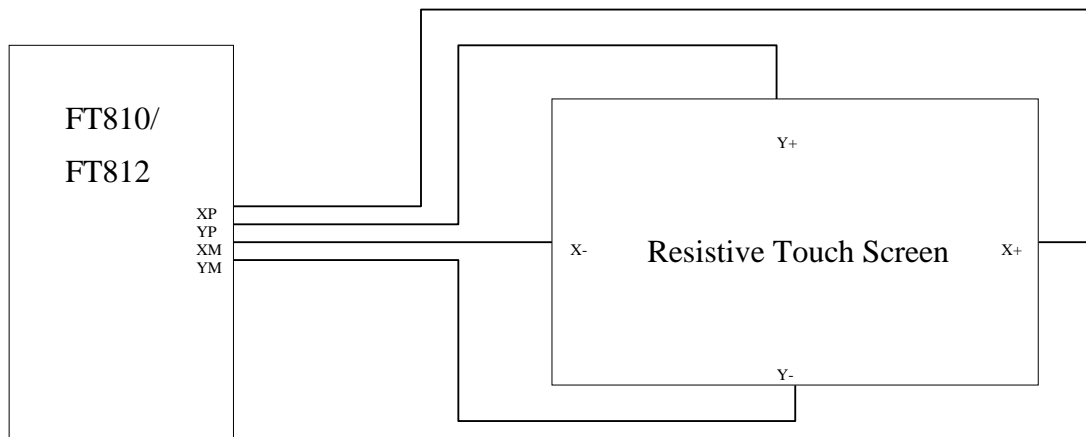


Figure 4-8 Resistive Touch screen connection

The host controls the TOUCH SCREEN ENGINE operation mode by writing the REG_TOUCH_MODE.

| REG_TOUCH_MODE | Mode | Description |
|----------------|------------|---|
| 0 | OFF | Acquisition stopped, only touch detection interrupt is still valid. |
| 1 | ONE-SHOT | Perform acquisition once every time the MPU writes '1' to REG_TOUCH_MODE. |
| 2 | FRAME-SYNC | Perform acquisition for every frame sync (~60 data acquisition/second). |
| 3 | CONTINUOUS | Perform acquisition continuously at approximately 1000 data acquisition / second. |

Table 4-17 Resistive Touch Controller Operating Mode

The Touch Screen Engine captures the raw X and Y coordinate and writes to register REG_TOUCH_RAW XY. The range of these values is 0-1023. If the touch screen is not being pressed, both registers read 65535 (FFFFh).

These touch values are transformed into screen coordinates using the matrix in registers REG_TOUCH_TRANSFORM_A-F. The post-transform coordinates are available in register REG_TOUCH_SCREEN_XY. If the touch screen is not being pressed, both registers read -32768 (8000h). The values for REG TOUCH TRANSFORM A-F may be computed using an on-screen calibration process.

If the screen is being touched, the screen coordinates are looked up in the screen's tag buffer, delivering a final 8-bit tag value, in REG TOUCH TAG. Because the tag lookup takes a full frame, and touch coordinates change continuously, the original (x; y) used for the tag lookup is also available in REG_TOUCH_TAG_XY.

Screen touch pressure is available in REG_TOUCH_RZ. The value is relative to the resistance of the touch contact, a lower value indicates more pressure. The register defaults to 32767 when touch is not detected. The REG_TOUCH_THRESHOLD can be set to accept a touch only when the force threshold is exceeded.

4.7.2 Capacitive Touch Control

The Capacitive Touch Screen Engine (CTSE) of the FT81x communicates with the external capacitive touch panel module (CTPM) through an I²C interface. The CTPM will assert its interrupt line when there is a touch detected. Upon detecting CTP_INT_N line active, the FT81x will read the touch data through I²C. Up to 5 touches can be reported and stored in FT81x registers.

For a supported CTPM list please consult FTDI website.

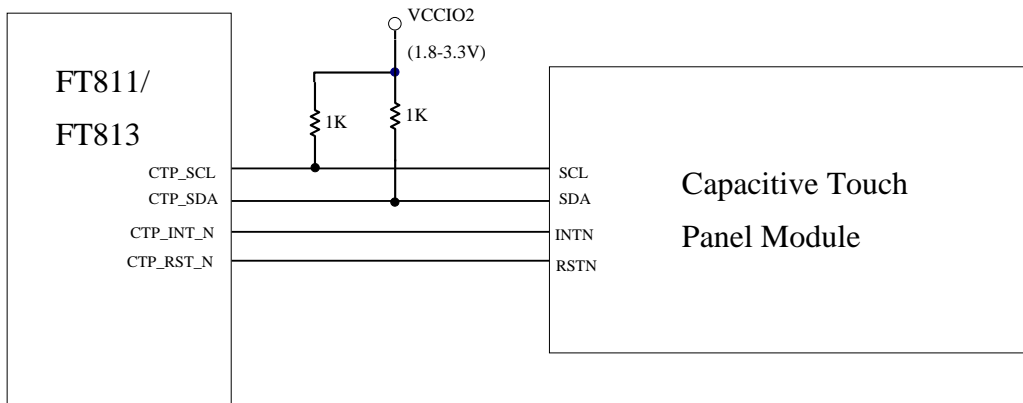


Figure 4-9 Touch screen connection

The host controls the CTSE operation mode by writing the REG_CTOUCH_MODE.

| REG_CTOUCH_MODE | Mode | Description |
|-----------------|------------|---|
| 0 | OFF | Acquisition stopped |
| 1-2 | Reserved | Reserved |
| 3 | CONTINUOUS | Perform acquisition continuously at the reporting rate of the connected CTPM. |

Table 4-18 Capacitive Touch Controller Operating Mode

The FT81x CTSE supports compatibility mode and extended mode. By default the CTSE runs in compatibility mode where the touch system provides an interface very similar to the resistive touch engine. In this mode the same application code can run on FT810/FT812 and FT811/FT813 without alteration. In extended mode, the touch register meanings are modified, and a second set of registers are exposed. These allow multi-touch detection (up to 5 touches).

4.7.3 Compatibility mode

The CTSE reads the X and Y coordinates from the CTPM and writes to register REG_CTOUCH_RAW_XY. If the touch screen is not being pressed, both registers read 65535 (FFFFh).

These touch values are transformed into screen coordinates using the matrix in registers REG_CTOUCH_TRANSFORM_A-F. The post-transform coordinates are available in register REG_CTOUCH_SCREEN_XY. If the touch screen is not being pressed, both registers read -32768 (8000h). The values for REG_CTOUCH_TRANSFORM_A-F may be computed using an on-screen calibration process.

If the screen is being touched, the screen coordinates are looked up in the screen's tag buffer, delivering a final 8-bit tag value, in REG_TOUCH_TAG. Because the tag lookup takes a full frame, and touch coordinates change continuously, the original (x; y) used for the tag lookup is also available in REG_TOUCH_TAG_XY.

4.7.4 Extended mode

Setting REG_CTOUCH_EXTENDED to 1b'0 enables extended mode. In extended mode a new set of readout registers are available, allowing gestures and up to five touches to be read. There are two classes of registers: control registers and status registers. Control registers are written by the MCU. Status registers can be read out by the MCU and the FT81x's hardware tag system.

The five touch coordinates are packed in REG_CTOUCH_TOUCH0_XY, REG_CTOUCH_TOUCH1_XY, REG_CTOUCH_TOUCH2_XY, REG_CTOUCH_TOUCH3_XY, REG_CTOUCH4_X and REG_CTOUCH4_Y.

Coordinates stored in these registers are signed 16-bit values, so have range -32768 to 32767. The no-touch condition is indicated by x=y= -32768. These coordinates are already transformed into screen coordinates based on the raw data read from the CTPM, using the matrix in registers REG_CTOUCH_TRANSFORM_A-F. To obtain raw (x,y) coordinates read from CTPM, the user sets the REG_CTOUCH_TRANSFORM_A-F registers to the identity matrix.

The FT81x tag mechanism is implemented by hardware, where up to 5 tags can be looked up.

4.7.5 Short-circuit protection

For resistive touch it is useful to protect the chip from permanent damage due to potential short-circuits on the 4 XY lines. When a short circuit on the touch screen happens, the FT81x can detect it and stop the touch detection operation, leaving the 4 XY pins in the high impedance state.

The short-circuit protection can be enabled/disabled by the REG_TOUCH_CONFIG.

4.7.6 Capacitive touch configuration

On capacitive touch system some users may need to adjust the CTPM default values, such as the registers affecting touch sensitivity. To do this the following sequence shall be executed once after chip reset:

- Hold the touch engine in reset (set REG_CPURESET = 2)
- Write the CTPM configure register address and value to FT81x designated memory location
- Up to 10 register address/value can be added
- Release the touch engine reset (set REG_CPURESET = 0)

The CTPM can be enabled in low power state when the touch function is not required by the application. Setting the low-power bit in REG_TOUCH_CONFIG will enable the low power mode of the CTPM. When the low-power bit is cleared, the FT81x touch engine will send a reset to the CTPM, thus re-enabling the touch detection function.

4.7.7 Touch detection in none-ACTIVE state

When FT81x is in none-ACTIVE state, a touch event can still be detected and reported to the host through the INT_N pin. In other words, a touch event can wake-up the host if needed.

For resistive touch, the INT_N pin will be asserted low when the screen is touched, regardless of the setting of the interrupt registers. This will happen when the FT81x is in STANDBY or SLEEP state, but not in POWERDOWN state.

For capacitive touch, the INT_N pin will follow CTP_INT_N pin when the FT81x is in STANDBY, SLEEP or POWERDOWN state.

4.8 Power Management

4.8.1 Power supply

The FT81x may be operated with a single supply of 3.3V applied to VCC and VCCIO pins. For operation with a host MPU/MCU at a lower supply, connect the VCCIO1 to the MPU IO supply to match the interface voltage. For operation with LCD/touch panels at lower voltages, connect the VCCIO2 to the LCD/touch IO supply.

| Symbol | Typical | Description |
|---------|------------------------|--|
| VCCIO1 | 1.8V, or 2.5V, or 3.3V | Supply for Host interface digital I/O pins |
| VCCIO2 | 1.8V, or 2.5V, or 3.3V | Supply for RGB and touch interface I/O pins |
| VCC | 3.3V | Supply for 3.3V circuits and internal regulator |
| VOUT1V2 | 1.2V | Supply for digital core. Generated by internal regulator |

Table 4-19 Power supply

4.8.2 Internal Regulator and POR

The internal regulator provides power to the core circuit. A 47kΩ resistor is recommended to pull the PD_N pin up to VCCIO1, together with a 100nF capacitor to ground in order to delay the internal regulator powering up after the VCC and VCCIO are stable.

The internal regulator requires a compensation capacitor to be stable. A typical design requires a 4.7uF capacitor between the VOUT1V2 and GND pins. Do not connect any other load to the VOUT1V2 pin.

The internal regulator will generate a Power-On-Reset (POR) pulse when the output voltage rises above the POR threshold. The POR will reset all the core digital circuits.

It is possible to use PD_N pin as an asynchronous hardware reset input. Drive PD_N low for at least 5ms and then drive it high will reset the FT81x chip.

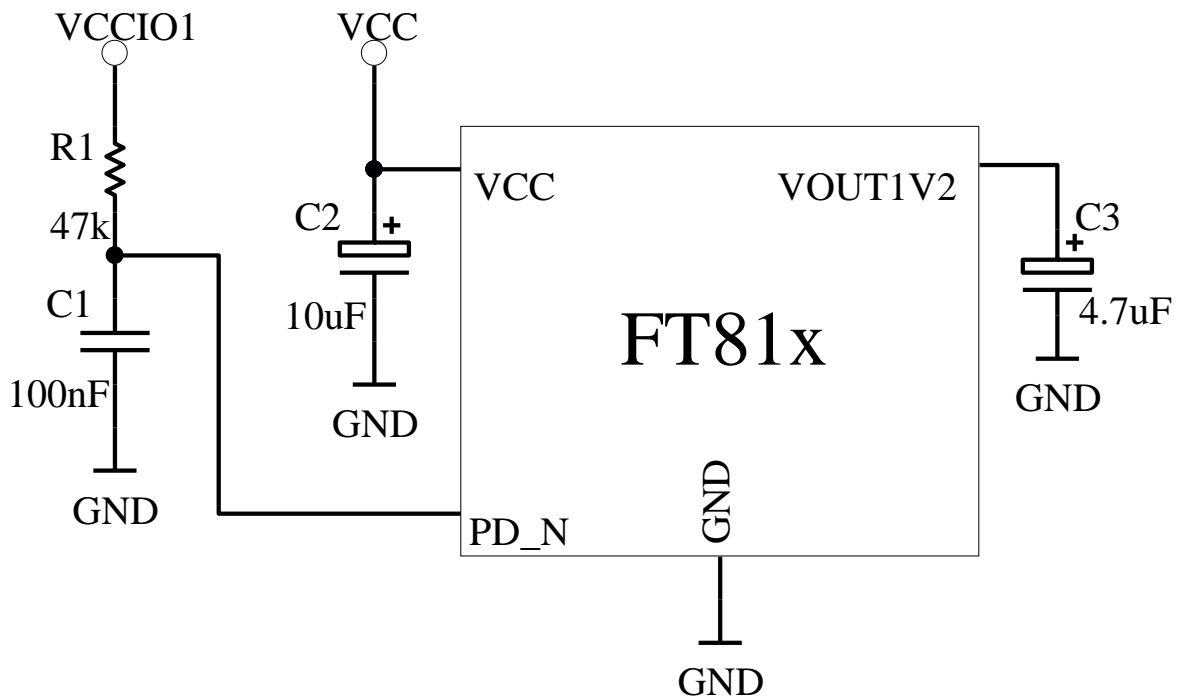


Figure 4-10 Internal regulator

4.8.3 Power Modes

When the supply to VCCIO and VCC is applied, the internal regulator is powered by VCC. An internal POR pulse will be generated during the regulator power up until it is stable. After the initial power up, the FT81x will stay in the SLEEP state. When needed, the host can set the FT81x to the ACTIVE state by performing a SPI ACTIVE command. The graphics engine, the audio engine and the touch engine are only functional in the ACTIVE state. To save power the host can send a command to put the FT81x into any of the low power modes: STANDBY, SLEEP and POWERDOWN. In addition, the host is allowed to put the FT81x in POWERDOWN mode by driving the PD_N pin to low, regardless of what state it is currently in. Refer to Figure 4-11 for the power state transitions.

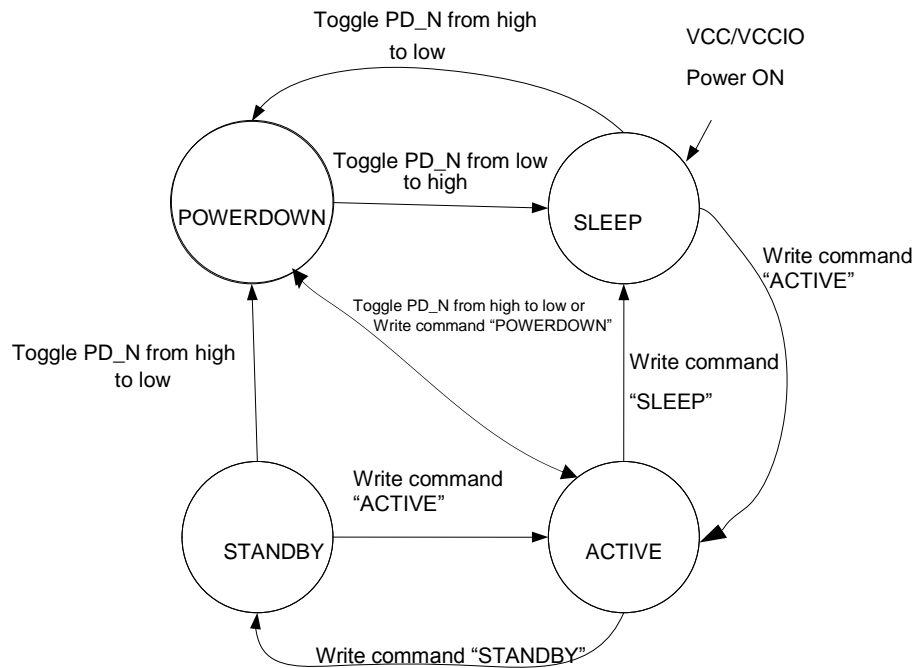


Figure 4-11 Power State Transition

4.8.3.1 ACTIVE state

In ACTIVE state, the FT81x is in normal operation. The clock oscillator and PLL are functioning. The system clock applied to the FT81x core engines is enabled.

4.8.3.2 STANDBY state

In STANDBY state, the clock oscillator and PLL remain functioning; the system clock applied to the FT81x core engines is disabled. All register contents are retained.

4.8.3.3 SLEEP state

In SLEEP state, the clock oscillator, PLL and system clock applied to the FT81x core engines are disabled. All register contents are retained.

4.8.3.4 POWERDOWN state

In POWERDOWN state, the clock oscillator, the PLL and the system clock applied to the FT81x core is disabled. The core engines are powered down while the SPI interface for host commands remains functional. All register contents are lost and reset to default when the chip is next switched on. The internal regulator remains on.

4.8.3.5 Wake up to ACTIVE from other power states

When in the POWER DOWN state, if the device enters this state via an SPI command, then only the SPI ACTIVE command will bring the device back to the ACTIVE state, provided PD_N pin is also high. However, if PD_N is used instead, then making PD_N high followed by a SPI ACTIVE command will wake up the device. Upon exiting this state, the device will perform a global reset, and will go through the same power up sequence. All settings from SPI commands will be reset except those that pertain to pin states during power down. The clock enable sequence mentioned in section 4.2.3 shall be executed to properly select and enable the system clock.

From the SLEEP state, the host MPU sends an SPI ACTIVE command to wake the FT81x into the ACTIVE state. The host needs to wait for at least 20ms before accessing any registers or commands. This is to guarantee the clock oscillator and PLL are up and stable.

From the STANDBY state, the host MPU sends SPI ACTIVE command to wake the FT81x into the ACTIVE state. The host can immediately access any register or command.

4.8.4 Reset and boot-up sequence

There are a few hardware and software reset events which can be triggered to reset the FT81x.

Hardware reset events:

- Power-on-Reset(POR)
- Toggle the PD_N pin

Software reset events:

- SPI command RST_PULSE
- SPI command to switch between the internal clock and the external clock
- SPI command to enter POWERDOWN then wakeup

After reset the FT81x will be in the SLEEP state. Upon receiving an SPI ACTIVE command, the internal oscillator and PLL will start up. Once the clock is stable, the chip will check and repair its internal RAM, running the configuration and release the clock to the system. The chip will exit the reset and boot-up state and enter into normal operations. The boot-up may take up to 300ms to complete.

4.8.5 Pin Status at Different Power States

The FT81x pin status depends on the power state of the chip. See the following table for more details. At the power transition from ACTIVE to STANDBY or ACTIVE to SLEEP, all pins retain their previous status. The software needs to set AUDIO_L, BACKLIGHT to a known state before issuing power transition commands.

The pin status in the power down state can be changed by SPI command PIN_PD_STATE.

| Pin Name | Default Drive | Reset | Normal | Power Down (Default) |
|----------|---------------|--------------------------|--------|----------------------|
| AUDIO_L | 20mA | Out, Float | Out | Pull Low |
| SCK | - | In | In | In |
| MISO | 5mA | Out, Float (CS_N = 1) | IO | Out, Float |
| MOSI | 5mA | In | IO | In |
| CS_N | - | In | In | In |
| IO2 | 5mA | In | IO | Float |
| GPIO0 | 5mA | In | IO | Float |
| IO3 | 5mA | In | IO | Float |
| GPIO1 | 5mA | In | IO | Float |
| GPIO2 | 5mA | In | IO | Float |

| Pin Name | Default Drive | Reset | Normal | Power Down (Default) |
|-----------|---------------|-----------------------|-----------------------|-----------------------|
| INT_N | 5mA | OD, Float | OD / Out | Float |
| PD_N | - | In | In | In |
| GPIO3 | 5mA | In | IO | Float |
| X1/CLK | - | In | In | In |
| XP | - | IO, Float | IO | Float |
| YP | - | IO, Float | IO | Float |
| XM | - | IO, Float | IO | Float |
| YM | - | IO, Float | IO | Float |
| CTP_RST_N | 5mA | Out | Out | Pull Low |
| CTP_INT_N | - | In (internal pull-up) | In (internal pull-up) | In (internal pull-up) |
| CTP_SCL | 20mA | OD | IO | Float |
| CTP_SDA | 20mA | OD | IO | Float |
| BACKLIGHT | 5mA | Out | Out | Pull Low |
| DE | 5mA | Out | Out | Pull Low |
| VSYNC | 5mA | Out | Out | Pull Low |
| HSYNC | 5mA | Out | Out | Pull Low |
| DISP | 5mA | Out | Out | Pull Low |
| PCLK | 5mA | Out | Out | Pull Low |
| R/G/B | 5mA | Out | Out | Pull Low |

Table 4-20 Pin Status

5 Memory Map

All memory and registers in the FT81x core are memory mapped in 22-bit address space with a 2-bit SPI command prefix. Prefix 0'b00 for read and 0'b10 for write to the address space, 0'b01 is reserved for Host Commands and 0'b11 undefined. The following are the memory space definition.

| Start Address | End Address | Size | NAME | Description |
|---------------|-------------|---------|---------------|------------------------------|
| 00 0000h | 0F FFFFh | 1024 kB | RAM_G | General purpose graphics RAM |
| 1E 0000h | 2F FFFBh | 1152 kB | ROM_FONT | Font table and bitmap |
| 2F FFFCh | 2F FFFFh | 4 B | ROM_FONT_ADDR | Font table pointer address |
| 30 0000h | 30 1FFFh | 8 kB | RAM_DL | Display List RAM |
| 30 2000h | 30 2FFFh | 4 kB | RAM_REG | Registers |
| 30 8000h | 30 8FFFh | 4 kB | RAM_CMD | Command buffer |

Table 5-1 FT81x Memory Map

Note 1: The addresses beyond this table are reserved and shall not be read or written unless otherwise specified.

5.1 Registers

The table **Error! Reference source not found.** shows the complete list of the FT81x registers. Refer to [FT81x_Series_Programmers_Guide](#), Chapter 2 for details of the register function.

| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---------------|----------------|------|-----|-------------|---|
| 302000h | REG_ID | 8 | r/o | 7Ch | Identification register, always reads as 7Ch |
| 302004h | REG_FRAMES | 32 | r/o | 0 | Frame counter, since reset |
| 302008h | REG_CLOCK | 32 | r/o | 0 | Clock cycles, since reset |
| 30200Ch | REG_FREQUENCY | 28 | r/w | 60000000 | Main clock frequency (Hz) |
| 302010h | REG_RENDERMODE | 1 | r/w | 0 | Rendering mode: 0 = normal, 1 = single-line |
| 302014h | REG_SNAPY | 11 | r/w | 0 | Scanline select for RENDERMODE 1 |
| 302018h | REG_SNAPSHOT | 1 | r/w | - | Trigger for RENDERMODE 1 |
| 30201Ch | REG_SNAPFORMAT | 6 | r/w | 20h | Pixel format for scanline readout |
| 302020h | REG_CPURESET | 3 | r/w | 2 | Graphics, audio and touch engines reset control. Bit2: audio, bit1: touch, bit0: graphics |
| 302024h | REG_TAP_CRC | 32 | r/o | - | Live video tap crc. Frame CRC is computed every DL SWAP. |

| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---------------|---------------|------|-----|-------------|---|
| 302028h | REG_TAP_MASK | 32 | r/w | FFFFFFFh | Live video tap mask |
| 30202Ch | REG_HCYCLE | 12 | r/w | 224h | Horizontal total cycle count |
| 302030h | REG_HOFFSET | 12 | r/w | 02Bh | Horizontal display start offset |
| 302034h | REG_HSIZE | 12 | r/w | 1E0h | Horizontal display pixel count |
| 302038h | REG_HSYNC0 | 12 | r/w | 000h | Horizontal sync fall offset |
| 30203Ch | REG_HSYNC1 | 12 | r/w | 029h | Horizontal sync rise offset |
| 302040h | REG_VCYCLE | 12 | r/w | 124h | Vertical total cycle count |
| 302044h | REG_VOFFSET | 12 | r/w | 00Ch | Vertical display start offset |
| 302048h | REG_VSIZE | 12 | r/w | 110h | Vertical display line count |
| 30204Ch | REG_VSYNC0 | 10 | r/w | 000h | Vertical sync fall offset |
| 302050h | REG_VSYNC1 | 10 | r/w | 00Ah | Vertical sync rise offset |
| 302054h | REG_DLSWAP | 2 | r/w | 0 | Display list swap control |
| 302058h | REG_ROTATE | 3 | r/w | 0 | Screen rotation control. Allow normal/mirrored/inverted for landscape or portrait orientation. |
| 30205Ch | REG_OUTBITS | 9 | r/w | 1B6h/000h | Output bit resolution, 3 bits each for R/G/B. Default is 6/6/6 bits for FT810/FT811, and 8/8/8 bits for FT812/FT813 (0b'000 means 8 bits) |
| 302060h | REG_DITHER | 1 | r/w | 1 | Output dither enable |
| 302064h | REG_SWIZZLE | 4 | r/w | 0 | Output RGB signal swizzle |
| 302068h | REG_CSPREAD | 1 | r/w | 1 | Output clock spreading enable |
| 30206Ch | REG_PCLK_POL | 1 | r/w | 0 | PCLK polarity: 0 = output on PCLK rising edge, 1 = output on PCLK falling edge |
| 302070h | REG_PCLK | 8 | r/w | 0 | PCLK frequency divider, 0 = disable |
| 302074h | REG_TAG_X | 11 | r/w | 0 | Tag query X coordinate |
| 302078h | REG_TAG_Y | 11 | r/w | 0 | Tag query Y coordinate |
| 30207Ch | REG_TAG | 8 | r/o | 0 | Tag query result |
| 302080h | REG_VOL_PB | 8 | r/w | FFh | Volume for playback |
| 302084h | REG_VOL_SOUND | 8 | r/w | FFh | Volume for synthesizer sound |
| 302088h | REG_SOUND | 16 | r/w | 0 | Sound effect select |
| 30208Ch | REG_PLAY | 1 | r/w | 0h | Start effect playback |

| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|-------------------|---|------|-----|-------------|---|
| 302090h | REG_GPIO_DIR | 8 | r/w | 80h | Legacy GPIO pin direction, 0 = input , 1 = output |
| 302094h | REG_GPIO | 8 | r/w | 00h | Legacy GPIO read/write |
| 302098h | REG_GPIOX_DIR | 16 | r/w | 8000h | Extended GPIO pin direction, 0 = input , 1 = output |
| 30209Ch | REG_GPIOX | 16 | r/w | 0080h | Extended GPIO read/write |
| 3020A0h-3020A4h | Reserved | - | - | - | Reserved |
| 3020A8h | REG_INT_FLAGS | 8 | r/o | 00h | Interrupt flags, clear by read |
| 3020Ach | REG_INT_EN | 1 | r/w | 0 | Global interrupt enable, 1=enable |
| 3020B0h | REG_INT_MASK | 8 | r/w | FFh | Individual interrupt enable, 1=enable |
| 3020B4h | REG_PLAYBACK_START | 20 | r/w | 0 | Audio playback RAM start address |
| 3020B8h | REG_PLAYBACK_LENGTH | 20 | r/w | 0 | Audio playback sample length (bytes) |
| 3020BCh | REG_PLAYBACK_READPTR | 20 | r/o | - | Audio playback current read pointer |
| 3020C0h | REG_PLAYBACK_FREQ | 16 | r/w | 8000 | Audio playback sampling frequency (Hz) |
| 3020C4h | REG_PLAYBACK_FORMAT | 2 | r/w | 0 | Audio playback format |
| 3020C8h | REG_PLAYBACK_LOOP | 1 | r/w | 0 | Audio playback loop enable |
| 3020CCh | REG_PLAYBACK_PLAY | 1 | r/w | 0 | Start audio playback |
| 3020D0h | REG_PWM_HZ | 14 | r/w | 250 | BACKLIGHT PWM output frequency (Hz) |
| 3020D4h | REG_PWM_DUTY | 8 | r/w | 128 | BACKLIGHT PWM output duty cycle 0=0%, 128=100% |
| 3020D8h | REG_MACRO_0 | 32 | r/w | 0 | Display list macro command 0 |
| 3020DCh | REG_MACRO_1 | 32 | r/w | 0 | Display list macro command 1 |
| 3020E0h – 3020F4h | Reserved | - | - | - | Reserved |
| 3020F8h | REG_CMD_READ | 12 | r/w | 0 | Command buffer read pointer |
| 3020FCh | REG_CMD_WRITE | 12 | r/o | 0 | Command buffer write pointer |
| 302100h | REG_CMD_DL | 13 | r/w | 0 | Command display list offset |
| 302104h | REG_TOUCH_MODE | 2 | r/w | 3 | Touch-screen sampling mode |
| 302108h | REG_TOUCH_ADC_MODE REG_CTOUCH_EXTENDED | 1 | r/w | 1 | Set Touch ADC mode Set capacitive touch operation mode: 0: extended mode (multi-touch) 1: FT800 compatibility mode (single |

| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---------------|---|------|-----|-------------|--|
| | | | | | touch). |
| 30210Ch | REG_TOUCH_CHARGE | 16 | r/w | 9000 | Touch charge time, units of 6 clocks |
| 302110h | REG_TOUCH_SETTLE | 4 | r/w | 3 | Touch settle time, units of 6 clocks |
| 302114h | REG_TOUCH_OVERSAMPLE | 4 | r/w | 7 | Touch oversample factor |
| 302118h | REG_TOUCH_RZTHRESH | 16 | r/w | FFFFh | Touch resistance threshold |
| 30211Ch | REG_TOUCH_RAW_XY REG_CTOUCH_TOUCH1_XY | 32 | r/o | - | Compatibility mode: touch-screen raw (x-MSB16; y-LSB16) Extended mode: touch-screen screen data for touch 1 (x-MSB16; y-LSB16) |
| 302120h | REG_TOUCH_RZ REG_CTOUCH_TOUCH4_Y | 16 | r/o | - | Compatibility mode: touch-screen resistance Extended mode: touch-screen screen Y data for touch 4 |
| 302124h | REG_TOUCH_SCREEN_XY REG_CTOUCH_TOUCH0_XY | 32 | r/o | - | Compatibility mode: touch-screen screen (x-MSB16; y-LSB16) Extended mode: touch-screen screen data for touch 0 (x-MSB16; y-LSB16) |
| 302128h | REG_TOUCH_TAG_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 0 lookup |
| 30212Ch | REG_TOUCH_TAG | 8 | r/o | - | Touch-screen tag result 0 |
| 302130h | REG_TOUCH_TAG1_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 1 lookup |
| 302134h | REG_TOUCH_TAG1 | 8 | r/o | - | Touch-screen tag result 1 |
| 302138h | REG_TOUCH_TAG2_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 2 lookup |
| 30213Ch | REG_TOUCH_TAG2 | 8 | r/o | - | Touch-screen tag result 2 |
| 302140h | REG_TOUCH_TAG3_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 3 lookup |
| 302144h | REG_TOUCH_TAG3 | 8 | r/o | - | Touch-screen tag result 3 |
| 302148h | REG_TOUCH_TAG4_XY | 32 | r/o | - | Touch-screen screen (x-MSB16; y-LSB16) used for tag 4 lookup |
| 30214Ch | REG_TOUCH_TAG4 | 8 | r/o | - | Touch-screen tag result 4 |
| 302150h | REG_TOUCH_TRANSFORM_A | 32 | r/w | 00010000h | Touch-screen transform coefficient (s15.16) |

| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|---------------|-----------------------|------|-----|--|--|
| 302154h | REG_TOUCH_TRANSFORM_B | 32 | r/w | 00000000h | Touch-screen transform coefficient (s15.16) |
| 302158h | REG_TOUCH_TRANSFORM_C | 32 | r/w | 00000000h | Touch-screen transform coefficient (s15.16) |
| 30215Ch | REG_TOUCH_TRANSFORM_D | 32 | r/w | 00000000h | Touch-screen transform coefficient (s15.16) |
| 302160h | REG_TOUCH_TRANSFORM_E | 32 | r/w | 00010000h | Touch-screen transform coefficient (s15.16) |
| 302164h | REG_TOUCH_TRANSFORM_F | 32 | r/w | 00000000h | Touch-screen transform coefficient (s15.16) |
| 302168h | REG_TOUCH_CONFIG | 16 | r/w | 8381h(FT810/FT812) 0381h(FT811/FT813) | Touch configuration. RTP/CTP select RTP: short-circuit, sample clocks CTP: I2C address, CTPM type, low-power mode |
| 30216Ch | REG_CTOUCH_TOUCH4_X | 16 | r/o | - | Extended mode: touch-screen screen X data for touch 4 |
| 302170h | Reserved | - | - | - | Reserved |
| 302174h | REG_BIST_EN | 1 | r/w | 0 | BIST memory mapping enable |
| 302178h | Reserved | - | - | - | Reserved |
| 30217Ch | Reserved | - | - | - | Reserved |
| 302180h | REG_TRIM | 8 | r/w | 0 | Internal relaxation clock trimming |
| 302184h | REG_ANA_COMP | 8 | r/w | 0 | Analogue control register |

| Address (hex) | Register Name | Bits | r/w | Reset value | Description |
|-----------------|---|------|-----|-------------|--|
| 302188h | REG_SPI_WIDTH | 3 | r/w | 0 | QSPI bus width setting Bit [2]: extra dummy cycle on read Bit [1:0]: bus width (0=1-bit, 1=2-bit, 2=4-bit) |
| 30218Ch | REG_TOUCH_DIRECT_XY REG_CTOUCH_TOUCH2_XY | 32 | r/o | - | Compatibility mode: Touch screen direct (x-MSB16; y-LSB16) conversions Extended mode: touch-screen screen data for touch 2 (x-MSB16; y-LSB16) |
| 302190h | REG_TOUCH_DIRECT_Z1Z2 REG_CTOUCH_TOUCH3_XY | 32 | r/o | - | Compatibility mode: Touch screen direct (z1-MSB16; z2-LSB16) conversions Extended mode: touch-screen screen data for touch 3 (x-MSB16; y-LSB16) |
| 302194h-302560h | Reserved | - | - | - | Reserved |
| 302564h | REG_DATESTAMP | 128 | r/o | - | Stamp date code |
| 302574h | REG_CMDB_SPACE | 12 | r/w | FFCh | Command DL (bulk) space available |
| 302578h | REG_CMDB_WRITE | 32 | w/o | 0 | Command DL (bulk) write |

Table 5-2 Overview of FT81x Registers

Note: All register addresses are 4-byte aligned. The value in the "Bits" column refers to the number of valid bits from bit 0 unless otherwise specified; other bits are reserved.

5.2 Chip ID

The FT81x Chip ID can be read at memory location 0C0000h – 0C0003h. The reset values of these bytes are:

- 0C0000h: 08h
- 0C0001h: 10h (FT810), 11h(FT811), 12h(FT812), 13h(FT813)
- 0C0002h: 01h
- 0C0003h: 00h

Note that the Chip ID location can be over-written by software.

6 Devices Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT81x device are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

| Parameter | Value | Unit |
|---|---|-------|
| Storage Temperature | -65 to +150 | °C |
| Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity) | 168 (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)* | Hours |
| Ambient Temperature (Power Applied) | -40 to +85 | °C |
| VCC Supply Voltage | 0 to +4 | V |
| VCCIO Supply Voltage | 0 to +4 | V |
| DC Input Voltage | -0.5 to + (VCCIO + 0.3) | V |

Table 6-1 Absolute Maximum Ratings

* If the devices are stored out of the packaging, beyond this time limit, the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

6.2 ESD and Latch-up Specifications

| Description | Specification |
|----------------------------------|----------------------------|
| Human Body Mode (HBM) | > ± 2kV |
| Machine mode (MM) | > ± 200V |
| Charged Device Mode (CDM) | > ± 500V |
| <u>Latch-up</u> | <u>> ± 200mA</u> |

Table 6-2 ESD and Latch-Up Specifications

6.3 DC Characteristics

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-------------------|--------------------------------|---------|---------|---------|-------|------------------|
| VCCIO1/ VCCIO2 | VCCIO operating supply voltage | 1.62 | 1.80 | 1.98 | V | Normal Operation |
| | | 2.25 | 2.50 | 2.75 | V | |

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------|------------------------------|---------|---------|---------|-------|------------------|
| | | 2.97 | 3.30 | 3.63 | V | |
| VCC | VCC operating supply voltage | 2.97 | 3.30 | 3.63 | V | Normal Operation |
| Icc1 | Power Down current | - | 0.17 | - | mA | Power down mode |
| Icc2 | Sleep current | - | 0.76 | - | mA | Sleep Mode |
| Icc3 | Standby current | - | 1.8 | - | mA | Standby Mode |
| Icc4 | Operating current | - | 22 | - | mA | Normal Operation |

Table 6-3 Operating Voltage and Current

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------|----------------------------------|-----------|---------|---------|-------|------------------|
| Voh | Output Voltage High | VCCIO-0.4 | - | - | V | Ioh=5mA |
| Vol | Output Voltage Low | - | - | 0.4 | V | Iol=5mA |
| Vih | Input High Voltage | 2.0 | - | - | V | |
| Vil | Input Low Voltage | - | - | 0.8 | V | |
| Vth | Schmitt Hysteresis Voltage | 0.22 | - | 0.3 | V | |
| Iin | Input leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Ioz | Tri-state output leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Rpu | Pull-up resistor | - | 42 | - | kΩ | |
| Rpd | Pull-down resistor | - | 44 | - | kΩ | |

Table 6-4 Digital I/O Pin Characteristics (VCCIO = +3.3V)

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------|----------------------------|-----------|---------|---------|-------|------------------|
| Voh | Output Voltage High | VCCIO-0.4 | - | - | V | Ioh=5mA |
| Vol | Output Voltage Low | - | - | 0.4 | V | Iol=5mA |
| Vih | Input High Voltage | 1.7 | - | - | V | - |
| Vil | Input Low Voltage | - | - | 0.7 | V | - |
| Vth | Schmitt Hysteresis Voltage | 0.2 | - | 0.3 | V | - |
| Iin | Input leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |

| | | | | | | |
|-----|----------------------------------|-----|----|----|----|------------------|
| Ioz | Tri-state output leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Rpu | Pull-up resistor | - | 57 | - | kΩ | |
| Rpd | Pull-down resistor | - | 59 | - | kΩ | |

Table 6-5 Digital I/O Pin Characteristics (VCCIO = +2.5V)

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------|----------------------------------|-----------|---------|---------|-------|------------------|
| Voh | Output Voltage High | VCCIO-0.4 | - | - | V | Ioh=5mA |
| Vol | Output Voltage Low | - | - | 0.4 | V | Iol=5mA |
| Vih | Input High Voltage | 1.2 | - | - | V | - |
| Vil | Input Low Voltage | - | - | 0.6 | V | - |
| Vth | Schmitt Hysteresis Voltage | 0.17 | - | 0.3 | V | - |
| Iin | Input leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Ioz | Tri-state output leakage current | -10 | - | 10 | uA | Vin = VCCIO or 0 |
| Rpu | Pull-up resistor | - | 90 | - | kΩ | |
| Rpd | Pull-down resistor | - | 97 | - | kΩ | |

Table 6-6 Digital I/O Pin Characteristics (VCCIO = +1.8V)

| Parameter | Description | Minimum | Typical | Maximum | Units | Conditions |
|-----------|--|---------|---------|---------|-------|------------|
| Rsw-on | X-,X+,Y- and Y+ Drive On resistance | - | 6 | 10 | Ω | VCCIO=3.3V |
| | | - | 9 | 16 | Ω | VCCIO=1.8V |
| Rsw-off | X-,X+,Y- and Y+ Drive Off resistance | 10 | - | - | MΩ | |
| Rpu | Touch sense pull up resistance | 78 | 100 | 125 | kΩ | |
| Vth+ | Touch Detection rising-edge threshold on XP pin | 1.59 | - | 2.04 | V | VCCIO=3.3V |
| | | 0.58 | - | 0.68 | V | VCCIO=1.8V |
| Vth- | Touch Detection falling-edge threshold on XP pin | 1.23 | - | 1.55 | V | VCCIO=3.3V |
| | | 0.51 | - | 0.56 | V | VCCIO=1.8V |
| RI | X-axis and Y-axis drive load resistance | 200 | - | - | Ω | |

Table 6-7 Touch Sense Characteristics

6.4 AC Characteristics

6.4.1 System clock and reset

| Parameter | Value | | | Units |
|---------------------------|---------|---------|---------|-------|
| | Minimum | Typical | Maximum | |
| Internal Relaxation Clock | | | | |
| Trimmed frequency | - | 12 | - | MHz |
| Frequency variation | -5.5 | - | +5.5 | % |
| Crystal | | | | |
| Frequency | - | 12.000 | - | MHz |
| X1/X2 Capacitance | - | - | 10 | pF |
| External clock input | | | | |
| Frequency | - | 12.000 | - | MHz |
| Duty cycle | 45 | 50 | 55 | % |
| Input voltage on X1/CLK | - | 3.3 | - | V |
| Reset | | | | |
| Reset pulse on PD_N | 5 | | | ms |

Table 6-8 System clock characteristics

6.4.2 SPI interface timing

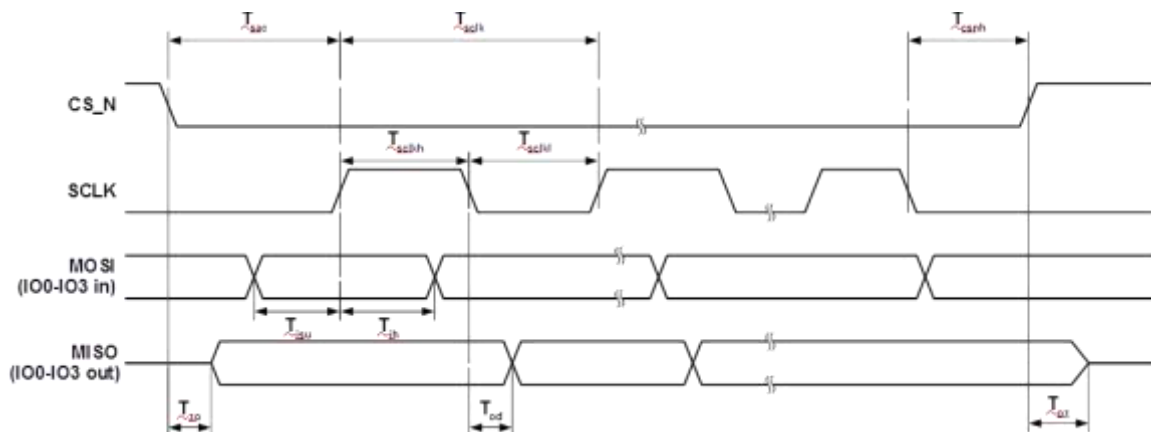


Figure 6-1 SPI Interface Timing

| Parameter | Description | VCCIO=1.8V | | VCCIO=2.5V | | VCCIO=3.3V | | Units |
|-----------|-------------------------------------|------------|-----|------------|-----|------------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| Tsclk | SPI clock period (SINGLE/DUAL mode) | 33.3 | | 33.3 | | 33.3 | | ns |
| Tsclk | SPI clock period (QUAD mode) | 40 | | 40 | | 40 | | ns |
| Tsckl | SPI clock low duration | 13 | | 13 | | 13 | | ns |
| Tsckh | SPI clock high duration | 13 | | 13 | | 13 | | ns |
| Tsac | SPI access time | 4 | | 3.5 | | 3 | | ns |
| Tisu | Input Setup | 4 | | 3.5 | | 3 | | ns |
| Tih | Input Hold | 0 | | 0 | | 0 | | ns |
| Tzo | Output enable delay | | 16 | | 13 | | 11 | ns |
| Toz | Output disable delay | | 13 | | 11 | | 10 | ns |
| Tod | Output data delay | | 15 | | 12 | | 11 | ns |
| Tcsnh | CSN hold time | 0 | | 0 | | 0 | | ns |

Table 6-9 SPI Interface Timing Specification

6.4.3 RGB Interface Timing

| Parameter | Description | Value | | | Units |
|-----------|---|-------|-----|-----|-------|
| | | Min | Typ | Max | |
| Tpclk | Pixel Clock period | 15.7 | | | ns |
| Tpclkdc | Pixel Clock duty cycle | 40 | 50 | 60 | % |
| Td | Output delay relative to PCLK rising edge (REG_PCLK_POL=0) or falling edge (REG_PCLK_POL=1). Applied for all the RGB output pins. | | | 4 | ns |
| Th | Output hold time relative to PCLK rising edge (REG_PCLK_POL=0) or falling edge (REG_PCLK_POL=1). Applied for all the RGB output pins. | 0.5 | | | ns |

Table 6-10 RGB interface timing characteristics

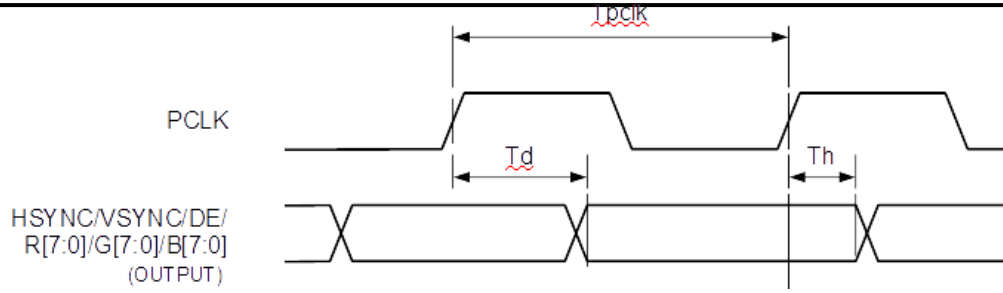


Figure 6-2 RGB Interface Timing

7 Application Examples

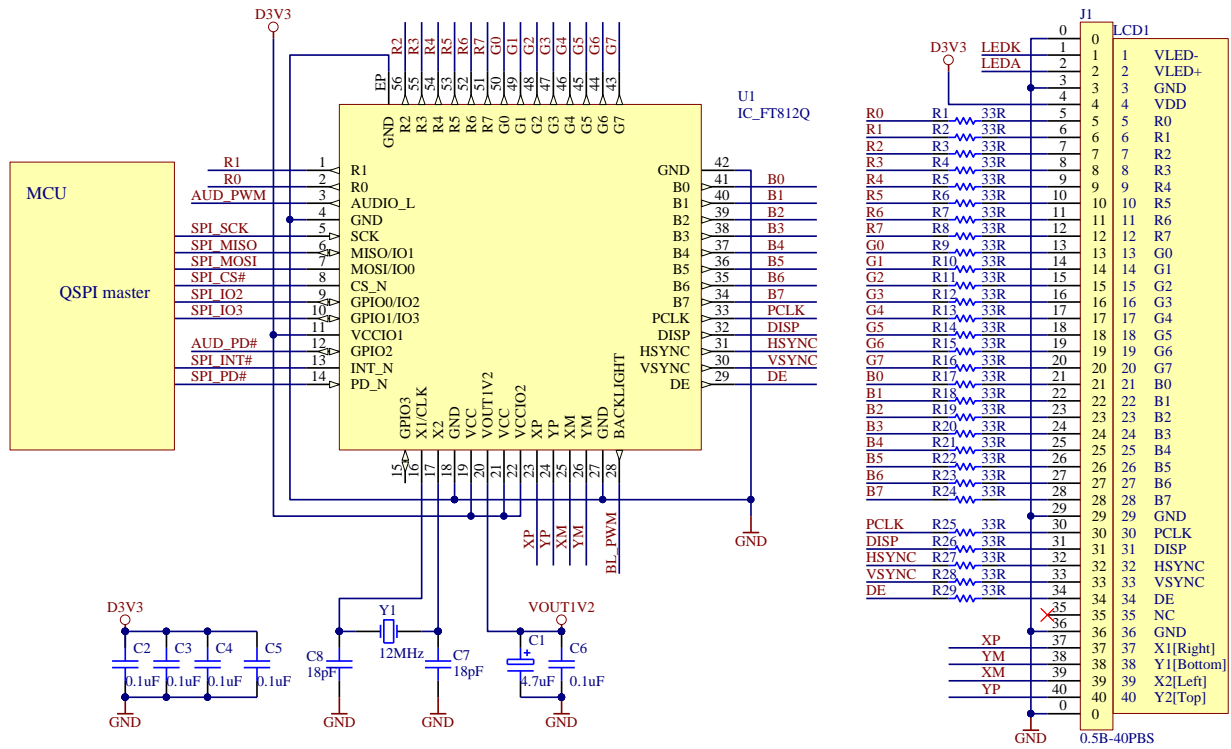


Figure 7-1 FT812 application circuit

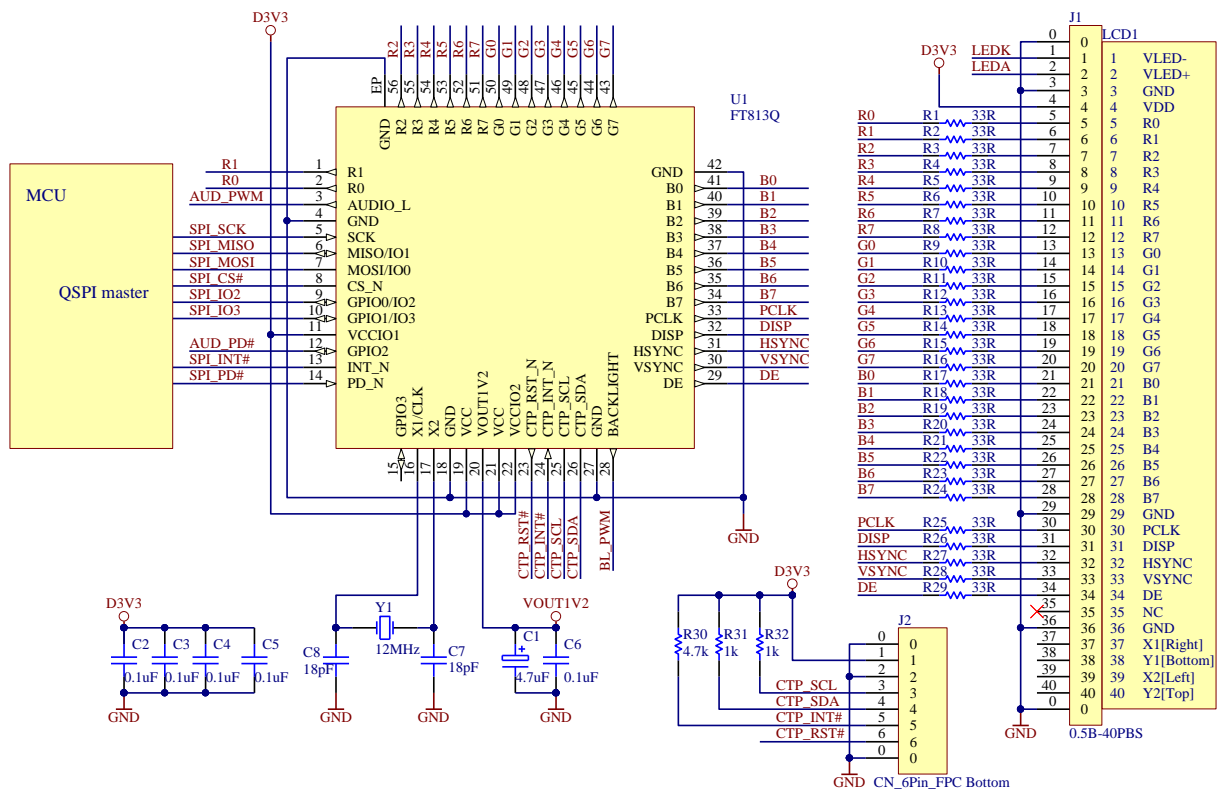


Figure 7-2 FT813 application circuit

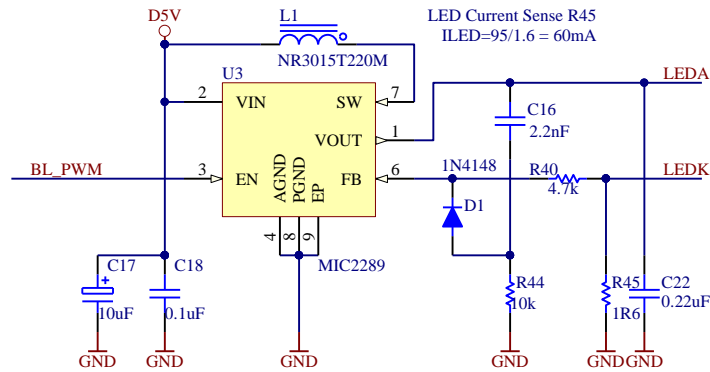


Figure 7-3 Backlight drive circuit

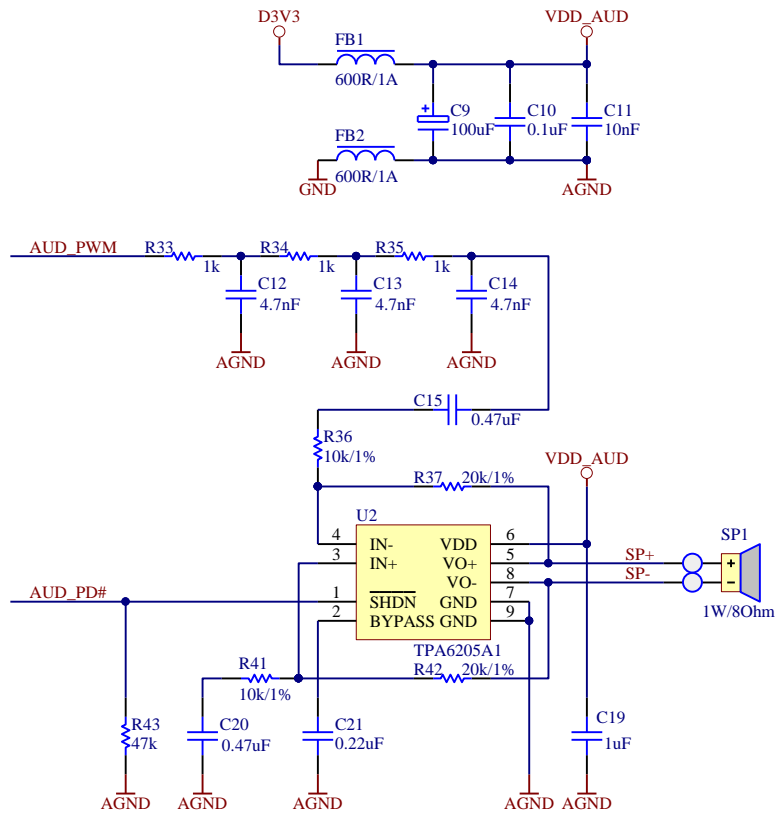


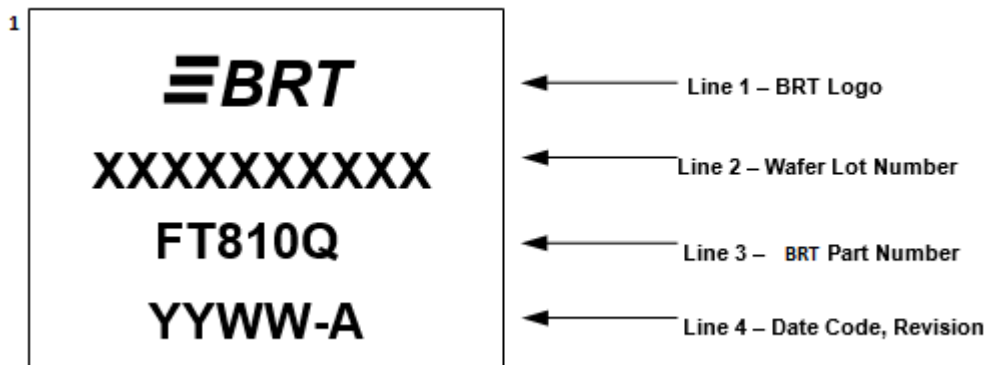
Figure 7-4 Audio filter and amplifier circuit

8 Package Parameters

The FT81x is available in VQFN-48 and VQFN-56 packages. The package dimensions, markings and solder reflow profile for all packages are described in following sections.

8.1 Part Markings

8.1.1 Top side



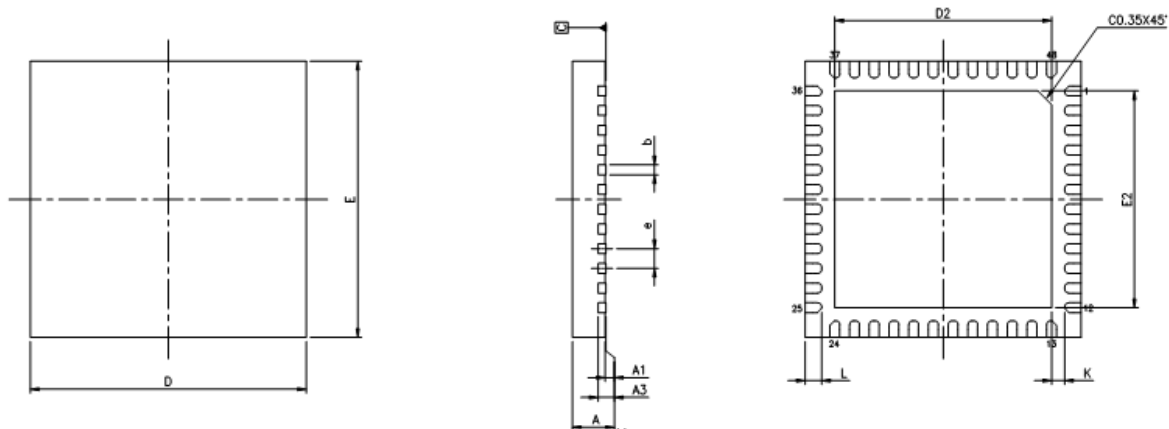
Notes:

1. YYWW = Date Code, where YY is year and WW is week number
2. Pre date code 1727 – company logo was FTDI
3. Marking alignment should be centre justified
4. Laser Marking should be used
5. All marking dimensions should be marked proportionally. Marking font should be using standard font (Roman Simplex)
6. BRT part number will be either FT810Q, FT811Q, FT812Q, FT813Q as per device selected.

8.1.3 Bottom Side

No markings should be placed on the bottom side.

8.2 VQFN-48 Package Dimensions

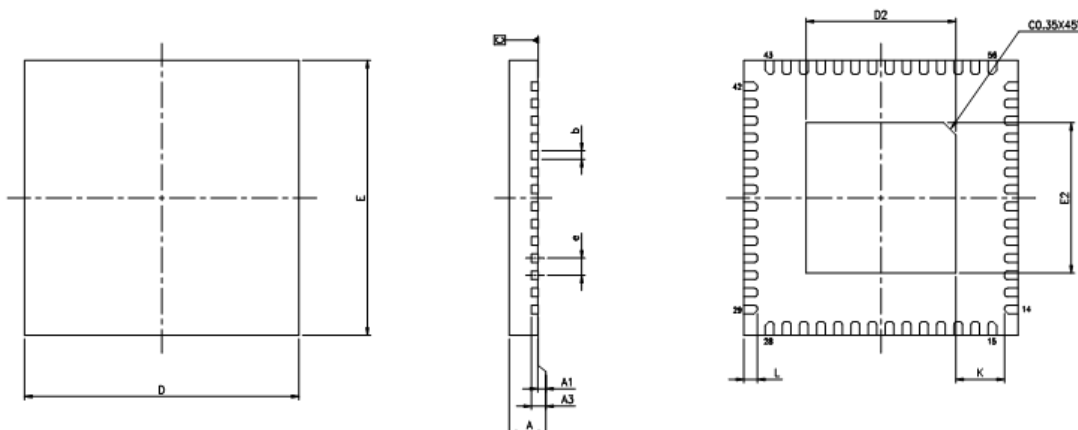


| | A | A1 | A3 | b | D | E | D2 | E2 | e | L | K |
|------|------|------|------|------|------|------|------|------|------|------|------|
| MIN. | 0.80 | 0.00 | | 0.20 | | | 5.15 | 5.15 | | 0.35 | 0.20 |
| NOM. | 0.85 | 0.02 | 0.20 | 0.25 | 7.00 | 7.00 | 5.20 | 5.20 | 0.50 | 0.40 | |
| MAX. | 0.90 | 0.05 | | 0.30 | | | 5.25 | 5.25 | | 0.45 | |

All dimensions are in millimetres (mm)

Figure 8-1 VQFN-48 Package Dimensions

8.3 VQFN-56 Package Dimensions



| | A | A1 | A3 | b | D | E | D2 | E2 | e | L | K |
|------|------|------|------|------|------|------|------|------|------|------|------|
| MIN. | 0.80 | 0.00 | | 0.20 | | | 5.85 | 5.85 | | 0.30 | 0.20 |
| NOM. | 0.85 | 0.02 | 0.20 | 0.25 | 8.00 | 8.00 | 5.90 | 5.90 | 0.50 | 0.40 | |
| MAX. | 0.90 | 0.05 | | 0.30 | | | 5.95 | 5.95 | | 0.50 | |

All dimensions are in millimetres (mm)

Figure 8-2 VQFN-56 Package Dimensions

8.4 Solder Reflow Profile

The FT81x is supplied in a Pb free VQFN-48 or VQFN-56 package. The recommended solder reflow profile for the package is shown in Figure 8-3.

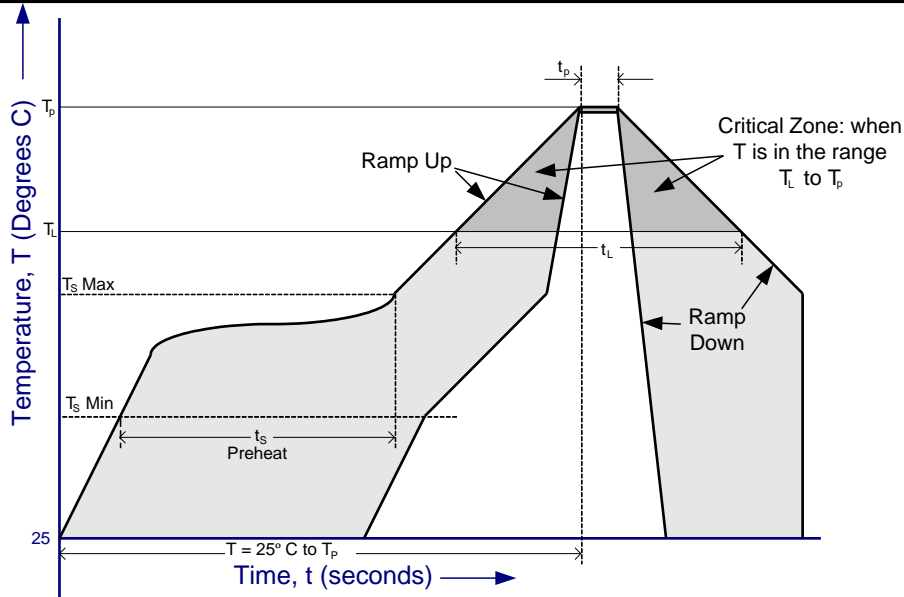


Figure 8-3 FT81x Solder Reflow Profile

The recommended values for the solder reflow profile are detailed in **Error! Reference source not found.** Values are shown for both a completely Pb free solder process (i.e. the FT81x is used with Pb free solder), and for a non-Pb free solder process (i.e. the FT81x is used with non-Pb free solder).

| Profile Feature | Pb Free Solder Process | Non-Pb Free Solder Process |
|---|-------------------------------------|-------------------------------------|
| Average Ramp Up Rate (T_s to T_p) | 3°C / second Max. | 3°C / Second Max. |
| Preheat - Temperature Min (T_s Min.) - Temperature Max (T_s Max.) - Time (t_s Min to t_s Max) | 150°C 200°C 60 to 120 seconds | 100°C 150°C 60 to 120 seconds |
| Time Maintained Above Critical Temperature T_L : - Temperature (T_L) - Time (t_L) | 217°C 60 to 150 seconds | 183°C 60 to 150 seconds |
| Peak Temperature (T_p) | 260°C | 240°C |
| Time within 5°C of actual Peak Temperature (t_p) | 20 to 40 seconds | 20 to 40 seconds |
| Ramp Down Rate | 6°C / second Max. | 6°C / second Max. |
| Time for T= 25°C to Peak Temperature, T_p | 8 minutes Max. | 6 minutes Max. |

Table 8-1 Reflow Profile Parameter Values

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Appendix A – References

Document References

[FT81x Series Programmer Guide](#)
[AN_252_FT800_Audio_Primer](#)
[AN_254_FT800_Designs_with_Visual_TFT](#)
[AN_259_FT800_Example_with_8-bit_MCU](#)
[AN_275_FT800_Example_with_Arduino](#)
[AN_276_Audio_File_Conversion](#)
[AN_277_FT800_Create_User_Defined_Font](#)
[AN_281_FT800_Emulator_Library_User_Guide](#)
[AN_291_FT800_Create_Multi-Language_Font](#)
[AN_299_FT800_FT801_Internal_Clock_Trimming](#)
[AN_303 - FT800 Image File Conversion](#)
[AN_308_FT800_Example_with_an_8-bit_MCU](#)
[AN_312_FT800_Example_with_ARM](#)
[AN_314_FT800_Advanced_Techniques - Working with Bitmaps](#)
[AN_318_Arduino_Library_for_FT800_Series](#)
[AN_320_FT800_Example_with_PIC](#)
[AN_327_EVE_Screen_Editor_Installation_Guide](#)
[AN_333_FT800_and_FT801_Touch_Capabilities](#)
[AN_336_FT800 - Selecting an LCD Display](#)
[FT800 Series Sample Application](#)
[EVE Frequently Asked Questions](#)

Acronyms and Abbreviations

| Terms | Description |
|------------------|--|
| ADPCM | Adaptive Differential Pulse Code Modulation |
| ASCII | American Standard Code for Information Interchange |
| EVE | Embedded Video Engine |
| HMI | Human Machine Interfaces |
| I ² C | Inter-Integrated Circuit |
| LCD | Liquid Crystal Display |
| LED | Light Emitting Diode |
| MCU | Micro Controller Unit |
| MPU | Micro Processor Unit |

| | |
|------|--|
| PCM | Pulse Code Modulation |
| PLL | Phased Locked Loop |
| PWM | Pulse Width Modulation |
| QVGA | Quarter Video Graphics Array |
| ROM | Read Only Memory |
| SPI | Serial Peripheral Interface |
| VQFN | Very Thin Quad Flat Non-Leaded Package |

Appendix B - List of Figures and Tables

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Appendix C - Revision History

Document Title: FT81X Embedded Video Engine Datasheet
 Document Reference No.: BRT_000002
 Clearance No.: BRT#004
 Product Page: <http://brtchip.com/product>
 Document Feedback: [Send Feedback](#)

| Revision | Changes | Date |
|----------|--|------------|
| Draft | Initial Release | 2015-02-15 |
| 1.0 | Revised Release | 2015-07-07 |
| 1.1 | Revised Release | 2015-09-14 |
| 1.2 | Revised Release | 2015-09-29 |
| 1.3 | Dual branding to reflect the migration of the product to the Bridgetek name – logo changed, copyright changed, contact information changed Updated table 4-10 ROM Font Extended ASCII characters | 2016-09-13 |
| 1.4 | Document Migrated from Dual branding (FTDI/BRT) to Bridgetek – Dual branding logo replaced with BRT Logo All document reference hyperlinks updated to point BRT website Updated all the chip markings from FTDI to BRT | 2017-06-30 |