High Efficiency Single Synchronous Buck PWM Controller

General Description

The RT8126A/B/C PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers.

The constant on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The RT8126A/B/C achieves high efficiency at a reduced cost by eliminating the current sense resistor found in traditional current mode PWMs. Efficiency is further enhanced by its ability to drive very large synchronous rectifier MOSFETs. To eliminate noise in audio applications, the RT8126B provides Audio-Skipping mode, which maintains the switching frequency above 25kHz. The buck conversion allows this device to directly step down high voltage batteries at the highest possible efficiency. The RT8126A/B/C is intended for CPU core, chipset, DRAM, or other low voltage supplies as low as 0.6V.

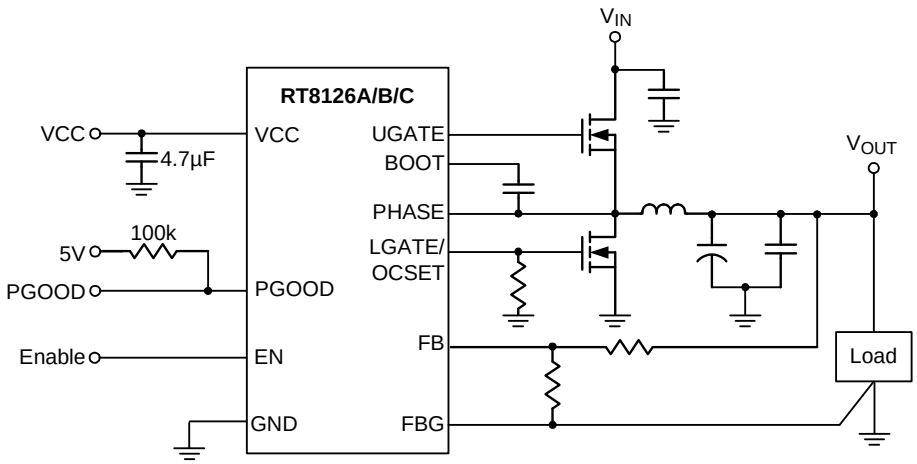
Features

- **VCC Input Range : 4.5V to 13.2V**
- **VOUT Operating Range : 0.6V to 5V**
- **Power Stage Input Range : 2.5V to 24V**
- **Shutdown Current <10μA**
- **Operating Frequency : Fixed 300kHz**
- **Diode Emulation Mode (RT8126A)**
- **Audio Skipping Mode (RT8126B)**
- **VIN Detection**
- **Pinless LGATE Over Current Setting (LGOCS)**
- **Power Good Indication**
- **Embedded Bootstrap Switch**
- **Current Limit with Low Side Current Sense Scheme**
- **1% High Accuracy Internal V_{REF} = 0.6V**
- **Enable Function**
- **Differential Output Sense**
- **OVP/UVP/OTP/Pre-OVP/OCP**

Applications

- Chipset/RAM Supply as Low as 0.6V
- Generic DC/DC Power Regulator

Simplified Application Circuit



Ordering Information

RT8126A/B/C□□

- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- A : Diode Emulation Mode
  B : Audio Skipping Mode
  C : FCCM

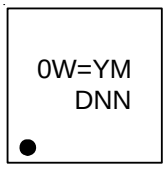
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information

RT8126AGQW



0W= : Product Code

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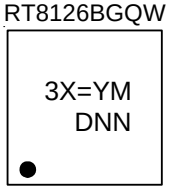
RT8126BGQW



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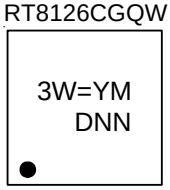
RT8126CGQW



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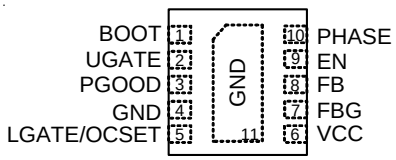
Pin Configurations

(TOP VIEW)

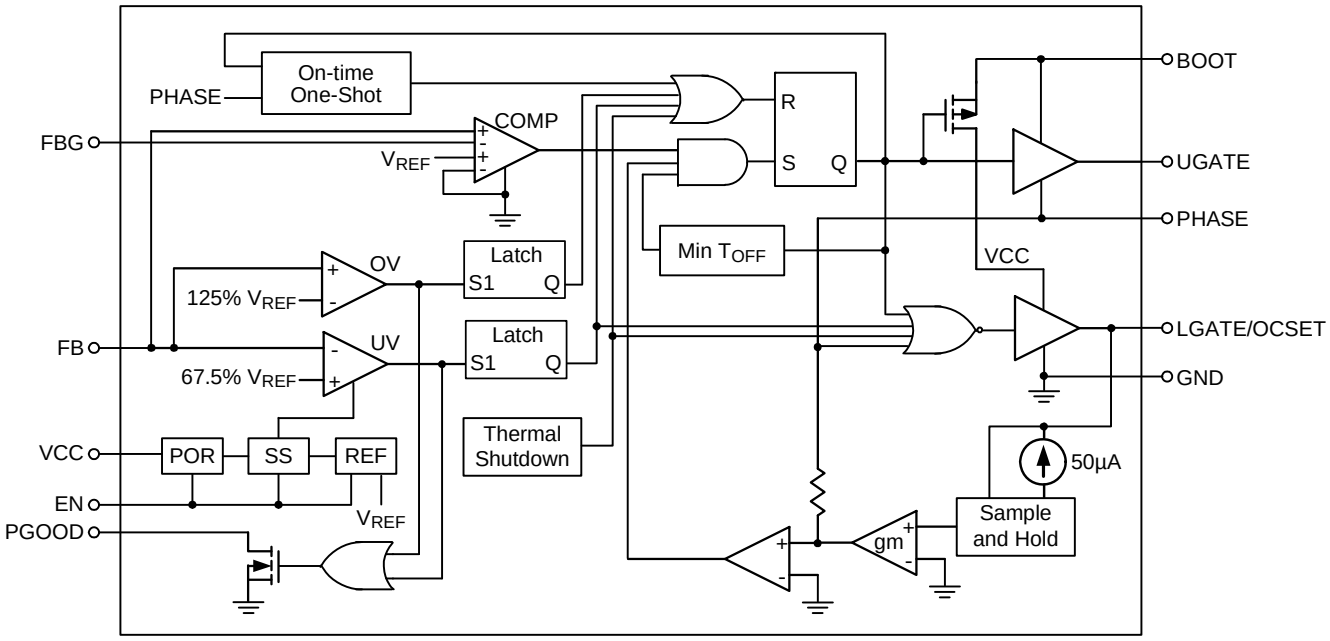


WDFN-10L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Supply Input for High Side Driver. Connect a capacitor between the BOOT pin and PHASE pin.
2	UGATE	Gate Drive Output for the High Side External MOSFET.
3	PGOOD	Open-drain Power Good Indicator. High impedance indicates power is good.
4, 11 (Exposed pad)	GND	Ground. Connect this pin directly to the low side MOSFET source and ground plane with the lowest impedance. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	LGATE/OCSET	Gate Drive Output for the Low Side External MOSFET. This pin is also used to set the OCP threshold. Please refer the application information.
6	VCC	Control Voltage Input. It supports the power for the PWM controller, the low side driver and the bootstrap circuit for high side driver. Bypass to GND with a 4.7μF ceramic capacitor.
7	FBG	Output Voltage Feedback Negative Input.
8	FB	Output Voltage Feedback Positive Input. Connect FB and FBG to a resistive voltage divider to set the output voltage level. The internal reference voltage is 0.6V typically.
9	EN	Active-High Enable Input. Pull low to GND to disable the PWM controller.
10	PHASE	External Inductor Connection Pin for PWM Converter. It behaves as the current sense comparator input for low side MOSFET $R_{DS(ON)}$ sensing and reference voltage for on time generation.

Functional Block Diagram



Operation

The RT8126 series controller is suitable for low external component count configuration with appropriate amount of Equivalent Series Resistance (ESR) capacitor(s) at the output. The output ripple valley voltage is monitored at a feedback point voltage. Refer to the function block diagrams of the RT8126A/B/C, the synchronous high side MOSFET is turned on at the beginning of each cycle. After the internal one-shot timer expires, the MOSFET is turned off. The pulse width of this one-shot is determined by the converter's input and output voltages to keep the frequency fairly constant over the entire input voltage range. Another one-shot sets a minimum off-time (400ns typ.).

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high side switch directly proportional to the output voltage and inversely proportional to the input voltage. The implementation results in a nearly constant switching frequency without the need of a clock generator.

The RT8126B operates in audio skipping mode with a minimum switching frequency of 25kHz. This mode eliminates audio frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In audio skipping mode, the low side switch gate driver signal is ORed with an internal oscillator (>25kHz). Once the internal oscillator is triggered, the audio skipping controller pulls LGATE logic high, turning on the low side MOSFET to induce a negative inductor current. After the output voltage rises above VREF, the controller turns off the low side MOSFET (LGATE pulled logic low) and triggers a constant on-time operation (UGATE driven logic high). When the on-time operation expires, the controller re-enables the low side MOSFET until the inductor current drops below the zero crossing threshold.

Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 15V
- PGOOD, FB, EN ---------- –0.3V to 6.5V
- BOOT to GND
  - DC ---------- –0.3V to 40V
  - <100ns ---------- –0.3V to 45V
- BOOT to PHASE
  - DC ---------- –0.3V to 15V
  - <100ns ---------- –0.3V to 20V
- PHASE to GND
  - DC ---------- –5V to 25V
  - <100ns ---------- –10V to 30V
- UGATE to GND
  - DC ---------- –0.3V to 40V
  - <100ns ---------- –10V to 45V
- UGATE to PHASE
  - DC ---------- –0.3V to 15V
  - <100ns ---------- –5V to 20V
- LGATE to GND
  - DC ---------- –0.3V to 15V
  - <100ns ---------- –5V to 20V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 3.27W
- Package Thermal Resistance (Note2)
  - WDFN-10L 3x3, θ_{JA} ---------- 30.5°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage, V_{IN} ---------- 2.5V to 24V
- Supply Voltage, V_{CC} ---------- 4.5V to 13.2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, V_{IN} = 15V, V_{EN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM Controller						
V_{CC} Quiescent Supply Current	I_Q	FB forced above the regulation point, V_{EN} = 5V	--	0.5	1.25	mA
V_{CC} POR Threshold		Rising edge, hysteresis = 120mV, PWM disable below this level	3.8	4	4.2	V
V_{CC} Shutdown Current	I_{SHDN}	V_{CC} current, V_{EN} = 0V	--	--	10	μA
Feedback Threshold (Note 5)	V_{FB}	V_{CC} = 4.5 to 13.2V	588	594	600	mV
FB Input Bias Current	I_{FB}	V_{FB} = 0.6V	–1	--	1	μA
Output Voltage Range	V_{OUT}		0.6	--	5	V
Switching Frequency	f_{OSC}	(Note 6)	270	300	330	kHz
OCSET Current	I_{OCSET}		45	50	55	μA
Zero Crossing Threshold			–6	--	8	mV
ASM Minimum Frequency	f_{ASM}		22	--	--	kHz
TSS			--	3	--	ms
Protection Function						
Current Limit Threshold Offset			–20	--	20	mV
Current Limit Threshold Setting Range			50	--	400	mV
UV Threshold		UVP detect, FB falling edge	60	--	75	%
OVP Threshold		OVP detect, FB rising edge	120	125	130	%
Thermal Shutdown			--	140	--	°C
Driver On-Resistance						
UGATE Driver (Source)	R_{UG_SRC}	V_{BOOT} – V_{PHASE} = 12V, source current = 100mA	--	1.5	3	Ω
UGATE Driver (Sink)	R_{UG_SNK}	V_{UGATE} – V_{PHASE} = 0.1V, I_{SNK} = 50mA	--	2.25	4	Ω
LGATE Driver (Source)	R_{LG_SRC}	V_{CC} = 12V, source current = 100mA	--	1.5	3	Ω
LGATE Driver (Sink)	R_{LG_SNK}	V_{LGATE}, I_{SNK} = 50mA	--	1	2	Ω
Dead Time		LGATE rising (V_{PHASE} = 1.5V)	--	30	--	ns
Dead Time		UGATE rising	--	30	--	ns
Internal Boost Charging Switch On-Resistance		VCC to BOOT, 10mA	--	--	80	Ω
EN Threshold						
EN Threshold Voltage	Logic-High	V_{IH}	--	--	2.4	V
	Logic-Low	V_{IL}	0.4	--	--	
EN Current		High State, forced to 5V	--	--	10	μA
PGOOD (Upper Side Threshold Decided by OV Threshold)						
PGOOD Blanking Time		PGOOD rising edge from enable	--	--	10	ms
Output Low Voltage		I_{SINK} = 4mA	--	--	0.3	V
Leakage Current		High state, forced to 5V	--	--	1	μA

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

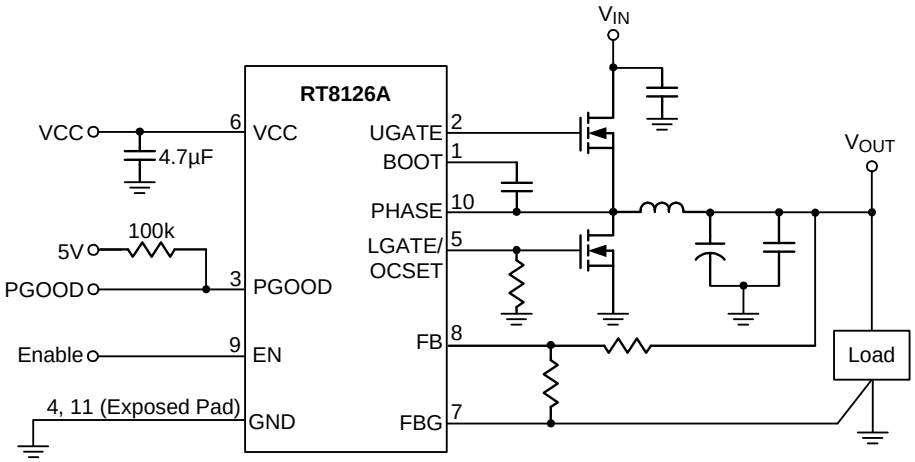
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

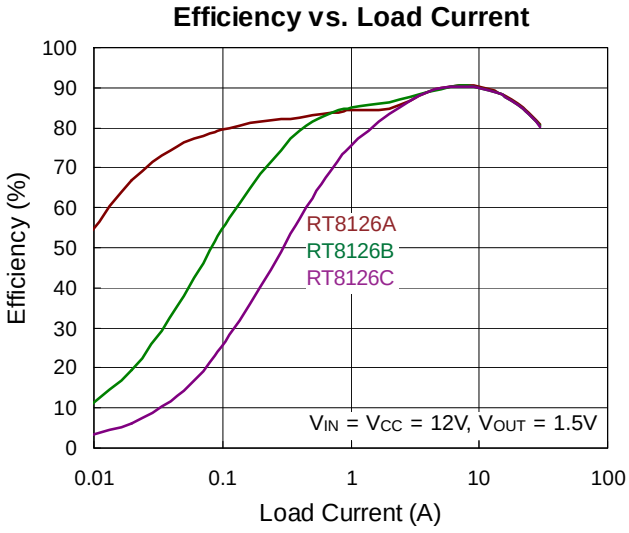
Note 5. The reference voltage shift –6mV from 0.6V for offset canceling under feedback valley control.

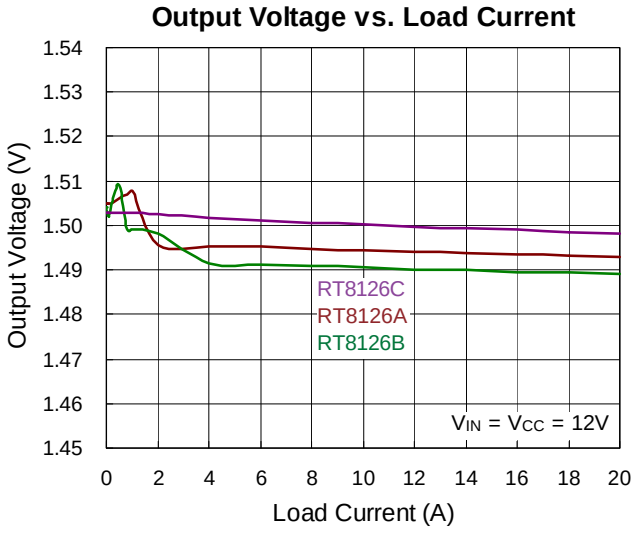
Note 6. No production tested. Test condition V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A using application circuit.

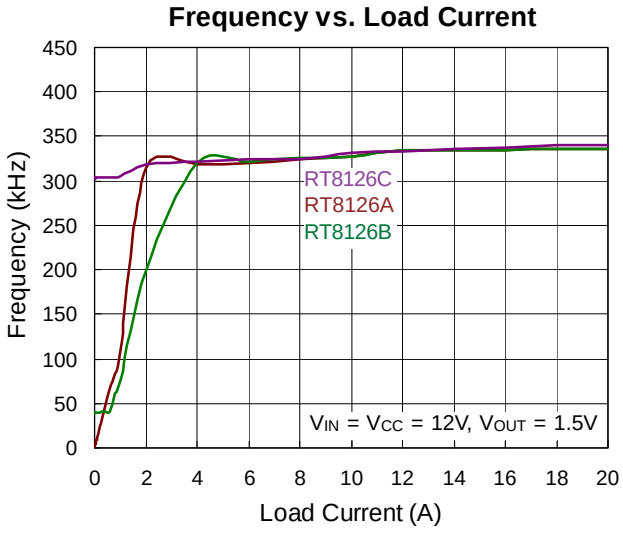
Typical Application Circuit

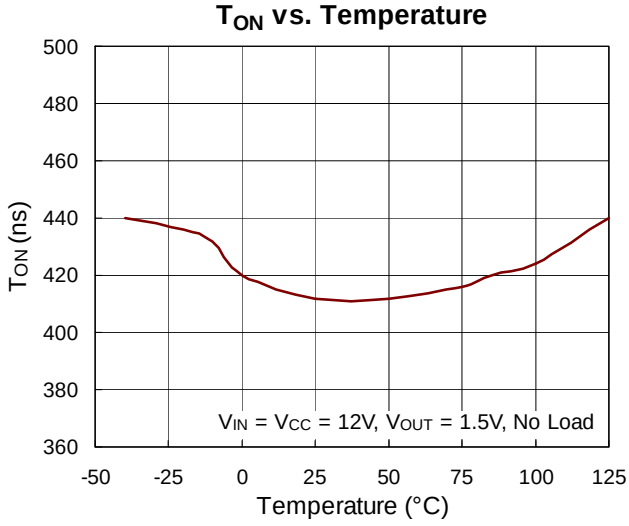


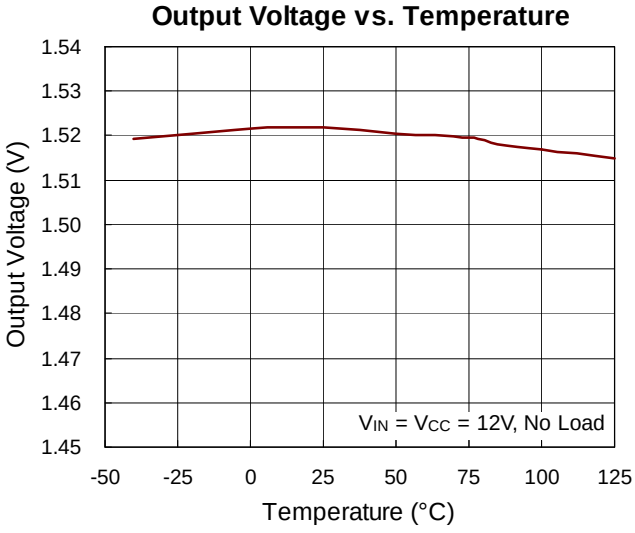
Typical Operating Characteristics

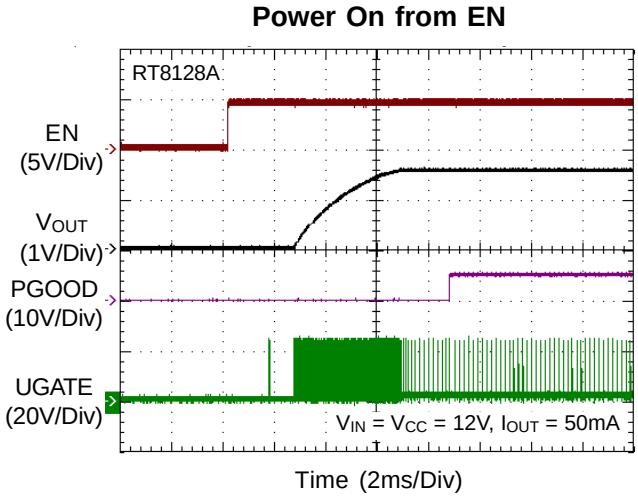




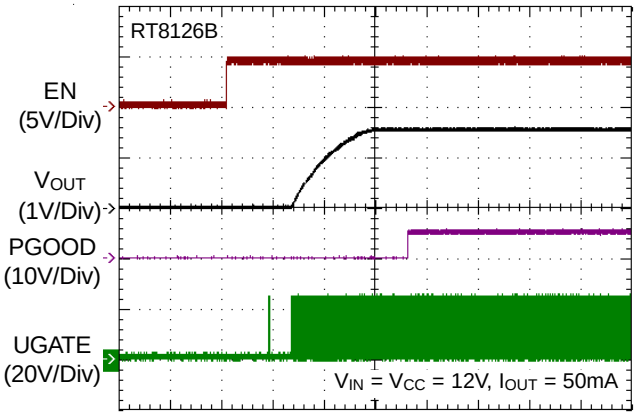




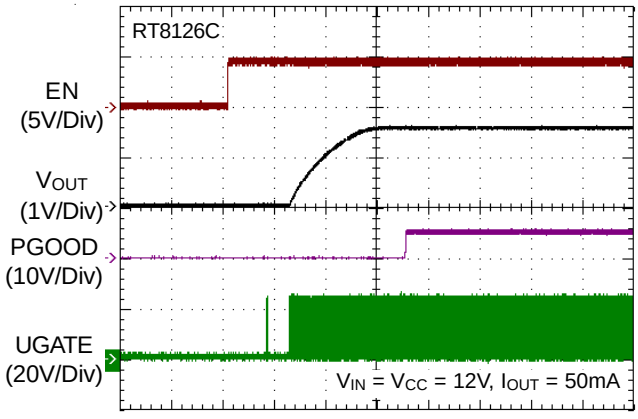




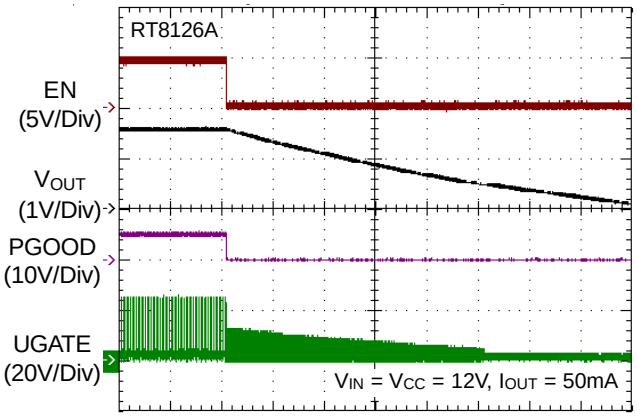
Power On from EN



Power On from EN



Power Off from EN



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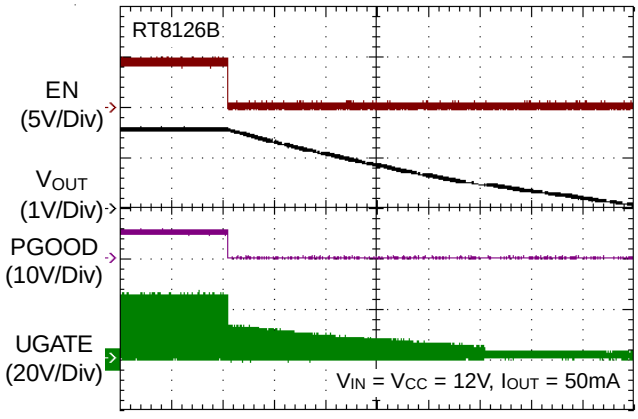

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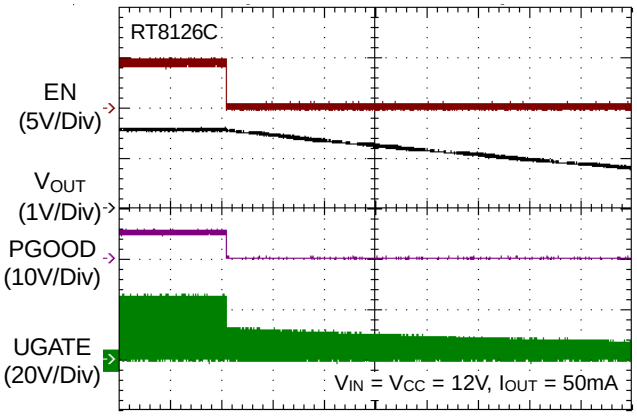
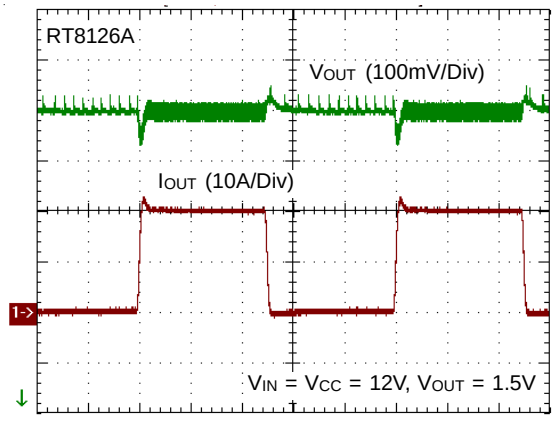
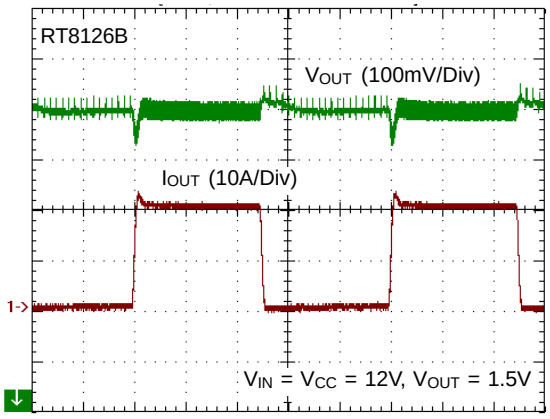


Load Transient Response

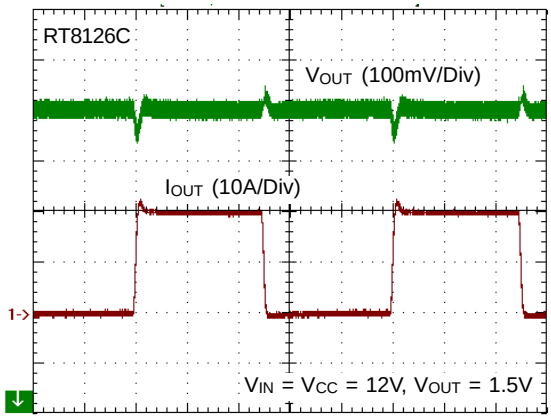


Load Transient Response



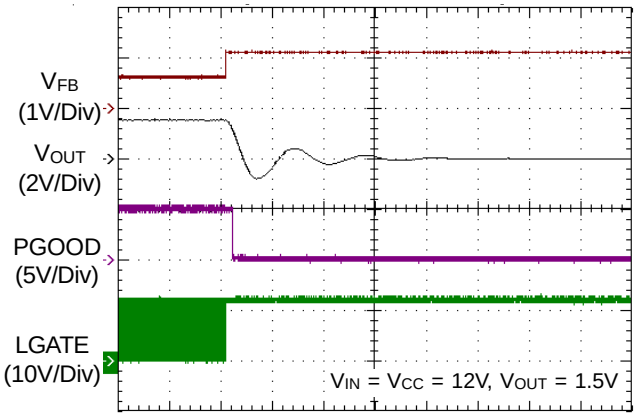
Time (200µs/Div)

Load Transient Response



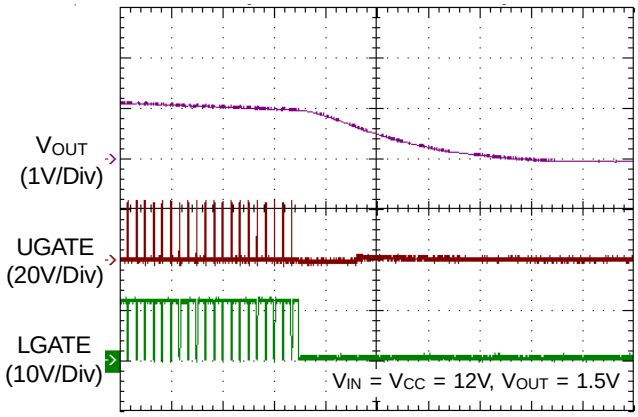
Time (200µs/Div)

OVP



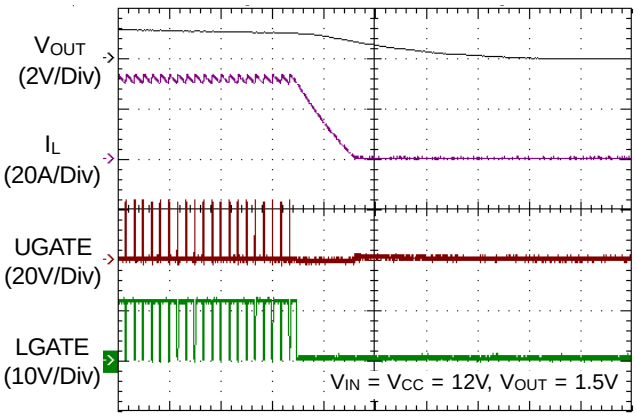
Time (100µs/Div)

UVP



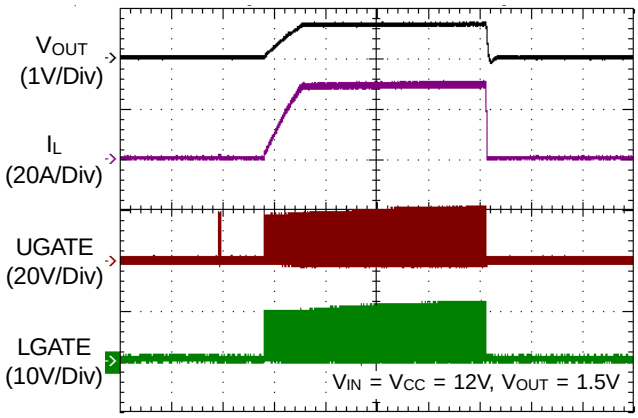
Time (20µs/Div)

OCP



Time (20µs/Div)

Short Circuit before Power On



Time (1ms/Div)

Applications Information

The RT8126A/B/C PWM controller provides high efficiency, excellent transient response, and high DC output accuracy needed for stepping down high voltage batteries to generate low voltage CPU core, I/O, and chipset RAM supplies in notebook computers. Richtek Mach Response™ technology is specifically designed for providing 100ns "instant-on" response to load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The topology circumvents the poor load transient timing problems of fixed frequency current mode PWMs while avoiding the problems caused by widely varying switching frequencies in conventional constant on-time and constant off-time PWM schemes. The RT8126 series controller is specifically designed to have better noise immunity for such a single output application.

Supply Voltage and Power On Reset (POR)

The input voltage range for VCC is from 4.5V to 13.2V with respect to GND. An internal linear regulator regulates the supply voltage for internal control logic circuit. A minimum 0.1μF ceramic capacitor is recommended to bypass the supply voltage. Place the bypassing capacitor physically near the IC. VCC also supplies the integrated MOSFET drivers. A bootstrap diode is embedded to facilitate PCB design and reduce the total BOM cost. No external Schottky diode is required in real applications.

The Power On Reset (POR) circuit monitors the supply voltage at the VCC pin. If VCC exceeds the POR rising threshold voltage (typ. 4V), the controller resets and prepares the PWM for operation. If VCC falls below the POR falling threshold during normal operation, all MOSFETs stop switching. The POR rising and falling threshold has a hysteresis (typ. 0.12V) to prevent unintentional noise based reset.

VIN Detection

Once VCC exceeds its Power On Reset (POR) rising threshold voltage, UGATE will output continuous pulses and LGATE will be forced low for converter input voltage VIN detection. If the voltage pulses at the PHASE pin is greater than 2V when UGATE is turned off more than 3 times cycle, VIN is recognized as ready. Then, the controller will initiate soft-start operation.

Internal Soft-Start

The RT8126A/B/C provides an internal soft-start function. The soft-start function is used to prevent large inrush current and output voltage overshoot while the converter is being powered-up. The soft-start function automatically begins once the chip is enabled. An internal current source charges the internal soft-start capacitor such that the internal soft-start voltage ramps up uniformly. The FB voltage will track the internal soft-start voltage during the soft-start interval. Therefore, the PWM pulse width increases gradually to limit the input current. After the internal soft-start voltage exceeds the reference voltage, the FB voltage no longer tracks the soft-start voltage but rather follows the reference voltage. Therefore, the duty cycle of the UGATE signal as well as the input current at power up are limited.

Over Current Protection

The RT8126A/B/C provides lossless over current protection by detecting the voltage drop across the low side MOSFET when it is turned on. The over current trip threshold is set by an external resistor, R_{OCSET}, at LGATE. During the initial stage when LGATE is turned on, the RT8126A/B/C samples and holds the phase voltage. The sample and hold voltage represents the valley inductor current and is compared to the OCP threshold. If the sensed phase voltage is lower than the OCP threshold, OCP will be triggered. When OCP is triggered, LGATE will turn on to prevent inductor current increasing until the OCP condition is released.

LGATE Over Current Setting (LGOCS)

Over current threshold is externally programmed by adding a resistor (R_{OCSET}) between LGATE and GND. Once VCC exceeds the POR threshold, an internal current source I_{OCSET} flows through R_{OCSET}. The voltage across R_{OCSET} is stored as the over current protection threshold V_{OCSET}.

After that, the current source is switched off. R_{OCSET} can be determined using the following equation :

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

where I_{VALLEY} represents the desired inductor OCP trip current (valley inductor current). If R_{OCSET} is not present, there is no current path for I_{OCSET} to build the OCP threshold. In this situation, the OCP threshold is internally preset to 50mV (typ.).

Over Voltage Protection (OVP)

The output voltage is scaled by the divider resistors and fed back to the FB pin. The voltage on the FB pin will be compared to the internal reference voltage VREF for voltage related protection functions, including over voltage protection and under voltage protection. If the FB voltage is higher than the OVP threshold during operation, OVP will be triggered. When OVP is triggered, UGATE will go low and LGATE will go high to discharge the output capacitor. Once OVP is triggered, controller will be latched unless VCC POR is detected again.

Pre-OVP Function

The RT8128A/B/C provides pre-OVP function to prevent output over voltage before chip enable. When EN signal is low, the pre-OVP circuit senses the PHASE voltage. Once the PHASE voltage exceeds 0.2V, LGATE will deliver 10% duty pulse to discharge the output voltage for protecting the load. Pre-OVP protection is not latch mode. Once the PHASE voltage is less than 0.2V, LGATE will terminate the discharge pulse immediately.

Under Voltage Protection (UVP)

The voltage on the FB pin is monitored for under voltage protection. Controller begins detecting UVP after soft-start finish. If the FB voltage is lower than the UVP threshold during normal operation, UVP will be triggered. When the UVP is triggered, both UGATE and LGATE go low and latched.

Output Voltage Setting

The RT8126A/B/C allows the output voltage of the DC/DC converter to be adjusted from 0.6V to 5V via an external resistive divider. It will try to maintain the feedback pin at internal reference voltage (0.6V).

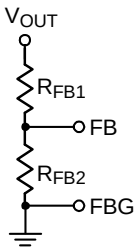


Figure 1. Output Voltage Setting

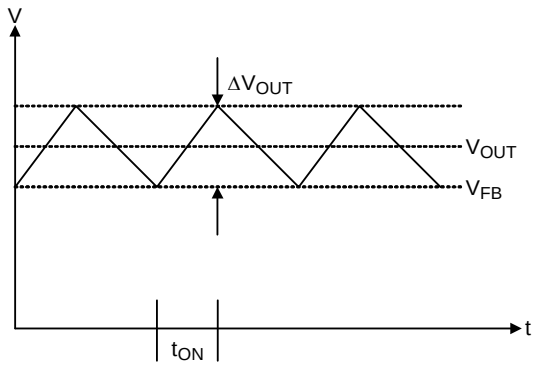


Figure 2. Output Voltage Waveform

According to the resistor divider network above, the output voltage is set as :

$$V_{OUT} = \left[V_{FB} \times \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) \right] + \frac{\Delta V_{OUT}}{2}$$

Note that the reference voltage at DEM is exceeds than CCM 1%.

MOSFET Drivers

The RT8126A/B/C integrates high current gate drivers for the two N-MOSFETs to obtain high efficiency power conversion in synchronous buck topology. A dead time is used to prevent crossover conduction for the high side and low side MOSFETs. Because both gate signals are off during dead time, the inductor current freewheels through the body diode of the low side MOSFET. The freewheeling current and the forward voltage of the body diode contribute to power loss. The RT8126A/B/C employs constant dead time control scheme to ensure safe operation without sacrificing efficiency. Furthermore, elaborate logic circuit is implemented to prevent cross conduction.

For high output current applications, two or more power MOSFETs are usually paralleled to reduce $R_{DS(ON)}$. The gate driver needs to provide more current to switch on/off these paralleled MOSFETs. Gate driver with lower source/sink current capability results in longer rising/falling time in gate signals, and therefore higher switching loss.

The RT8126A/B/C embeds high current gate drivers to obtain high efficiency power conversion. The embedded drivers contribute to the majority of the power dissipation of the controller. Therefore, WDFN package is chosen for its power dissipation rating. If no gate resistor is used, the power dissipation of the controller can be approximately calculated using the following equation :

$$P_{DRIVER} = f_{SW} \times (Q_G \times V_{BOOT} + Q_{G\_LOW\ SIDE} \times V_{DRIVER\_LOW\ SIDE})$$

where V_{BOOT} represents the voltage across the bootstrap capacitor and f_{SW} is the switching frequency. It is important to ensure the package can dissipate the switching loss and have enough room for safe operation.

Inductor Selection

The inductor plays an important role in step-down converters because it stores the energy from the input power rail and then releases the energy to the load. From the viewpoint of efficiency, the DC Resistance (DCR) of the inductor should be as small as possible to minimize the conduction loss. In addition, the inductor covers a significant proportion of the board space, so its size is also important. Low profile inductors can save board space especially when the height has a limitation. However, low DCR and low profile inductors are usually cost ineffective.

Additionally, larger inductance results in lower ripple current, which translates into the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off among performance, size and cost.

In general, inductance is chosen such that the ripple current ranges between 20% to 40% of the full load current. The inductance can be calculated using the following equation :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters when selecting an input capacitor. Conservatively speaking, an input capacitor should have a voltage rating 1.5 times greater than the maximum input voltage to be considered a safe design. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for the RMS current rating. Using more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Placing the ceramic capacitor close to the drain of the high side MOSFET can also be helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. Also, the capacitance must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

For CPU core voltage converters and other applications where the output is subject to violent load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance :

$$ESR \leq \frac{V_{P-P}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple :

$$ESR \leq \frac{V_{P-P}}{L_{IR} \times I_{LOAD(MAX)}}$$

where V_{P-P} is the peak-to-peak output voltage ripple.

Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended.

For low input-to-output voltage differentials (V_{IN} / V_{OUT} < 2), additional output capacitance is required to maintain stability and good efficiency in ultrasonic mode.

The amount of overshoot due to stored inductor energy can be calculated as :

$$V_{SOAR} = \frac{(I_{PEAK})^2 \times L}{2 \times C_{OUT} \times V_{OUT}}$$

where I_{PEAK} is the peak inductor current.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation :

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic, unstable operation. However, it is easy to add enough series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting V_{OUT} or the FB voltage-divider close to the inductor.

Unstable operation manifests itself in two related and distinctly different ways : double-pulsing and feedback loop instability.

Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the 400ns minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR.

Loop instability can result in oscillations at the output in the form of line or load perturbations, which can trip the over-voltage protection latch or cause the output voltage to fall below the tolerance limit.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under- or over-shoot.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high side MOSFET is small. Therefore, the switching loss of the high side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application. However, the small duty cycle means the low side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low side MOSFET driver capability and the budget.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 3x3, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.5°C/W) = 3.27W for a WDFN-10L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

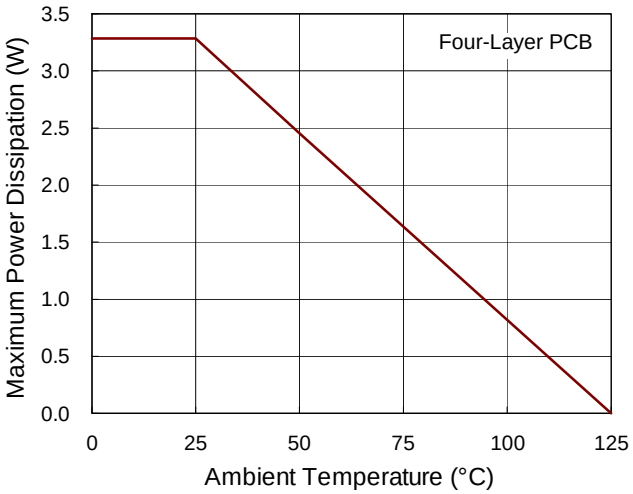


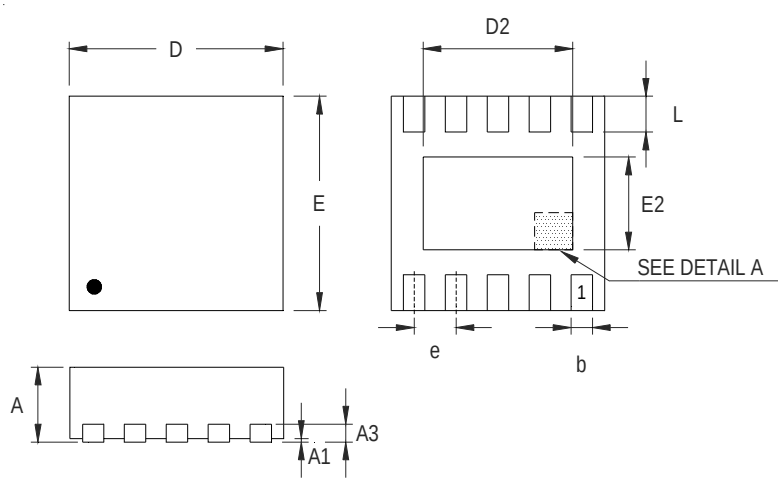
Figure 3. Derating Curve of Maximum Power Dissipation

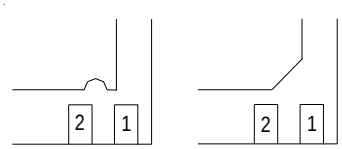
Layout Considerations

PCB layout is critical to high current high-frequency switching converter designs. A good layout can help the controller to function properly and achieve expected performance. On the other hand, PCB without a careful layout can radiate excessive noise, having more power loss and even malfunction in the controller. In order to avoid the above condition, the general guidelines can be followed in PCB layout.

- Power stage components should be placed first. Place the input bulk capacitors close to the high side power MOSFETs, and then locate the output inductor and finally the output capacitors.
- Placing the ceramic capacitor physically close to the drain of the high side MOSFET. This can reduce the input voltage drop when high side MOSFET is turned on. If more than one MOSFET is paralleled, each should have its own individual ceramic capacitor.
- Keep the high current loops as short as possible. During high speed switching, the current transition between MOSFETs usually causes di/dt voltage spike due to the parasitic components on PCB trace. Therefore, making the trace length between power MOSFETs and inductors wide and short can reduce the voltage spike and EMI.
- Make MOSFET gate driver path as short as possible. Since the gate driver uses narrow-width high current pulses to switch on/off power MOSFET, the driver path must be short to reduce the trace inductance. This is especially important for low side MOSFET, because this can reduce the possibility of shoot-through.
- Providing enough copper area around power MOSFETs to help heat dissipation. Using thick copper also reduces the trace resistance and inductance to have better performance.
- The output capacitors should be placed physically close to the load. This can minimize the trace parasitic components and improve transient response.
- All small signal components should be located close to the controller. The small signal components include the feedback voltage divider resistors, function setting components and high frequency bypass capacitors. The feedback voltage divider resistor must be placed close to FB pin, because the FB pin is inherently noise-sensitive.
- Voltage feedback path must be away from switching nodes. The noisy switching node is, for example, the interconnection among high side MOSFET, low side MOSFET and inductor. Feedback path must be away from this kind of noisy node to avoid noise pick-up.
- A multi layer PCB design is recommended. Make use of one single layer as the ground and have separate layers for power rail or signal is suitable for PCB design.

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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