

## GENERAL DESCRIPTION

The DS26503DK is an easy-to-use evaluation board for the DS26503 T1/E1/J1 BITS element. The DS26503DK is intended to be used as a stand-alone design kit. The board is complete with a DS26503 BITS element, transformers, termination resistors, FPGA-based configuration switches, and network connectors. Dallas' ChipView software gives point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status as well as multiple clock and signal routing configurations.

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## DESIGN KIT CONTENTS

DS26503DK Design Kit  
CD\_ROM Including:

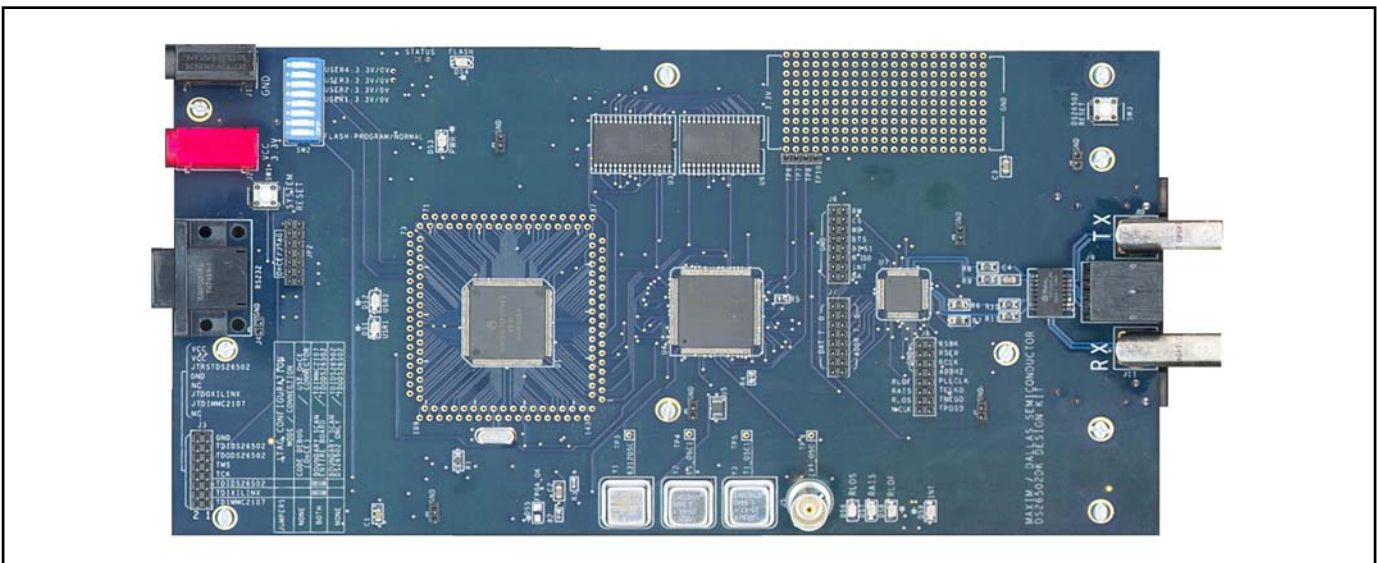
- ChipView Software
- DS26503DK Data Sheet
- DS26503 Data Sheet
- DS26503 Errata Sheet (if applicable)

## ORDERING INFORMATION

PART	DESCRIPTION
DS26503DK	Stand-Alone Design Kit for DS26503

## FEATURES

- **Expedites New Designs by Eliminating First-Pass Prototyping**
- **Demonstrates Key Functions of DS26503 BITS Element**
- **Includes DS26503 BITS Element, Transformers, BNC, and RJ48 Network Connectors and Termination Passives**
- **BNC Connections for 75Ω E1**
- **Bantam and RJ48 Connectors for 120Ω E1 and 100Ω T1**
- **Interface Directly to Windows-Based Computers**
- **ChipView Software Provides Point-and-Click Access to the DS26503 Register Set**
- **Software-Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing**
- **All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink**
- **LEDs for Loss-of-Signal and Interrupt Status as well as Indications for Multiple Clock and Signal Routing Configurations**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

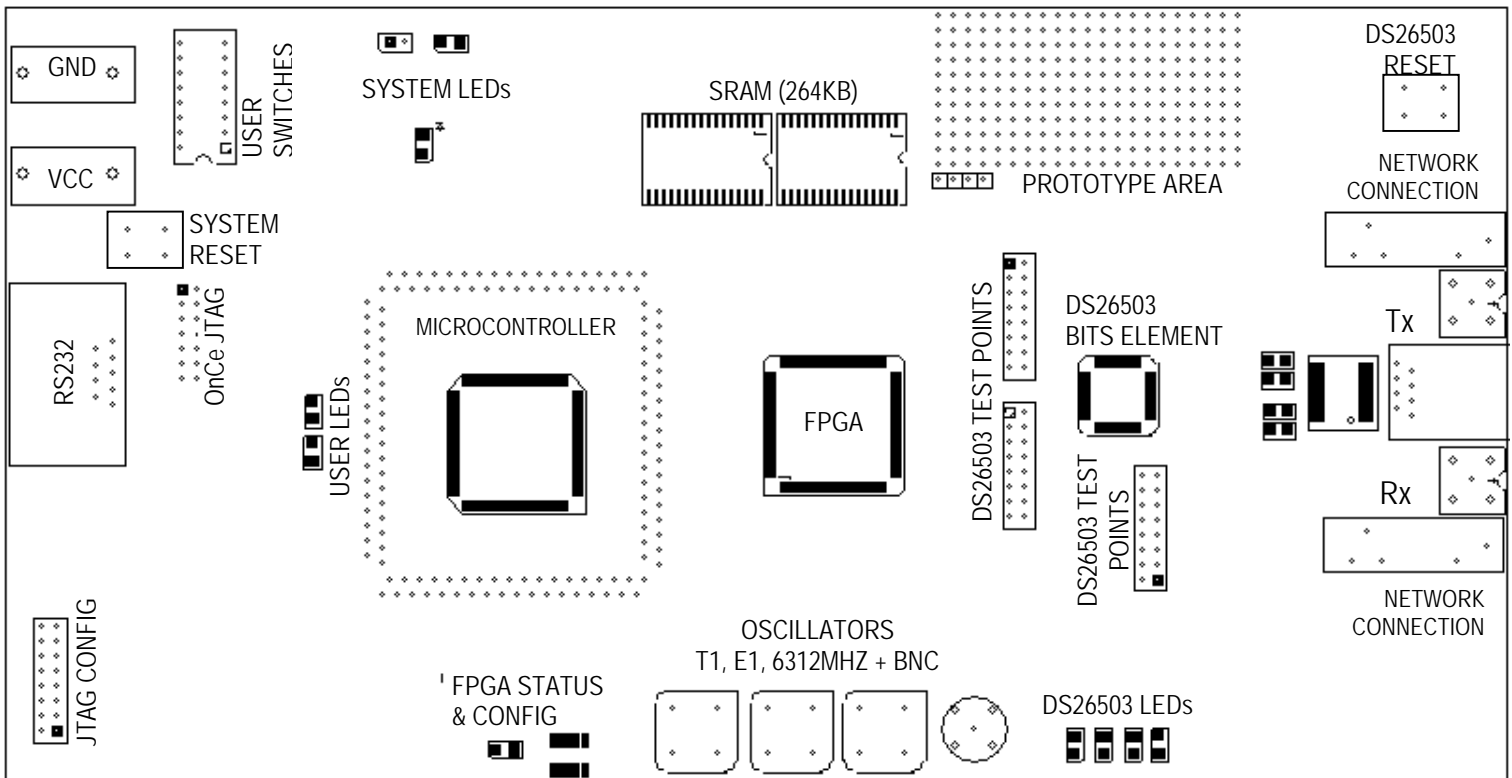


## COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1, C4, C23, C51, C53	5	10 $\mu$ F 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
C2–C3, C6–C9, C11, C12, C14, C15, C17, C18, C20, C21, C25–C30, C32, C33, C35, C36, C38, C45–C50, C52, C54, C55, C57–C60, C62, C63, C68	41	1 $\mu$ F 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C5, C10, C22, C24, C31, C34, C37, C39–C41, C43, C65–C67, C69, C70	16	0.1 $\mu$ F 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C13, C19, C42, C44, C64	5	10 $\mu$ F 20%, 16V tantalum capacitors (B case)	Panasonic	ECS-T1CX106R
C16, C56, C61	3	68 $\mu$ F 20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
D1	1	1A 50V general-purpose silicon diode	General Semiconductor	1N4001
DS1, DS2, DS6–DS9	6	Red LEDs, SMD	Panasonic	LN1251C
DS3	1	Green LED, SMD	Panasonic	LN1351C
DS4	1	Amber LED, SMD	Panasonic	LN1451C
DS5	1	Green LED, SMD (Not populated)	Panasonic	LN1351C
DS10	1	Red/green LED, 5mm right-angle PCMT	Digi-Key	350-1055-ND
J1	1	Socket, banana plug, horizontal, black	Mouser Electronics	164-6218
J2	1	Socket, banana plug, horizontal, red	Mouser Electronics	164-6219
J3, J6–J8	4	Terminal strip, 16-pin, dual row, vertical	Samtec	TSW-108-07-T-D
J4	1	DB9 right-angle, long case connector	AMP	747459-1
J5	1	75 $\Omega$ vertical 5-pin BNC connector	Cambridge	CP-BNCPC-004
J9	1	RJ48 8-pin, single-port connector	MOLEX	15-43-8588
J10, J11	2	BNC connectors, 75 $\Omega$ right-angle 5-pin	Kruidand	UCBJR220
J12, J13	2	Bantam jack, right-angle connectors	Switchcraft	RTT34B02
JP1, JP3–JP8	7	100-mil, 2-position jumper	labstock	
JP2	1	14-pin header, remove 'missing pin'	labstock	
L1	1	Inductor, 22.0 $\mu$ H 2-pin SMT 20%	Coiltronics	UP1B-220
NP1, NP2	2	10pF 5%, 50V tall case ceramic capacitors (1206) Do not populate	Phycomp	1206CG100J9B200
R1, R8–R11	5	0 $\Omega$ 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
R2, R13, R23, R27, R43, R47, R67–R70	10	330 $\Omega$ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R3, R18–R20, R22, R25, R26, R28–R31, R33–R42, R44–R46, R49, R50, R53, R56, R59, R61, R62, R65, R72	33	10kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R4, R5, R48, R51, R54, R55, R57, R58	8	30Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ300V
R6, R7	2	61.9Ω 1%, 1/8W resistors (1206)	Panasonic	ERJ-8ENF61R9V
R12	1	51Ω 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ510V
R14–R17, R21, R24, R63, R64, R66, R71	10	1.0kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
R32	1	1.0kΩ 5%, 1/10W resistor (0805)	Panasonic	ERJ-6GEYJ102V
R52	1	51.1Ω 1%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF51R1V
R60	1	1.0MΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
SW1, SW3	2	Switch MOM 4-pin single pole	Panasonic	EVQPAE04M
SW2	1	Switch 8-position, 16-pin DIP, low profile	AMP	435668-7
T1	1	XFMR 16P SMT	Pulse	TX1099
TP1, TP2	2	Test point, 1 plate thru-hole	NA	NA
TP3–TP10	8	Test point, 1 plated hole DO NOT STUFF	NA	NA
U1	1	32-bit microcontroller (lab stock)	Avnet	MMC2107CFCV33
U3, U6	2	SRAM 5V, 1Mb SO (in lab stock)	Cypress	CY62128V
U4	1	Xilinx Spartan 2.5V FPGA, 20mm x 20mm 144-pin TQFP	Xilinx	XC2S50-5TQ144C
U5	1	8-Pin μMAX/SO 2.5V or Adj	Maxim	MAX1792EUA25
U7	1	64-pin LQFP T1/E1/J1 BITS element (0°C to +70°C)	Dallas Semiconductor	DS26503L
U8, U9, U13	3	High-speed inverter	Fairchild	NC7SZ86
U10	1	High-speed buffer	Fairchild	NC7SZ86
U11	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	Maxim	MAX3233E
U12	1	1Mb flash-based config mem	Xilinx	XCF01SV020C
U14	1	8-pin SO step-up DC-DC converter 0.5A limit	Maxim	MAX1675EUA
X1	1	Low-profile 8.0MHz crystal	PEI	EC1-8.000M
Y1	1	Oscillator, crystal clock, 3.3V, 6.312MHz	SaRonix	NTH069A3-6.312
Y2	1	Oscillator, crystal clock, 3.3V, 2.048MHz	SaRonix	NTH039A3-2.0480
Y3	1	Oscillator, crystal clock, 3.3V, 1.544MHz	SaRonix	NTH039A3-1.5440

## BOARD FLOORPLAN



## ERRATA

The design kit errata refer to two different PC board revisions: the DS26502DK01A0 and DS26502DK01B0. The PC board revision code is found on the bottom of the board in the lower right corner.

### **DS26502DK01A0 Circuit Boards**

- RCLK did not get connected to FPGA. A jumper wire was run from RCLK to TP10 to provide the connection.
- Silkscreen for J3.4 is incorrect. Silkscreen reads “JTDIMMC2107” and should read “JTDOMMC2107.”
- RJ45 connector J4 does not use the standard pin numbers for connection to the transformer (and subsequently to TTIP/TRING and RTIP/RRING). This connector has been left unpopulated to avoid confusion. The schematic has been updated and is correct.
- DC blocking capacitor C4 on TTIP too small. A 10 $\mu$ F capacitor is recommended; a 1 $\mu$ F capacitor was populated.

### **DS26502DK01B0 Circuit Boards**

- RJ45 connector J4 does not use the standard pin numbers for connection to the transformer (and subsequently to TTIP/TRING and RTIP/RRING). This connector has been left unpopulated to avoid confusion. The schematic has been updated and is correct.

## ADDITIONS

The following signals have been connected to test points via the FPGA:

- TP6 is driven with data present at the TS\_8K\_4 pin of the DS26503.
- TP7 is driven with the 400Hz signal mentioned in the TS\_8Ksrc register (page 15).
- TP8 is driven with the 8KHz signal mentioned in the TS\_8Ksrc register (page 15).

## BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at [www.maxim-ic.com/telecom](http://www.maxim-ic.com/telecom). See the DS26503DK QuickView data sheet for these files.

### Hardware Configuration

- Supply 3.3V to the banana-plug receptacles marked GND and VCC\_3.3V.
- DIP switches are unused and can be in either the ON or OFF position with exception for the Flash programming switch, which should be OFF.
- From the Programs menu, launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.

### General

- Upon power-up the RLOS and RLOF LEDs (red) will be lit, the INT LED (red) will not be lit, and Status LED (DS10 red/green bicolor) will be green.

### Quick Setup (Register View)

- The PC will load ChipView offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select Register View.
- The program will then request a definition file. Select DS26503DC\_FPGA.def. Through the 'links' section, this will also load DS26503.def.
- The Register View Screen will appear, showing the register names, acronyms, and values for the DS26503.
- Predefined Register settings for several functions are available as initialization files.
  - ini files are loaded by selecting the menu File→Reg ini File→Load ini File.
  - Load the ini file "CompositeClock.ini."
  - Load the ini file "DS26502FPGA\_2048Clks.ini," which sets the DS26503 in Intel nonmultiplexed mode with MCLK driven at 2.048MHz.
  - After loading the ini files the following may be observed:
    - The RLOS and RLOF LEDs extinguishes upon external loopback.
    - The part begins operating in composite clock mode.

### Miscellaneous

- Clock frequencies and certain pin bias levels are provided by a register-mapped FPGA.
- The definition file for this FPGA is named DS26503DC\_FPGA.def. [Table 2](#) shows the FPGA register definitions. A drop-down menu on the top of the screen allows for switching between definition files.
- All files referenced above are available for download as described in the section marked "BASIC OPERATION."

## ADDRESS MAP

Device address space (DS26503 and FPGA) begins at 0x81000000.

All offsets given below are relative to the beginning of the device address space (shown above).

**Table 1. Device Address Map**

OFFSET	DEVICE	DESCRIPTION
0x0000 to 0x0030	FPGA	Board identification and clock/signal routing
0x8000 to 0x80ff	DS26503 T1/E1/J1 BITS element	DS26503 T1/E1/J1 BITS element

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named "DS26503DC\_FPGA.def".

## FPGA Register Map

**Table 2. FPGA Register Map**

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x0000	BID	Read only	BOARD ID
0x0001	Unused	—	—
0x0002	XBIDH	Read only	HIGH NIBBLE EXTENDED BOARD ID
0x0003	XBIDM	Read only	MIDDLE NIBBLE EXTENDED BOARD ID
0x0004	XBIDL	Read only	LOW NIBBLE EXTENDED BOARD ID
0x0005	BREV	Read only	BOARD FAB REVISION
0x0006	AREV	Read only	BOARD ASSEMBLY REVISION
0x0007	PREV	Read only	PLD REVISION
0x0007	BUSMO	Read only	BUS MODE INFORMATION
0x0009-0x0010	Unused	—	—
0x0011	LEVEL1	Control	DS26503 pin settings (THZE, BTS-HBE, BIS1, BIS0)
0x0012	LEVEL2	Control	DS26503 pin settings (RMODE3, RMODE2, RMODE1, RMODE0)
0x0013	LEVEL3	Control	DS26503 pin settings (RSM, RITD)
0x0014	LEVEL4	Control	DS26503 pin settings (TSM, TITD)
0x0015	LEVEL5	Control	DS26503 pin settings (TCSS1, TCSS0)
0x0016	LEVEL6	Control	DS26503 pin settings (TMODE3, TMODE2, TMODE1, TMODE0)
0x0017	LEVEL7	Control	DS26503 pin settings (L2, L1, L0)
0x0018	LEVEL8	Control	DS26503 pin settings (TAIS, RLB)
0x0019	LEVEL9	Control	DS26503 pin settings (MPS1, MPS0)
0x001A	LEVEL10	Control	DS26503 pin settings (JAMUX, E1TS)
0x001B	Unused	—	—
0x001C	TSERsrc	Control	DS26503 TSER source selection
0x001D	MCLKsrc	Control	DS26503 MCLK source selection
0x001E	TCLK	Control	DS26503 TCLK source selection
0x001F	TS_8K	Control	DS26503 TS_8K source selection
0x0020	Unused	—	—
0x0021	Unused	—	—

## FPGA ID Registers

### BID: BOARD ID (Offset = 0x0000)

BID is read only with a value of 0xD.

### XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0x0002)

XBIDH is read only with a value of 0x0.

### XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0x0003)

XBIDM is read only with a value of 0x1.

### XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0x0004)

XBIDL is read only with a value of 0x6.

### BREV: BOARD FAB REVISION (Offset = 0x0005).

BREV is read only and displays the current fab revision.

### AREV: BOARD ASSEMBLY REVISION (Offset = 0x0006)

AREV is read only and displays the current assembly revision.

### PREV: PLD REVISION (Offset = 0x0007)

PREV is read only and displays the current PLD firmware revision.

## FPGA Status Registers

Register Name: **BUSMO**

Register Description: **DS26503 Bus Mode**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	LevCPOL	LevCPHA	HW	SPI	INMUX	IMUX	MNMUX	MMUX
Default	—	—	—	—	—	—	—	—

The FPGA derives values in the BUSMO register from the levels present at the DS26503 pins.

**Bit 7: LevCPOL.** When set the DS26503 CPOL pin is high. Note: This pin is called A3/CPOL/L1 in parallel/serial/hardware modes.

**Bit 6: LevCPHA.** When set the DS26503 CPHA pin is high. Note: This pin is called A2/CPHA/L0 in parallel/serial/hardware modes.

**Bit 5: HW.** When set the DS26503 is in hardware mode.

**Bit 4: SPI.** When set the DS26503 is in SPI (3-wire) mode.

**Bit 3: INMUX.** When set the DS26503 is in Intel nonmultiplexed mode.

**Bit 2: IMUX.** When set the DS26503 is in Intel multiplexed mode.

**Bit 1: MNMUX.** When set the DS26503 is in Motorola nonmultiplexed mode.

**Bit 0: MMUX.** When set the DS26503 is in Motorola multiplexed mode.

## FPGA Control Registers

The FPGA register set consists of two types of registers: level setting and clock multiplexing. There are 10 registers for tri-state and level-control setting when in hardware mode. The level-setting registers are only valid when the DS26503 is in hardware mode (BIS1:0 = 11). When in nonhardware mode, the FPGA pins affected by the level registers are automatically either tri-stated, or assume an alternate function (e.g., they function as address databus pins or SPI pins). Exceptions are given with the register descriptions.

Register Name: **LEVEL1**

Register Description: **DS26503 Pin Settings (THZE, BTS, BIS1, BIS0)**

Register Offset: **0x0011**

Bit #	7	6	5	4	3	2	1	0
Name	THZEtri	THZE_Lev	BTStri	BTS_Lev	BIS1tri	BIS1_Lev	BIS0tri	BIS0_Lev
Default	0	0	0	0	0	0	0	1

**Note:** This register is only valid in ALL modes (many of the level registers are only valid in hardware mode).

### Bits 7 and 6: DS26503 THZE Tri-State and Level (THZEtri and THZE\_Lev)

- 00 = FPGA drives THZE with 0V
- 01 = FPGA drives THZE with 3.3V
- 1x = FPGA tri-states THZE pin

### Bit 5 and 4: DS26503 BTS Tri-State and Level (BTStri and BTS\_Lev)

- 00 = FPGA drives BTS with 0V
- 01 = FPGA drives BTS with 3.3V
- 1x = FPGA tri-states BTS pin

### Bits 3 and 2: DS26503 BIS1 Tri-State and Level (BIS1tri and BIS1\_Lev)

- 00 = FPGA drives BIS1 with 0V
- 01 = FPGA drives BIS1 with 3.3V
- 1x = FPGA tri-states BIS1 pin

### Bits 1 and 0: DS26503 BIS0 Tri-State and Level (BIS0tri and BIS0\_Lev)

- 00 = FPGA drives BIS0 with 0V
- 01 = FPGA drives BIS0 with 3.3V
- 1x = FPGA tri-states BIS0 pin



Register Name: **LEVEL2**

Register Description: **DS26503 Pin Settings (RMODE3, RMODE2, RMODE1, RMODE0)**

Register Offset: **0x0012**

Bit #	7	6	5	4	3	2	1	0
Name	RMODE3 tri	RMODE3 _Lev	RMODE2 tri	RMODE2 _Lev	RMODE1 tri	RMODE1 _Lev	RMODE0 tri	RMODE0 _Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode ( $BIS[1:0] = 11$ ), and is ignored for other modes.

**Bits 7 and 6: DS26503 RMODE3 Tri-State and Level (RMODE3tri and RMODE3\_Lev)**

- 00 = FPGA drives RMODE3 with 0V
- 01 = FPGA drives RMODE3 with 3.3V
- 1x = FPGA tri-states RMODE3 pin

**Bits 5 and 4: DS26503 RMODE2 Tri-State and Level (RMODE2tri and RMODE2\_Lev)**

- 00 = FPGA drives RMODE2 with 0V
- 01 = FPGA drives RMODE2 with 3.3V
- 1x = FPGA tri-states RMODE2 pin

**Bits 3 and 2: DS26503 RMODE1 Tri-State and Level (RMODE1tri and RMODE1\_Lev)**

- 00 = FPGA drives RMODE1 with 0V
- 01 = FPGA drives RMODE1 with 3.3V
- 1x = FPGA tri-states RMODE1 pin

**Bits 1 and 0: DS26503 RMODE0 Tri-State and Level (RMODE0tri and RMODE0\_Lev)**

- 00 = FPGA drives RMODE0 with 0V
- 01 = FPGA drives RMODE0 with 3.3V
- 1x = FPGA tri-states RMODE0 pin

Register Name: **LEVEL3**

Register Description: **DS26503 Pin Settings (RSM, RITD)**

Register Offset: **0x0013**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RSMtri	RSM_Lev	—	—	RITDtri	RITD_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode ( $BIS[1:0] = 11$ ), and is ignored for other modes.

**Bits 5 and 4: DS26503 RSM Tri-State and Level (RSMtri and RSM\_Lev)**

- 00 = FPGA drives RSM with 0V
- 01 = FPGA drives RSM with 3.3V
- 1x = FPGA tri-states RSM pin

**Bits 1 and 0: DS26503 RITD Tri-State and Level (RITDtri and RITD\_Lev)**

- 00 = FPGA drives RITD with 0V
- 01 = FPGA drives RITD with 3.3V
- 1x = FPGA Tristates RITD pin

Register Name: **LEVEL4**

Register Description: **DS26503 Pin Settings (TSM, TITD)**

Register Offset: **0x0014**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TSMtri	TSM_Lev	—	—	TITDtri	TITD_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode ( $BIS[1:0] = 11$ ), and is ignored for other modes.

**Bits 5 and 4: DS26503 TSM Tri-State and Level (TSMtri and TSM\_Lev)**

00 = FPGA drives TSM with 0V

01 = FPGA drives TSM with 3.3V

1x = FPGA tri-states TSM pin

**Bits 1 and 0: DS26503 TITD Tri-State and Level (TITDtri and TITD\_Lev)**

00 = FPGA drives TITD with 0V

01 = FPGA drives TITD with 3.3V

1x = FPGA tri-states TITD pin

Register Name: **LEVEL5**

Register Description: **DS26503 Pin Settings (TCSS1, TCSS0)**

Register Offset: **0x0015**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TCSS1tri	TCSS1_Lev	—	—	TCSS0tri	TCSS0_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode ( $BIS[1:0] = 11$ ), and is ignored for other modes.

**Bits 5 and 4: DS26503 TCSS1 Tri-State and Level (TCSS1tri and TCSS1\_Lev)**

00 = FPGA drives with TCSS1 0V

01 = FPGA drives with TCSS1 3.3V

1x = FPGA tri-states TCSS1 pin

**Bits 1 and 0: DS26503 TCSS0 Tri-State and Level (TCSS0tri and TCSS0\_Lev)**

00 = FPGA drives TCSS0 with 0V

01 = FPGA drives TCSS0 with 3.3V

1x = FPGA tri-states TCSS0 pin

Register Name: **LEVEL6**

Register Description: **DS26503 Pin Settings (TMODE3, TMODE2, TMODE1, TMODE0)**

Register Offset: **0x0016**

Bit #	7	6	5	4	3	2	1	0
Name	TMODE3 tri	TMODE3 _Lev	TMODE2 tri	TMODE2 _Lev	TMODE1 tri	TMODE1 _Lev	TMODE0 tri	TMODE0 _Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode ( $BIS[1:0] = 11$ ), and is ignored for other modes.

**Bits 7 and 6: DS26503 TMODE3 Tri-State and Level (TMODE3tri and TMODE3\_Lev)**

00 = FPGA drives TMODE3 with 0V

01 = FPGA drives TMODE3 with 3.3V

1x = FPGA tri-states TMODE3 pin

**Bits 5 and 4: DS26503 TMODE2 Tri-State and Level (TMODE2tri and TMODE2\_Lev)**

00 = FPGA drives TMODE2 with 0V

01 = FPGA drives TMODE2 with 3.3V

1x = FPGA tri-states TMODE2 pin

**Bits 3 and 2: DS26503 TMODE1 Tri-State and Level (TMODE1tri and TMODE1\_Lev)**

00 = FPGA drives TMODE1 with 0V

01 = FPGA drives TMODE1 with 3.3V

1x = FPGA tri-states TMODE1 pin

**Bits 1 and 0: DS26503 TMODE0 Tri-State and Level (TMODE0tri and TMODE0\_Lev)**

00 = FPGA drives TMODE0 with 0V

01 = FPGA drives TMODE0 with 3.3V

1x = FPGA tri-states TMODE0 pin

Register Name: **LEVEL7**

Register Description: **DS26503 Pin Settings (L2, L1, L0)**

Register Offset: **0x0017**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	L2tri	L2_Lev	L1tri	L1_Lev	L0tri	L0_Lev
Default	0	0	0	0	0	0	0	0

**Note:** Settings for L2 are only valid in hardware mode ( $BIS[1:0] = 11$ ), and ignored for other modes. In serial mode ( $BIS[1:0] = 10$ ), L0 and L1 are used to set levels for CPHA and CPOL, respectively.

**Bits 5 and 4: DS26503 L2 Tri-State and Level (L2tri and L2\_Lev)**

- 00 = FPGA drives L2 with 0V
- 01 = FPGA drives L2 with 3.3V
- 1x = FPGA tri-states L2 pin

**Bits 3 and 2: DS26503 L1 Tri-State and Level (L1tri and L1\_Lev)**

- 00 = FPGA drives L1 with 0V
- 01 = FPGA drives L1 with 3.3V
- 1x = FPGA tri-states L1 pin

**Bits 1 and 0: DS26503 L0 Tri-State and Level (L0tri and L0\_Lev)**

- 00 = FPGA drives L0 with 0V
- 01 = FPGA drives L0 with 3.3V
- 1x = FPGA tri-states L0 pin

Register Name: **LEVEL8**

Register Description: **DS26503 Pin Settings (TAIS, RLB)**

Register Offset: **0x0018**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TAIS tri	TAIS_Lev	—	—	RLBtri	RLB_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode ( $BIS[1:0] = 11$ ), and is ignored for other modes.

**Bits 5 and 4: DS26503 TAIS Tri-State and Level (TAIS tri and TAIS\_Lev)**

- 00 = FPGA drives TAIS with 0V
- 01 = FPGA drives TAIS with 3.3V
- 1x = FPGA tri-states TAIS pin

**Bits 1 and 0: DS26503 RLB Tri-State and Level (RLBtri and RLB\_Lev)**

- 00 = FPGA drives RLB with 0V
- 01 = FPGA drives RLB with 3.3V
- 1x = FPGA tri-states RLB pin

Register Name: **LEVEL9**

Register Description: **DS26503 Pin Settings (MPS1, MPS0)**

Register Offset: **0x0019**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	MPS1tri	MPS1_Lev	—	—	MPSOtri	MPSO_Lev
Default	0	0	0	0	0	0	0	0

**Bits 5 and 4: DS26503 MPS1 Tri-State and Level (MPS1tri and MPS1\_Lev)**

00 = FPGA drives MPS1 with 0V

01 = FPGA drives MPS1 with 3.3V

1x = FPGA tri-states MPS1 pin

**Bits 1 and 0: DS26503 MPS0 Tri-State and Level (MPSOtri and MPSO\_Lev)**

00 = FPGA drives MPS0 with 0V

01 = FPGA drives MPS0 with 3.3V

1x = FPGA tri-states MPS0 pin

Register Name: **LEVEL10**

Register Description: **DS26503 Pin Settings (JAMUX, E1TS)**

Register Offset: **0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	JAMUXtri	JAMUX_Lev	—	—	E1Tstri	E1TS_Lev
Default	0	0	0	0	0	0	0	0

**Note:** This register is only valid in hardware mode ( $BIS[1:0] = 11$ ), and is ignored for other modes.

**Bits 5 and 4: DS26503 JAMUX Tri-State and Level (JAMUXtri and JAMUX\_Lev)**

00 = FPGA drives JAMUX with 0V

01 = FPGA drives JAMUX with 3.3V

1x = FPGA tri-states JAMUX pin

**Bits 1 and 0: DS26503 E1TS Tri-State and Level (E1Tstri and E1TS\_Lev)**

00 = FPGA drives E1TS with 0V

01 = FPGA drives E1TS with 3.3V

1x = FPGA tri-states E1TS pin

Register Name: **TSERsrc**

Register Description: **DS26503 TSER Pin Source**

Register Offset: **0x001C**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	ZEROS	ONES	RSER
Default	0	0	0	0	0	0	1	0

**Note:** Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TSER. Setting to 0 also tri-states this pin.

**Bit 2: ZEROS.** When set DS26503\_TSER ← 0.0V.

**Bit 1: ONES.** When set DS26503\_TSER ← 3.3V.

**Bit 0: RSER.** When set DS26503\_TSER ← DS26503\_RSER.

Register Name: **MCLKsrc**

Register Description: **DS26503 MCLK Pin Source**

Register Offset: **0x001D**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	ZERO	EXT	T1	E1
Default	0	0	0	0	0	0	1	0

**Note:** Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to MCLK. Setting to 0 also tri-states this pin.

**Bit 3: ZERO.** When set DS26503\_MCLK ← 0.0V.

**Bit 2: EXT.** When set DS26503\_MCLK ← External\_Osc (BNC connector).

**Bit 1: T1.** When set DS26503\_MCLK ← T1\_OSC (1.544MHz).

**Bit 0: E1.** When set DS26503\_MCLK ← E1\_OSC (2.048MHz).

Register Name: **TCLKsrc**

Register Description: **DS26503 TCLK Pin Source**

Register Offset: **0x001E**

Bit #	7	6	5	4	3	2	1	0
Name	—	EXT	T1	E1	64KHZ	6312	PLL	RCLK
Default	0	0	1	0	0	0	0	0

**Note:** Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TCLK. Setting to 0 also tri-states this pin.

**Bit 6: EXT.** When set DS26503\_TCLK ← External\_Osc (BNC connector).

**Bit 5: T1.** When set DS26503\_TCLK ← T1\_OSC (1.544MHz).

**Bit 4: E1.** When set DS26503\_TCLK ← E1\_OSC (2.048MHz).

**Bit 3: 64KHZ.** When set DS26503\_TCLK ← 64kHz clock.

**Bit 2: 6312.** When set DS26503\_TCLK ← 6312kHz clock.

**Bit 1: PLL.** When set DS26503\_TCLK ← DS26503\_PLL.

**Bit 0: RCLK.** When set DS26503\_TCLK ← DS26503\_RCLK.

Register Name: **TS\_8Ksrc**

Register Description: **DS26503 TS\_8K Pin Source**

Register Offset: **0x001F**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	EXT	_8KHz	400HZ	400HZ_502	RS_8K
Default	0	0	0	0	0	0	1	0

**Note:** Only one bit in this register should be set at a time. Setting multiple bits tri-states the FPGA pin connected to TS\_8K. Setting to 0 also tri-states this pin.

**Bit 4: EXT.** When set DS26503\_TS\_8K ← External\_Osc (BNC connector).

**Bit 3: \_8KHz.** When set DS26503\_TS\_8K ← 8kHz (derived by FPGA).

**Bit 2: 400HZ.** When set DS26503\_TS\_8K ← 400Hz clock (derived by FPGA).

**Bit 1: 4KHZ\_502.** When set DS26503\_TS\_8K ← DS26503\_400hz.

**Bit 0: RS\_8K.** When set DS26503\_TS\_8K ← DS26503\_RS\_8K.

## DS26503 INFORMATION

For more information about the DS26503, consult the DS26503 data sheet available on our website at [www.maxim-ic.com/DS26503](http://www.maxim-ic.com/DS26503). Software downloads are also available for this design kit.

## DS26503DK INFORMATION

For more information about the DS26503DK, including software downloads, consult the DS26503DK data sheet available on our website at [www.maxim-ic.com/DS26503DK](http://www.maxim-ic.com/DS26503DK).

## TECHNICAL SUPPORT

For additional technical support, go to [www.maxim-ic.com/support](http://www.maxim-ic.com/support).

## SCHEMATICS

The DS26503DK schematics are featured in the following pages.

## DOCUMENT REVISION HISTORY

REVISION DATE	DESCRIPTION
110205	Initial DS26503DK data sheet release.
071006	Updated descriptions for FPGA Control Registers LEVEL1 to LEVEL10.
110106	Updated schematics.
031507	Corrected typo on Bit 0 of TSERsrc register Corrected typo on Bit 0 of TS_8Ksrc register

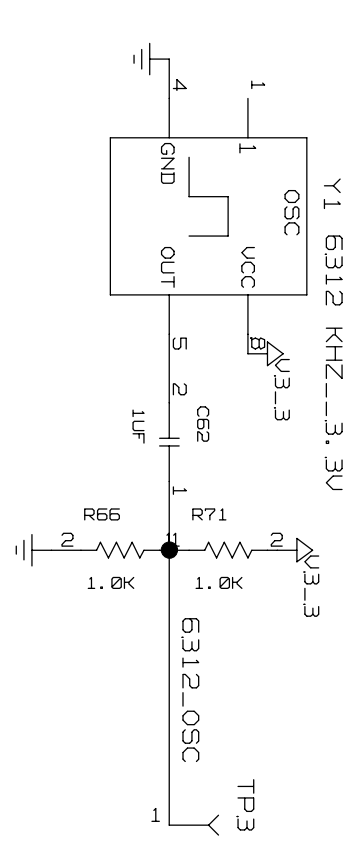
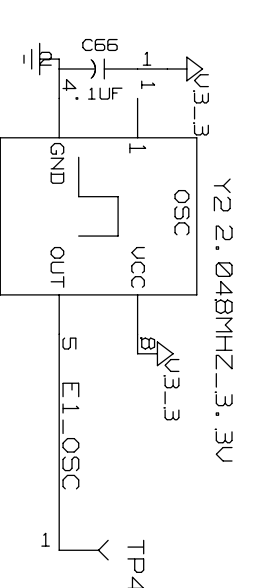
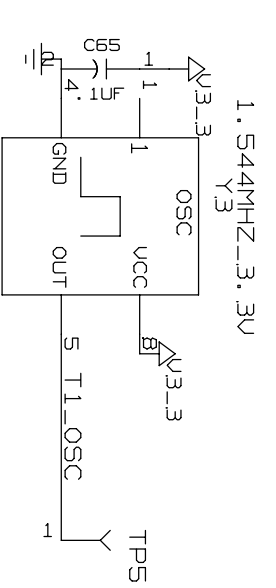
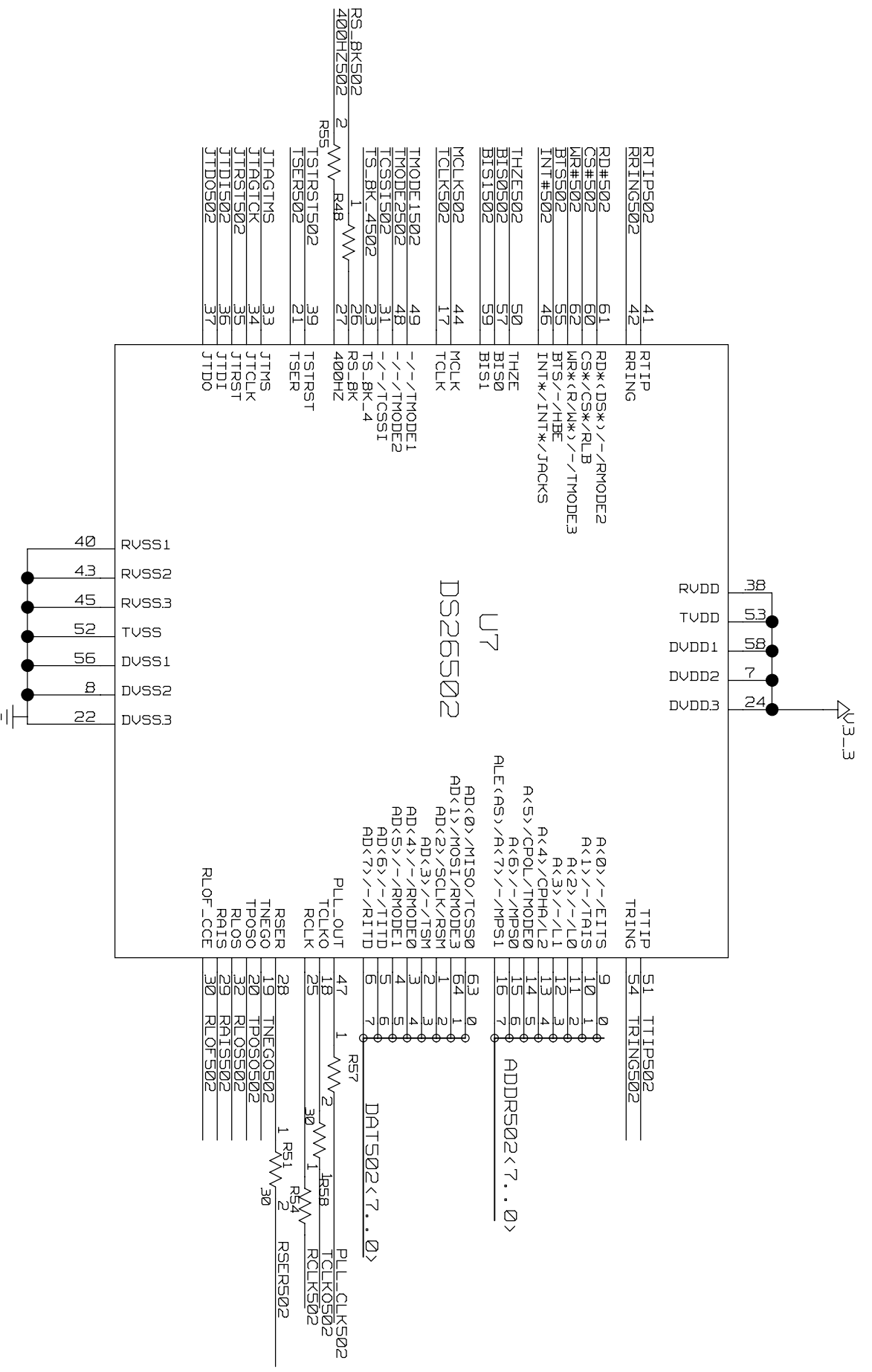


# DS26502 DESIGN KIT

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2. DS26502 AND OSCILLATORS
3. DS26502 LINE BUILD OUT
4. XILINX CLOCK MUX AND BUS CONVERSION
5. TEST POINTS FOR DS26502
6. MMC2107 PROCESSOR
7. PROCESSOR CONFIGURATION
8. XILINX CONFIGURATION AND CORE VOLTAGE
9. SERIAL PORTS AND JTAG CONFIGURATION
10. MEMORY
11. PROCESSOR TEST POINTS
12. FLASH VOLTAGE AND DECOUPLING
13. SIGNAL CROSS REFERENCE
14. PART CROSS REFERENCE AND REVISION HISTORY

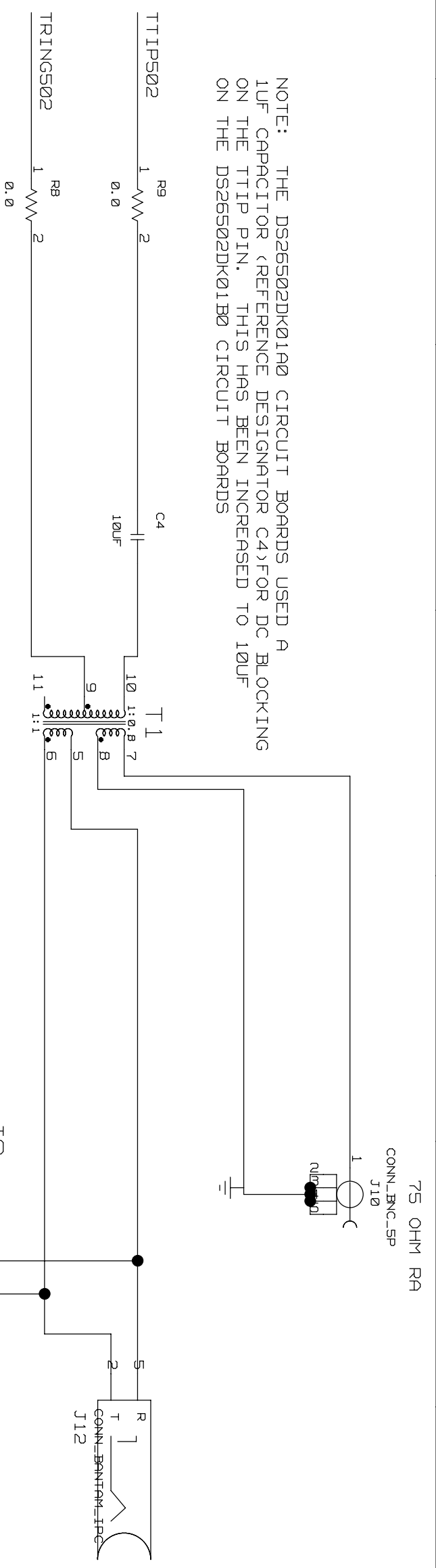
CONVERTED TO PDF: Fri Oct 20 10:08:32 2006

TITLE:	DS26502DK01B0	DATE:	041205
ENGINEER:	STEVE SCULLY	PAGE:	1 / 14

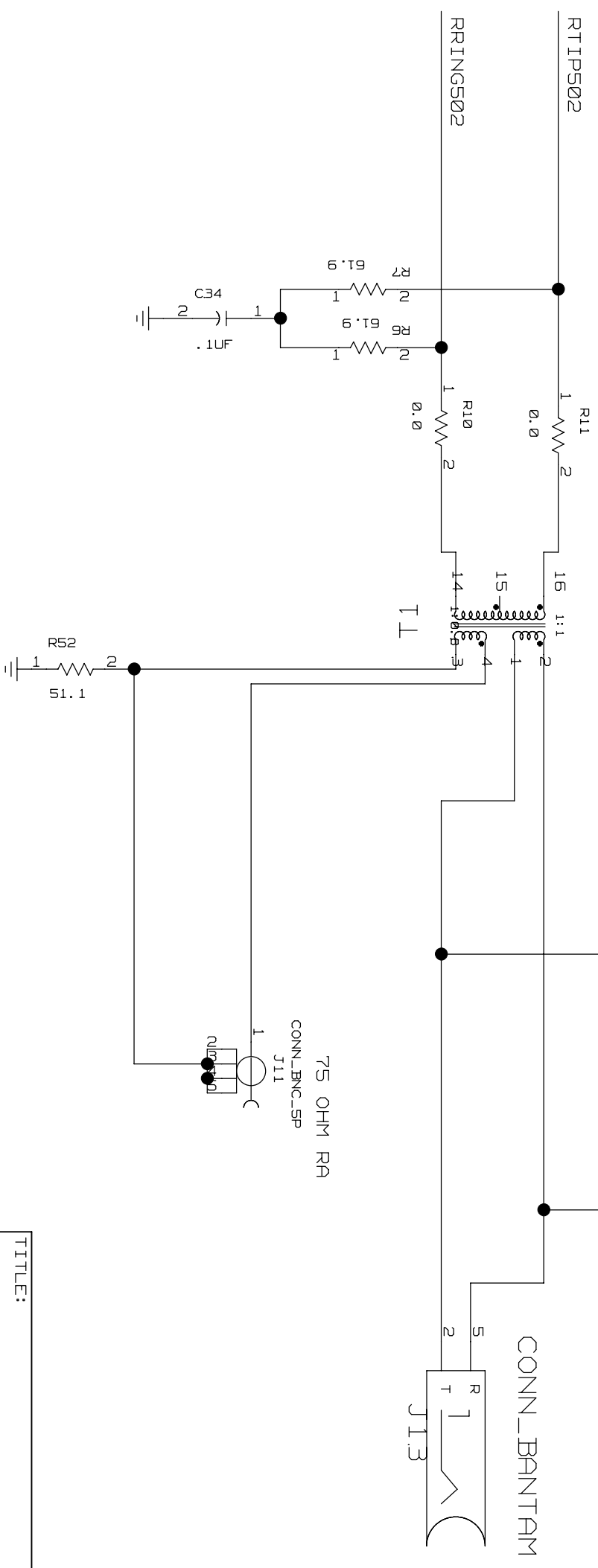


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NOTE: THE DS26502DK01A0 CIRCUIT BOARDS USED A 1UF CAPACITOR (REFERENCE DESIGNATOR C4)FOR DC BLOCKING ON THE TTIP PIN. THIS HAS BEEN INCREASED TO 10UF ON THE DS26502DK01B0 CIRCUIT BOARDS

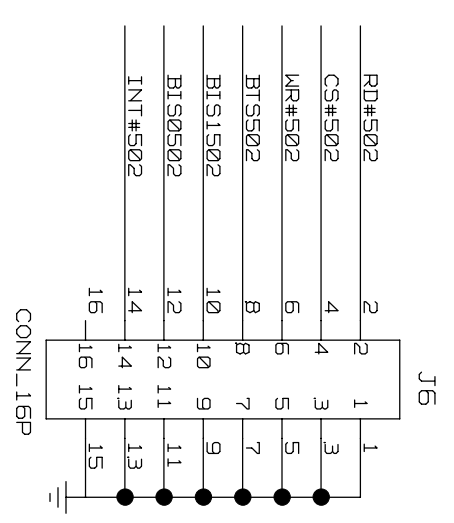
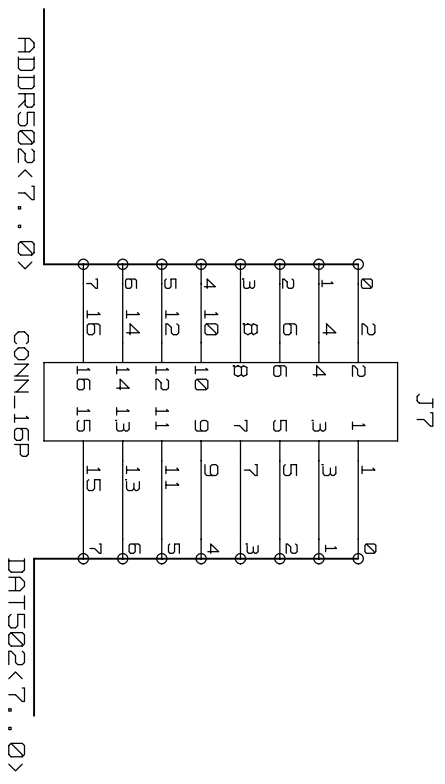
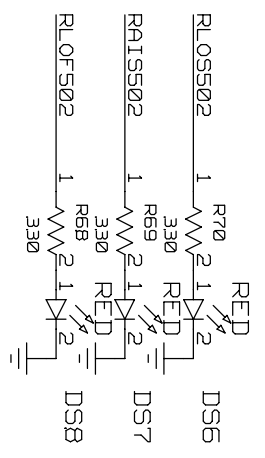
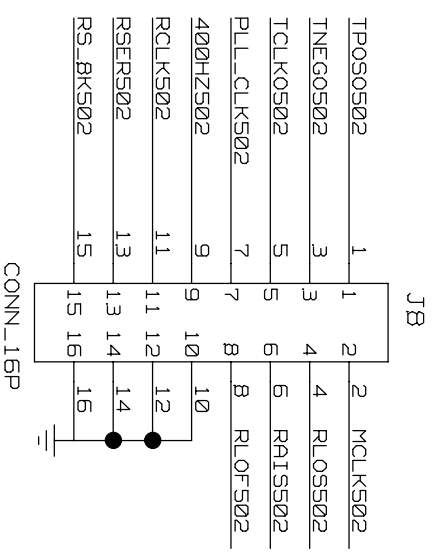
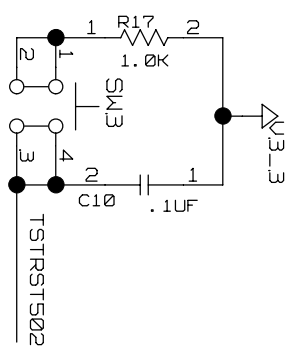


NOTE: BOARD REVISIONS DS26502DK01A0 AND DS26502DK01B0 DO NOT USE THE CORRECT PIN NUMBERS ON THE RJ48 CONNECTOR (REFERENCE DESIGNATOR J9). THE RJ48 CONNECTOR SHOULD BE REMOVED SINCE IT HAS NON-STANDARD CONNECTION. THE SCHEMATIC HAS BEEN UPDATED AND IS CORRECT.

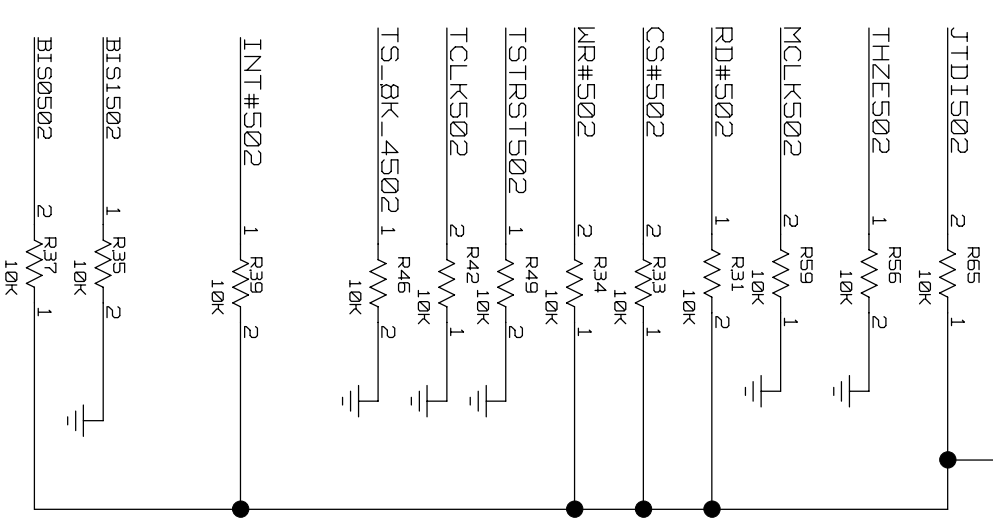


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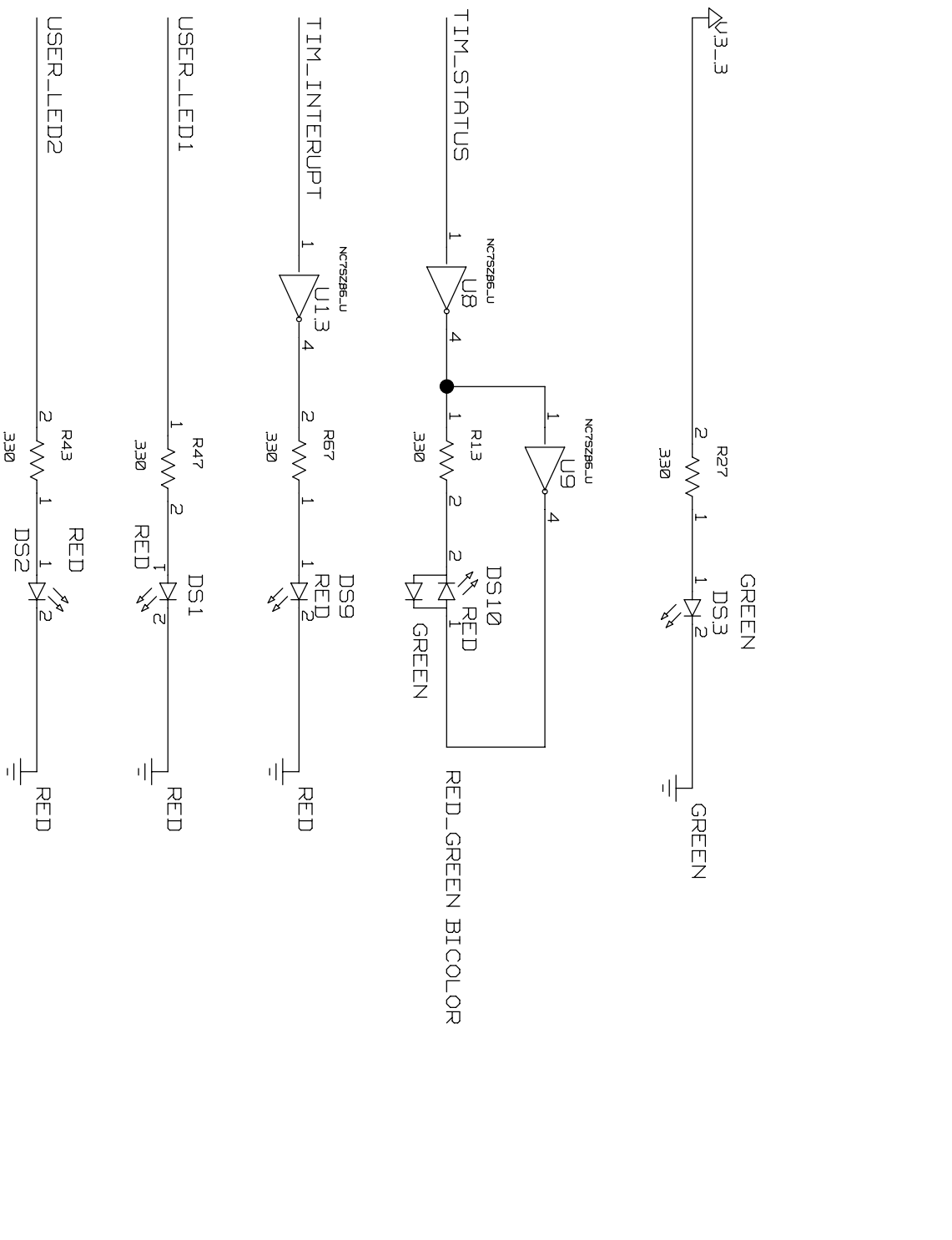
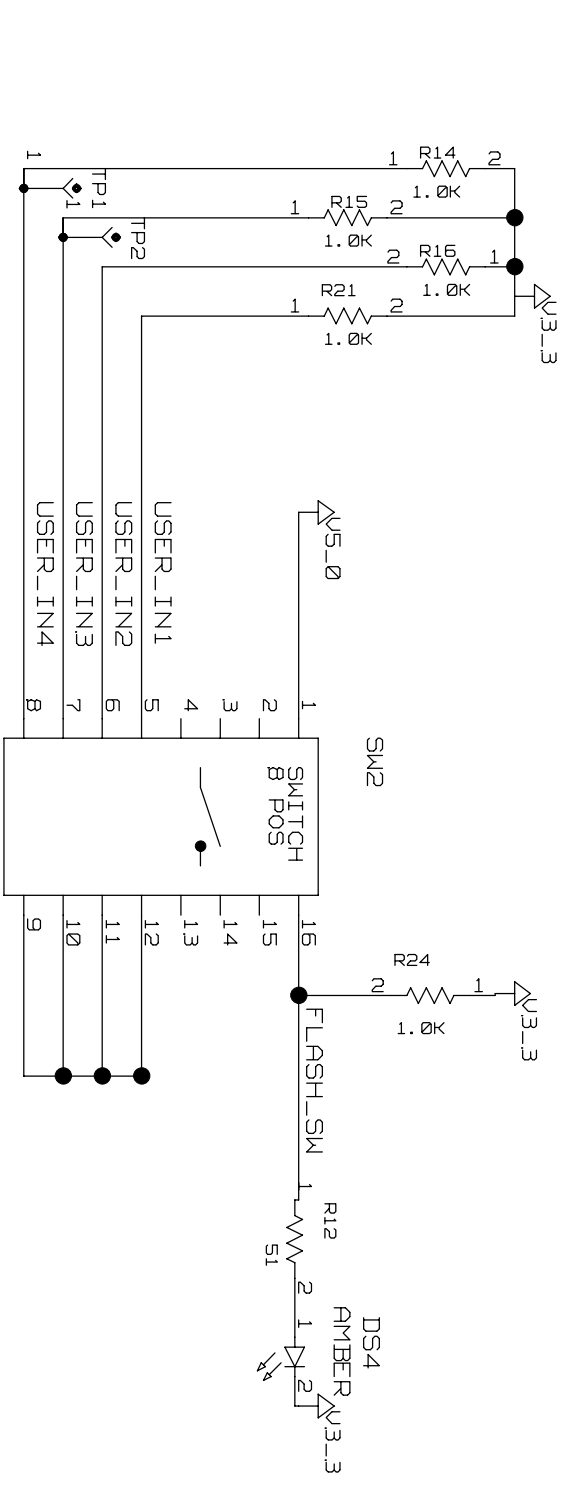
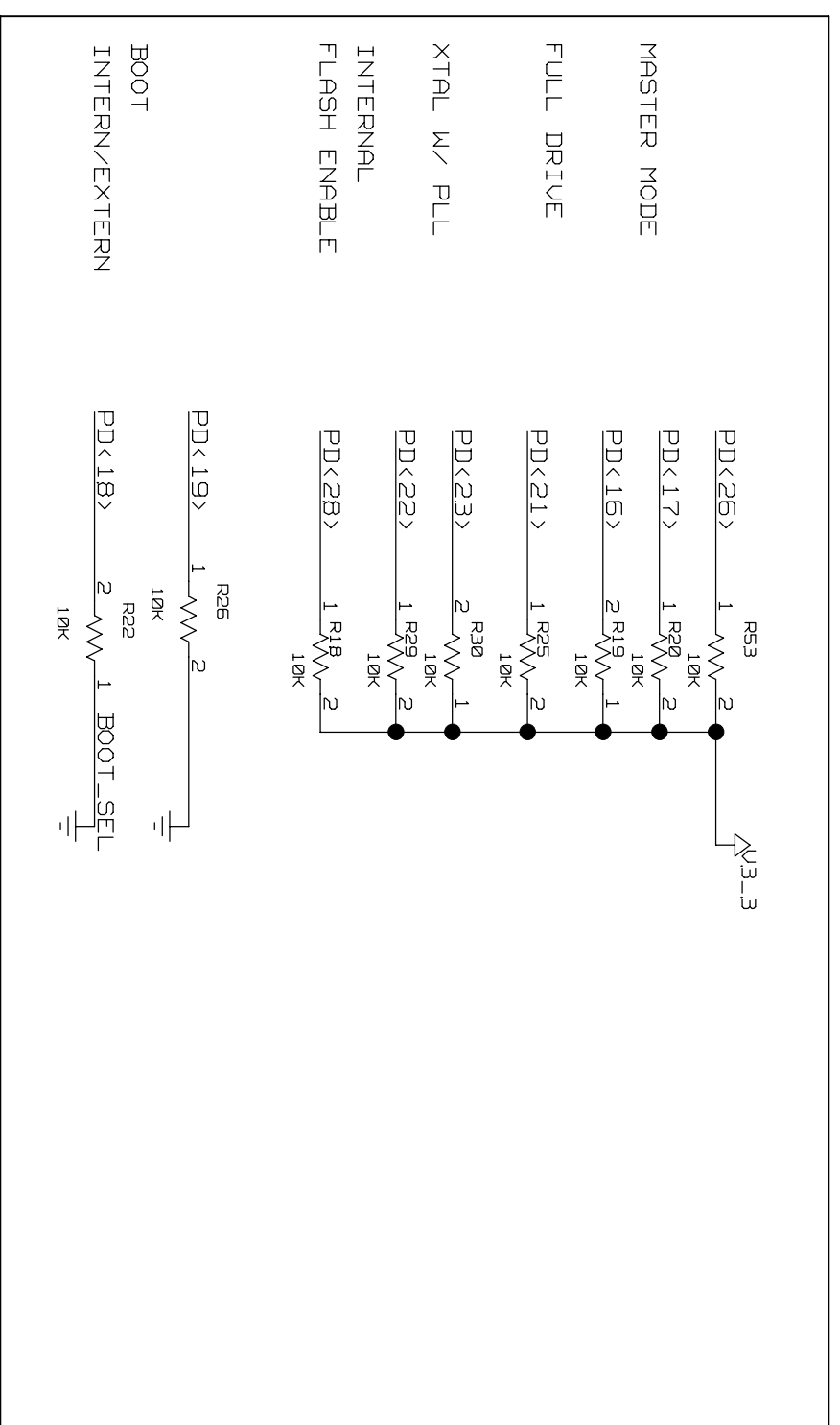
BIS01:0J : 01 = PARALLEL PORT MODE  
 DEFAULT MODE (NON-MULTIPLEXED)



TITLE:	DS26S02DK01B0	DATE:	041205
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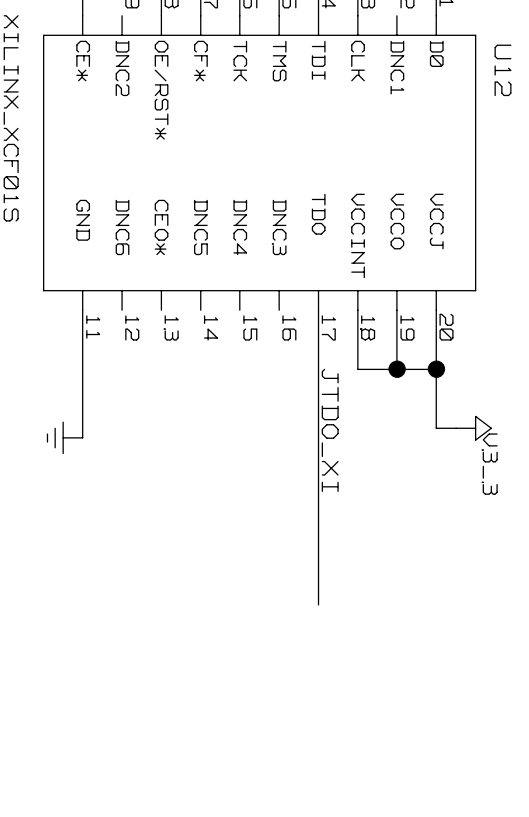
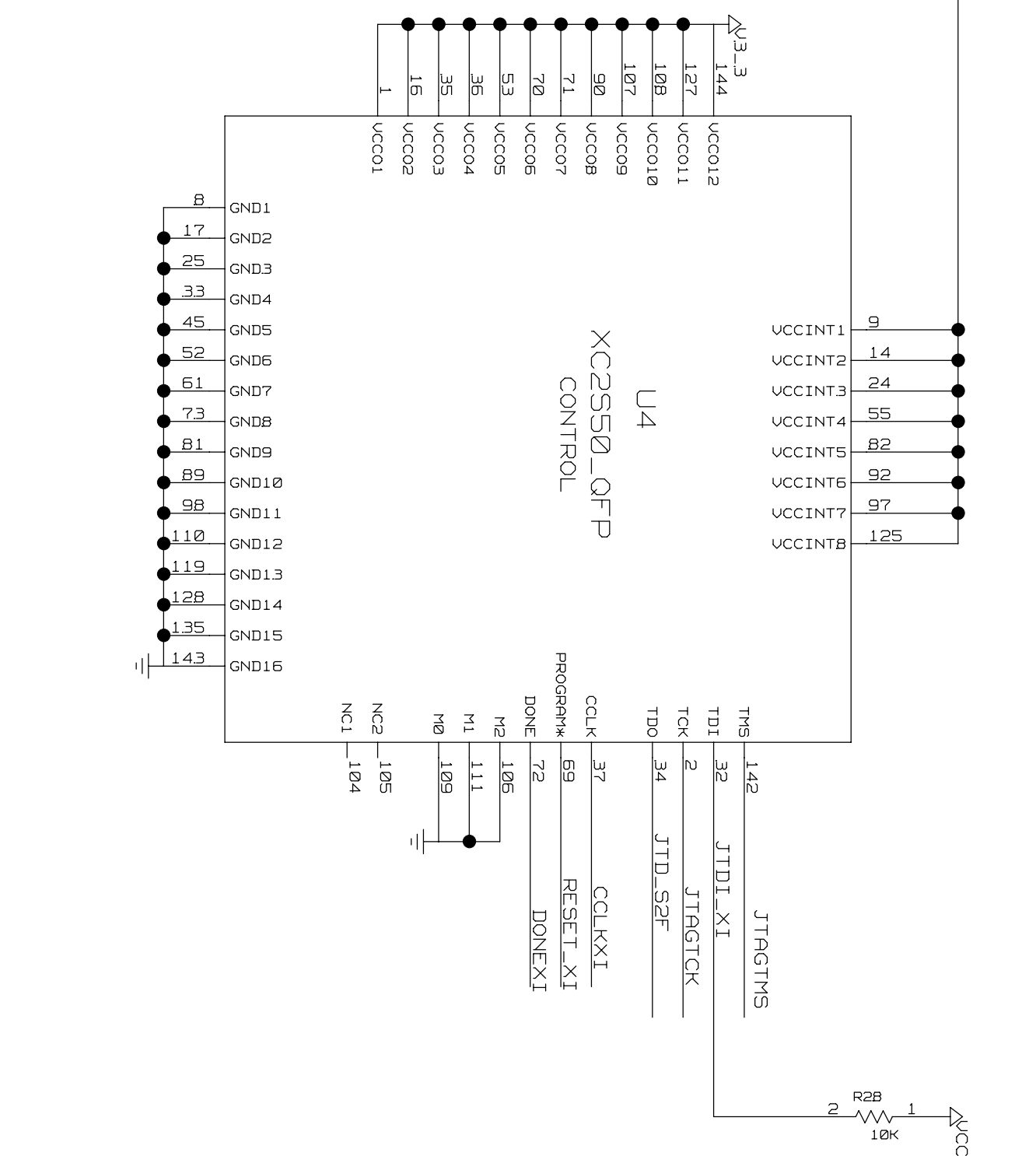
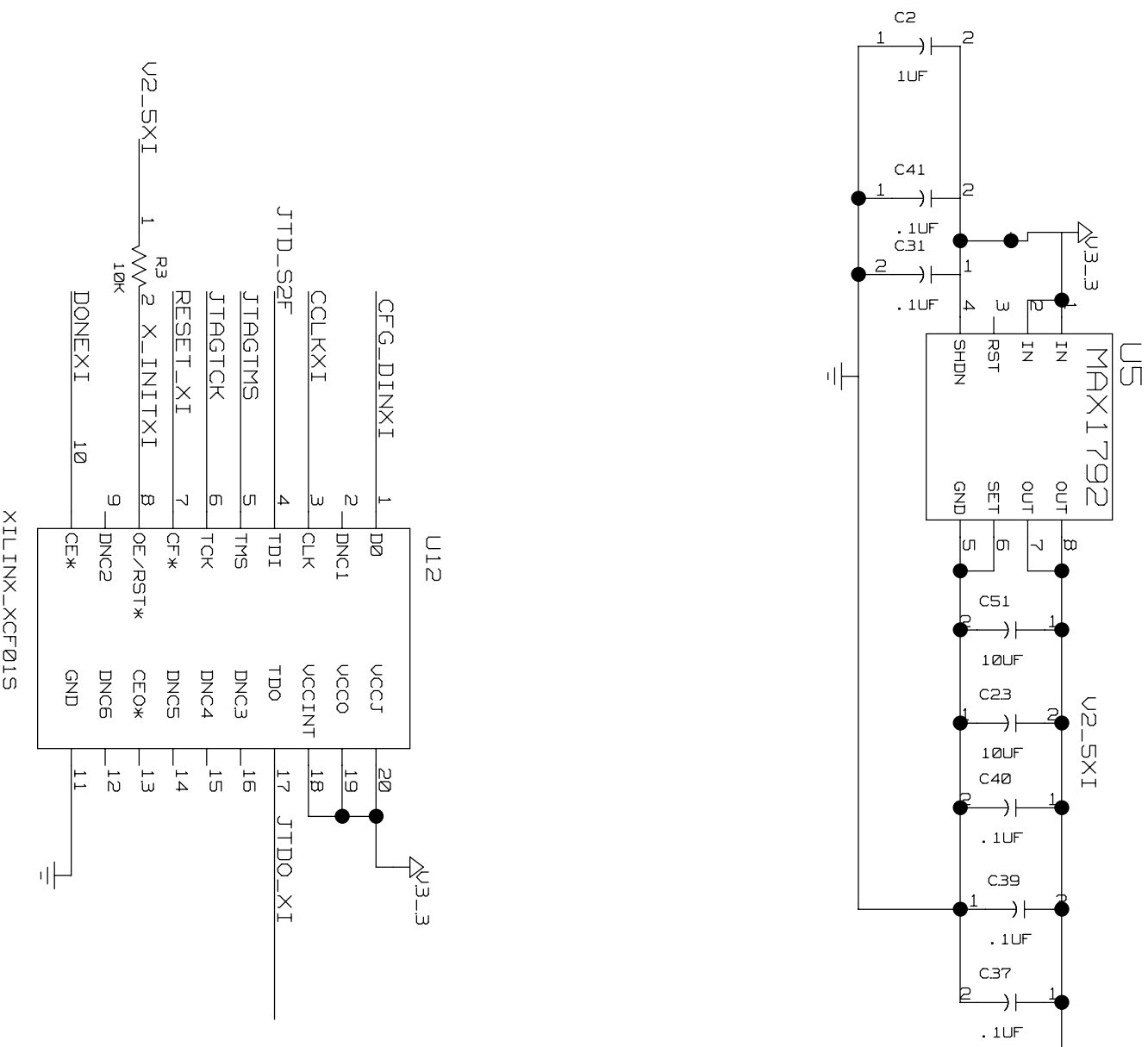


# RESET CONFIGURATION



## RESET AND CHIP CONFIGURATION

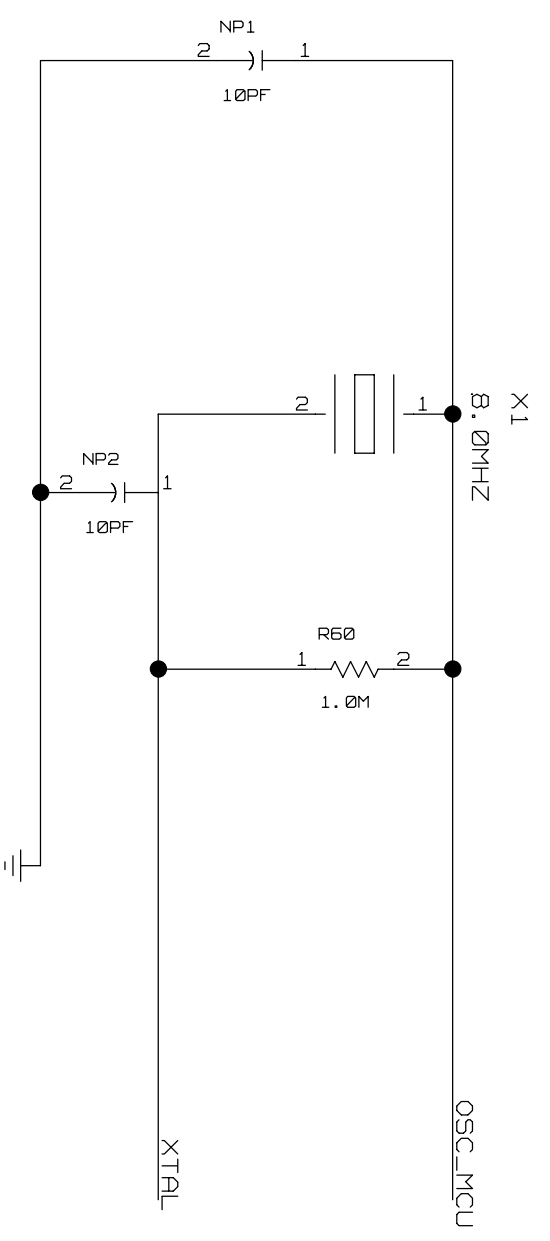
TITLE:	DS26502DK01B0	DATE:	041205
ENGINEER:	STEVE SCULLY	PAGE:	7 / 14



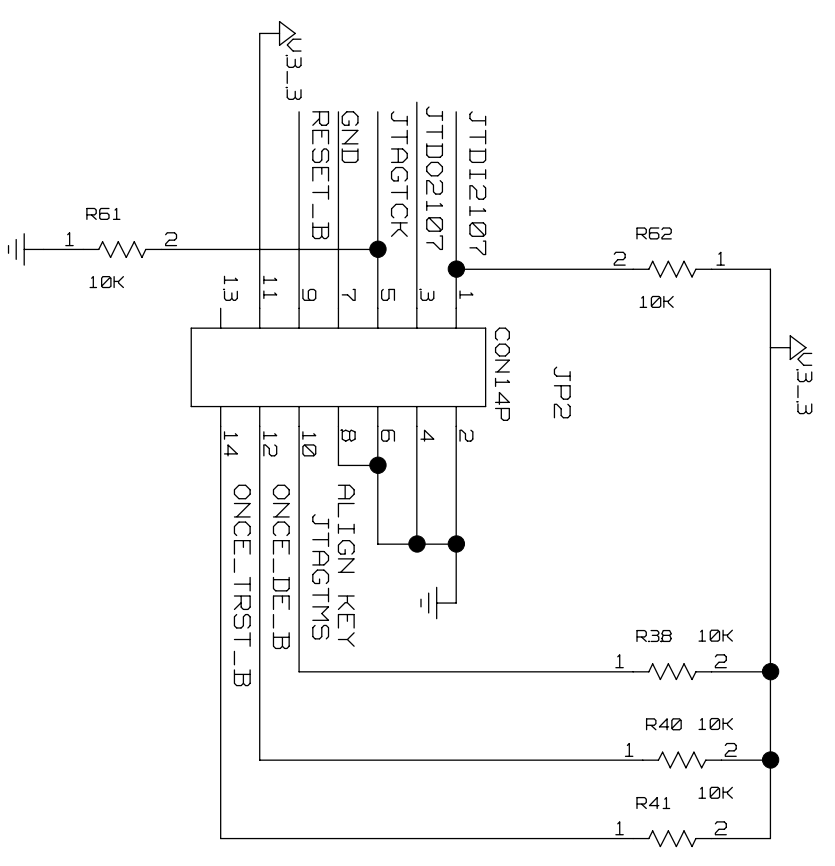
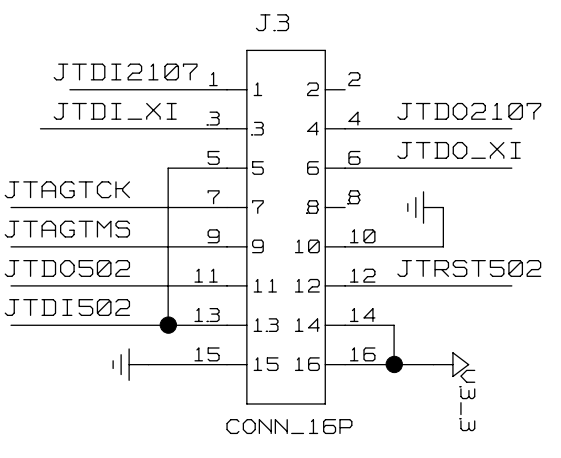
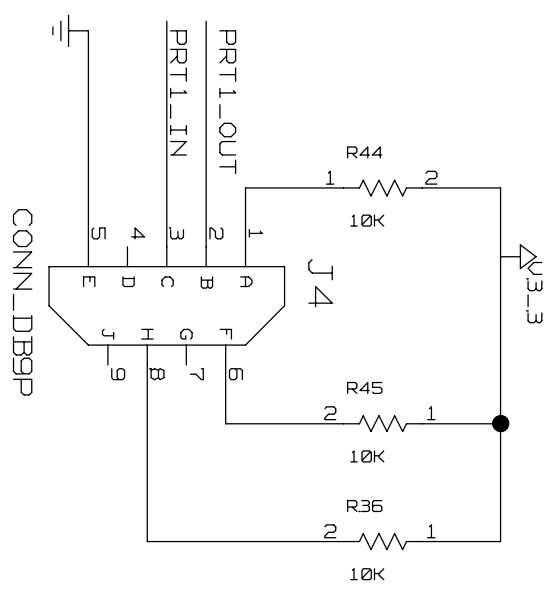
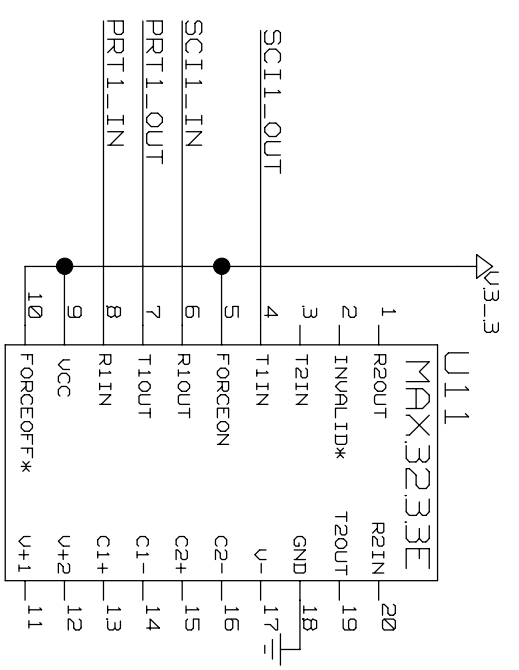
CLOCKS

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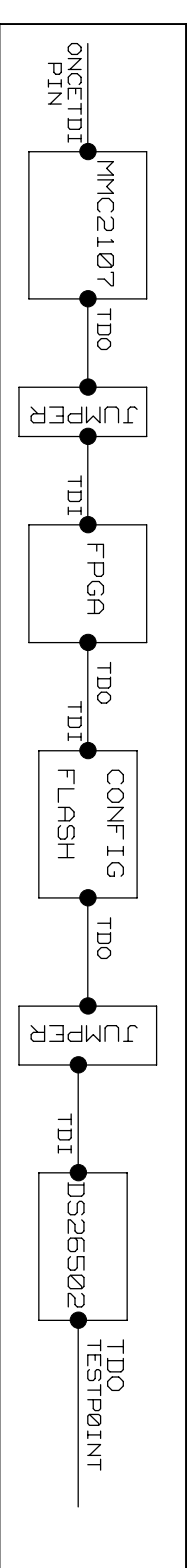




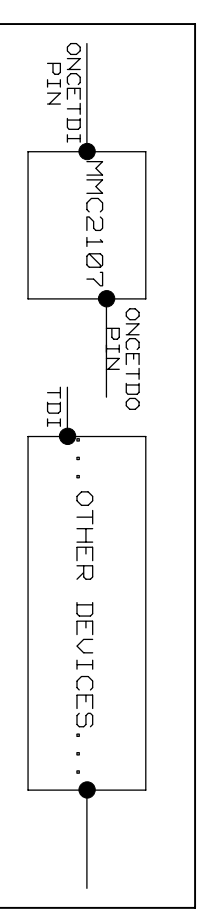
JTAG / ONCE  
DEBUG SELECTION



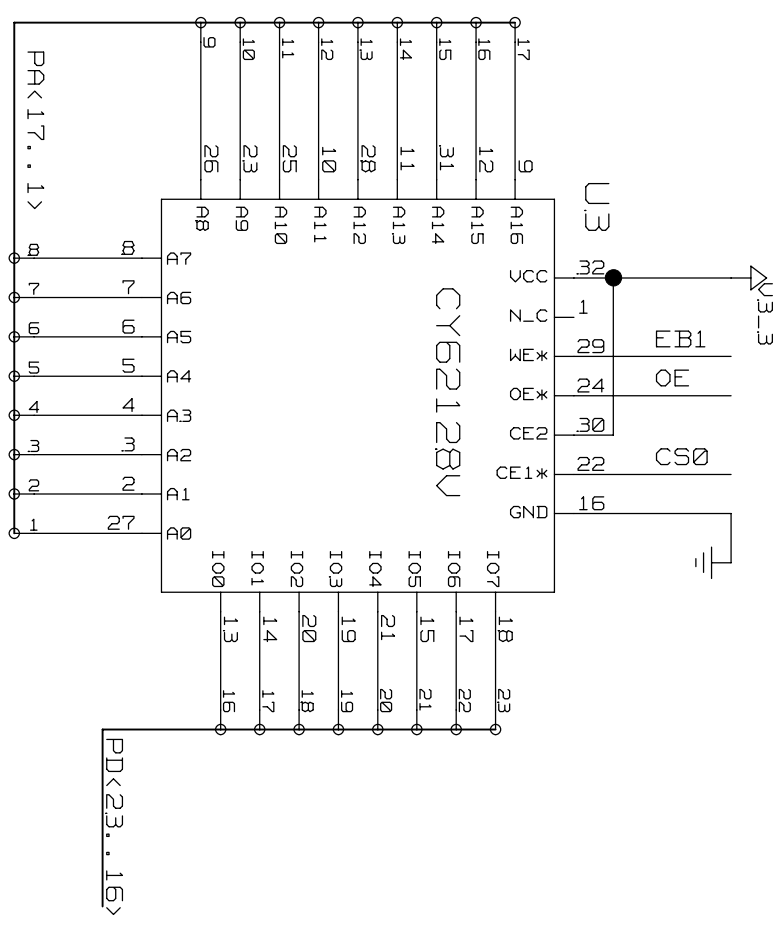
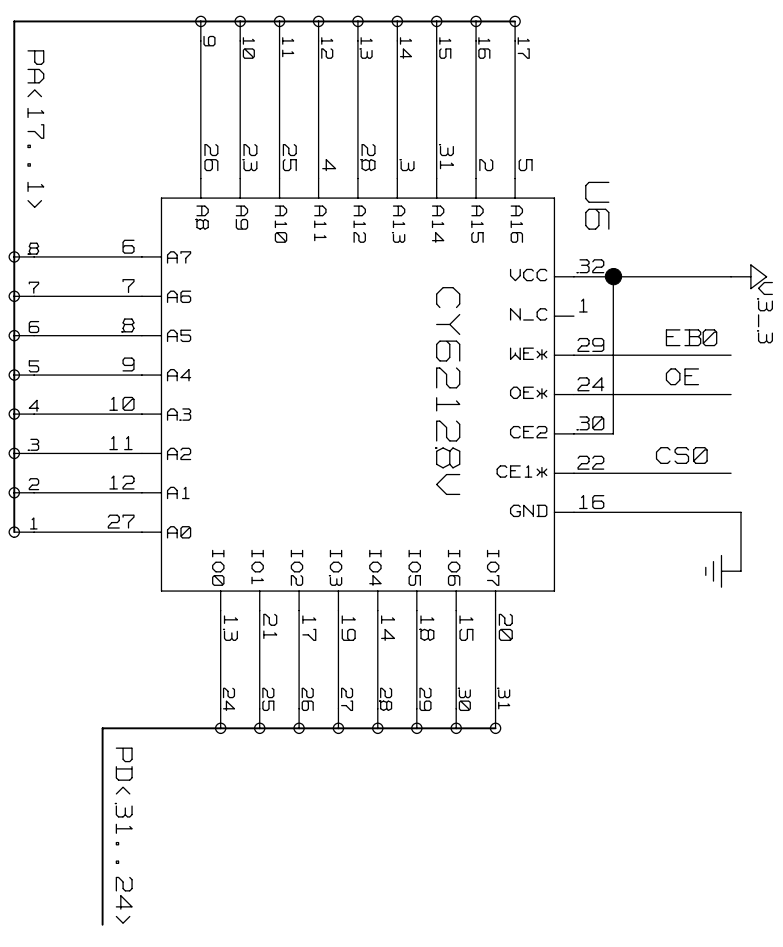
JTAG CONFIGURATION (BOUNDARY SCAN)



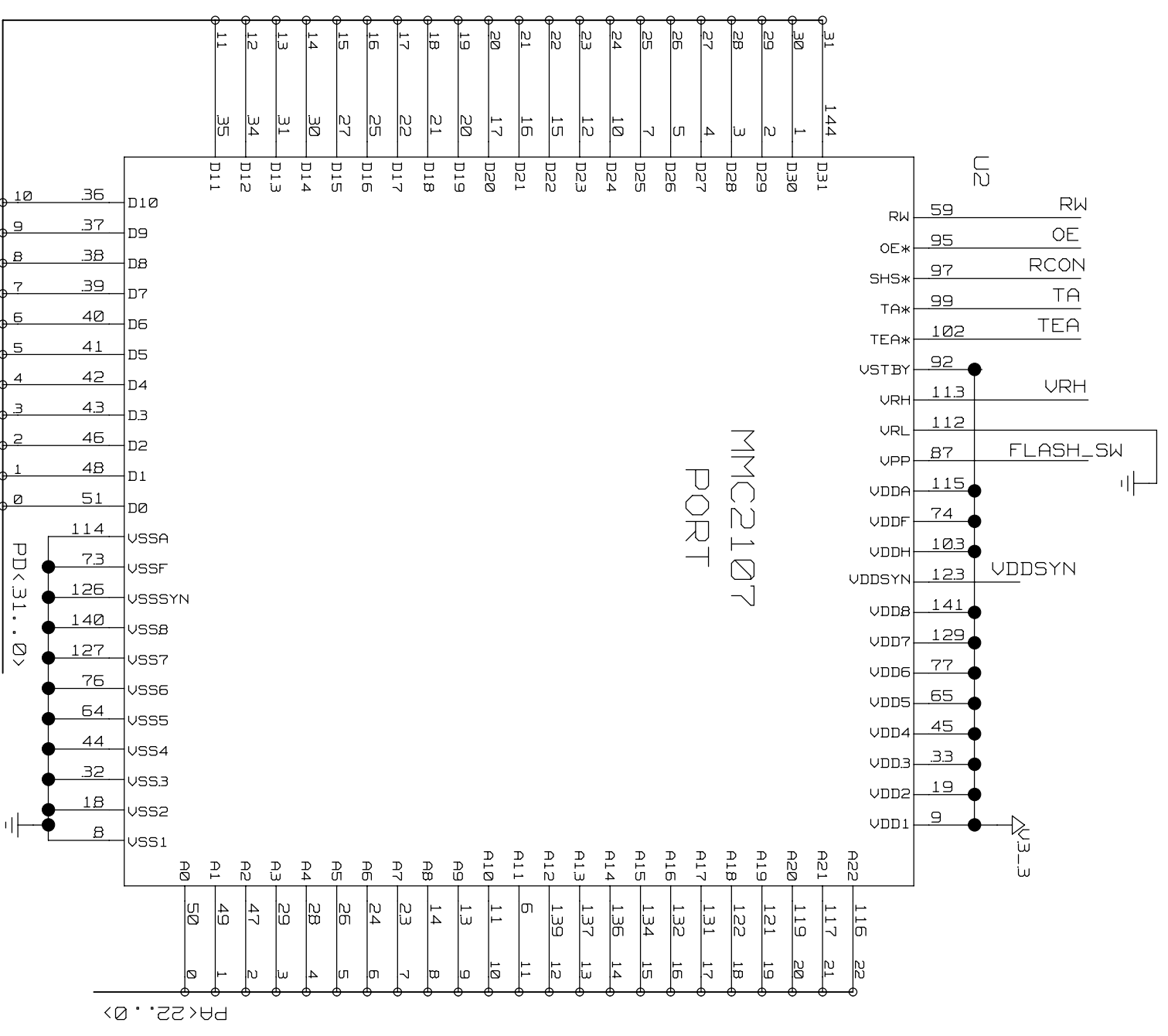
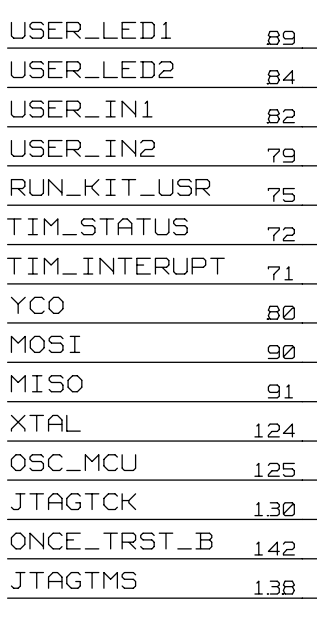
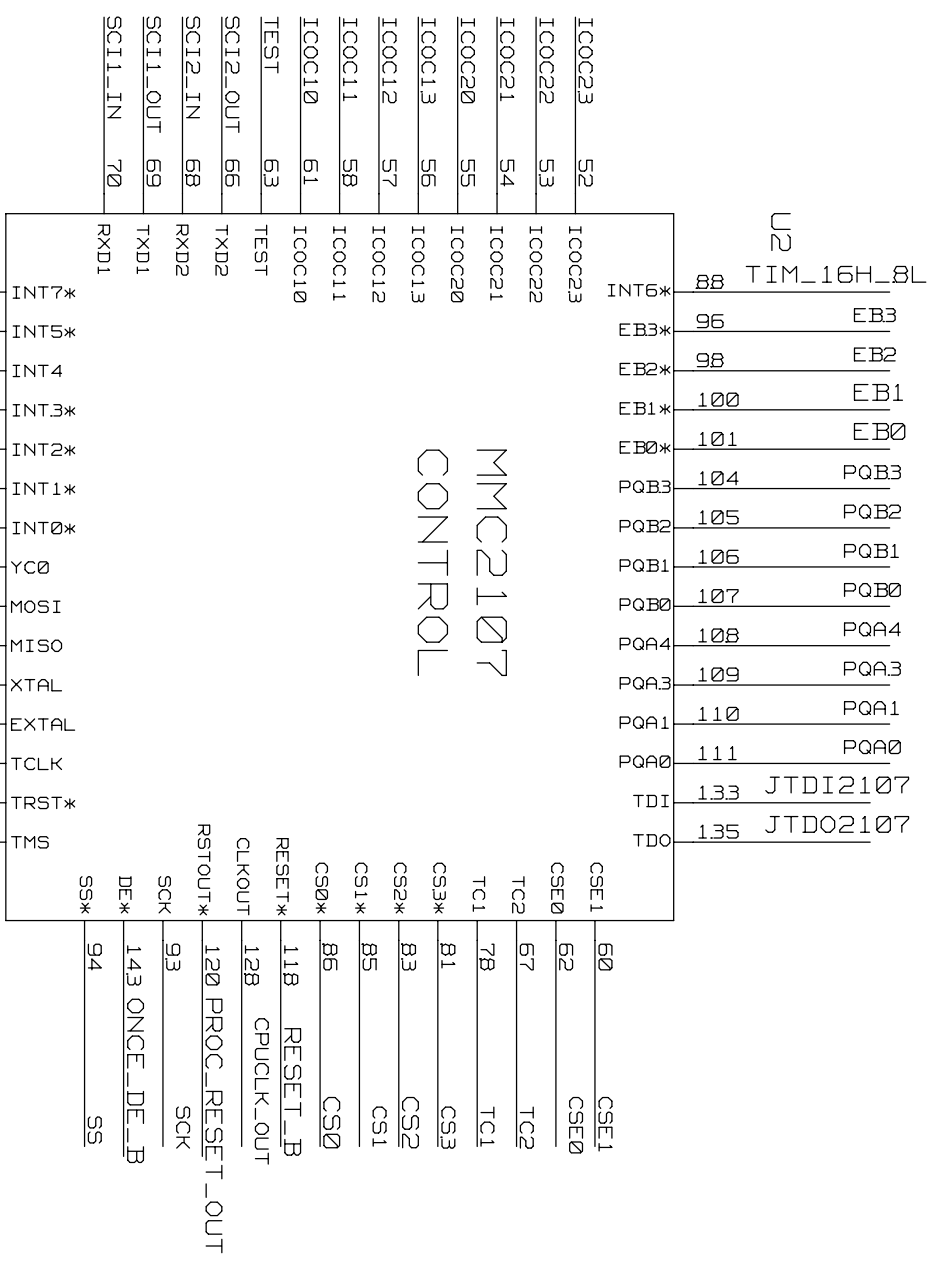
PROCESSOR DEBUG CONFIGURATION (ONCE)



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TEST-POINTS FOR PROCESSOR

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\*\*\* Signal Cross-Reference for the entire design \*\*\*

```

400HZ502      4D6<> 5CB<> 2CB<
6312_05C      2A1<> 4D6<>
ADDR502<7..0> 2C4> 4C1 5D4<
BIS0502       4A3<> 5B4<> 2CB< 5A2<
BIS1502       4A2<> 5B4<> 2CB< 5A3<
BOOT_SEL      7B5<
BT5502        4A2<> 5B4<> 2CB<
CCLKXI        B77<> BC1<
CFG_DINXI     4B2<> B77<>
CPULCK_OUT    4B5<> 11B5<> 4CB<
CS#502        4A3<> 5B4<> 2CB< 5C2<
CS0           6B5<> 10D3<> 10D6<> 11C5<>
CS1           6C5<> 11C5<>
CS2           4A6<> 6C5<> 11C5<>
CS3           6C5<> 11C5<>
CSE0          6C5<> 11C5<>
CSEL1         6C5<> 11C5<>
DAT502<7..0> 2C4> 5C2> 4C4
D0NEXI        B77<> BB1<
E1_05C        2B2<> 4D6<>
EB0           4B5<> 6D7<> 10D7<> 11D7<>
EB1           4B5<> 6D7<> 10D3<> 11D7<>
EB2           6D7<> 11D7<>
EB3           6D7<> 11D7<>
EXT_05C       4D2<>
FLASH_SM      7D2<> 6D2< 11D3<
IC0C10        6B8<> 11B8<>
IC0C11        6B8<> 11CB<>
IC0C12        6CB<> 11CB<>
IC0C13        6CB<> 11CB<>
IC0C20        6CB<> 11CB<>
IC0C21        6CB<> 11CB<>
IC0C22        6CB<> 11CB<>
IC0C23        6CB<> 11CB<>
INT#502       2CB> 4B2<> 5B4<> 5B2<
JTAGTCK       6A6<> B77<> 9B4<> 9C3<> 11A6<>
                2B8< BC1<
                6A6<> B77<> 9B4<> 9C2<> 11A6<>
                2CB< BC1<
                9B4<> 2B8< 5C2<
                6D6<> 9B5<> 9C3<> 11D6<>
                9B5<> BC2<
                2B8> 9B4<>
                6D6<> 9C3<> 9C5<> 11D6<>
                B85<> 9C5<>
                B77<> BC1>
                9C4<> 2B8<
                5C7<> 2CB< 4A3< 5C2<
                4A3<>
                4A6<> 6A6<> 11A7<>
                4A6<> 6A6<> 11A7<>
                4A6<> 6D3<> 10D3<> 10D7<> 11D3<>
                6B5<> 9B2<> 11B5<>
                6A6<> 9B2<> 11A6<>
                6A6<> 9D5<> 11A6<>
                4C4
                6B1> 11A1>
                PA<17..1> 10B4 10B7
                PD<31..0> 6A2> 11A2>
                PD<23..16> 10B2>
                PD<31..16> 4B8 4B8
                PD<31..24> 10B5>
                PLL_CLKS02 4D6<> 5CB<> 2C4<
                POA0      6D6<> 11D6<>
                POA1      6D6<> 11D6<>
                POA3      6D6<> 11D7<>
                POA4      6D6<> 11D7<>
                POB0      6D6<> 11D7<>
                POB1      6D7<> 11D7<>
                POB2      6D7<> 11D7<>
                POB3      6D7<> 11D7<>
                PROC_RESET_OUT 4D6<> 6B5<> 11B5<>
                PRT1_IN  9A8<> 9B8<
                PRT1_OUT 9A8<> 9B8>
                RA15S02 2B4> 5C7<> 5B8<
    
```

```

RCLKS02       5B8<> 2C4<
RCON          6D3<> 11D3<> 7B8<
RD#502        4A3<> 5B4<> 2D8< 5C2<
RESET_B       6B5<> 9C3<> 11B5<> 7A6<
RESET_XI      7A7<> B77<> BC1<
RLOF502       2B4> 5C7<> 5B8<
RLOS502       2B4> 5C7<> 5B8<
RRING502      2D8< 3B7<
RERS502       4B1<> 5B8<> 2C4<
RS_BK502      4D6<> 5B8<> 2CB<
RTIPS02       2D8< 3B7<
RUN_KIT_USR   6A7<> 11A7<>
RM            4A6<> 6D3<> 11D3<>
SCI1_IN       6B8<> 9B8> 11B8<>
SCI1_OUT      6B8<> 11B8<> 9B8<
SCI2_IN       6B8<> 11B8<>
SCI2_OUT      6B8<> 11B8<>
SCK           4A6<> 6B5<> 11B5<>
SS            4A5<> 6B5<> 11B5<>
T1_05C        2D2<> 4D6<>
TA            4A6<> 6D3<> 11D3<>
TC1           6C5<> 11C5<>
TC2           6C5<> 11C5<>
TCLKS02       2CB< 4A3< 5B2<
TCLKS02XI     4A3<>
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TCLKS02       2CB<> 4D3<>
TCSS1502      6D3<> 11D3<>
TEA           6B8<> 11B8<>
TEST          6B8<> 11B8<>
THZ502        4A3<> 2CB< 5C2<
TIM_1BH_BL    6D7<> 11D8<>
TIM_INTERRUPT 4B1> 6A7<> 7A4<> 11A7<>
TIM_STATUS    6A7<> 7B4<> 11A7<>
TMODE1502     4D3<> 2CB<
TMODE2502     4D3<> 2CB<
TNEG0502      2C4> 5CB<>
TPOS0502      2B4> 5CB<>
TRINGS02      2D4> 3CB<
TSERS02       4B1<> 2CB<
TSTR502       5D8<> 2CB< 5B2<
TS_BK_4502    4A3<> 2CB< 5B2<
TTIPS02       2D4> 3CB<
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USER_IN2      6A7<> 7C3<> 11A7<>
USER_IN3      7C3<>
USER_IN4      7C3<>
USER_LED1     6A7<> 11A8<> 7A4<
USER_LED2     6A7<> 11A7<> 7A4<
V2_5XI        8D6<> 8A8<
VSU           12D4<>
VDD5YN        6D2< 11D2< 12C1<
WR#502        6D3< 11D3<
XTRL          4A3<> 5B4<> 2CB< 5B2<
X_INITXI      6A6<> 9C5<> 11A7<>
YCO           4A2<> B77<>
                6A7<> 11A7<>
    
```

TITLE: DS26502DK01B0 DATE: 041205

ENGINEER: STEVE SCULLY PAGE: 13/14

\*\*\* Part Cross-Reference for the entire design \*\*\*

C1	CAP1	12A5
C2	CAP1	BCB
C3	CAP	12B5
C4	CAP	3D5
C5	CAP1	12B3
C6	CAP	12B5
C7	CAP	12B1
C8	CAP	12B4
C9	CAP	12B5
C10	CAP1	5D8
C11	CAP	12B3
C12	CAP	12B2
C13	CAP	12C6
C14	CAP	12B5
C15	CAP	12B3
C16	CAP1	12A4
C17	CAP	12B6
C18	CAP	12B1
C19	CAP	12C5
C20	CAP	12B3
C21	CAP	12B5
C22	CAP1	12A4
C23	CAP1	BC5
C24	CAP1	12A4
C25	CAP	12B3
C26	CAP	12B3
C27	CAP	12B5
C28	CAP	12C6
C29	CAP	12B5
C30	CAP	12B6
C31	CAP1	BC8
C32	CAP	12B7
C33	CAP	12B2
C34	CAP1	3A6
C35	CAP	12C4
C36	CAP	12B7
C37	CAP1	BC5
C38	CAP	12B5
C39	CAP1	BC6
C40	CAP1	BC6
C41	CAP1	BC8
C42	CAP	12C5
C43	CAP1	12A5
C44	CAP	12C7
C45	CAP	12B5
C46	CAP	12B5
C47	CAP	12C5
C48	CAP	12B4
C49	CAP	12C6
C50	CAP	12B6
C51	CAP1	BC7
C52	CAP	12B3
C53	CAP1	12A3
C54	CAP	12B2
C55	CAP	12B1
C56	CAP	12C3
C57	CAP	12B1
C58	CAP1	4D1
C59	CAP	12B4
C60	CAP1	12A4
C61	CAP	12D3
C62	CAP1	2A2
C63	CAP	12D4
C64	CAP	12D4
C65	CAP1	2D3
C66	CAP1	2B3
C67	CAP1	12A4
C68	CAP	12B2
C69	CAP1	12C2
C70	CAP1	12A5
D1	DIODE	12C4
DS1	LED	7A3
DS2	LED	7A3
DS3	LED	7B3
DS4	LED	7D1

DS5	LED	4B1
DS6	LED	5B7
DS7	LED	5B7
DS8	LED	5B7
DS9	LED	7B3
DS10	LED2	7B3
J1	CONN_BANANA_2P	12D7
J2	CONN_BANANA_2P	12C7
J3	CONN_16P	9B5
J4	CONN_D50P	9A7
J5	CONN_16P	5D1
J6	CONN_16P	5B3
J7	CONN_16P	5D3
J8	CONN_16P	5C7
J9	CONN_R748	3B4
J10	CONN_16P	3D3
J11	CONN_16P	3A4
J12	CONN_BANTAM_IPC	3C2
J13	CONN_BANTAM	3B2
J14	CONN_16P	12B5
J15	CONN_16P	9C2
J16	CONN_16P	12B5
J17	CONN_16P	12B5
J18	CONN_16P	12B5
J19	CONN_16P	12B5
J20	CONN_16P	12B5
J21	CONN_16P	12B5
J22	CONN_16P	12B5
J23	CONN_16P	12B5
J24	CONN_16P	12B5
J25	CONN_16P	12B5
J26	CONN_16P	12B5
J27	CONN_16P	12B5
J28	CONN_16P	12B5
J29	CONN_16P	12B5
J30	CONN_16P	12B5
J31	CONN_16P	12B5
J32	CONN_16P	12B5
J33	CONN_16P	12B5
J34	CONN_16P	12B5
J35	CONN_16P	12B5
J36	CONN_16P	12B5
J37	CONN_16P	12B5
J38	CONN_16P	12B5
J39	CONN_16P	12B5
J40	CONN_16P	12B5
J41	CONN_16P	12B5
J42	CONN_16P	12B5
J43	CONN_16P	12B5
J44	CONN_16P	12B5
J45	CONN_16P	12B5
J46	CONN_16P	12B5
J47	CONN_16P	12B5
J48	CONN_16P	12B5
J49	CONN_16P	12B5
J50	CONN_16P	12B5
J51	CONN_16P	12B5
J52	CONN_16P	12B5
J53	CONN_16P	12B5
J54	CONN_16P	12B5
J55	CONN_16P	12B5
J56	CONN_16P	12B5
J57	CONN_16P	12B5
J58	CONN_16P	12B5
J59	CONN_16P	12B5
J60	CONN_16P	12B5
J61	CONN_16P	12B5
J62	CONN_16P	12B5
J63	CONN_16P	12B5
J64	CONN_16P	12B5
J65	CONN_16P	12B5
J66	CONN_16P	12B5
J67	CONN_16P	12B5
J68	CONN_16P	12B5
J69	CONN_16P	12B5
J70	CONN_16P	12B5
J71	CONN_16P	12B5
J72	CONN_16P	12B5
J73	CONN_16P	12B5
J74	CONN_16P	12B5
J75	CONN_16P	12B5
J76	CONN_16P	12B5
J77	CONN_16P	12B5
J78	CONN_16P	12B5
J79	CONN_16P	12B5
J80	CONN_16P	12B5
J81	CONN_16P	12B5
J82	CONN_16P	12B5
J83	CONN_16P	12B5
J84	CONN_16P	12B5
J85	CONN_16P	12B5
J86	CONN_16P	12B5
J87	CONN_16P	12B5
J88	CONN_16P	12B5
J89	CONN_16P	12B5
J90	CONN_16P	12B5
J91	CONN_16P	12B5
J92	CONN_16P	12B5
J93	CONN_16P	12B5
J94	CONN_16P	12B5
J95	CONN_16P	12B5
J96	CONN_16P	12B5
J97	CONN_16P	12B5
J98	CONN_16P	12B5
J99	CONN_16P	12B5
J100	CONN_16P	12B5
L1	COTL_2P	12C3
MNT_HOLE1	MNT_HOLE	12A6
MNT_HOLE2	MNT_HOLE	12A6
MNT_HOLE3	MNT_HOLE	12A7
MNT_HOLE4	MNT_HOLE	12A6
MNT_HOLE5	MNT_HOLE	12A7
MNT_HOLE6	MNT_HOLE	12A7
MNT_HOLE7	MNT_HOLE	12A7
MNT_HOLE8	MNT_HOLE	12A7
MNT_HOLE9	MNT_HOLE	12A7
MNT_HOLE10	MNT_HOLE	12A7
MNT_HOLE11	MNT_HOLE	12A7
MNT_HOLE12	MNT_HOLE	12A7
MNT_HOLE13	MNT_HOLE	12A7
MNT_HOLE14	MNT_HOLE	12A7
MNT_HOLE15	MNT_HOLE	12A7
MNT_HOLE16	MNT_HOLE	12A7
MNT_HOLE17	MNT_HOLE	12A7
MNT_HOLE18	MNT_HOLE	12A7
MNT_HOLE19	MNT_HOLE	12A7
MNT_HOLE20	MNT_HOLE	12A7
MNT_HOLE21	MNT_HOLE	12A7
MNT_HOLE22	MNT_HOLE	12A7
MNT_HOLE23	MNT_HOLE	12A7
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MNT_HOLE26	MNT_HOLE	12A7
MNT_HOLE27	MNT_HOLE	12A7
MNT_HOLE28	MNT_HOLE	12A7
MNT_HOLE29	MNT_HOLE	12A7
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MNT_HOLE73	MNT_HOLE	12A7
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MNT_HOLE81	MNT_HOLE	12A7
MNT_HOLE82	MNT_HOLE	12A7
MNT_HOLE83	MNT_HOLE	12A7
MNT_HOLE84	MNT_HOLE	12A7
MNT_HOLE85	MNT_HOLE	12A7
MNT_HOLE86	MNT_HOLE	12A7
MNT_HOLE87	MNT_HOLE	12A7
MNT_HOLE88	MNT_HOLE	12A7
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MNT_HOLE91	MNT_HOLE	12A7
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MNT_HOLE105	MNT_HOLE	12A7
MNT_HOLE106	MNT_HOLE	12A7
MNT_HOLE107	MNT_HOLE	12A7
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MNT_HOLE110	MNT_HOLE	12A7
MNT_HOLE111	MNT_HOLE	12A7
MNT_HOLE112	MNT_HOLE	12A7
MNT_HOLE113	MNT_HOLE	12A7
MNT_HOLE114	MNT_HOLE	12A7
MNT_HOLE115	MNT_HOLE	12A7
MNT_HOLE116	MNT_HOLE	12A7
MNT_HOLE117	MNT_HOLE	12A7
MNT_HOLE118	MNT_HOLE	12A7
MNT_HOLE119	MNT_HOLE	12A7
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MNT_HOLE125	MNT_HOLE	12A7
MNT_HOLE126	MNT_HOLE	12A7
MNT_HOLE127	MNT_HOLE	12A7
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MNT_HOLE135	MNT_HOLE	12A7
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MNT_HOLE145	MNT_HOLE	12A7
MNT_HOLE146	MNT_HOLE	12A7
MNT_HOLE147	MNT_HOLE	12A7
MNT_HOLE148	MNT_HOLE	12A7
MNT_HOLE149	MNT_HOLE	12A7
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MNT_HOLE154	MNT_HOLE	12A7
MNT_HOLE155	MNT_HOLE	12A7
MNT_HOLE156	MNT_HOLE	12A7
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MNT_HOLE161	MNT_HOLE	12A7
MNT_HOLE162	MNT_HOLE	12A7
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MNT_HOLE168	MNT_HOLE	12A7
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MNT_HOLE170	MNT_HOLE	12A7
MNT_HOLE171	MNT_HOLE	12A7
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MNT_HOLE176	MNT_HOLE	12A7
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MNT_HOLE204	MNT_HOLE	12A7
MNT_HOLE205	MNT_HOLE	12A7
MNT_HOLE206	MNT_HOLE	12A7
MNT_HOLE207	MNT_HOLE	12A7
MNT_HOLE208	MNT_HOLE	12A7
MNT_HOLE209	MNT_HOLE	12A7
MNT_HOLE210	MNT_HOLE	12A7
MNT_HOLE211	MNT_HOLE	12A7
MNT_HOLE212	MNT_HOLE	12A7
MNT_HOLE213	MNT_HOLE	12A7
M		