THE DPS1035 IS OBSOLETE.

PLEASE USE THE DPS1135FIA-13.

Lead-free Green

DPS1035

24V/3.5A 1-CH POWER SWITCH W/ REVERSE-VOLTAGE PROTECTION

Description

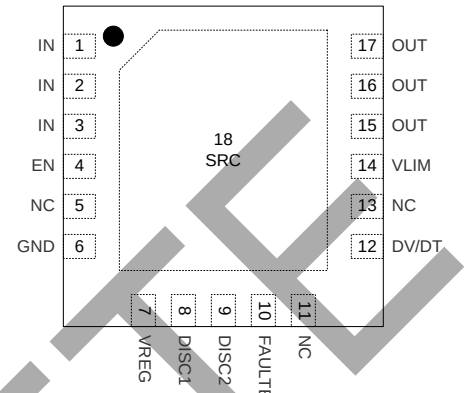
The DPS1035 is part of a family of power switches optimized for the USB Type-C® and other hot-swap applications. Through the analog interface, exception status is reported and functions like voltage limiting and output voltage ramp-up rate can be programmed.

This device is designed to operate between 4.5V and 24V. Its built-in fault-handling mechanism includes reverse voltage and current blocking, input over-voltage protection, and thermal shutdown. In addition, the ramp-up time of the output voltage can be adjusted to minimize in-rush current and to ensure system stability. Before any exception condition is notified via the low-active FAULTB signal, de-glitch of 7ms is applied to prevent false triggering.

The DPS1035 is housed in the low-profile and space-saving V-QFN4040-17 package which is manufactured with environmentally friendly material.

Pin Assignments

(Top View)



V-QFN4040-17

Features

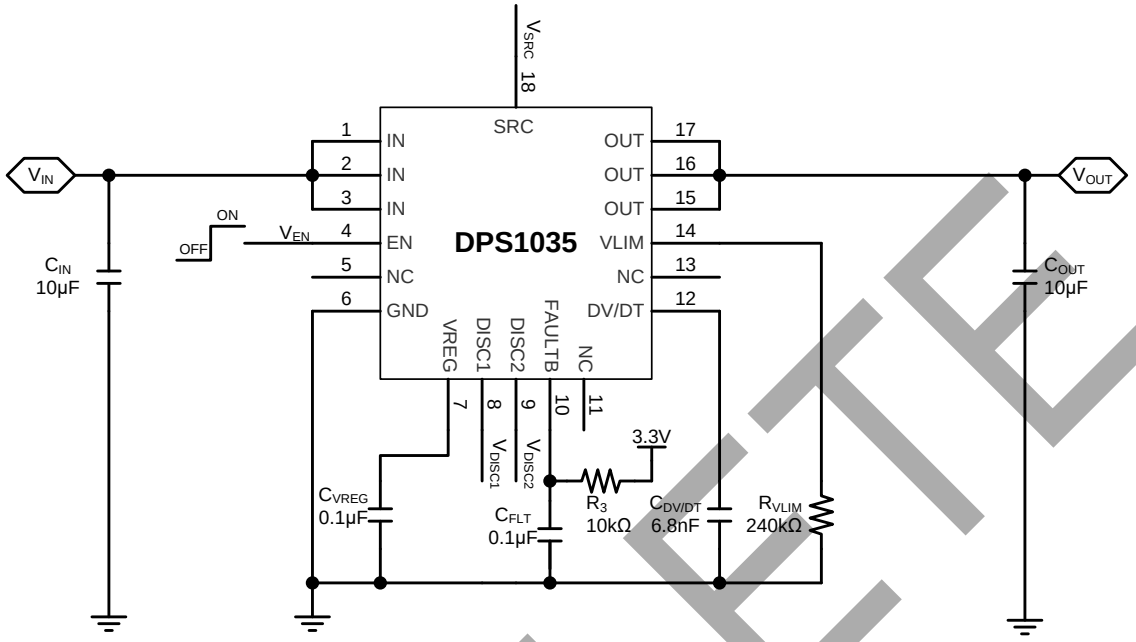
- Wide Operating Voltage Range: 4.5V to 24V
- 1-Channel Power Switch with Built-In Fault Detection and Recovery Mechanisms like Input Under-Voltage Lockout, Reverse-Voltage and Current Blocking, Thermal Shutdown and Input Over-Voltage Protection
- $R_{DS(ON)}$ of Embedded Power MOSFET at 30mΩ
- Adjustable DV/DT Control at Start-Up
- Manual Discharge ON/OFF Control for IN and OUT Ports
- Fault Reporting (FAULTB) with Blanking Time at 7ms Typical
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- Notebooks, desktops and AIO PCs; servers and tablets
- Docking stations, universal and multimedia hubs
- FPTVs, PC monitors
- Set-Top boxes, residential gateways, storage devices

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

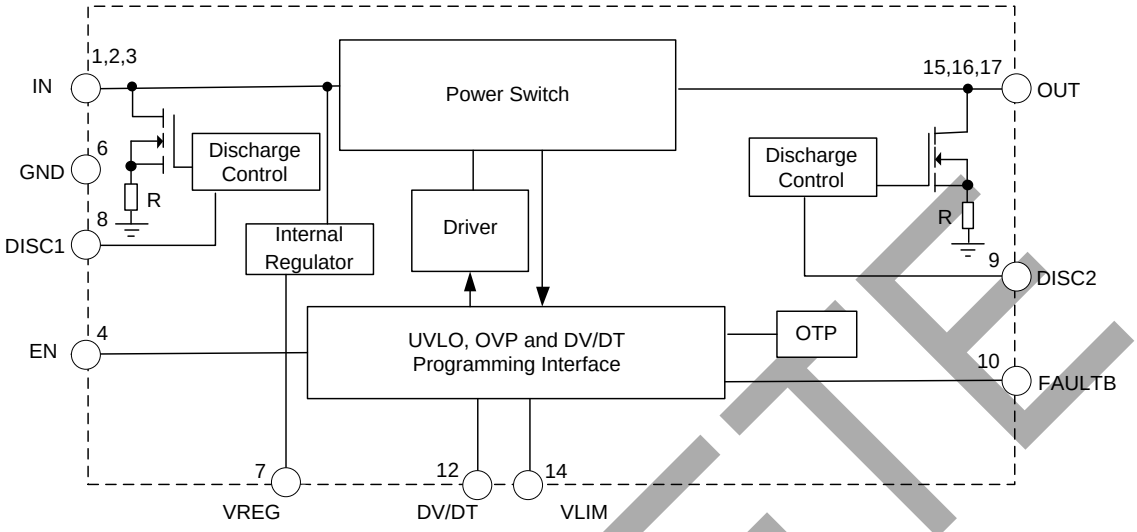
Typical Application Circuit



Pin Descriptions

Pin Number	Pin Name	Type	Function
1, 2, 3	IN	P	Power Supply and Input Port.
4	EN	I	Enable. '0' = device OFF; '1' = device ON. This pin must not be left floating.
5, 11, 13	NC	—	No Connection. All NC pins must be left floating.
6	GND	GND	Device Ground
7	VREG	I/O	Voltage Regulator. A 0.1µF capacitor is recommended between this pin and ground.
8	DISC1	I	IN Port Discharge Control. '1' = port voltage to be discharged; '0' = disabled.
9	DISC2	I	OUT Port Discharge Control. '1' = port voltage to be discharged; '0' = disabled.
10	FAULTB	O	Fault Status Indicator. An external pull-up resistor is required. This active-low pin shall be tied to GND when not used.
12	DV/DT	I/O	Ramp-up Control. A capacitor between this pin and GND sets the ramp-up rate.
14	VLIM	I/O	Voltage Limit Setting. A resistor between this pin and GND sets the over-voltage limit of the IN port.
15, 16, 17	OUT	O	Output Port.
18 (Exposed Pad)	SRC	I/O	Common Source. The exposed pad of the V-QFN4040-17 package must not be connected to any signal.

Functional Block Diagram



Absolute Maximum Ratings (@ T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Voltage Range of IN and OUT Pins	-0.3 to 30	V
$V_{I/O}$	Voltage Range of Others (EN, VREG, DISC1, DISC2, FAULTB, DV/DT and VLIM Pin)	-0.3 to 6	V
I_{OUT}	Output Load Current Range	5	A
T_J	Operating Junction Temperature	-40 to +125	°C
T_L	Lead Temperature	+260	°C
T_{ST}	Storage Temperature	-65 to +150	°C
ESD	Human Body Model (HBM), JESD22-A114	2	kV
	Charge Device Model (CDM)	0.5	

Note: 4. These are stress ratings only. Operation outside the absolute maximum ratings can cause device failure. Operation at the absolute maximum rating for extended periods can reduce device reliability.

Thermal Characteristics (@ T_A = +25°C, unless otherwise specified.) (Note 5)

Symbol	Parameter	Rating	Unit
P_D	Power Dissipation	2.1	W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	58.5	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	9.4	°C/W

Note: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1”x1” copper pad layout.

Recommended Operating Conditions (@ T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Supply Voltage	4.5	24	V
V_{OUT}	Output Voltage	0	24	V
I_{OUT}	Output Load Current	0	3.5	A
C_{IN}	Input Capacitance	1	—	µF
C_{OUT}	Output Capacitance	1	—	µF
V_{EN}	Input Voltage on EN	0	5	V
V_{DISC1}, V_{DISC2}	Input Voltage on DISC1 and DISC2	0	5.5	V

Electrical Characteristics

(@T_A = +25°C, V_{IN} = 4.5V to 24V, C_{IN} = C_{OUT} = 10µF, V_{EN} = 3.3V, $C_{DV/DT}$ = 1nF, R_{VLIM} = 240kΩ, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Bias Supply						
V_{UVLO}	V_{IN} Under-Voltage Lockout Threshold	V_{IN} Rising	3.2	3.7	4	V
V_{UVHY}	V_{IN} Under-Voltage Lockout Threshold Hysteresis	V_{IN} Falling	—	250	—	mV
I_{SHDN}	Shutdown Current (Disabled)	V_{IN} = 5V, V_{EN} = 0V	—	—	10	µA
		V_{IN} = 12V, V_{EN} = 0V	—	—	25	
		V_{IN} = 20V, V_{EN} = 0V	—	—	50	
I_Q	Quiescent Current (Enabled)	V_{IN} = 5V, No Load	—	—	3	mA
		V_{IN} = 12V, No Load	—	—	4	
		V_{IN} = 20V, No Load	—	—	4.5	
Enable Control						
V_{ENL}	EN Threshold Voltage Low	V_{EN} Falling	—	—	0.4	V
V_{ENH}	EN Threshold Voltage High	V_{EN} Rising	1.4	—	—	
I_{EN}	EN Input Leakage Current	V_{IN} = 5V, V_{EN} = 5V	—	—	1	µA
Over-Voltage Protection						
I_{VLIM}	V_{LIM} Sourcing Current	V_{IN} = 5V, R_{VLIM} = 57.6kΩ	—	10	—	µA
R_{VLIM_MAX}	Maximum R_{VLIM}	—	—	—	300	kΩ
V_{OVPRTH}	Input Over-Voltage Threshold, Rising	R_{VLIM} = 57.6kΩ, V_{IN} Rising	—	6	—	V
		R_{VLIM} = 240kΩ, V_{IN} Rising	—	24	—	
V_{OVPFTH}	Input Over-Voltage Threshold, Falling	R_{VLIM} = 57.6kΩ, V_{IN} Falling	—	5.6	—	
		R_{VLIM} = 240kΩ, V_{IN} Falling	—	23.6	—	
MOSFET						
$R_{DS(ON)}$	Switch ON Resistance	V_{IN} = 5V, I_{OUT} = 1A	—	30	40	mΩ
		V_{IN} = 12V, I_{OUT} = 1A	—	30	40	
		V_{IN} = 20V, I_{OUT} = 1A	—	30	40	
I_{LKGSRC}	OUT Leakage Current in OFF State, Sourcing	V_{EN} = 0V, V_{OUT} =0V	—	—	1	µA
I_{LKGSNK}	OUT Leakage Current in OFF State, Sinking	V_{IN} = 3.3V, V_{EN} = 0V, V_{OUT} = 5V	—	—	1	µA
		V_{IN} = 3.3V, V_{EN} = 0V, V_{OUT} = 12V	—	—	1	
		V_{IN} = 3.3V, V_{EN} = 0V, V_{OUT} = 20V	—	—	1	
Reverse-Voltage Protection						
V_{RVPFTH}	V_{IN} - V_{OUT} Threshold Entering into Reverse Protection	V_{IN} - V_{OUT} Falling	—	-40	—	mV
V_{RVPRTH}	V_{IN} - V_{OUT} Threshold Exiting from Reverse Protection	V_{IN} - V_{OUT} Rising	-15	0	—	
t_{RVPTD}	Reverse Protection Response Time	—	—	—	2	µs

Electrical Characteristics (continued)

(@T_A = +25°C, V_{IN} = 4.5V to 24V, C_{IN} = C_{OUT} = 10µF, V_{EN} = 3.3V, $C_{DV/DT}$ = 1nF, R_{VLIM} = 240kΩ, unless otherwise specified.)

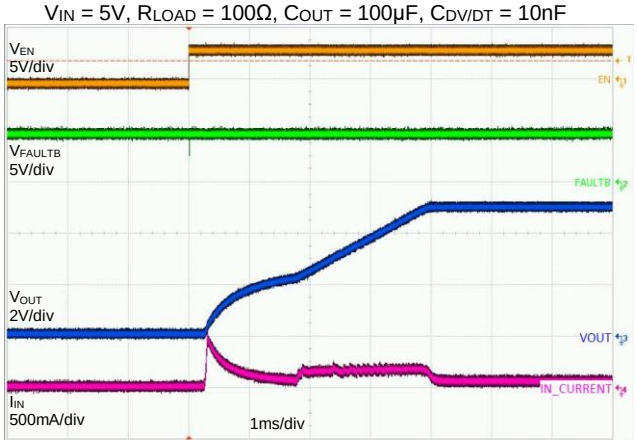
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Output Ramping Control						
$I_{DV/DT}$	DV/DT Sourcing Current	$V_{DV/DT}$ = 0V	—	1	—	µA
$G_{DV/DT}$	DV/DT to OUT Gain	ΔV_{OUT} / $\Delta V_{DV/DT}$, Guaranteed by Design	—	12	—	V/V
Output Timing						
t_{DON}	Output Turn-ON Delay Time	V_{IN} = 5V, C_{OUT} = 1µF, V_{EN} = 0V to 2V	—	0.2	—	ms
		V_{IN} = 12V, C_{OUT} = 1µF, V_{EN} = 0V to 2V	—	0.2	—	
		V_{IN} = 20V, C_{OUT} = 1µF, V_{EN} = 0V to 2V	—	0.2	—	
t_R	Output Turn-ON Rise Time	V_{IN} = 5V, C_{OUT} = 1µF, V_{EN} = 0V to 2V	—	0.3	—	ms
		V_{IN} = 12V, C_{OUT} = 1µF, V_{EN} = 0V to 2V	—	0.8	—	
		V_{IN} = 20V, C_{OUT} = 1µF, V_{EN} = 0V to 2V	—	1.6	—	
t_{DOFF}	Output Turn-OFF Delay Time	V_{IN} = 5V, C_{OUT} = 1µF, V_{EN} = 2V to 0V	—	1	—	µs
		V_{IN} = 12V, C_{OUT} = 1µF, V_{EN} = 2V to 0V	—	2	—	
		V_{IN} = 20V, C_{OUT} = 1µF, V_{EN} = 2V to 0V	—	4	—	
t_F	Output Turn-OFF Fall Time	V_{IN} = 5V, C_{OUT} = 1µF, V_{EN} = 2V to 0V	—	10	—	µs
		V_{IN} = 12V, C_{OUT} = 1µF, V_{EN} = 2V to 0V	—	25	—	
		V_{IN} = 20V, C_{OUT} = 1µF, V_{EN} = 2V to 0V	—	50	—	
Discharge Control on IN/OUT Pins						
$R_{DISC1/DISC2}$	IN/OUT Discharge Resistance	V_{DISC1} = 5V, V_{DISC2} = 5V	—	70	—	Ω
		V_{DISC1} = 3.3V, V_{DISC2} = 3.3V	—	82	—	Ω
V_{DISC1L}/ V_{DISC2L}	DISC1/DISC2 Threshold Voltage Low	V_{DISC1}/V_{DISC2} Falling	—	—	0.4	V
V_{DISC1H}/ V_{DISC2H}	DISC1/DISC2 Threshold Voltage High	V_{DISC1}/V_{DISC2} Rising	1.4	—	—	V
Fault Flag (FAULTB): Active Low						
R_{FAULTB}	FAULTB Pull-Down Resistor	V_{IN} = 7V, R_{VLIM} = 57.6kΩ, I_{FAULTB} = 10mA Sinking	—	25	—	Ω
$I_{LKGFAULTB}$	FAULTB Leakage Current	V_{IN} = 5V, R_{VLIM} = 57.6kΩ, V_{FAULTB} = 5V	—	—	1	µA
$t_{BLANKFAULTB}$	FAULTB Blanking Time	V_{IN} = 5V, R_{VLIM} = 57.6kΩ, V_{FAULTB} = 5V	—	7	—	ms
Thermal Shutdown						
T_{SHDN}	Thermal Shutdown Threshold	—	—	+155	—	°C
T_{HYS}	Thermal Shutdown Hysteresis	—	—	+20	—	

Performance Characteristics

($@T_A$ = +25°C, C_{IN} = C_{OUT} = 10µF, V_{EN} = 3.3V, $C_{DV/DT}$ = 1nF, R_{VLIM} = 240kΩ, unless otherwise specified.)

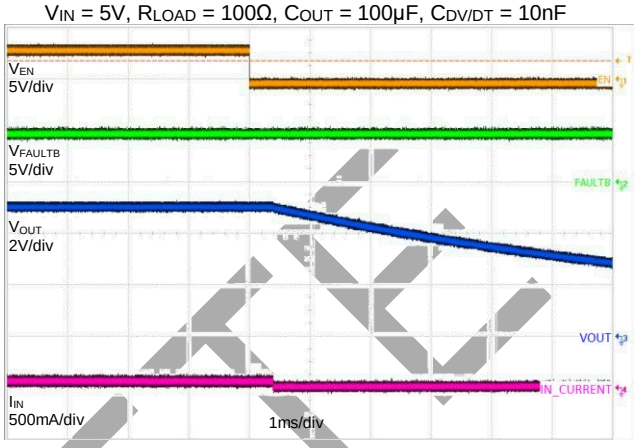
EN Turn ON and In-Rush Current at 5V

V_{IN} = 5V, R_{LOAD} = 100Ω, C_{OUT} = 100µF, $C_{DV/DT}$ = 10nF



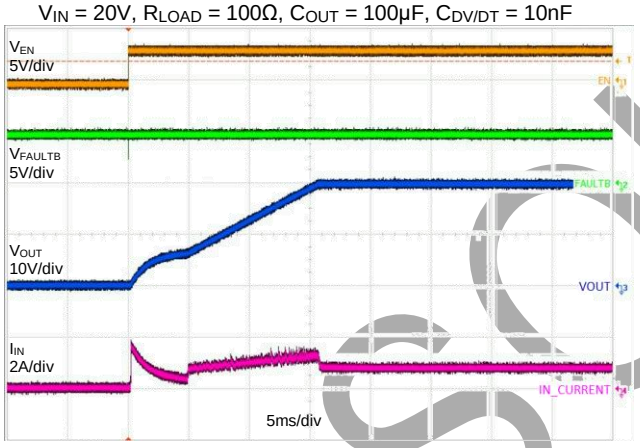
EN Turn OFF at 5V

V_{IN} = 5V, R_{LOAD} = 100Ω, C_{OUT} = 100µF, $C_{DV/DT}$ = 10nF



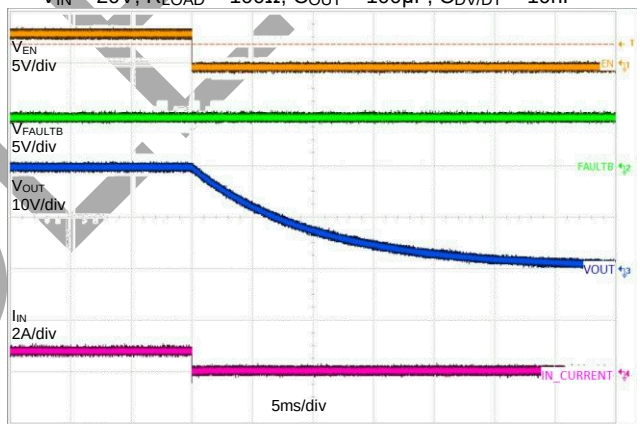
EN Turn ON and In-Rush Current at 20V

V_{IN} = 20V, R_{LOAD} = 100Ω, C_{OUT} = 100µF, $C_{DV/DT}$ = 10nF



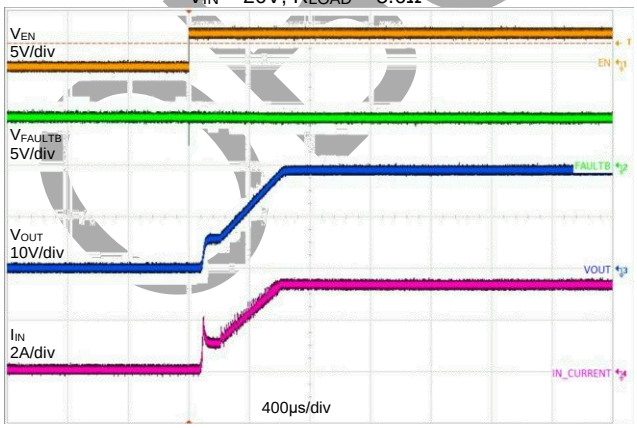
EN Turn OFF at 20V

V_{IN} = 20V, R_{LOAD} = 100Ω, C_{OUT} = 100µF, $C_{DV/DT}$ = 10nF



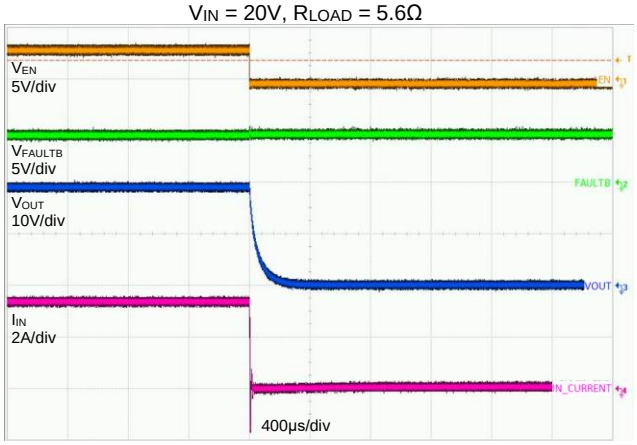
EN Turn ON with a 5.6Ω Load at 20V

V_{IN} = 20V, R_{LOAD} = 5.6Ω



EN Turn OFF with a 5.6Ω Load at 20V

V_{IN} = 20V, R_{LOAD} = 5.6Ω



Application Information

General Description

The DPS1035 is a unidirectional power switch designed to meet the input and output voltage/current requirement which is common with many hot-pluggable serial interfaces found in the computing and consumer electronics equipment.

Ramp-Up Time and In-Rush Current Control

An external capacitor connected from the DV/DT pin to GND defines the slew rate of the output voltage at power-on:

$$dV_{OUT} / dt = (I_{DV/DT} / C_{DV/DT}) \times G_{DV/DT}$$, where $I_{DV/DT}$ =1μA typ. and $G_{DV/DT}$ = 12

The total ramp-up time $t_{DV/DT}$ of V_{OUT}, increasing from 0 to V_{IN}, can be calculated using the following equation:

$$t_{DV/DT} = 8.3 \times 10^4 \times V_{IN} \times C_{DV/DT}$$

The in-rush current at power-up shall be limited by the regulated output voltage ramp.

Input Over-Voltage Protection (OVP)

The voltage at the IN port is monitored continuously. Whenever voltage at the IN port is found to be larger than the V_{OVPRTH} value, the built-in over-voltage protection (OVP) fault-handling mechanism is triggered. The internal power MOSFET will be turned OFF to protect the downstream equipment connected. The V_{OVPRTH} value is determined by:

$V_{OVPRTH} = 0.1 \times R_{VLIM}$, where the unit of R_{VLIM} is kΩ and 51kΩ ≤ R_{VLIM} ≤ 240kΩ.

Over-Temperature Protection (OTP)

When the junction temperature T_J reaches the thermal shutdown threshold T_{SHDN}, the internal power MOSFET would be turned OFF. The internal power MOSFET will be turned ON again once the condition [T_J < (T_{SHDN} - T_{HYS})] becomes valid.

Reverse-Voltage Protection (RVP)

The voltage difference, [V_{IN} - V_{OUT}], between the IN and OUT ports is monitored continuously. Once the voltage difference drops below the V_{RVPFTH} level, the device shall immediately turn OFF the internal power MOSFET to prevent the current flowing from the opposite direction. When the reverse-voltage condition is no longer valid, i.e. [V_{IN} - V_{OUT}] becomes greater than the V_{RVPRTH} level, the internal power MOSFET shall be turned ON.

Fault Response

An external pull-up resistor is required. The device generates a warning flag whenever one of the following fault conditions becomes valid: input over-voltage, reversed-voltage, over-temperature. After a de-glitch time-out of 7ms, the low-active FAULTB signal shall be asserted. The FAULTB signal shall remain 'low' and the internal power MOSFET remains OFF until the exception status is no longer valid.

Discharge Function

To facilitate the various applications envisioned by the system designers, the IN and OUT ports can be discharged via two external controls: DISC1, DISC2. The internal discharge resistor is around 80Ω. The settings are shown in the table below.

DISC1	DISC2	Description
0	0	Discharge function disabled
0	1	OUT Port is being discharged until the pin DISC2 is pulled 'low'
1	0	IN Port is being discharged until the pin DISC1 is pulled 'low'
1	1	Both IN and OUT ports are discharged simultaneously

Application Information (continued)

PCB Layout Consideration

1. Place the input and output capacitors, C_{IN} and C_{OUT}, as close as possible to the IN and OUT pins.
2. The power traces, including the power ground, the V_{IN} trace and the V_{OUT} trace should be kept direct, short and wide.
3. Place the resistors and capacitors (R_{VLIM}, $C_{DV/DT}$ and C_{VREG}) as close as possible to the corresponding device pins.
4. Connect the signal ground to the GND pin, and keep a single connection from GND pin to the power ground behind the input capacitor.
5. For better power dissipation, via holes are recommended to connect the exposed pad's landing area to a large copper polygon on the other side of the printed circuit board. The copper polygons and exposed pad of SRC (common source nodes of internal power MOSFET) shall not be connected to any of the signal and power grounds on the printed circuit board.

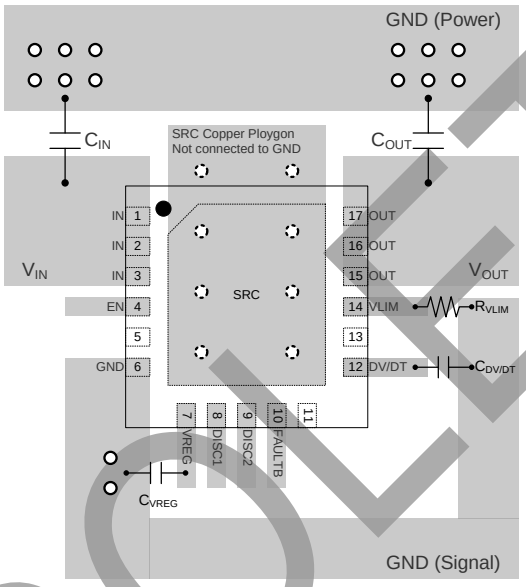
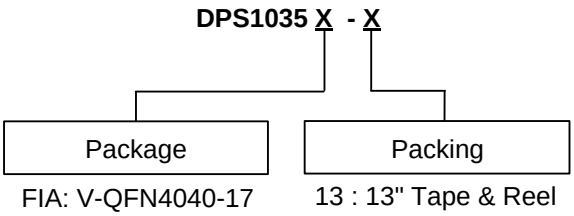


Figure 1. Suggested PCB Layout

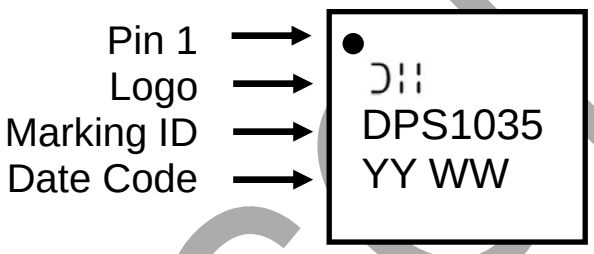
Ordering Information (Note 6)



Part Number	Package	Marking ID	Reel Size (inches)	Tape Width (mm)	Packing	
					Qty.	Carrier
DPS1035FIA-13	V-QFN4040-17	DPS1035	13	12	4,000	13” Tape and Reel

Note: 6. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

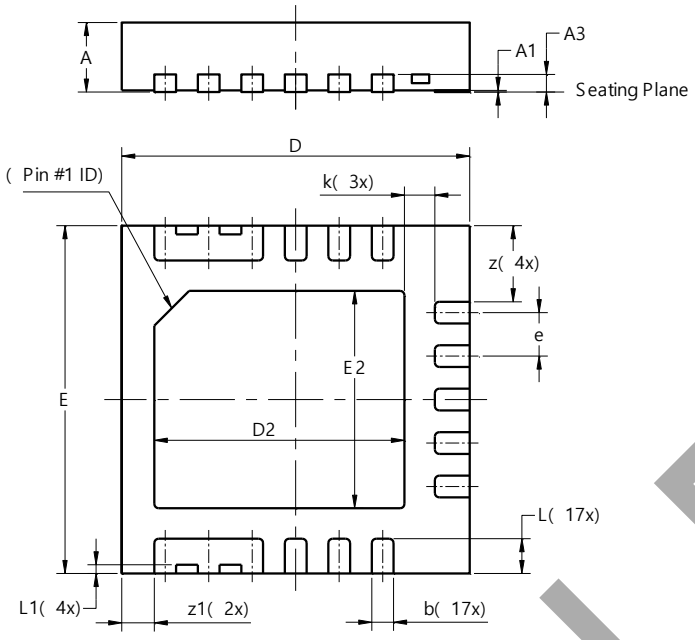


YY: Year
WW: Week 01 to 52; 52 Represents 52 and 53 Week

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN4040-17

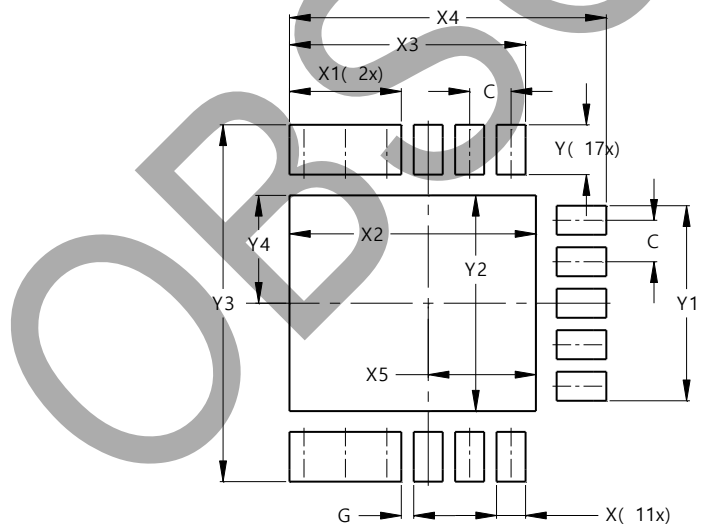


V-QFN4040-17			
Dim	**Min**	**Max**	**Typ**
A	0.75	0.85	0.80
A1	0.00	0.05	0.02
A3	—	—	0.203
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.775	2.975	2.875
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
k	—	—	0.35
L	0.35	0.45	0.40
L1	—	—	0.10
z	—	—	0.875
z1	—	—	0.375
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

V-QFN4040-17



Dimensions	Value (in mm)
C	0.500
G	0.150
X	0.350
X1	1.350
X2	2.975
X3	2.850
X4	3.825
X5	1.300
Y	0.600
Y1	2.350
Y2	2.600
Y3	4.300
Y4	1.300

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.041 grams (Approximate)

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