



P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	RDS(ON) Max	I _D T _A = +25°C
-20V	$78m\Omega$ @ V _{GS} = -8V	-3.4A
	100mΩ @ V _{GS} = -4.5V	-3.0A

Description

This new generation MOSFET is designed to minimize the footprint in handheld and mobile application. It can be used to replace many small signals MOSFET with really small footprint.

Applications

- Battery managements
- Load switches
- Battery protections
- Handheld and mobile applications

Features and Benefits

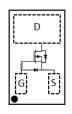
- Low Qg & Qgd
- Small Footprint
- Low Profile 0.20mm Height
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.

https://www.diodes.com/quality/product-definitions/

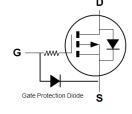
Mechanical Data

- Package: X4-DSN1006-3
- Terminal Connections: See Diagram Below
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish NiPdAu or NiAu Solderable per MIL-STD-202, Method 208
- Weight: 0.00029 grams (Approximate)





X4-DSN1006-3



Top View

Equivalent Circuit

Ordering Information (Note 4)

Part Number	Dookowa	Carrier Tape Width Carrier Tape Pitch		Packing		
Part Number	Package	Carrier Tape Width	Carrier Tape Pitch	Qty.	Carrier	
DMP2078LCA3-7	X4-DSN1006-3	8mm	2mm	10k	Tape & Reel	
DMP2078LCA3-7A	X4-DSN1006-3	8mm	4mm	5k	Tape & Reel	

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information



O = Product Type Marking Code YW = Date Code Marking Y or Y = Year (ex: 3 = 2023)

W or \overline{W} = Week (ex. a = Week 27; z Represents Weeks 52 and 53)

Date Code Key

Year	2017	-	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032
Code	7	-	3	4	5	6	7	8	9	0	1	2
Week	eek 1-26			27-52				53				
Code		A-Z				а	ı-Z				Z	·



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit		
Drain-Source Voltage	VDSS	-20	V		
Gate-Source Voltage	Vgss	-12	V		
Continuous Drain Current (Note 5) V _{GS} = -8V	Steady State	$T_A = +25$ °C $T_A = +70$ °C	I _D	-3.4 -2.7	А
Continuous Drain Current (Note 5) V _{GS} = -4.5V	Steady State	T _A = +25°C T _A = +70°C	lo	-3.0 -2.4	А
Pulsed Drain Current (Note 6)	IDM	-13	Α		
Human Body Model (HBM)	V _(ESD)	4	kV		

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 7)	PD	0.81	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 7)	RθJA	155.4	°C/W
Power Dissipation (Note 5)	PD	1.4	W
Thermal Resistance, Junction to Ambient @T _A = +25°C (Note 5)	R _{θJA}	90.4	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

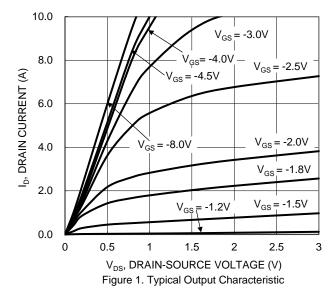
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BVDSS	-20	_	_	V	$V_{GS} = 0V, I_{D} = -250\mu A$	
Zero Gate Voltage Drain Current TJ = +25°C	IDSS	_	_	-100	nA	V _{DS} = -16V, V _{GS} = 0V	
Gate-Source Leakage	Igss	_	_	-50	nA	V _G S = -12V, V _D S = 0V	
ON CHARACTERISTICS (Note 8)							
Gate Threshold Voltage	Vgs(TH)	-0.7	-0.9	-1.2	>	$V_{DS} = V_{GS}$, $I_D = -250\mu A$	
			64	78		$V_{GS} = -8V, I_{D} = -0.5A$	
Static Drain-Source On-Resistance	D-s/s/		77	100	mΩ	$V_{GS} = -4.5V, I_D = -0.5A$	
Static Diain-Source On-Nesistance	R _{DS(ON)}	_	113	165	11122	$V_{GS} = -2.5V$, $I_{D} = -0.5A$	
		_	188	600		$V_{GS} = -1.8V$, $I_{D} = -0.1A$	
Diode Forward Voltage	VsD	_	-0.7	-1.0	V	$V_{GS} = 0V, I_{S} = -0.5A$	
Reverse Recovery Charge	Q _{RR}	_	1.3	_	nC	V _{DD} = -10V, I _F = -1A,	
Reverse Recovery Time	trr	_	7.7	_	ns	di/dt = 100A/µs	
DYNAMIC CHARACTERISTICS (Note 9)							
Input Capacitance	Ciss		152	228		10/1/	
Output Capacitance	Coss	_	78	117	pF	$V_{DS} = -10V$, $V_{GS} = 0V$, $f = 1MHz$	
Reverse Transfer Capacitance	Crss	_	4.3	6.4		1 – 11011 12	
Series Gate Resistance	Rg	_	21	31	Ω	$f = 1MHz$, $V_{GS} = 0V$, $V_{DS} = 0V$	
Total Gate Charge	Qg	_	1.1	1.6			
Gate-Source Charge	Qgs	_	0.2	_	nC	$V_{GS} = -4.5V$, $V_{DS} = -10V$,	
Gate-Drain Charge	Qgd	_	0.2	_	nc	$I_D = -0.5A$	
Gate Charge at VTH	Q _{g(th)}		3.6	_			
Turn-On Delay Time	t _{D(ON)}	_	4.1	6.1			
Turn-On Rise Time	t _R		5.6	_		V _{DS} = -10V, V _{GS} = -4.5V,	
Turn-Off Delay Time	tD(OFF)		9.5	14.2	ns	$R_G = 2\Omega$, $I_D = -0.5A$	
Turn-Off Fall Time	tF	_	4.6	_			

Notes:

- 5. Device mounted on FR-4 material with 1inch² (6.45cm²), 2oz. (0.071mm thick) Cu.
- 6. Repetitive rating, pulse width limited by junction temperature.
- 7. Device mounted on FR-4 PCB with minimum recommended pad layout, single sided.
- 8. Short duration pulse test used to minimize self-heating effect.
- 9. Guaranteed by design. Not subject to production testing.





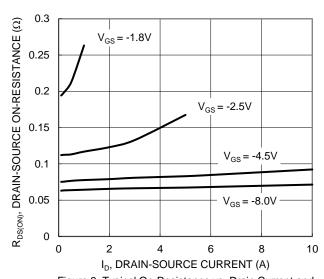


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

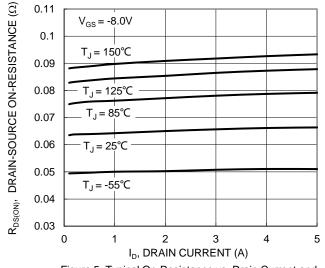


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

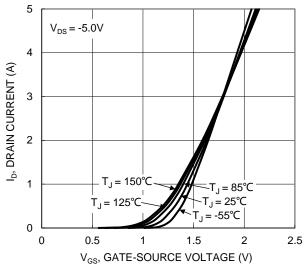


Figure 2. Typical Transfer Characteristic

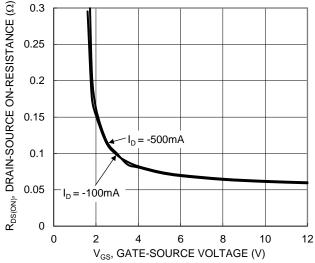


Figure 4. Typical Transfer Characteristic

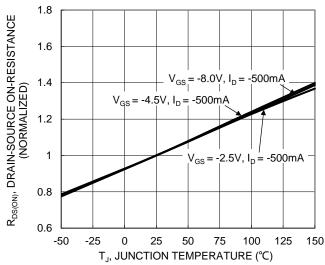


Figure 6. On-Resistance Variation with Junction Temperature



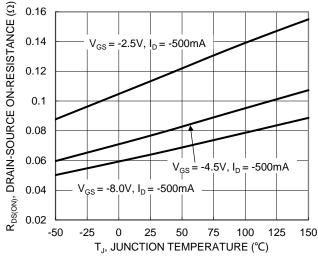
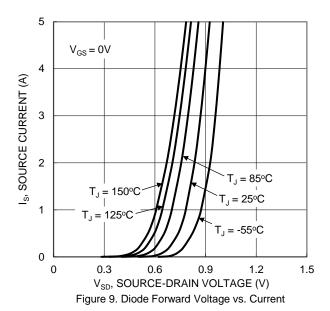


Figure 7. On-Resistance Variation with Junction Temperature



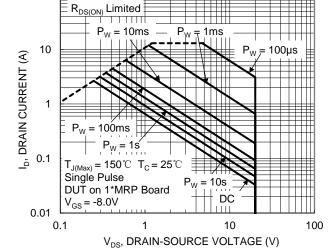


Figure 11. SOA, Safe Operation Area

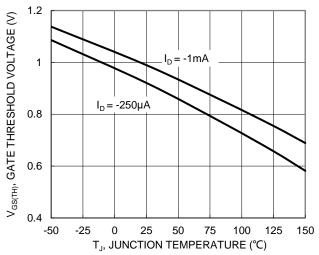
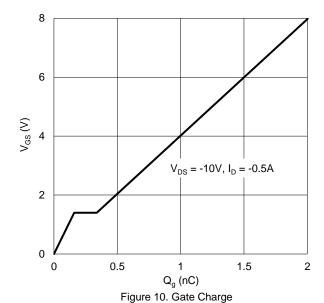


Figure 8. Gate Threshold Variation vs. Junction Temperature



100



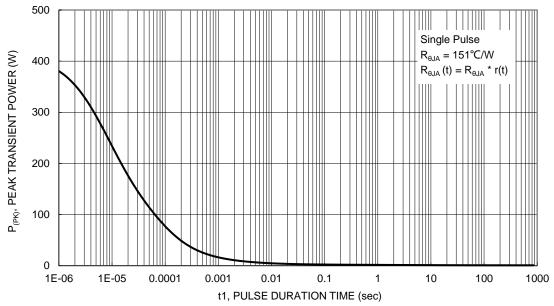


Figure 12. Single Pulse Maximum Power Dissipation

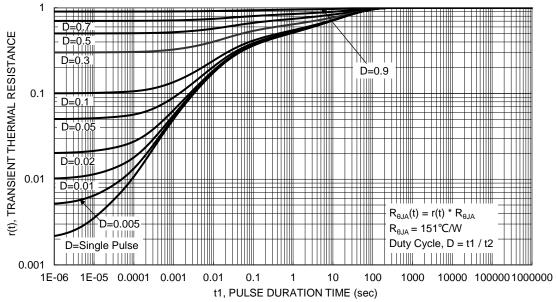


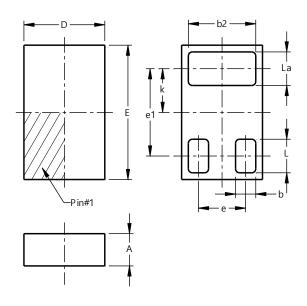
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X4-DSN1006-3

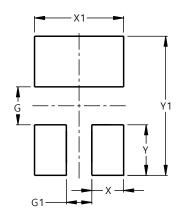


	X4-DSN1006-3							
Dim	Min	Max	Тур					
Α	0.18	0.22	0.20					
b	0.14	0.16	0.15					
b2	0.49	0.51	0.50					
D	0.56	0.64	0.60					
Е	0.96	1.04	1.00					
е			0.35					
e1			0.65					
k			0.325					
L	0.24	0.26	0.25					
La	0.24	0.26	0.25					
All	Dimensi	ions in	mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X4-DSN1006-3



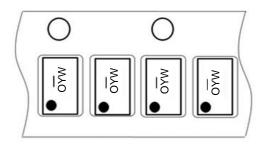
Dimensions	Value
Dilliensions	(in mm)
G	0.40
G1	0.20
Х	0.15
X1	0.50
Υ	0.25
Y1	0.90



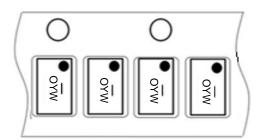
Tape and Reel Information

Please see https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf for the latest version.

DMP2078LCA3-7 Pin 1 orientation



DMP2078LCA3-7A Pin 1 orientation





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