

**N-CHANNEL ENHANCEMENT MODE FIELD MOSFET**
**Product Summary**

$BV_{SSS}$	$R_{SS(ON) MAX}$	$I_S$ $T_A = +25^\circ C$
30V	7.8m $\Omega$ @ $V_{GS} = 10V$	14.6A

**Description**

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{SS(ON)}$ ) with a 3.37mm x 1.47mm x 0.2mm size and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

**Applications**

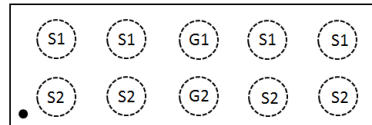
- Battery Management
- Load Switch
- Battery Protection

**Features**

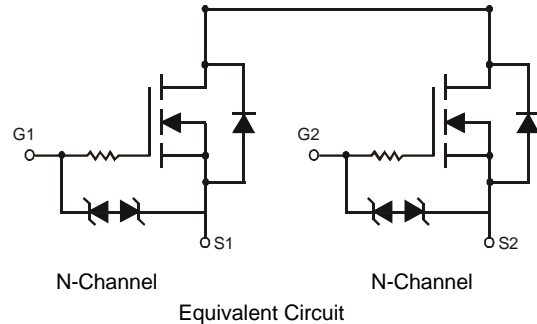
- Built-in G-S Protection Diode Against ESD 2kV HBM.
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

**Mechanical Data**

- Case: X4-DSN3415-10
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram



Top View

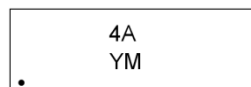


Equivalent Circuit

**Ordering Information (Note 4)**

Part Number	Case	Packaging
DMN3008SCP10-7	X4-DSN3415-10	3000/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**


4A = Product Type Marking Code  
 YM = Date Code Marking  
 Y or  $\bar{Y}$  = Year (ex: E = 2017)  
 M or  $\bar{M}$  = Month (ex: 9 = September)

## Date Code Key

Year	2015	2016	2017	2018	2019	2020	2021
Code	C	D	E	F	G	H	I

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Source -Source Voltage			V <sub>SSS</sub>	30	V
Gate-Source Voltage (Note 5)			V <sub>GSS</sub>	±20	V
Continuous Source Current @ T <sub>A</sub> = +25°C (Note 6)	Steady State	T <sub>A</sub> = +25°C	I <sub>S</sub>	14.6	A
		T <sub>A</sub> = +70°C		11.6	
Pulsed Source Current @ T <sub>A</sub> = +25°C (Notes 6 & 7)			I <sub>SM</sub>	80	A

**Thermal Characteristics**

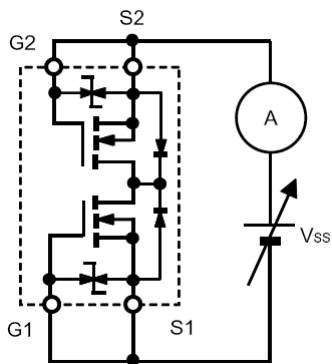
Characteristic	Symbol	Value	Unit
Power Dissipation, @ T <sub>A</sub> = +25°C (Note 6)	P <sub>D</sub>	2.7	W
Thermal Resistance, Junction to Ambient @ T <sub>A</sub> = +25°C (Note 6)	R <sub>θJA</sub>	46.9	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

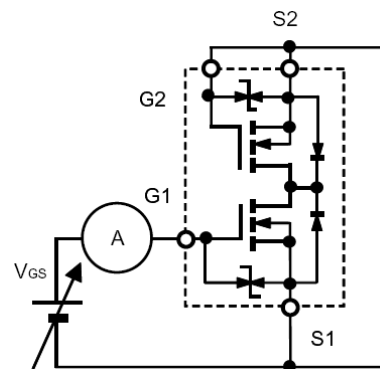
Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 8)</b>						
Source to Source Breakdown Voltage T <sub>J</sub> = +25°C	BV <sub>SSS</sub>	30	—	—	V	I <sub>S</sub> = 250µA, V <sub>GS</sub> = 0V TEST CIRCUIT 1
Zero Gate Voltage Source Current T <sub>J</sub> = +25°C	I <sub>SSS</sub>	—	—	1.0	µA	V <sub>SS</sub> = 24V, V <sub>GS</sub> = 0V TEST CIRCUIT 1
Gate-Body Leakage	I <sub>GSS</sub>	—	—	10	µA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V TEST CIRCUIT 2
<b>ON CHARACTERISTICS (Note 8)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1.3	1.6	2.3	V	V <sub>SS</sub> = 10V, I <sub>S</sub> = 250µA TEST CIRCUIT 3
Static Source -Source On-Resistance	R <sub>SS(ON)</sub>	—	6.1 8.1	7.8 11	mΩ	V <sub>GS</sub> = 10 V, I <sub>S</sub> = 7.0A TEST CIRCUIT 5 V <sub>GS</sub> = 4.5V, I <sub>S</sub> = 7.0A TEST CIRCUIT 5
Body Diode Forward Voltage	V <sub>F(S-S)</sub>	—	0.8	—	V	I <sub>F</sub> = 7.0A, V <sub>GS</sub> = 0V, TEST CIRCUIT 6
<b>DYNAMIC CHARACTERISTICS (Note 9)</b>						
Input Capacitance	C <sub>iSS</sub>	—	1476	—	pF	V <sub>SS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHz TEST CIRCUIT 7
Output Capacitance	C <sub>oSS</sub>	—	204	—		
Reverse Transfer Capacitance	C <sub>rSS</sub>	—	97	—		
Gate Resistance	R <sub>g</sub>	—	436.8	—	Ω	V <sub>SS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1MHz
Total Gate Charge (10V)	Q <sub>g</sub>	—	31.3	—	nC	V <sub>SS</sub> = 15V, I <sub>S</sub> = 7A TEST CIRCUIT 9
Total Gate Charge (4.5V)	Q <sub>g</sub>	—	15.8	—	nC	
Gate-Source Charge	Q <sub>gs</sub>	—	4.7	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	6.3	—	nC	
Gate Charge at V <sub>TH</sub>	Q <sub>g(TH)</sub>	—	3.1	—	nC	
Turn-On Delay Time	t <sub>D(ON)</sub>	—	186	—	ns	V <sub>SS</sub> = 15V, R <sub>L</sub> = 2.1Ω, I <sub>S</sub> = 7A TEST CIRCUIT 8
Turn-On Rise Time	t <sub>R</sub>	—	314	—	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	928	—	ns	
Turn-Off Fall Time	t <sub>F</sub>	—	858	—	ns	

- Notes:
- AEC-Q101 V<sub>GS</sub> maximum is 16V.
  - Device mounted on FR-4 material with 1inch<sup>2</sup> (6.45cm<sup>2</sup>), 2oz (0.071mm thick) Cu.
  - Repetitive rating, pulse width limited by junction temperature.
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to production testing.

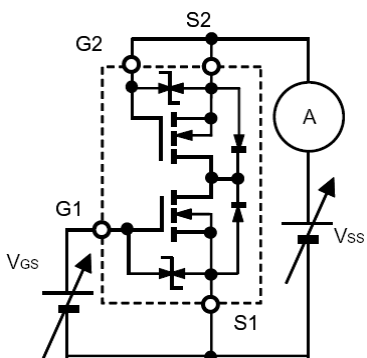
**Test Circuits**



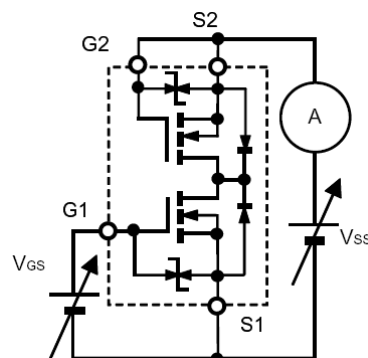
TEST CIRCUIT 1  $I_{SS}$



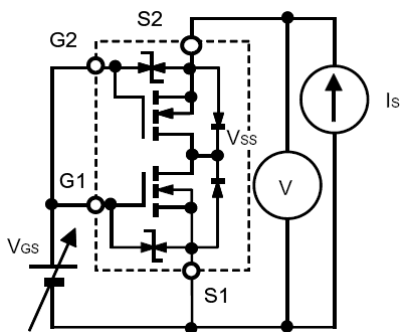
TEST CIRCUIT 2  $I_{GSS}$   
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



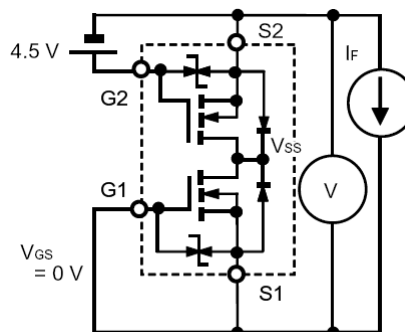
TEST CIRCUIT 3  $V_{GS(OFF)}$   
When FET1 is measured, between GATE and SOURCE of FET2 are shorted.



TEST CIRCUIT 4  $|y_{fs}|$   
 $\Delta I_S / \Delta V_{GS}$

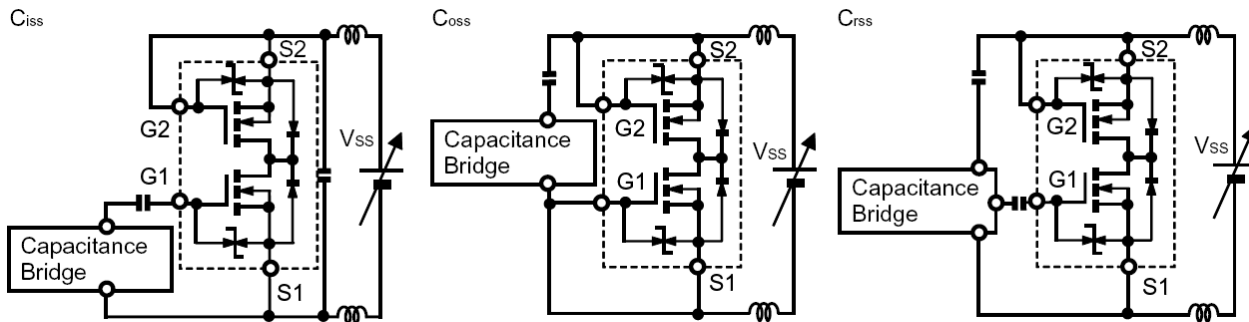


TEST CIRCUIT 5  $R_{SS(ON)}$   
 $V_{SS} / I_S$

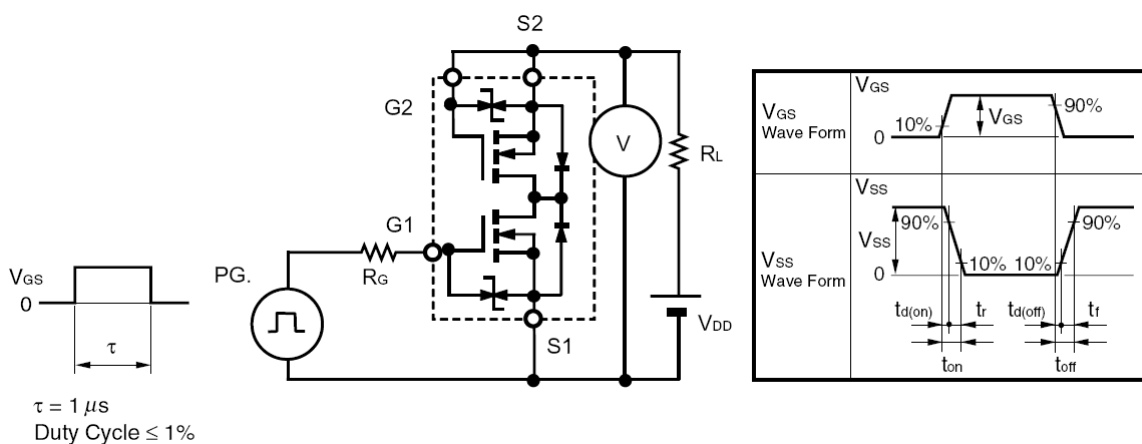


TEST CIRCUIT 6  $V_{F(S-S)}$   
When FET1 is measured, FET2 is added  $V_{GS} + 4.5V$ .

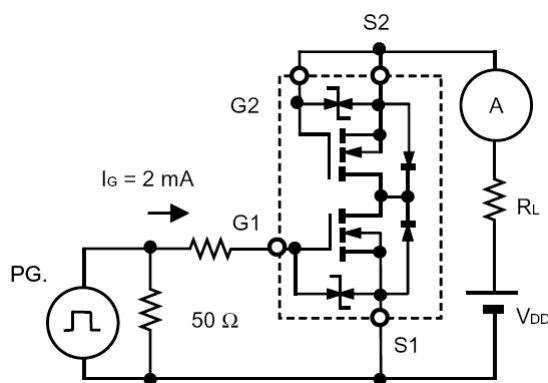
**Test Circuits (Cont.)**



TEST CIRCUIT 7



TEST CIRCUIT 8  $t_{d(on)}$ ,  $t_r$ ,  $t_{d(off)}$ ,  $t_{off}$



TEST CIRCUIT 9  $Q_G$

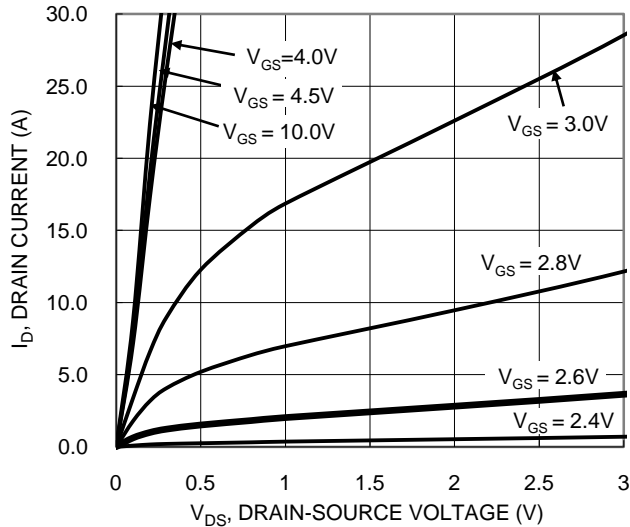


Figure 1. Typical Output Characteristic

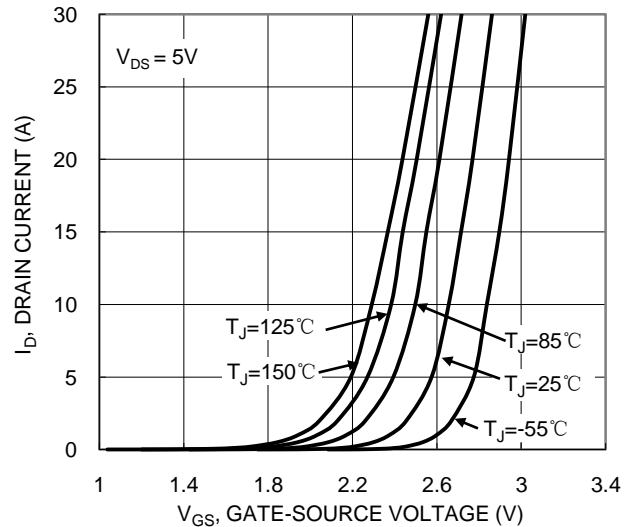


Figure 2. Typical Transfer Characteristic

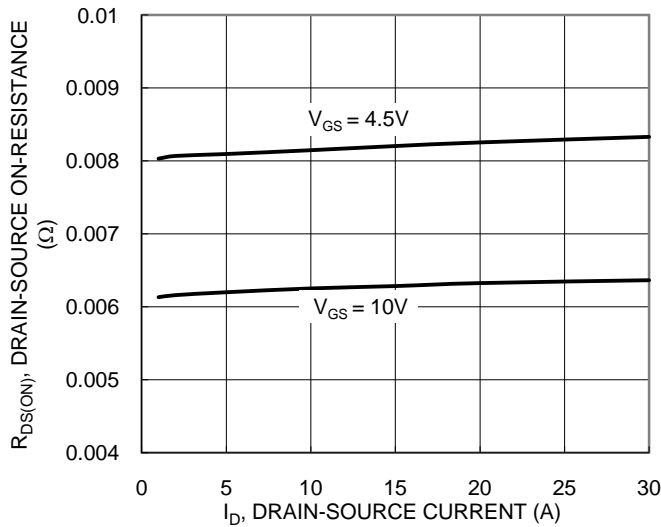


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

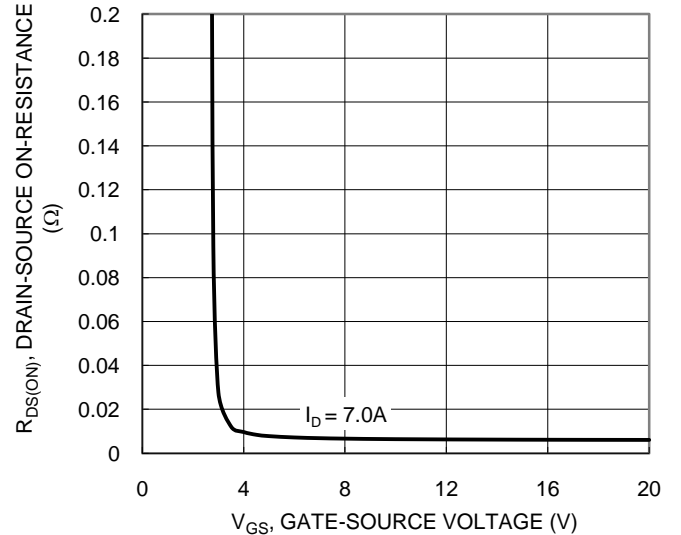


Figure 4. Typical Transfer Characteristic

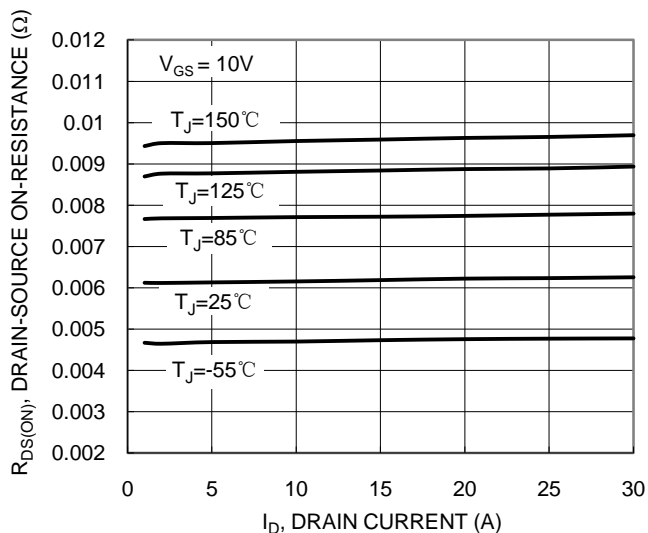


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

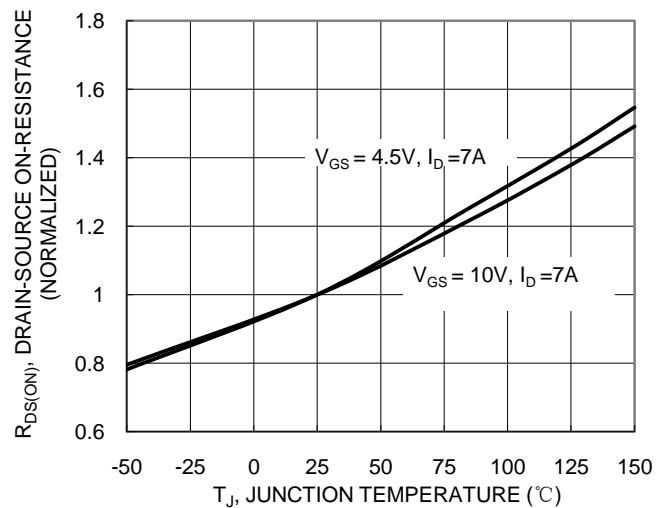


Figure 6. On-Resistance Variation with Junction Temperature

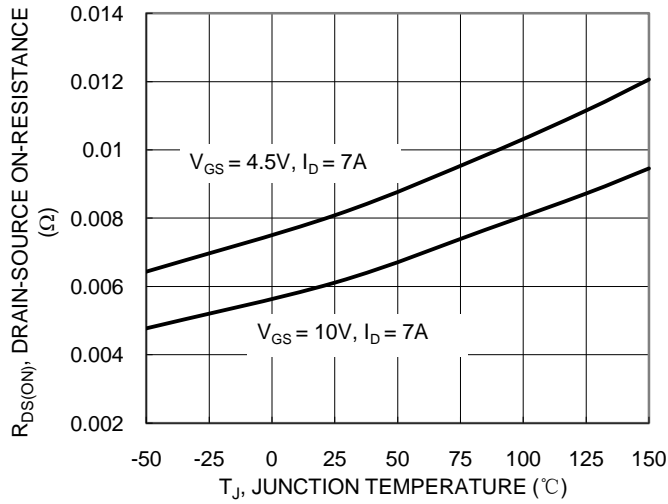


Figure 7. On-Resistance Variation with Junction Temperature

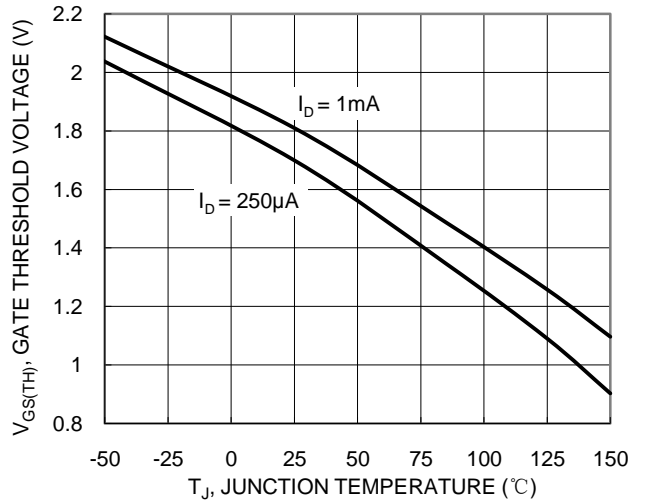


Figure 8. Gate Threshold Variation vs. Junction Temperature

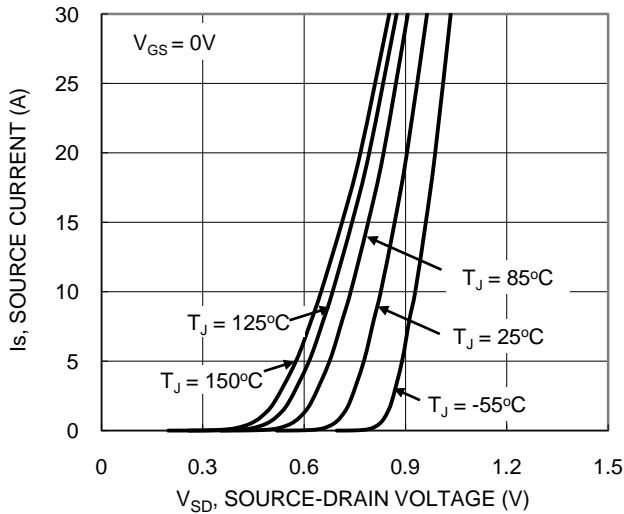


Figure 9. Diode Forward Voltage vs. Current

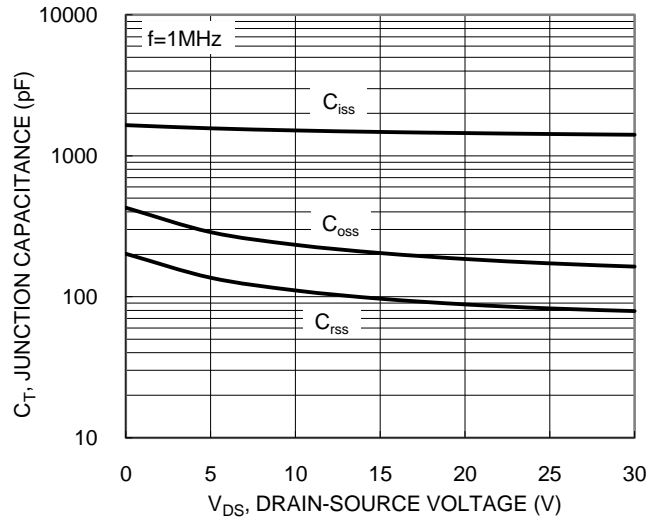


Figure 10. Typical Junction Capacitance

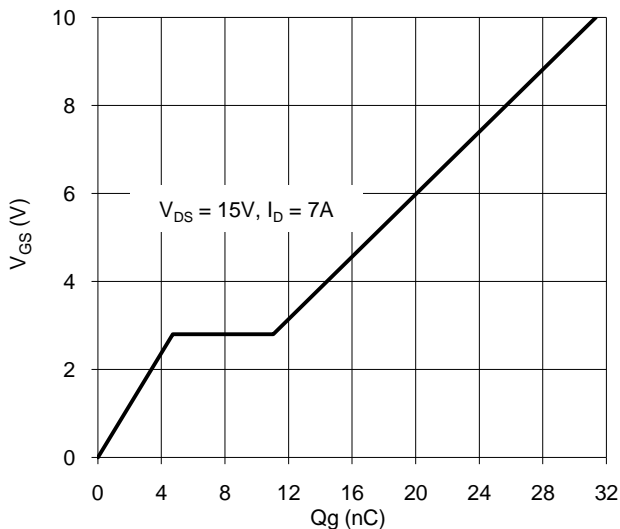


Figure 11. Gate Charge

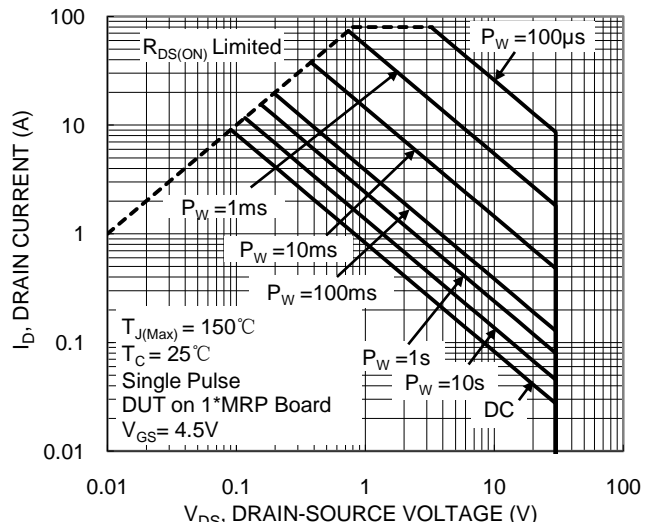


Figure 12. SOA, Safe Operation Area

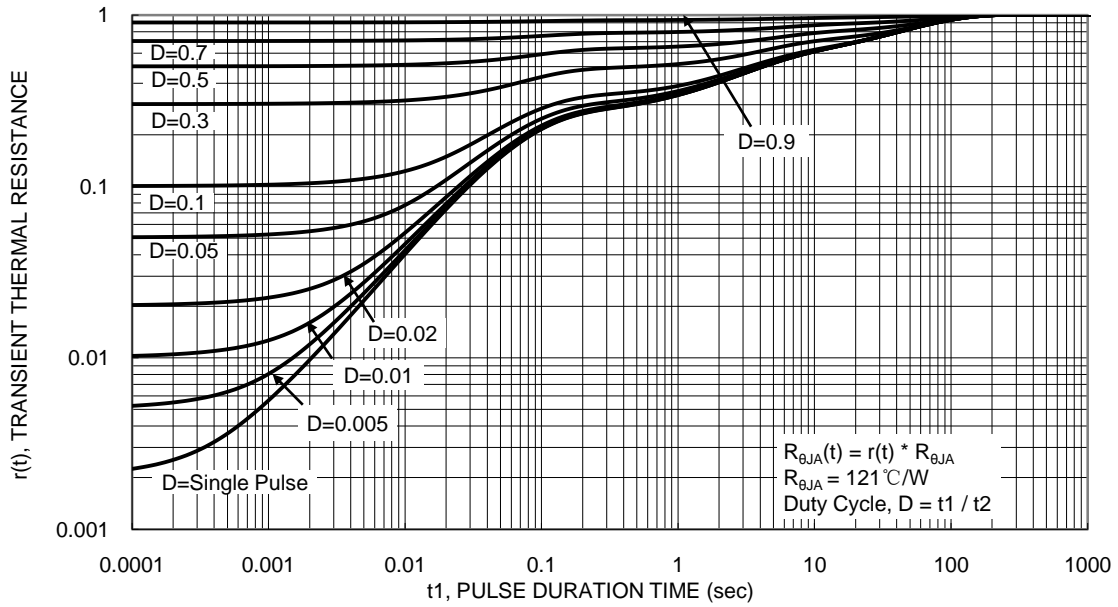
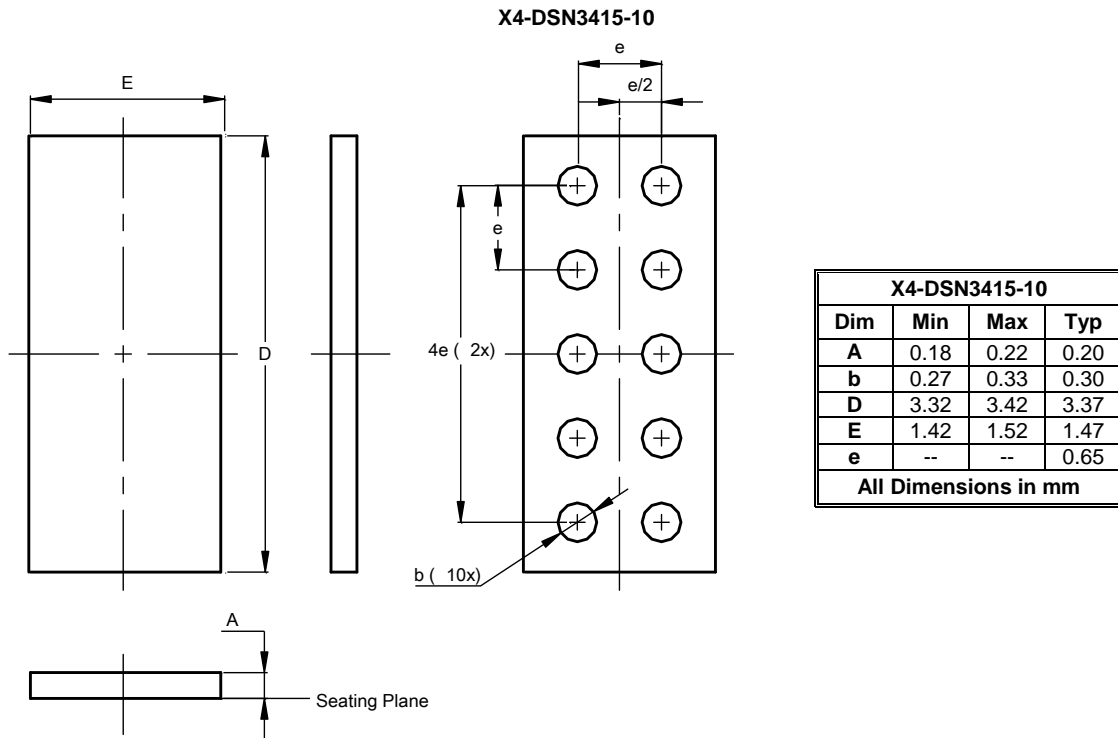


Figure 13. Transient Thermal Resistance

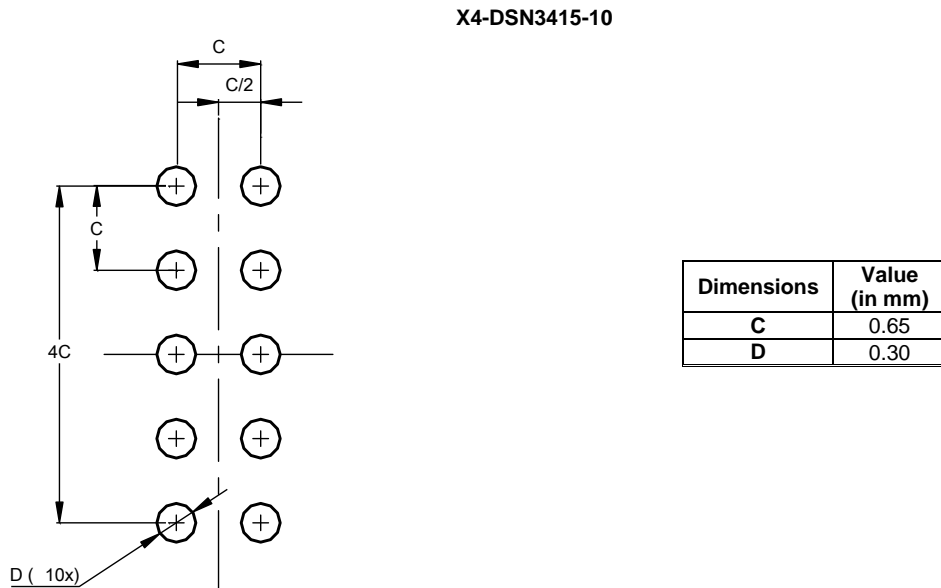
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**Suggested Pad Layout**

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