DAC5668/88/89EVM

1 Overview

1.1 Purpose

The DAC5668/88/89EVM provides a platform for evaluating the DAC5668, DAC5688, and DAC5689 digital-to-analog (DAC) converter under various signal, reference, and supply conditions. All three DACs are dual channel, 800MSPS interpolating DACs with DAC5668 being a 12-bit DAC and DAC5688/DAC5689 being 16-bit DACs. Also, both the DAC5668 and the DAC5688 have internal PLL/VCO, which is useful when a high-rate clock is not available at the system level. The table below summarizes the comparisons among the DAC family. The evaluation module also allows designers to analyze either a transformer-coupled output from the DAC or an RF-modulated output using Texas Instruments (TI) TRF3703 analog quadrature modulator. Use this document with the EVM schematic diagram and the corresponding device datasheet.

Table 1. Device Comparisons

	12-Bit	16-Bit	PLL/VCO	EVM Software
DAC5668	X		X	DAC5688
DAC5688		X	X	DAC5688
DAC5689		X		DAC5689

1.2 EVM Basic Functions

Digital inputs to the DAC can be provided with CMOS-level signals up to 250 MSPS through two 34-pin headers. The analog outputs from the DAC are available via SMA connectors. Because of its flexible design, the analog outputs of the DAC device can be configured to drive a 50-Ω terminated cable using a 4:1 or 1:1 impedance ratio transformer, or single-ended referred to AVDD. The EVM also allows for an option to use TI's TRF3703 analog quadrature modulator to mix the DAC outputs to RF.

The EVM also includes a TI CDCM7005 clock distribution device to clock the system. The CDCM7005 can be used with an onboard VCXO for full PLL functionality or with an external signal source, in which case the CDCM7005 functions as a buffer.

Power connections to the EVM are via banana jack sockets. In addition to the internal bandgap reference provided by the DAC device, the EVM allows an external reference to be provided to the DAC.

The DAC5668/88/89EVM allows the user to program the DAC and CDCM7005 registers through a USB port. The interface allows read and write access to all the DAC5668/88/89 registers and write-only access to the CDCM7005 registers.

1.3 Power Requirements

The DAC5668/88/89EVM requires 1.8-Vdc and 3.3-Vdc supplies for normal operation. An additional 5-Vdc supply is required to power up the TRF3703 for RF measurements.

1.3.1 Voltage Limits

CAUTION

Exceeding the maximum input voltages can damage EVM components. Undervoltage may cause improper operation of some or all of the EVM components.

2 Software Installation

The DAC5668/88/89EVM comes with a software package that allows the user to configure the DAC and CDCM7005 registers, save and load register settings to/from text files, and visualize the data path through the DAC. Communication with the EVM is achieved through a USB port on the host PC. The DAC5668 and the DAC5688 shares the same EVM software since both DACs have internal PLL/VCO. The DAC5689 has a stand-alone EVM software.

2.1 Minimum Requirements

Before installing the software, verify that the PC meets the following requirements:

- Microsoft Windows™ 2000 or later operating system
- 1024 × 768 screen resolution for optimal viewing
- USB 1.1 or later compatible input port

Other configurations may work; however, they remain untested.

2.2 Installing the EVM Control Software

Double-click the setup.exe file located on the installation CD. The EVM Installation Wizard opens.

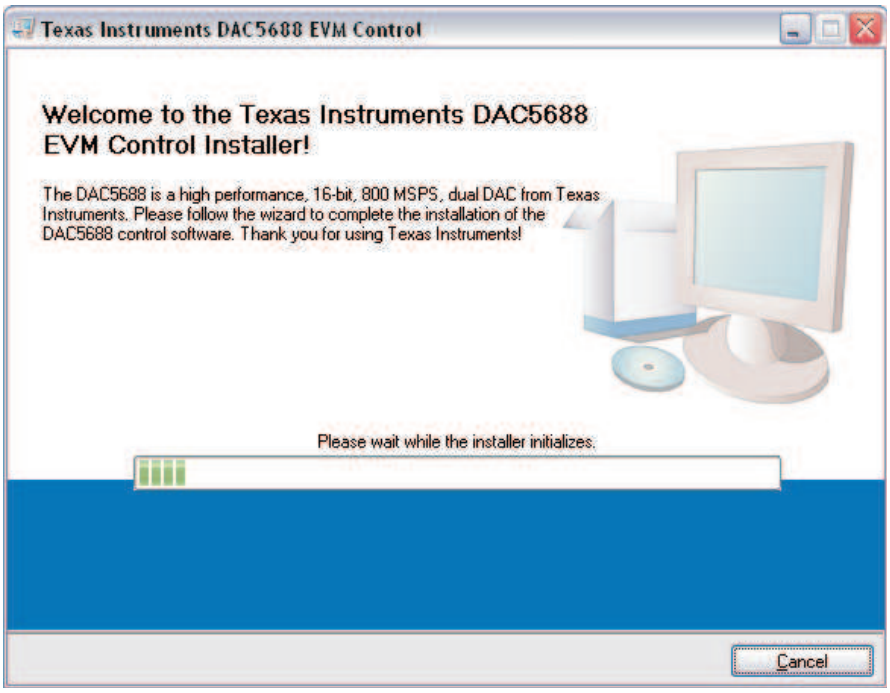


Figure 1. DAC5668/88/89/89EVM Install Screen

2.3 Installing the DAC5668/88/89EVM Instrument Drivers

As part of the installation Wizard, the EVM instrument drivers are installed automatically. Because the USB device driver is unsigned by Windows, the warning in Figure 2 appears. Press *Continue Anyway* to complete the installation.

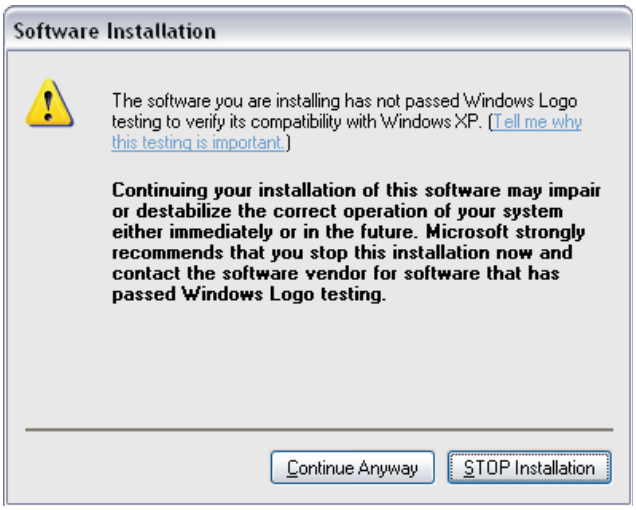


Figure 2. Windows USB Driver Warning

To finalize the installation, the installation Wizard asks the user to restart the computer. The system must be rebooted prior to running the software.

2.4 Installing the DAC5668/88/89EVM Hardware

After installing the EVM control software and drivers, connect the DAC5668/88/89EVM to a spare USB port of the host PC. If this is the first time connecting to the device, the Windows Found New Hardware Wizard guides you through the final setup steps. If the Hardware Wizard does not start, ensure that the cable is connected properly.

Instruct the Hardware Wizard to find the software automatically. If Windows is unable to find the drivers automatically, point it to the EVM program folder. The default folder for DAC5668/DAC5688 EVM software is *C:\Program Files\Texas Instruments\DAC5688\DAC5688 Drivers*. The default folder for DAC5689 EVM software is C:\Program Files\Texas Instruments\DAC5689\DAC5689 Drivers. A warning indicating that the drivers are unsigned by Windows appears. Press *Continue Anyway* to complete the setup.

To verify a complete installation, open Windows Hardware Device Manager and observe that the DAC5668/88/89EVM should be listed under the USB controllers list as shown in Figure 3.

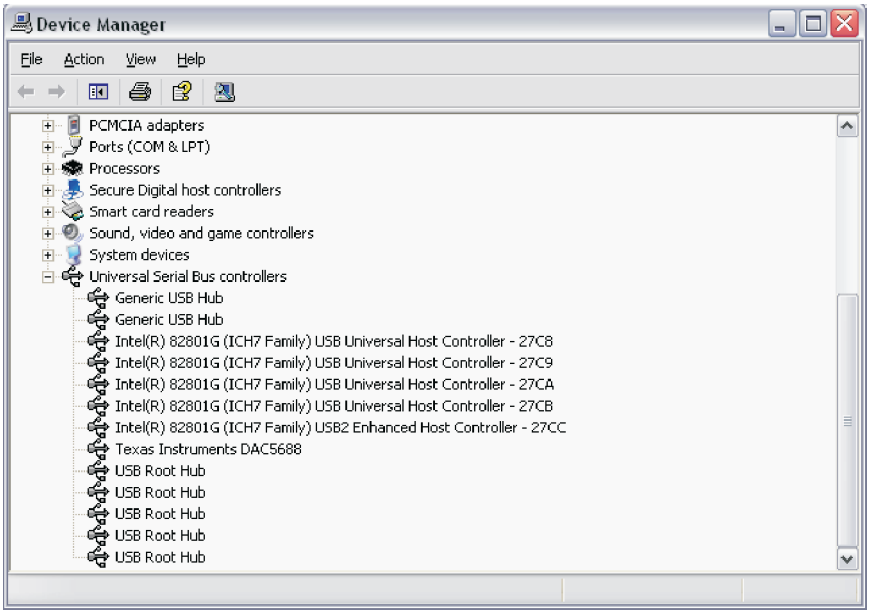


Figure 3. Hardware Device Manager

3 DAC5668/88/89EVM Description

The DAC5668/88/89EVM provides a robust and flexible evaluation system for the 800-MSPS interpolating DAC5668, DAC5688, and DAC5689 DAC family. In addition to the DAC5668/88/89, the EVM includes a CDCM7005 for clock distribution and a TRF3703 analog quadrature modulator path for RF measurements. For a complete hardware description, consult the schematics and layout sections at the end of this guide. See the DAC5668, DAC5688, DAC5689, CDCM7005, and TRF3703 data sheets for more information on each device.

3.1 Texas Instruments Components on the DAC5668/88/89EVM

A basic radio system block diagram is shown in Figure 4. The dashed-line box illustrates where the EVM fits in the system.

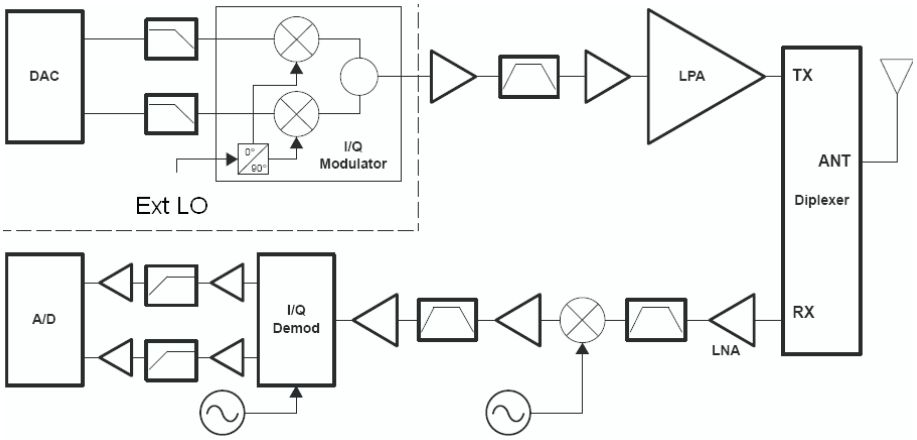


Figure 4. Basic Radio System

The block diagram of the EVM is shown in Figure 5. As illustrated on the block diagram, the DAC5668/88/89EVM includes three Texas Instruments components that make the entire solution an excellent choice for radio systems.

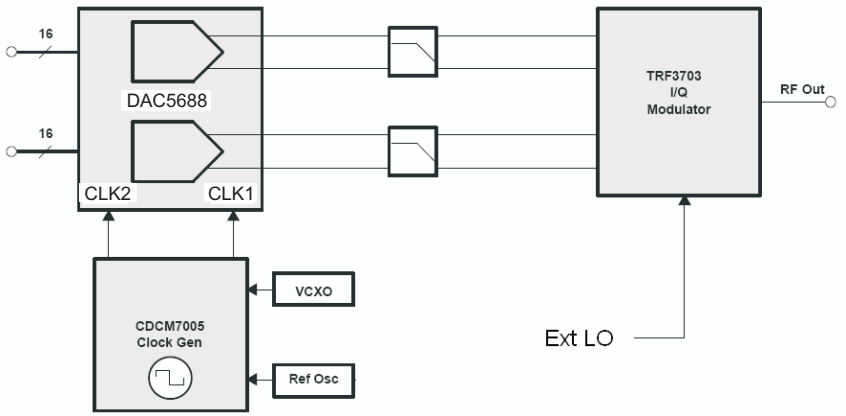


Figure 5. EVM Block Diagram

3.1.1 DAC5668/88/89

The DAC5668/88/89 are dual-channel, 800-MSPS interpolating DACs with dual CMOS digital data bus, integrated 2x-8x interpolation filters, a fine frequency mixer with 32-bit complex numerically controlled oscillator (NCO), IQ compensation, and internal voltage reference. Different modes of operation enable or bypass various signal processing blocks. The DAC5668 and the DAC5688 also include an internal 2x-32x clock multiplying PLL/VCO. This feature is useful when a high-rate clock is not available at the system level.

The DAC5668/88/89 dual-CMOS data bus provides 250-MSPS input data transfer per DAC channel. Several input data options are available: dual-bus data, single-bus interleaved data, even and odd multiplexing at half-rate, and an input FIFO with either external or internal clock to ease interface timing. Input data can be interpolated 2x, 4x, or 8x by onboard digital interpolating FIR filters with over 80 dB of stop-band attenuation.

The DAC5668/88/89 allows both complex and real output. An optional 32-bit NCO/mixer in complex mode provides frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. A digital inverse sinc filter compensates for natural DAC Sin(X)/X frequency rolloff. The digital Quadrature Modulator Correction (QMC) feature allows IQ compensation of phase, gain, and offset to maximize sideband rejection and minimize LO feedthrough of an external quadrature modulator performing the final single-sideband RF upconversion.

3.1.2 CDCM7005

The CDCM7005 is a high-performance, low-phase noise and low-skew clock synchronizer that synchronizes a VCXO (voltage-controlled crystal oscillator) or VCO (voltage-controlled oscillator) frequency to a reference clock. The CDCM7005 is used to generate and synchronize the clock outputs to the system. The device has five outputs which can be configured to LVPECL or LVCMOS levels and can be divided down by 1, 2, 3, 4, 6, 8, and 16. The divide by 16 can be replaced with a divide by 4 or 8 with a 90 degree phase shift.

3.1.3 TRF3703

The TRF3703 is a very-low-noise direct quadrature modulator, capable of converting complex modulated signals from baseband or IF directly up to RF based on the LO frequency.

4 DAC5668/88/89 Hardware Description

The DAC5668/88/89EVM can be set up in a variety of configurations to accommodate a specific mode of operation. Before starting evaluation, the user should decide on the configuration and make the appropriate connections or changes. The demonstration board comes with the following factory-set configuration:

- No VCXO installed. CDCM7005 in buffer mode which requires an input single-ended clock signal to SMA connector J20.
- The DAC outputs are set by default to drive the TRF3703.
- The converter is set to operate with internal reference. Jumper J5 EXTLO is installed between pins 1 and 2.
- Full-scale output current set to 20 mA through RBIAS resistor R91.

4.1 Jumper Settings

The DAC5668/88/89EVM has onboard jumpers that allow the user to modify the board configuration. Table 2 explains the functionality of the jumpers.

Table 2. Jumper List

JUMPER	LABEL	FUNCTION	DEFAULT CONDITION	SETTING
SW1	BRD_RESET	Resets the DAC and CDCM7005 devices		
JP1	REF_CLK	Chooses internal 10-MHz ref or external ref	Internal Ref	Pin 2-3
J1	VCXO_EN	VCXO power down	Disabled	Unpopulated
JP2	VCXOB	Chooses internal VCXO or external source	External source	Pin 2-3
JP3	VCXO	Chooses internal VCXO or external source	External source	Pin 2-3
JP4	CLK1/CLKOUT	Selects between CLK1 input to DAC or CLKOUT DAC output	CLKOUT	Pin 2-3
JP5	CLK1C/LOCK	Selects between CLK1C input to DAC or LOCK indicator DAC output	LOCK	Pin 2-3
JP6	VFUSE	Factory use only. Connect to 1.8VDD for normal operation.	1.8 VDD	Pin 1-2
J5	EXTLO	Internal (GND) or external (3.3V) voltage reference	Internal Reference	Pin 1-2
	$\overline{\text{CDC\_PD}}$	Active-low power down of CDCM7005	Active CDCM7005	Pin 2-3
	$\overline{\text{RESET}}$	DAC RESET Signal		Unpopulated
	$\overline{\text{CLKOUT\_EN}}$	Active-low enable of CLKOUT signal buffer	Enabled Buffer	Pin 1-2
	SYNC	DAC SYNC Signal	GND	Pin 1-2
	TX_ENABLE	DAC TX_ENABLE Signal	3.3V	Pin 2-3

4.2 Input/Output Connectors

Table 3 lists the input and output connectors on the DAC5668/88/89EVM.

Table 3. Input and Output Connections

REFERENCE DESIGNATOR	LABEL	CONNECTOR TYPE	DESCRIPTION
J2		34-pin Header	A-bus input data to the DAC.
J3	IOUTB1	SMA	Optional IOUTB1 output.
J4	IOUTB2	SMA	DACB transformer output. Optional IOUTB2 output.
J6	RFOUT	SMA	RF output from TRF3703.
J7		34-pin Header	B-bus input data to the DAC.
J8	IOUTA1	SMA	Optional IOUTA1 output.
J9	IOUTA2	SMA	DACA transformer output. Optional IOUTA2 output.
J10/J11	+5V	Banana Plug	+5-V connection pair. Required only for RF measurements.
J12	USB_CONN	USB	USB connector for software communication.
J13/J14	+1.8V	Banana Plug	+1.8-V connection pair.
J15/J16	3.3V	Banana Plug	+3.3-V connection pair.
J17	OUTCLK2 Y3A	SMA	Optional CDCM7005 clock output.
J18	OUTCLK2 Y4A	SMA	Optional CDCM7005 clock output.

Table 3. Input and Output Connections (continued)

REFERENCE DESIGNATOR	LABEL	CONNECTOR TYPE	DESCRIPTION
J19	OUTCLK1 Y4B	SMA	Optional CDCM7005 clock output.
J20	EXT_VCXO	SMA	External main clock input.
J21	DAC CLKOUT	SMA	CLKOUT output from DAC.
J22	EXT_REF_CLK	SMA	External reference clock input.
J23	RF_LO_IN	SMA	TRF3703 LO source input.

4.3 USB Interface

The DAC5668/88/89EVM contains a USB connector to interface to a USB 1.1 or later compliant USB port. Programming of the CDCM7005 and DAC is accomplished through this port.

4.4 Power Management

The DAC5668/88/89EVM requires 1.8-V and 3.3-V supplies for normal operation. An additional 5-V supply is required to power up the TRF3703 for RF measurements.

4.5 Input Data

The DAC5668/88/89EVM can accept 1.8-V or 3.3-V CMOS logic levels data inputs through the 34-pin headers J2 and J7 per Table 4 and Table 5. The board provides series dampening resistors to minimize digital ringing and switching noise. The DAC logic level is selected through software.

Table 4. Input Data Connector J2 – Data A Bus

Pin	Description	Pin	Description
1	CMOS data bit 15 (MSB)	18	GND
2	GND	19	CMOS data bit 6
3	CMOS data bit 14	20	GND
4	GND	21	CMOS data bit 5
5	CMOS data bit 13	22	GND
6	GND	23	CMOS data bit 4
7	CMOS data bit 12	24	GND
8	GND	25	CMOS data bit 3
9	CMOS data bit 11	26	GND
10	GND	27	CMOS data bit 2
11	CMOS data bit 10	28	GND
12	GND	29	CMOS data bit 1
13	CMOS data bit 9	30	GND
14	GND	31	CMOS data bit 0 (LSB)
15	CMOS data bit 8	32	GND
16	GND	33	SYNC
17	CMOS data bit 7	34	GND

Table 5. Input Data Connector J7 – Data B Bus

Pin	Description	Pin	Description
1	CMOS data bit 0 (LSB)	18	GND
2	GND	19	CMOS data bit 9
3	CMOS data bit 1	20	GND
4	GND	21	CMOS data bit 10
5	CMOS data bit 2	22	GND

Table 5. Input Data Connector J7 – Data B Bus (continued)

Pin	Description	Pin	Description
6	GND	23	CMOS data bit 11
7	CMOS data bit 3	24	GND
8	GND	25	CMOS data bit 12
9	CMOS data bit 4	26	GND
10	GND	27	CMOS data bit 13
11	CMOS data bit 5	28	GND
12	GND	29	CMOS data bit 14
13	CMOS data bit 6	30	GND
14	GND	31	CMOS data bit 15 (LSB)
15	CMOS data bit 7	32	GND
16	GND	33	TX_ENABLE
17	CMOS data bit 8	34	GND

4.6 Clock Configuration

The CDCM7005 requires a VCXO or external clock source to derive its output clock signals.

4.6.1 Buffer Mode

The DAC5668/88/89EVM does not come populated with a VCXO and requires an external sine wave source with a 1-Vrms, 0-V offset on SMA J20. Under this setup, the CDCM7005 operates as a buffer. To select this mode, the following changes need to be made:

1. JP2 and JP3 need to be set in position 2-3.
2. If a VCXO is installed, it is recommended to disable it by removing jumper J1.

4.6.2 PLL Mode

A VCXO can be installed in U6 to operate the CDCM7005 as a PLL. The following changes need to be made:

1. JP2 and JP3 need to be in the 1-2 position.
2. Install jumper J1.
3. A frequency reference (internal or external) needs to be provided.

4.6.3 DAC Clock Options

In both CDCM7005 configurations, the Y1A/Y1B outputs are used to drive the DAC5668/88/89 CLK2/CLK2C inputs. The DAC5668/88/89 can also be operated in dual-clock mode, in which case a second clock needs to be provided to the device. This clock may be single ended (CLK1) or differential (CLK1/CLK1C). The CDCM7005 Y2A/Y2B outputs may be used to provide this clock. To do this, the following changes need to be made:

1. If the clock is single ended, connect jumper JP4 in the 1-2 position.
2. If the clock is differential, connect jumpers JP4 and JP5 in the 1-2 position.

As an output, the CLK1 signal provides a clock at the data rate frequency. The data rate clock is used to drive a buffer and is accessible through SMA connector J21. This signal can be used to clock the data source to the DAC. To enable this output, the following changes need to be done to the board:

1. Connect jumper JP4 to position 2-3.
2. Jumper J5 /CLKOUT_EN must be in the 1-2 position.

If the device is not in dual-clock mode, the CLK1 pin can be configured as an output. The CLK1C pin can be configured as a PLL lock indicator. The PLL lock indicator is connected to LED D4 (JP5 must be in position 2-3). The DAC5689 does not have the internal PLL feature thus the PLL lock indicator is not functional.

4.7 Output Configuration

The DAC5668/88/89EVM has a resistor network that can be configured such that the DAC outputs are routed to the TRF3703 for an RF measurement or routed to the transformer path for a DAC measurement. The default setup on the board is for RF output.

4.7.1 DAC Outputs

To configure the DAC5668/88/89EVM to evaluate the DAC outputs, the following changes need to be done to the board:

1. R46, R56, R58, and R69 need to be uninstalled
2. R45, R55, R57, and R68 need to be installed

If the board is configured for DAC outputs, the TRF3703 modulator is not used and the 5-Vdc supply is unnecessary. The DAC outputs in this setup are in J4 and J9.

The DAC outputs can be configured to drive a doubly terminated 50-Ω cable or to provide unbuffered differential outputs.

4.7.1.1 Transformer-Coupled Signal Output

The factory-set configuration of the EVM provides the user with single-ended DAC output signals at SMA connectors J4 and J9. The DAC outputs are configured to drive a doubly terminated 50-Ω cable using a 4:1 impedance ratio transformer with the center tap of the transformers connected to +3.3 Vdc.

4.7.1.2 Unbuffered Differential Output

To provide unbuffered differential outputs, the EVM must be configured as follows:

1. Remove T1 and T2.
2. Install R36 (24.9 Ω), R37 (24.9 Ω), R74 (24.9 Ω), R75 (24.9 Ω), R34, R41, R42, R71, R72, and R77.

With a 20-mA, full-scale output current, this configuration provides a 0.5-Vpp output.

4.7.2 RF Output

To configure the DAC5668/88/89EVM to evaluate the RF output (default setup), the following changes need to be done to the board:

1. R46, R56, R58 and R69 need to be installed
2. R45, R55, R57, and R68 need to be uninstalled

If the board is configured for RF output, the 5-Vdc must be applied to power up the modulator. The output in this setup is in J6.

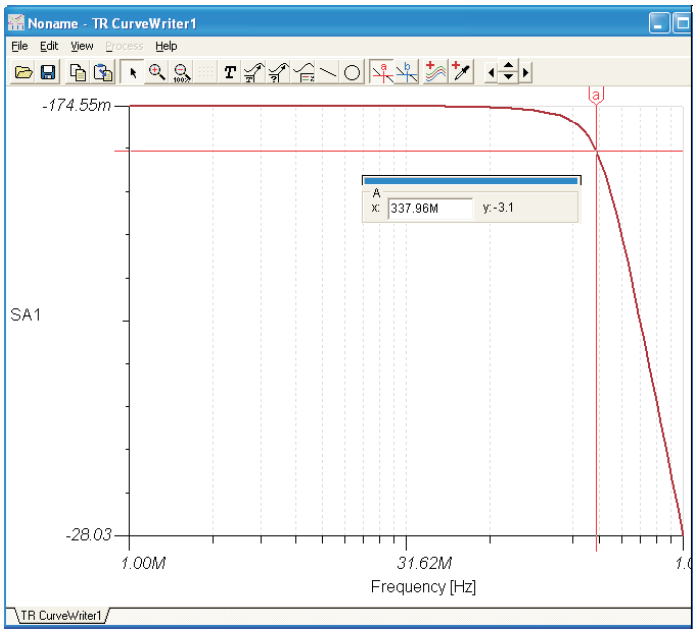
4.7.2.1 TRF3703 LO Source

The DAC5668/88/89EVM requires an external local oscillator (LO) source to drive the onboard TRF3703 modulator. This external LO input needs to be connected to the SMA connector J23. The signal level of the LO source must comply with the requirements in the TRF3703 data sheet (SLWS184), but typically an LO power around 0-to-3 dBm is adequate.

4.7.2.2 DAC-to-Modulator Interface

The TRF3703 quadrature modulator requires a common-mode dc voltage of approximately 3.3 V. In order to use the dc-offset adjustment capabilities of the DAC5668/88/89 for carrier suppression, it is imperative to maintain a dc path from the DAC output to the modulator input. The common-mode voltage for the modulator is maintained with a passive resistor network that is designed to provide the proper operation point for the DAC and the TRF3703 modulator.

The DAC5668/88/89EVM is configured with enough pads to provide a specific fifth-order differential passive LC filter. By default, it is only populated with a simple LC low-pass filter to attenuate the higher clock harmonics. The 3-dB corner of this filter is approximately 300 MHz.



The DAC5668/88/89EVM also includes a pi pad network on the modulator output to provide some matching or filtering, if desired. In its default state, the pad is not used and a series capacitor is used on the RF output.

4.8 Reference Operation

The DAC full-scale output current is set by applying an external resistor (R91) between the BIASJ pin of the device and ground. The full-scale output current can be adjusted from 20 mA down to 2 mA by varying this resistor. The full-scale output current, IOUTFS, is defined as follows:

$$IOUT_{FS} = 16 \times \left(\frac{V_{EXTIO}}{R91} \right) \quad (1)$$

where V_{EXTIO} is the voltage at pin EXTIO. This voltage is 1.2 V when using the internally provided bandgap reference voltage source. The internal reference can be disabled and overridden by an external reference by connecting a voltage source to EXTIO and connecting EXTLO to +3.3 Vdc (J5 EXTLO connected between pins 2 and 3). The specified range for external reference voltages must be observed.

5 DAC5668/88/89 EVM Software

The EVM Control Software is started by accessing the *Windows Start → All Programs → Texas Instruments DACs* cascading menus. The DAC5668 and the DAC5688 share the same EVM software, and the DAC5689 has a stand-alone EVM software.

The DAC EVM application allows users to:

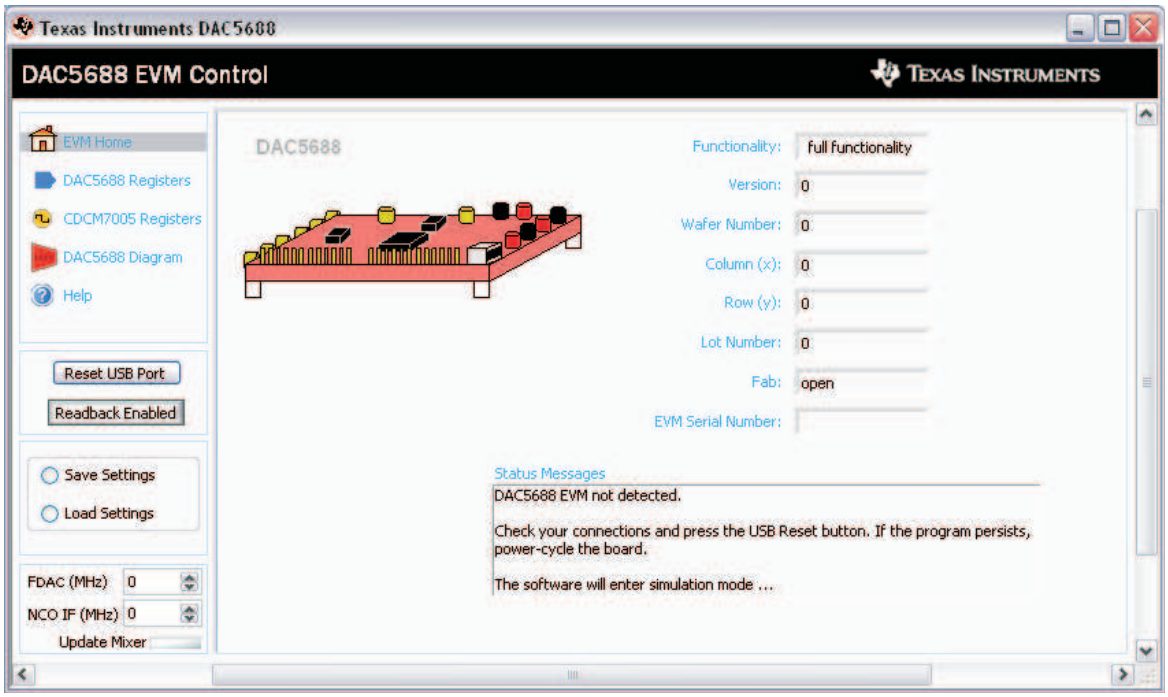
- Configure the DAC and CDCM7005 registers.
- Save and load register settings using text files.
- Visualize the data path through the DAC.

5.1 Software Description

The software has five main settings that allow you to modify the functionality of the active panels. You can switch between these settings by selecting one of the Menu items described in Table 6.

Table 6. Software Main Settings

SETTING	FUNCTION
EVM Home	EVM and DAC serial information. EVM communication status
DAC Registers	DAC register settings (See the DAC data sheet for detailed information on each register)
CDCM7005 Registers	CDCM7005 register settings (See the CDCM7005 data sheet for detailed information on each register)
DAC Diagram	DAC data path under current register settings
Help	Displays a short description of each DAC setting



5.1.1 General Controls

Reset USB Port:

Begins a new USB session. Click this button if a status error message occurs.

Readback Enabled/Disabled:

Enable or disables the DAC register reads. When Readback is disabled, the software enters simulation mode. If communicating with the DAC is a problem, the software enters into simulation mode automatically.

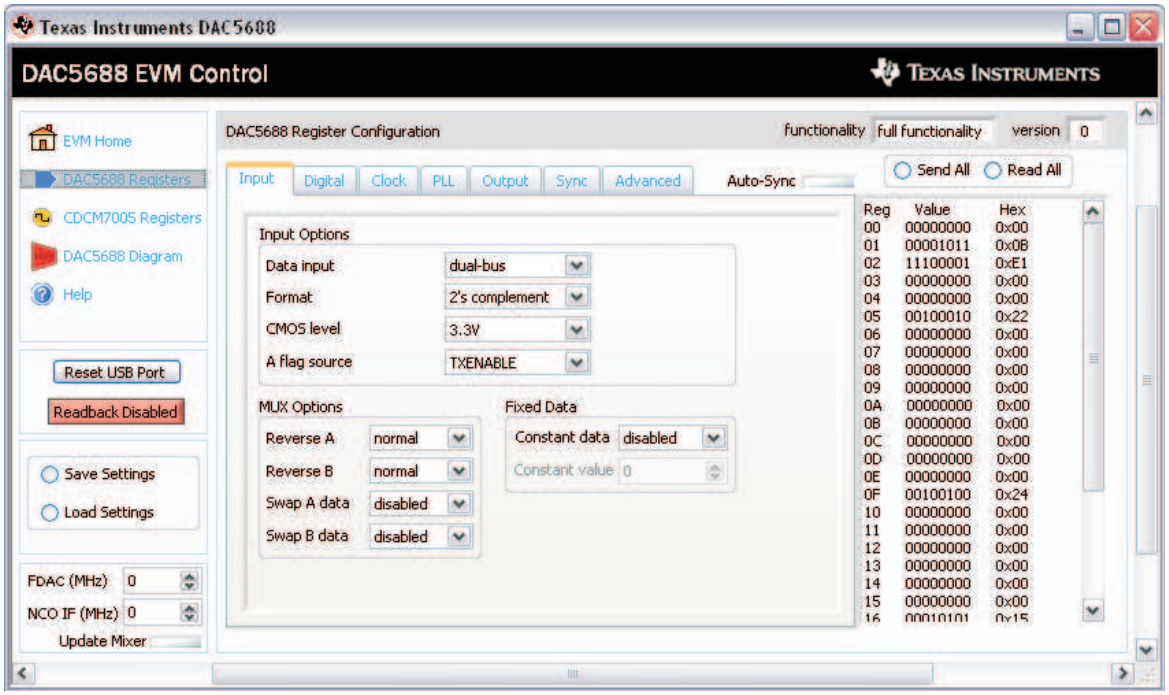
Save Settings:

Saves the DAC and CDCM7005 register configurations to a text file for future use.

Load Settings:

Loads a DAC and CDCM7005 register configuration from a text file and updates the GUI.

5.1.2 DAC5688 Specific Controls



Tab Control (Input, Digital, Clock, etc.):

Switches between the diffferent DAC registers.

Auto-Sync:

Synchronizes all the digital blocks on the DAC using the soft-sync register.

Send All:

Sends the current front panel registers to the device. This is generally only used when the EVM power has recycled, or the device has been reset and the user wants to load the displayed settings to the device.

Read All:

Reads the current registers on the DAC. This is used to verify settings on the front panel.

FDAC(MHz):

Enters the DAC frequency in MHz for NCO calculation.

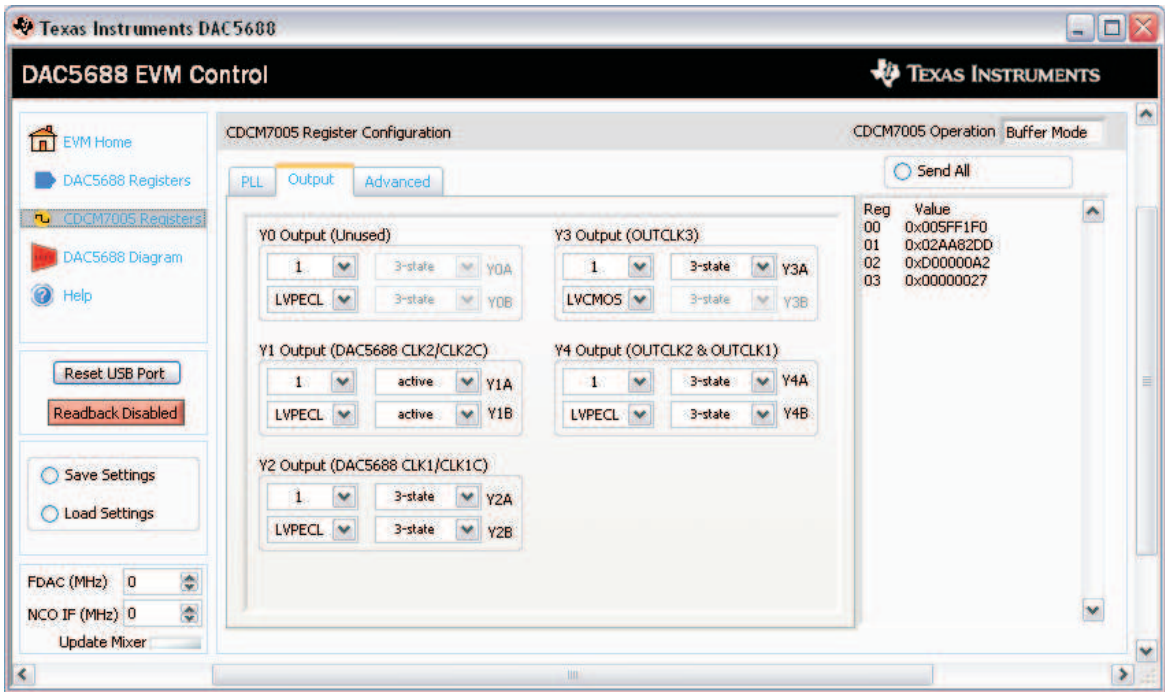
NCO IF (MHz):

Desired mixing frequency in MHz when using the DAC mixer.

Update mixer:

Used to update the NCO DDS register value.

5.1.3 CDCM7005 Specific Controls



Tab Control (PLL, Output, Advanced):

Switches between the different CDCM7005 registers.

CDCM7005 Operation:

Select *Buffer Mode* when no VCXO is installed or the VCXO is disabled. In this case, the CDCM7005 operates as a buffer. Select *PLL Mode* when a VCXO is being used by the CDCM7005.

Send All:

Sends the current front panel registers to the device. This is generally only used when the EVM power has recycled, or the device has been reset and the user wants to load the displayed settings to the device.

6 DAC5668/88/89EVM Initial Power Up and Test

The steps described in this section show how to connect and configure the DAC5668/88/89EVM for evaluation under the default settings.

1. Connect the DAC5668/88/89EVM digital connector (J2 and J7) to a digital test pattern generator capable of providing 3.3-V or 1.8-V CMOS logic level inputs such as Texas Instruments TSW3100.
2. Use the DAC5668/88/89 EVM DAC_CLKOUT (J21) SMA connector to trigger the pattern generator. In the case of the TSW3100 pattern generator, the trigger input is CMOS CLK (J73) SMA connector.
3. Connect the 1.8-V (J13/J14), 3.3-V (J15/J16) and 5-V (J10/J11) power supplies. Ensure that each supply is not drawing more than 1 A of current. Turn on the power supplies. Press SW1 to reset the board.
4. Provide a single-ended, 1-Vrms, 0-V, offset sine-wave signal to the DAC5668/88/89 EXT_VCXO (J20) SMA connector. LED D3 should illuminate indicating that a signal has been detected. If not, verify that the correct signal is being provided.
5. Connect a 0-dBm LO signal to the RF_LO_IN (J23) SMA connector.
6. Connect one end of the supplied USB cable to an available USB port on the host PC. Connect the other end of the cable to J1 on the DAC5668/88/89EVM.

7. Open the EVM Software. The DAC software detects if the USB port is active and if it is capable of reading the EVM serial number. Read the Status Messages to determine if the communication is successful.
8. Program the CDCM7005 and DAC registers as necessary. An example configuration file *example.txt* is included under the installation folder: *C:\Program Files\Texas Instruments\DAC5688/89\DAC5688/89 Configuration Files*
9. Program and run the pattern generator. If using the TSW3100, see the user's guide for more information on how to set up a digital pattern.
10. The DAC5668/88/89EVM RF output can be monitored using SMA connector J6 (RFOUT).

7 Bill of Materials and Schematics

This section contains the bill of materials, printed-circuit board layout, and schematics of the DAC5668/88/89EVM.

7.1 Bill of Materials

Qty	Part Reference	Value	PCB Footprint	Mfr_Name	Mfr_Part_Number	Note
42	C1 C6-C8 C14 C15 C18 C21 C24 C28 C29 C32 C52 C61-C65 C67-C75 C77-C79 C82 C87 C88 C91 C92 C98 C100-C104 C107	1μF	0402	Panasonic	ECJ-0EB1C104K	
1	C2	0.47μF	0603	Murata	GRM188R71C474KA88D	
6	C3 C55 C66 C85 C89 C113	1000pF	0402	Panasonic	ECJ-0EB1E102K	
1	C4	22μF	tant_a	Kemet	T494A226M010AS	
8	C5 C34 C42-C46 C111	1μF	0603	Panasonic	ECJ-1V41E105M	
5	C9 C10 C60 C97 C99	0.01μF	0402	Panasonic	ECJ-0EB1E103K	
12	C11 C33 C56 C57 C76 C81 C84 C90 C108 C112 C115 C126	10μF	tant_a	Kermet	T494A106M016AS	
0	C12 C13 C30 C31	4.7pF	0603	Panasonic	ECJ-1VC1H047C_DNI	DNI
0	C16 C26	2.2pF	0603	AVX	06035A2R2CAT2A_DNI	DNI
2	C17 C27	2.7pF	0603	AVX	06035A2R7CAT2A	
2	C19 C25	22pF	0402	Panasonic	ECJ-0EC1H220J	
2	C20 C80	100pF	0402	Panasonic	ECJ-0EB1E101K	
0	C22 C23	DNI	0402	Panasonic	ECJ-0EB1E103K_DNI	DNI
7	C35 C47-C51 C110	47μF	tant_b	Kemet	T494B476M010AS	
8	C36-C41 C54 C109	0.01μF	0603	Panasonic	ECJ-1VB1C103K	
3	C53 C83 C86	4.7μF	tant_a	AVX	TAJA475K020R	
1	C58	560pF	0402	Panasonic	ECJ-0EB1H561K	
1	C59	0.01μF	0603	Kemet	C0603C103K1RACTU	
1	C93	330pF	0402	Panasonic	ECJ-0EB1E331K	
2	C94 C96	3.3pF	0402	Murata	GRM1555C1H3R3CZ01D	
1	C95	0.033μF	0402	AVX	0402ZC333KAT2A	
2	C105 C106	47pF	0603	Panasonic	ECJ-1VC1H470J	
4	D1-D4	LED Green	LED_0805	Panasonic	LNJ306G5UUX	

Qty	Part Reference	Value	PCB Footprint	Mfr_Name	Mfr_Part_Number	Note
3	D5-D7	MBRB2515L	DIODE_MBRB2515L	Semiconductor	MBRB2515LT4G	
12	FB1-FB12	68 Ω at 100MHz	1206	Panasonic	EXC-ML32A680U	
1	J1	Header_1x2_100_230L	HDR_THVT_1x2_100_M	Samtec	TSW-103-07-L-S	
2	J2 J7	TSM-117-01-S-DV-LC	SAMTEC_TSM_117_01_S_DV_LC	Samtec	TSM-117-01-S-DV-LC	
0	J3 J8	SMA_PCB_THVT	SMA_THVT_312x312	Johnson Components	142-0701-201_DNI	DNI
2	J4 J9	SMA_PCB_THVT	SMA_THVT_312x312	Johnson Components	142-0701-201	
1	J5	HMTSW-107-07-G-T	HDR_THVT_3x7_100_M	Samtec	HMTSW-107-07-G-T	See Note
8	J6 J17-J23	SMA_END_RND	SMA_SMEL_218x247_096	Johnson Components	142-0761-801	
3	J10 J14 J16	BANANA_JACK_BLK	JACK_THVT_BANANA_250dia	Alectron	ST-351B BLK	
3	J11 J13 J15	BANANA_JACK_RED	JACK_THVT_BANANA_250dia	Alectron	ST-351A RED	
1	J12	USB_B_S_F_B_TH	CON_THRT_USB_B_F	Samtec	USB-B-S-F-B-TH	
5	JP1-JP5	HEADER_1x3_100_430L	HDR_THVT_1x3_100_M	Samtec	HMTSW-103-07-G-S-.240	(SHUNT 2-3)
0	JP6	HEADER_1x3_100_430L	HDR_THVT_1x3_100_M	Samtec	HMTSW-103-07-G-S-.240	DNI
0	L1 L10	56nH	ind_0603	Panasonic	ELJ-RE56NJF3_DNI	DNI
4	L2 L3 L8 L9	10nH	0603	Coilcraft	0603CS-10NXLU	
4	L4-L7	68nH	0603	Coilcraft	0603CS-68NXJL	
3	R1 R3 R84	1K	0402	Panasonic	ERJ-2RKF1001X	
13	R2 R27 R79 R88 R89 R96 R98-R104	22.1	0402	Panasonic	ERJ-2RKF22R1X	
0	R4	1K	0402	Panasonic	ERJ-2RKF1001X_DNI	DNI
1	R5	162	0402	Panasonic	ERJ-2RKF1620X	
7	R6 R7 R80 R81 R108 R112 R113	10K	0402	Panasonic	ERJ-2RKF1002X	
1	R8	4.75K	0402	Panasonic	ERJ-2RKF4751X	
4	R9 R15 R29 R93	750	0402	Panasonic	ERJ-2RKF7500X	
8	R10 R13 R16 R20 R30-R33	82.5	0402	Panasonic	ERJ-2RKF82R5X	
8	R11 R12 R17 R19 R23-R26	130	0402	Panasonic	ERJ-2RKF1300X	
5	R14 R18 R78 R85 R95	0	0402	Panasonic	ERJ-2GE0R00X	
3	R21 R22 R28	150	0402	Panasonic	ERJ-2RKF1500X	
0	R34 R41 R42 R46 R56 R58 R69 R71 R72 R77	0	0603	Panasonic	ERJ-3GEY0R00V_DNI	DNI
0	R35 R39 R73 R76	60.4	0603	Yageo	RC0603FR-0760R4L_DNI	DNI
11	R36 R37 R44 R74 R75 R92 R105 R107 R109-R111	100	0402	Panasonic	ERJ-2RKF1000X	
0	R38 R43 R86 R87	130	0402	Panasonic	ERJ-2RKF1300X_DNI	DNI
2	R40 R70	90.9	0603	Panasonic	ERJ-3EKF90R9V	
9	R45 R50 R51 R55 R57 R63 R64 R68 R94	0	0603	Panasonic	ERJ-3GEY0R00V	
4	R47 R53 R59 R66	115	0603	Yageo	RC0603FR-07115RL	
4	R48 R54 R60 R67	634	0603	Yageo	RC0603FR-07634RL	
4	R49 R52 R61 R65	60.4	0603	Yageo	RC0603FR-0760R4L	
1	R62	49.9	0402	Panasonic	ERJ-2RKF49R9X	

Qty	Part Reference	Value	PCB Footprint	Mfr_Name	Mfr_Part_Number	Note
0	R82	221	0603	Panasonic	ERJ-3EKF2210V_DNI	DNI
0	R83	110	0603	Panasonic	ERJ-3EKF1100V_DNI	DNI
1	R90	93.1	0402	Panasonic	ERJ-2RKF93R1X	
1	R91	953	0402	Panasonic	ERJ-2RKF9530X	
4	RN1-RN4	4816P-001-220	RNET_16_225x445_50	Bourns	4816P-001-220	
1	SW1	SW RESET	switch_reset	C&K	KT11P3JM	
2	T1 T2	ADT4-1T	TFMR_6_250x340_100_custom	Mini-Circuits	ADT4-1T	
6	TP1 TP2 TP4 TP6 TP8 TP10	Blk	TP_THVT_100_RND	Keystone Electronics Corp.	5001	
3	TP3 TP5 TP7	Testloop_Red	TP_THVT_060_RND	Keystone Electronics Corp.	5000	
1	U1	DAC5688/89	QFN_64_360x360_0p50mm_pwr pad	Texas Instruments	DAC5688/89RGC	
2	U2 U8	SN74LVC1G125DBVR	SOT_5_120x69_57	Texas Instruments	SN74LVC1G125DBVR	
0	U3	614.4MHZ	VCXO_6_CUSTOM	Toyocom	TCO-2111-491.52_DNI	DNI
1	U4	CDCM7005	QFN48	Texas Instruments	CDCM7005RGZT	
1	U5	TRF3703-33	QFN24	Texas Instruments	TRF3703-33IRGET	
1	U6	OSC-VECTRON	OSC_4_SM_460x386	VECTRON	VTD3-J0BC-10M00	
0	U7	OSC-VECTRON	XTAL_4_SM_203x132	VECTRON	VTC4_DNI	DNI
1	U9	FT245RL	ssop_28_413x220_26	FTDI Chip	FT245RL	
1	U10	SN74AHC541PW	tssop_20_260x177_26	Texas Instruments	SN74AHC541PW	
1	U11	SN74HC241PW	tssop_20_260x177_26	Texas Instruments	SN74HC241PW	
10	Z_SH-H1-Z_SH-H10	SHUNT-HEADER		Keltron	MJ-5.97-G	Shunt for header
6	X_SCREW1-X_SCREW6	SCREW PANHEAD 4-40 x 3/8		Building Fasteners	PMS 440 0038 PH	
4	X_STANDOFF1-X_STANDOFF4	STANDOFF ALUM HEX 4-40 x .500		Keystone	2203	

7.2 Printed-Circuit Board Layout

The following illustrations present the layers of the DAC5668/88/89EVM board.

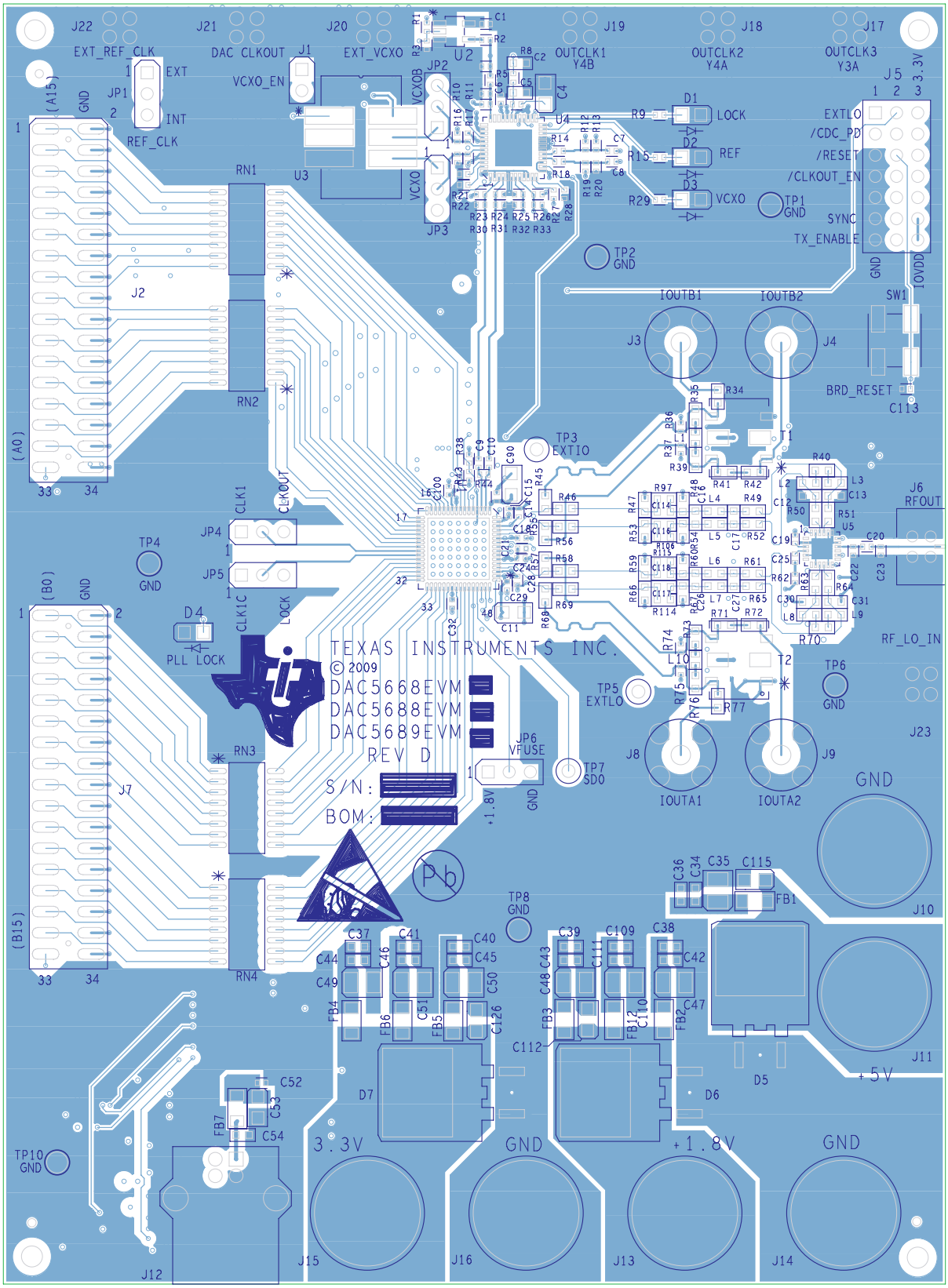


Figure 6. Top Silk Screen

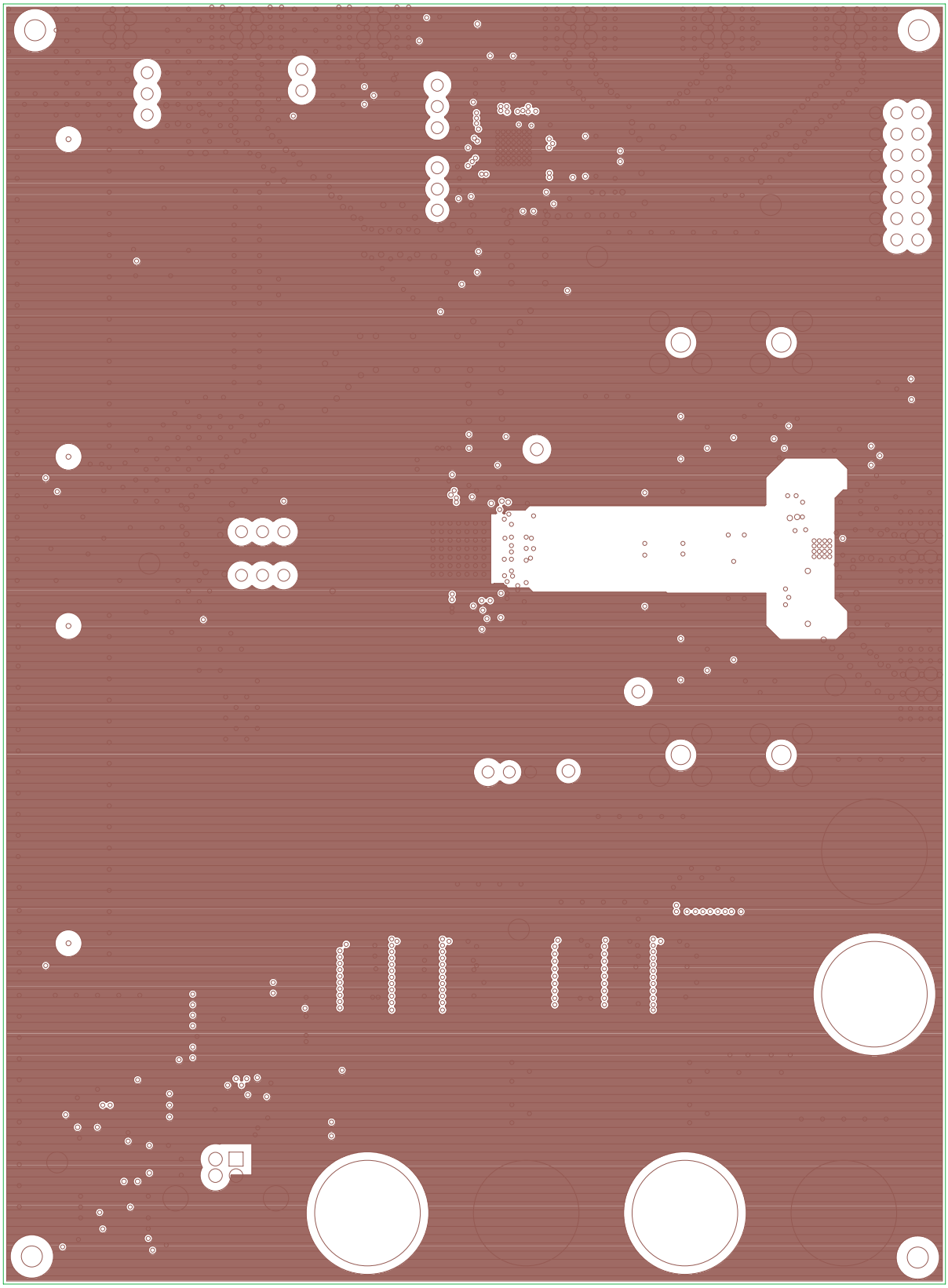


Figure 7. Layer 2, GND

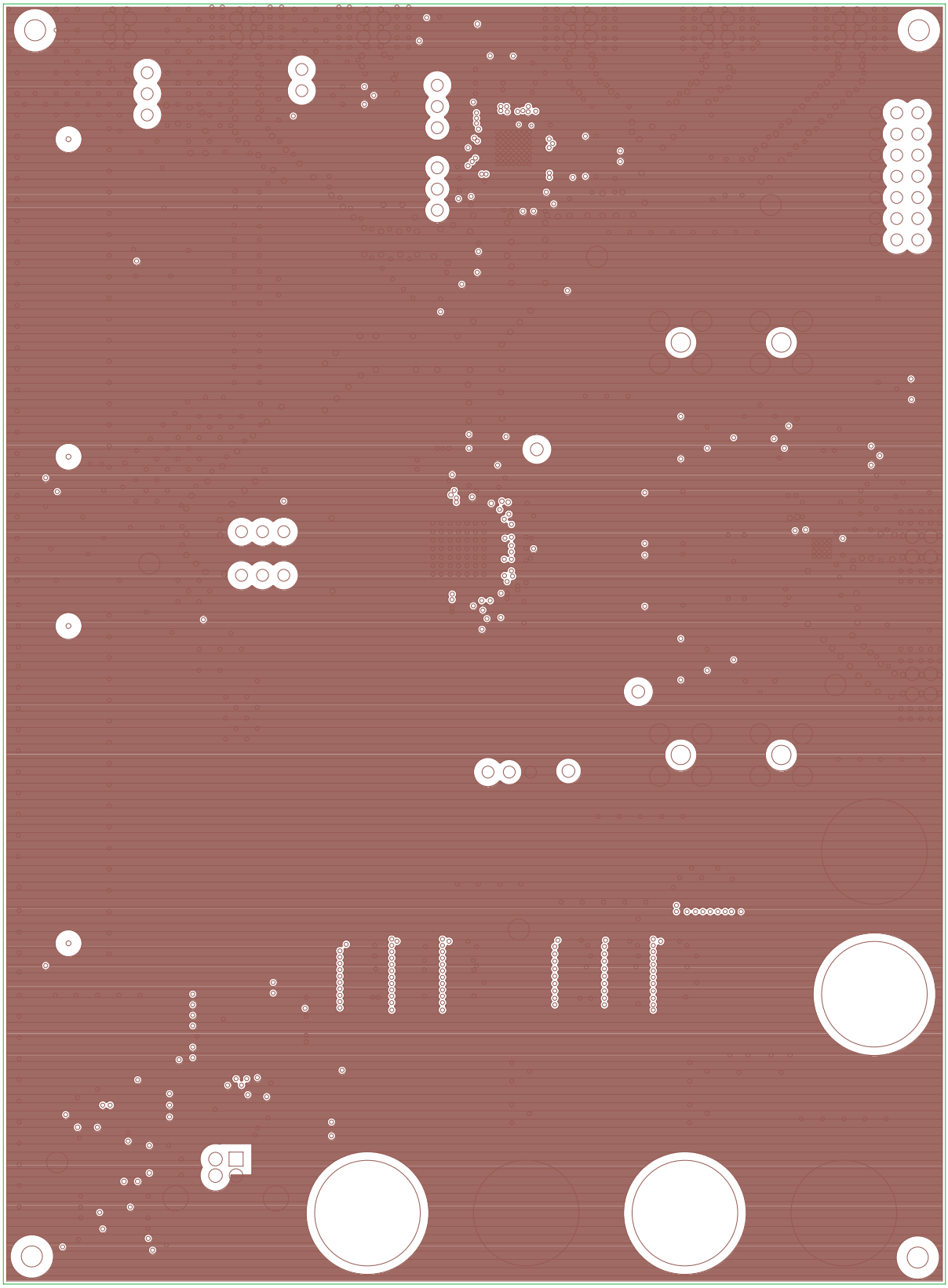


Figure 8. Layer 3, GND

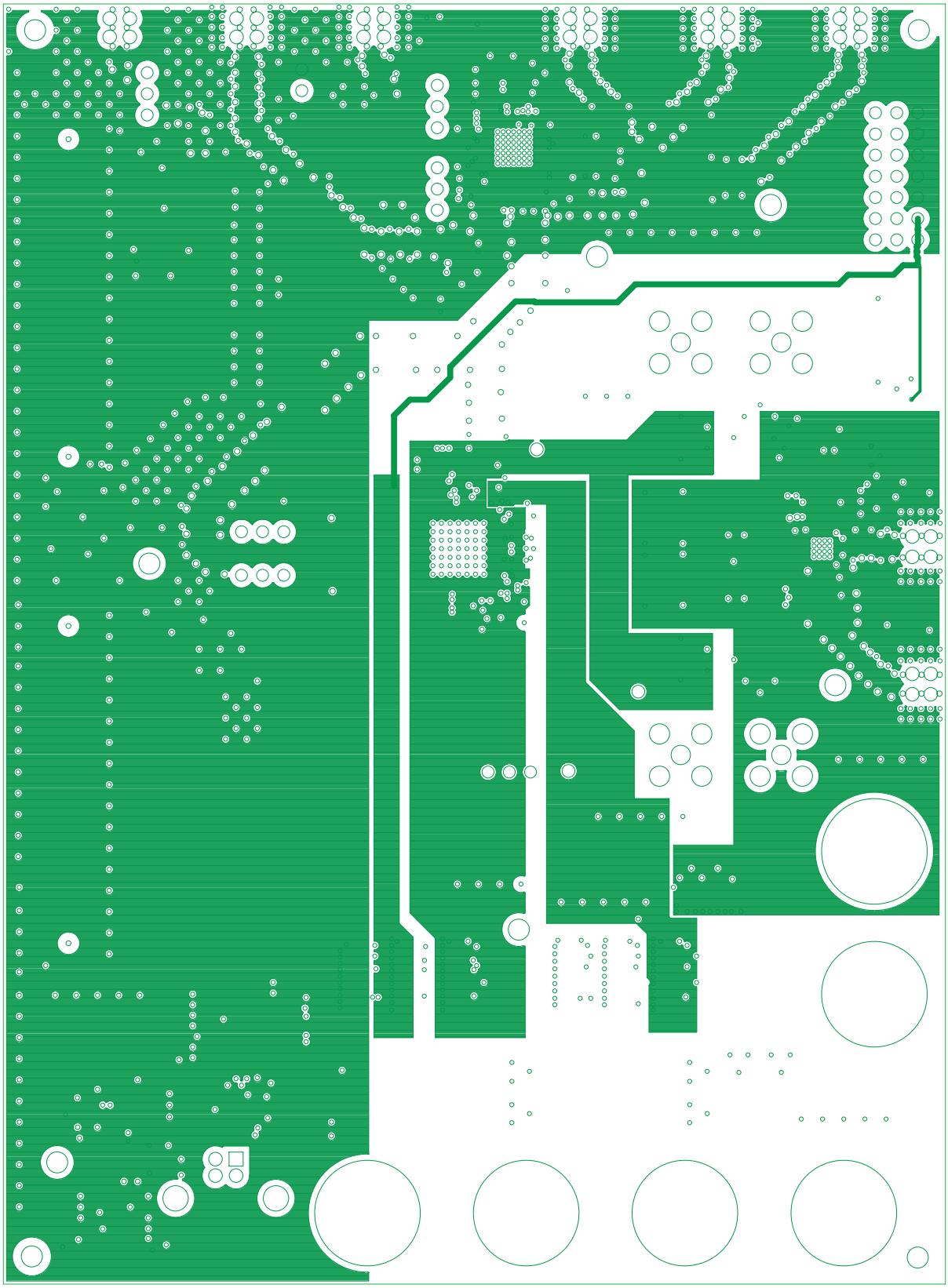


Figure 9. Layer 4, PWR

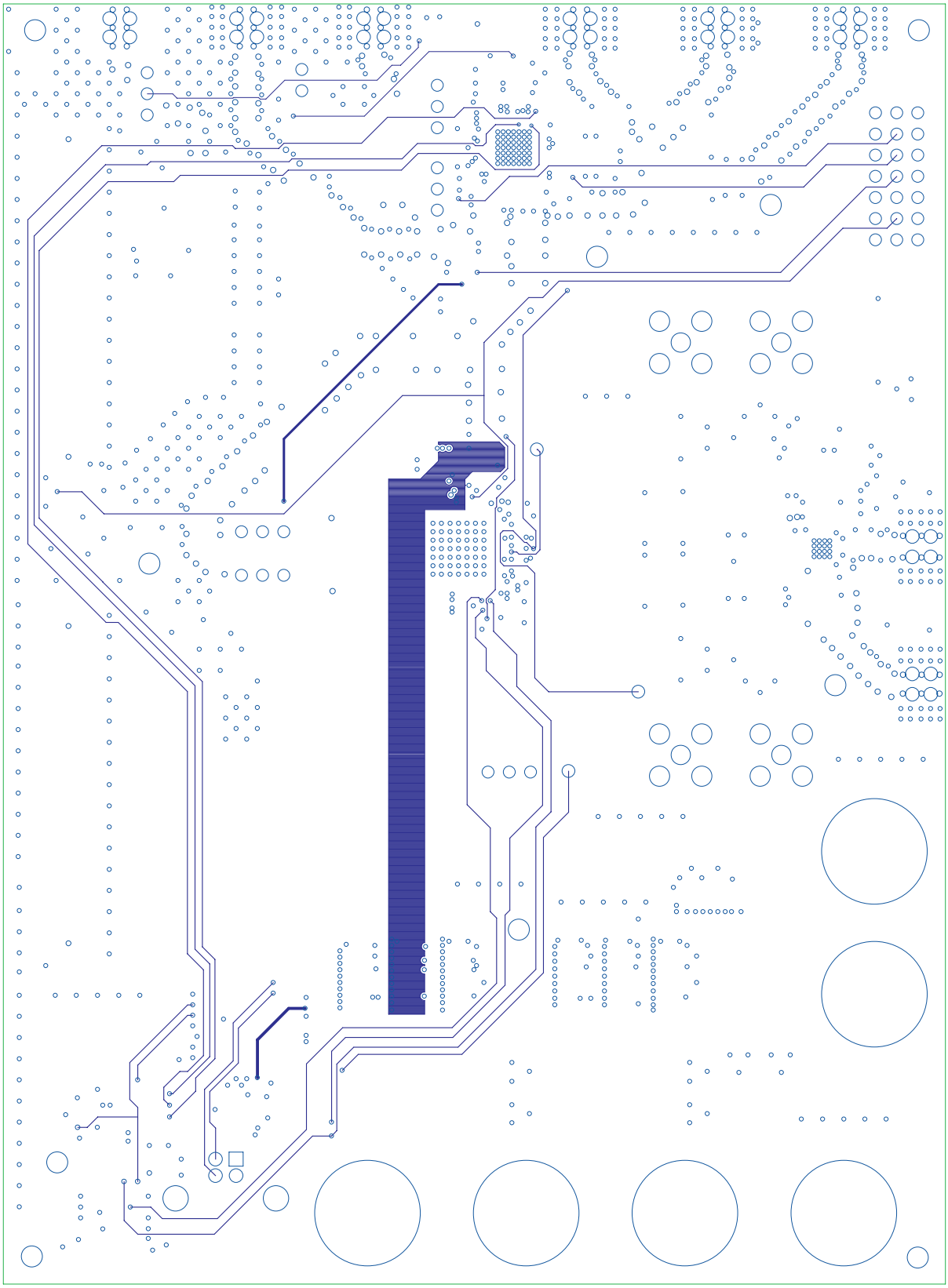


Figure 10. Layer 5

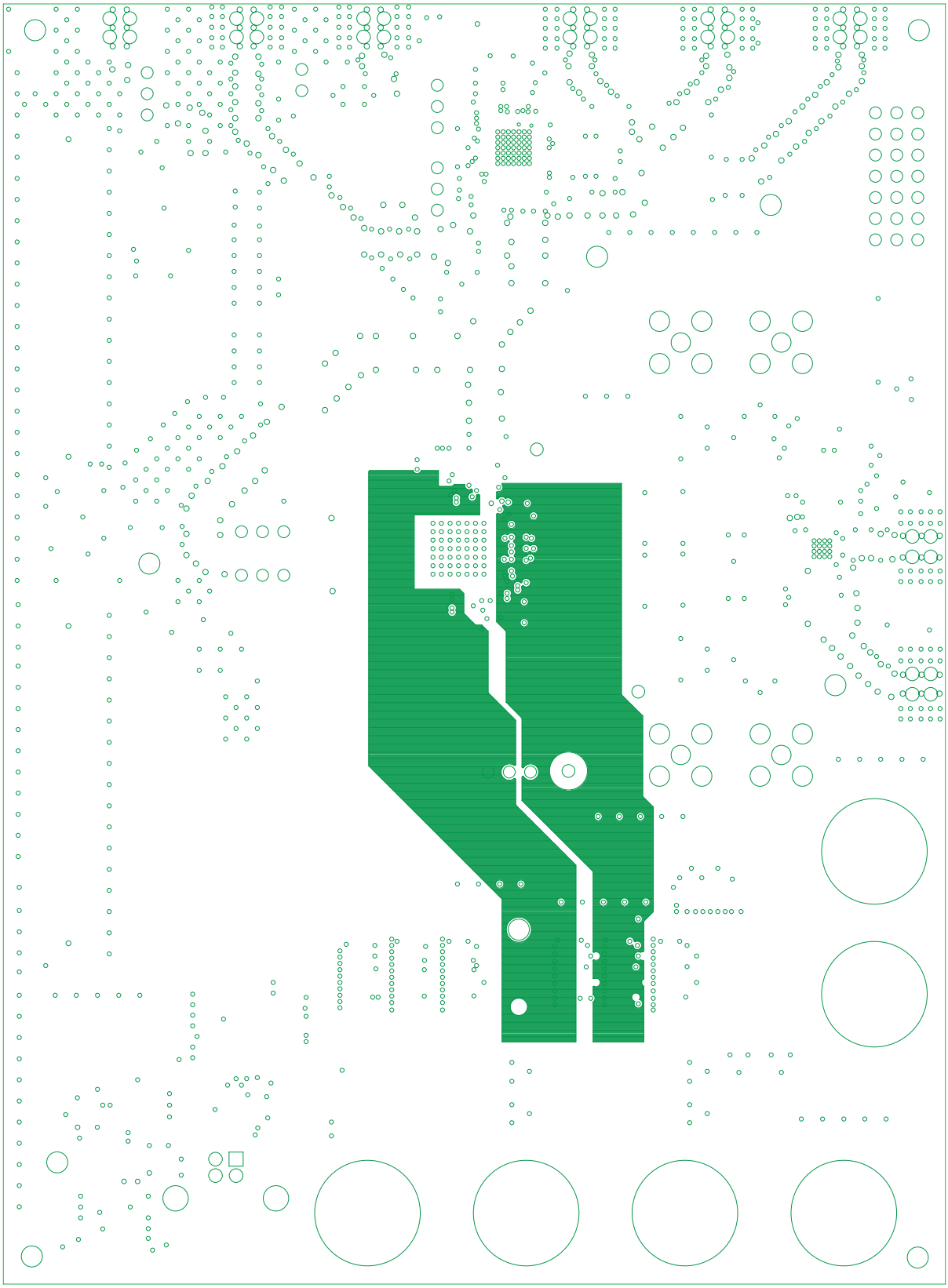


Figure 11. Layer 6, PWR

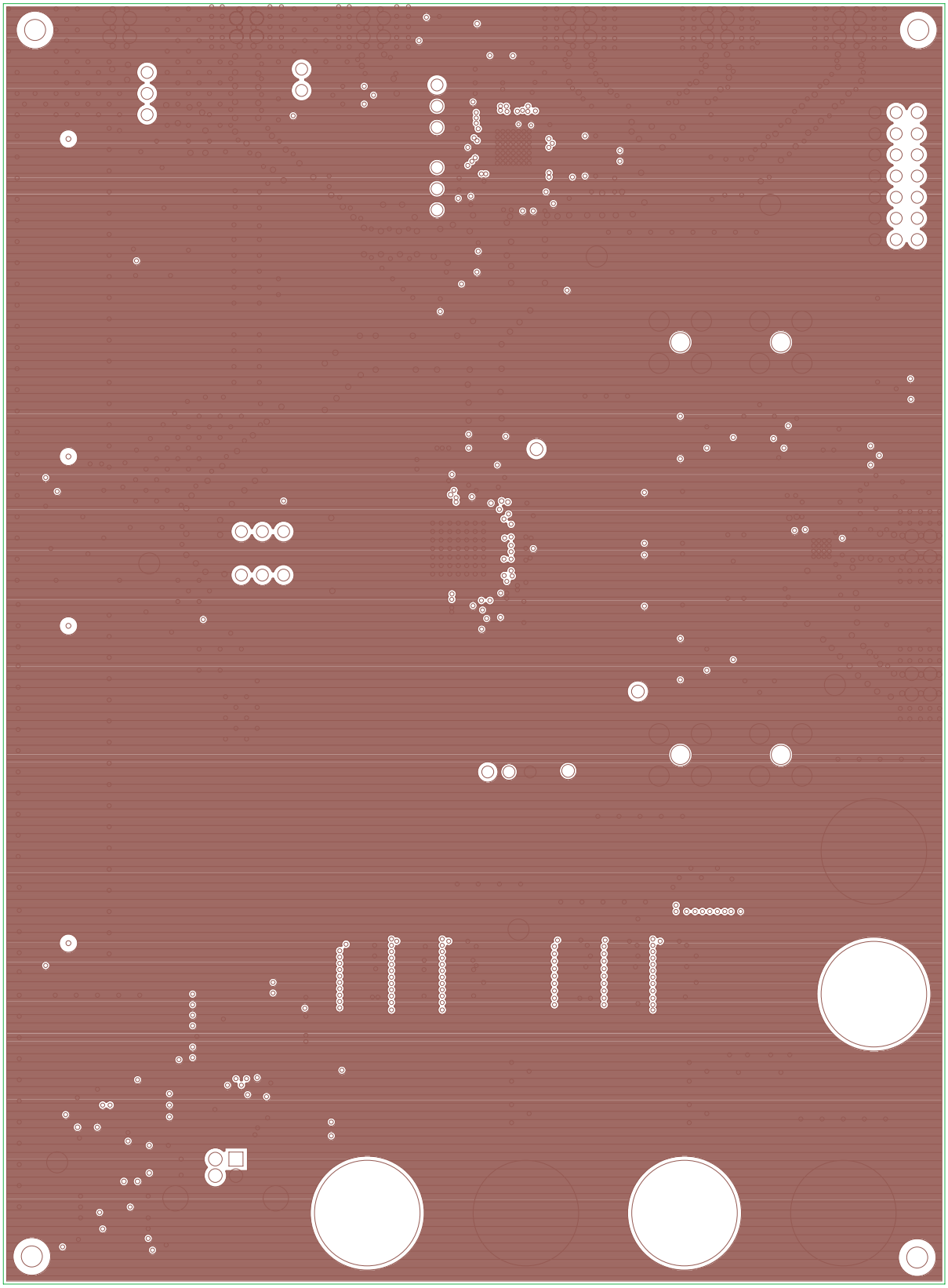


Figure 12. Layer 7, GND

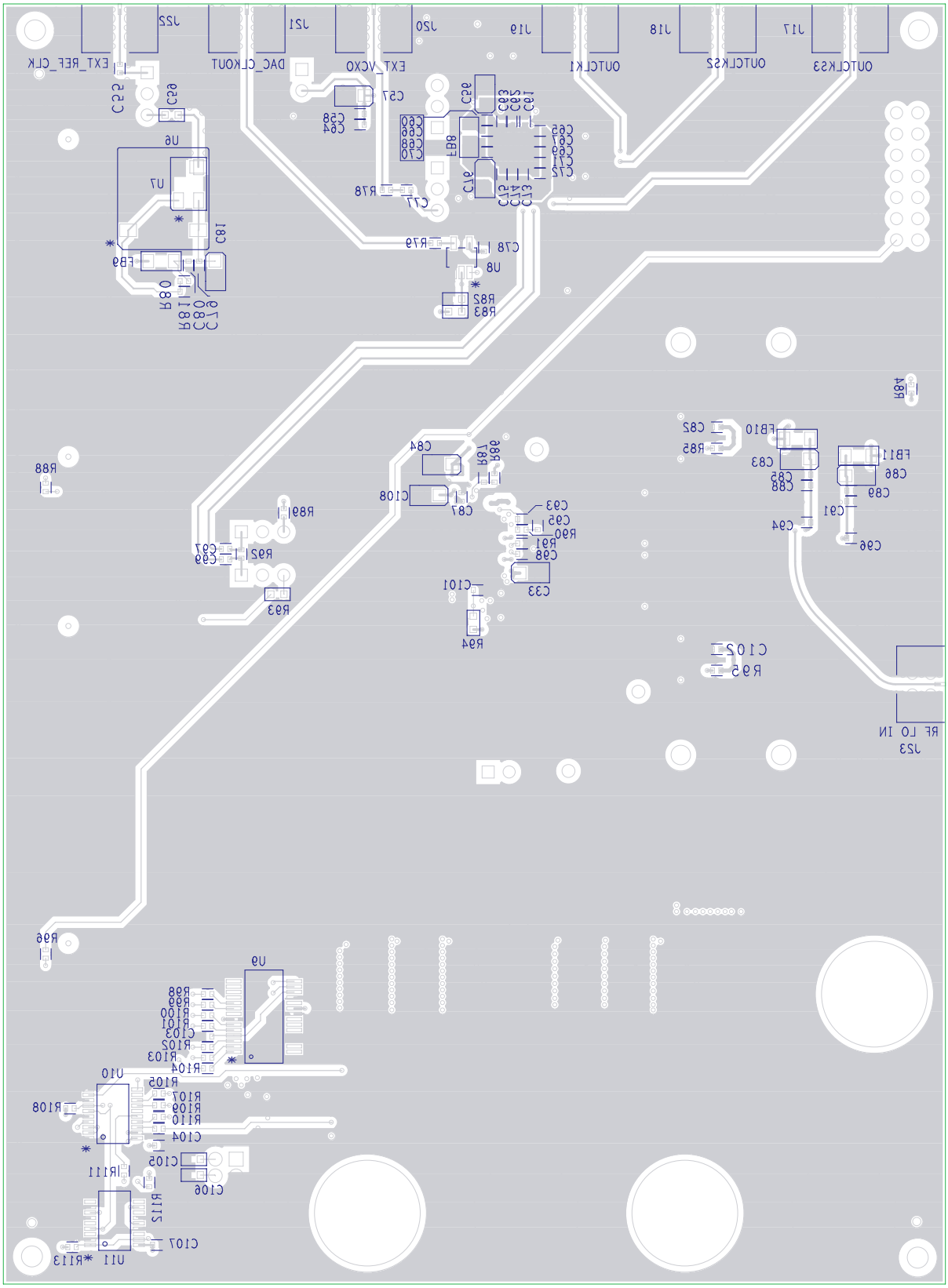
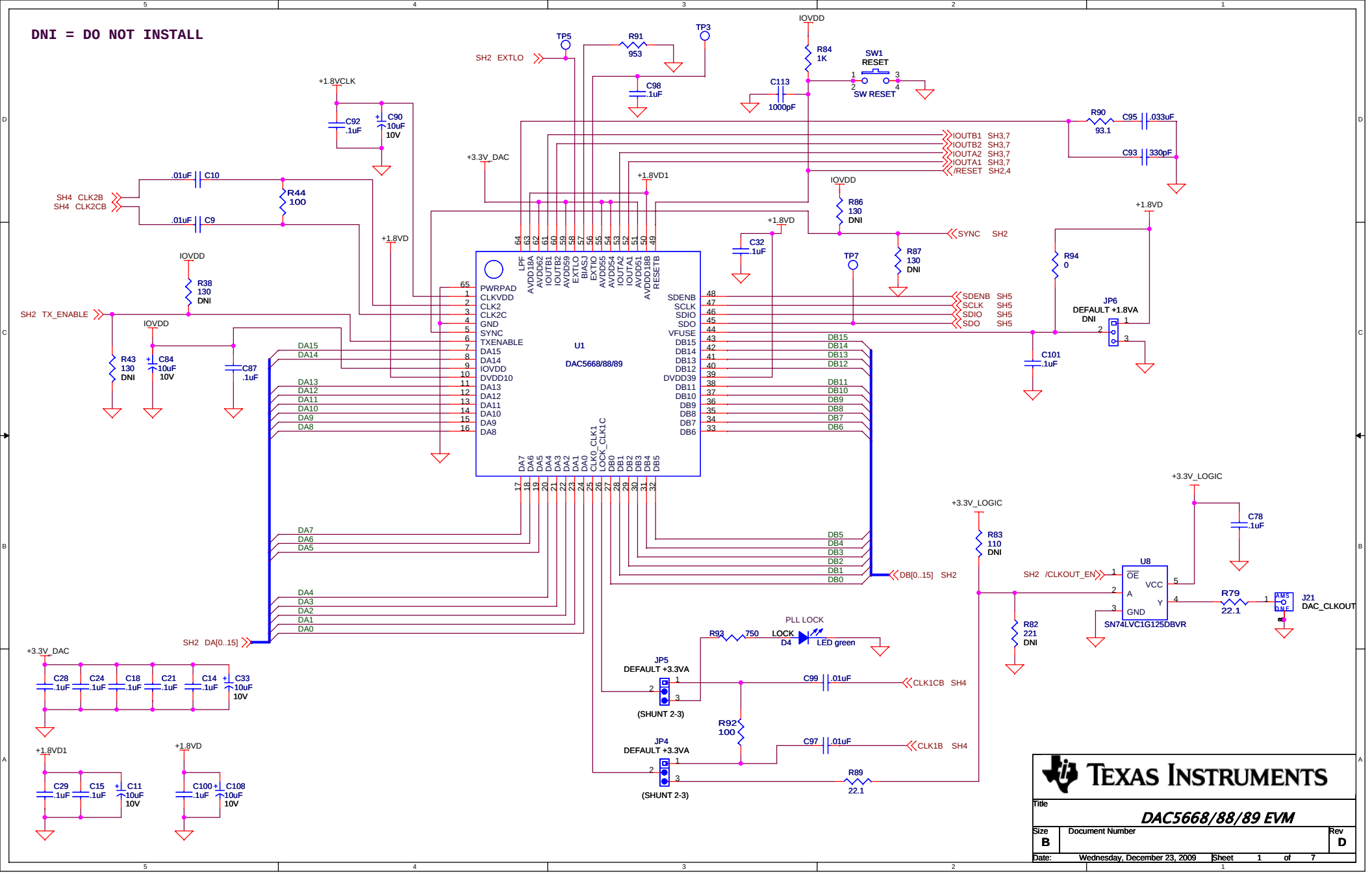
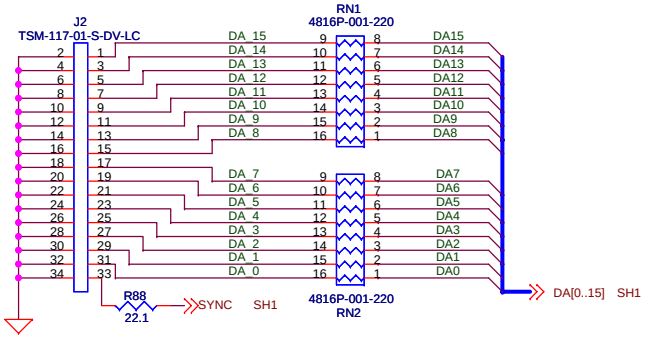


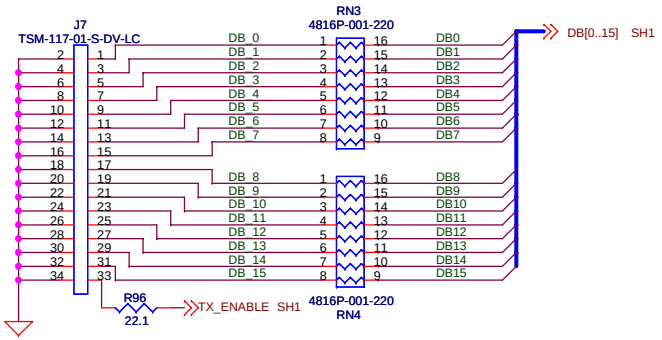
Figure 13. Bottom Silk Screen

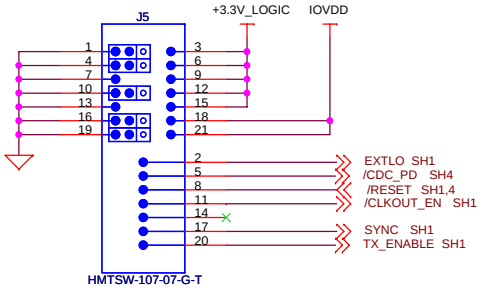
7.3 Schematics

The DAC5668/88/89EVM schematics appear on the following pages.


DNI = DO NOT INSTALL
U1
DAC5668/88/89
PWRPAD
CLKVDD
CLK2
CLK2C
GND
SYNC
TXENABLE
DA15
DA14
IOVDD
DVDD10
DA13
DA12
DA11
DA10
DA9
DA8
LPF
AVDD18A
AVDD62
IOUTB1
IOUTB2
AVDD59
EXTLO
BIASJ
EXTIO
AVDD55
AVDD54
IOUTA2
IOUTA1
AVDD51
AVDD18B
RESETB
SDENB
SCLK
SDIO
SDO
VFUSE
DB15
DB14
DB13
DB12
DVDD39
DB11
DB10
DB9
DB8
DB7
DB6
CLK0_CLK1
LOCK_CLK1C
DB0
DB1
DB2
DB3
DB4
DB5
SH2 EXTLO
SH2 TX_ENABLE
SH2 DA[0..15]
SH4 CLK2B
SH4 CLK2CB
IOUTB1 SH3,7
IOUTB2 SH3,7
IOUTA2 SH3,7
IOUTA1 SH3,7
/RESET SH2,4
SYNC SH2
SDENB SH5
SCLK SH5
SDIO SH5
SDO SH5
DB[0..15] SH2
SH2 /CLKOUT_EN
CLK1CB SH4
CLK1B SH4
PLL LOCK
LOCK D4 LED green
SW1 RESET
SW RESET
JP4 DEFAULT +3.3VA
JP5 DEFAULT +3.3VA
JP6 DEFAULT +1.8VA
DNI
(SHUNT 2-3)
U8
SN74LVC1G125DBVR
OE
A
GND
VCC
Y
J21 DAC_CLKOUT
TP3
TP5
TP7
R84 1K
R91 953
R90 93.1
R94 0
R86 130 DNI
R87 130 DNI
R38 130 DNI
R43 130 DNI
R44 100
R92 100
R93 750
R82 221 DNI
R83 110 DNI
R79 22.1
R89 22.1
C113 1000pF
C98 .1uF
C95 .033uF
C93 330pF
C32 .1uF
C101 .1uF
C78 .1uF
C92 .1uF
C90 10uF 10V
C10 .01uF
C9 .01uF
C84 10uF 10V
C87 .1uF
C28 .1uF
C24 .1uF
C18 .1uF
C21 .1uF
C14 .1uF
C33 10uF 10V
C29 .1uF
C15 .1uF
C11 10uF 10V
C100 .1uF
C108 10uF 10V
C99 .01uF
C97 .01uF
+1.8VCLK
+3.3V_DAC
+1.8VD1
+1.8VD
IOVDD
+3.3V_LOGIC
Title
DAC5668/88/89 EVM
Size B
Document Number
Rev D
Date: Wednesday, December 23, 2009
Sheet 1 of 7







J5 - JUMPER PINS 1 & 2
JUMPER PINS 5 & 6
JUMPER PINS 10 & 11
JUMPER PINS 16 & 17
JUMPER PINS 20 & 21

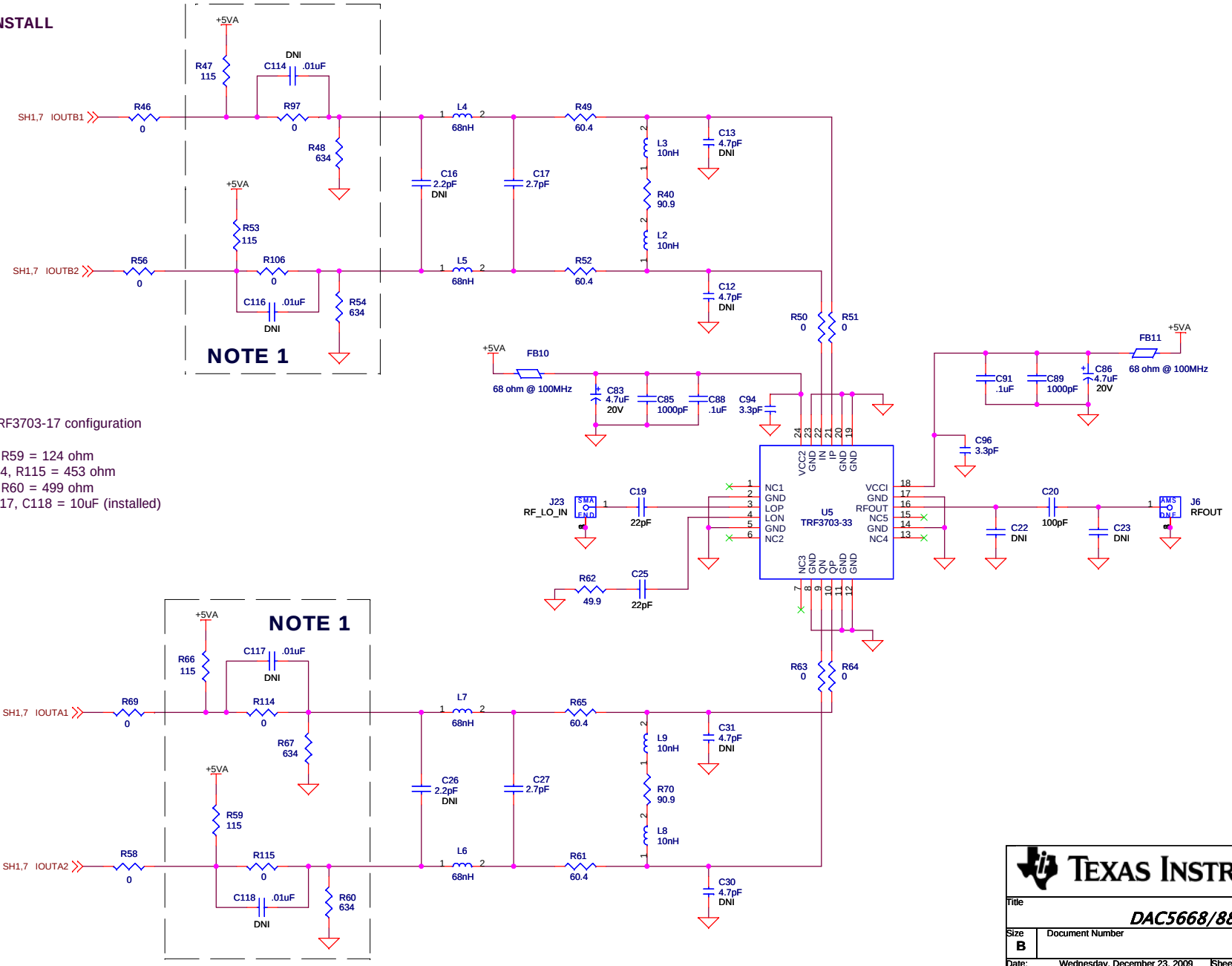
TEXAS INSTRUMENTS

Title: *DAC5668/88/89 EVM*

Size	Document Number	Rev
B		D

Date: Wednesday, December 23, 2009 Sheet 2 of 7

DNI = DO NOT INSTALL



NOTE 1: For TRF3703-17 configuration

R47, R53, R66, R59 = 124 ohm
R97, R106, R114, R115 = 453 ohm
R48, R54, R67, R60 = 499 ohm
C114, C116, C117, C118 = 10uF (installed)

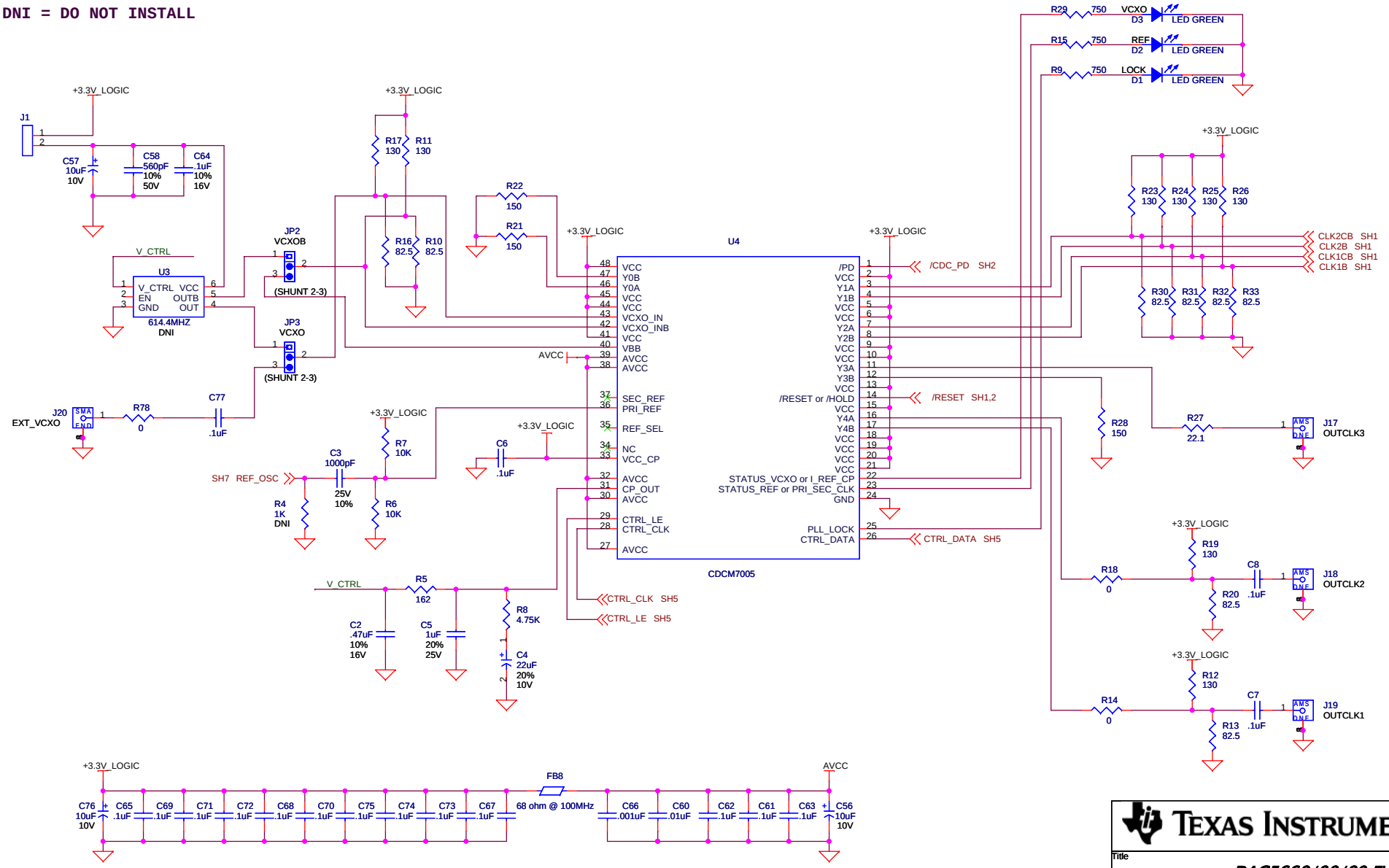
TEXAS INSTRUMENTS

Title: DAC5668/88/89 EVM

Size	Document Number	Rev
B		D

Date: Wednesday, December 23, 2009 Sheet 3 of 7

DNI = DO NOT INSTALL

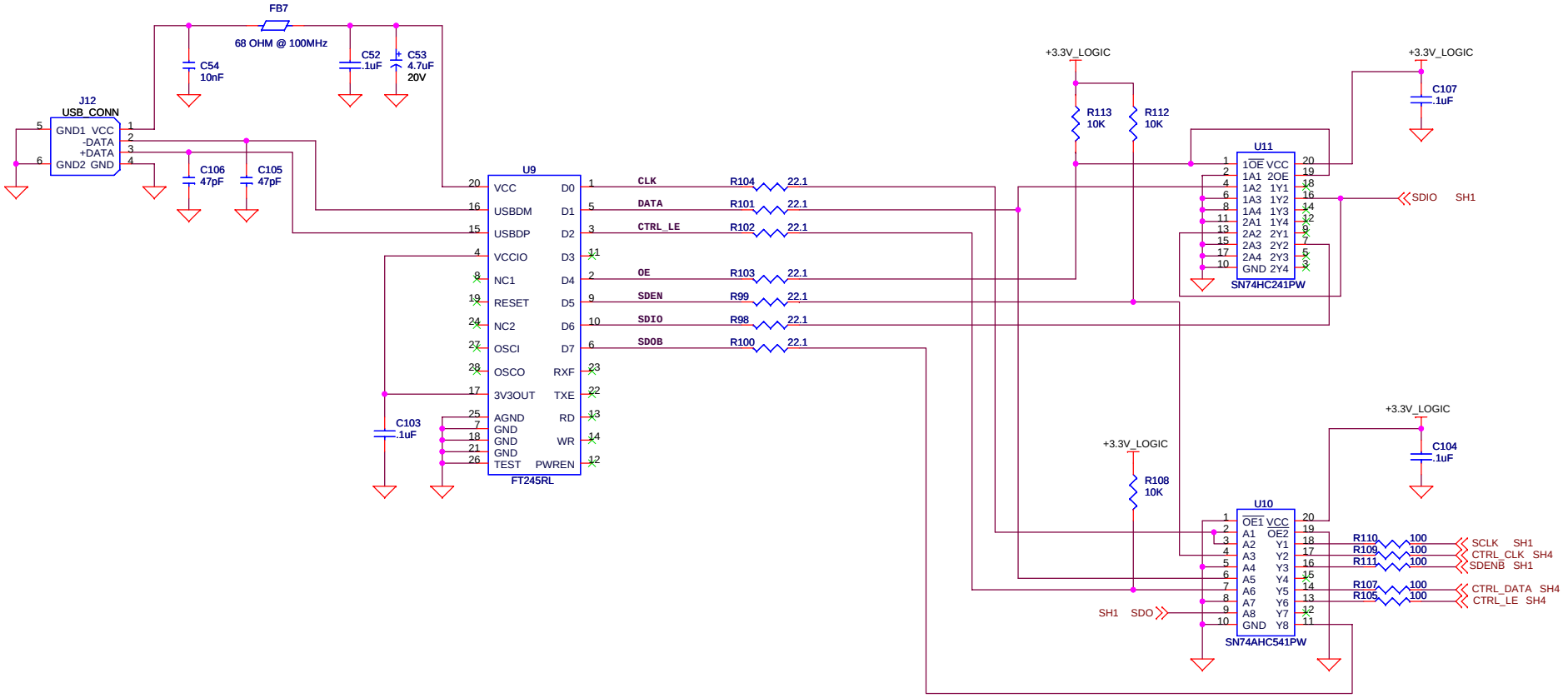


TEXAS INSTRUMENTS

Title: *DAC5668/88/89 EVM*

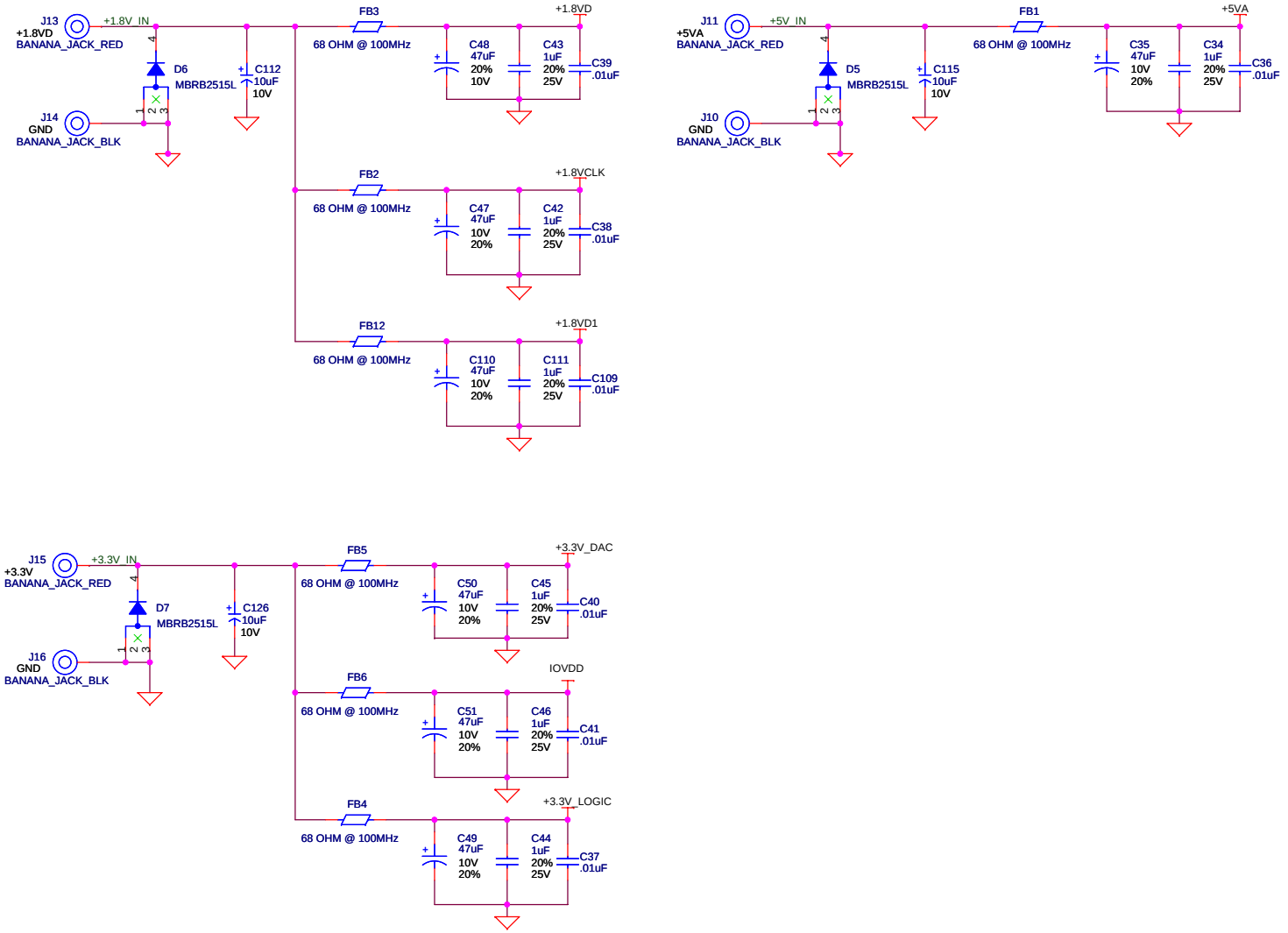
Size	Document Number	Rev
B		D

Date: Wednesday, December 23, 2009 Sheet 4 of 7



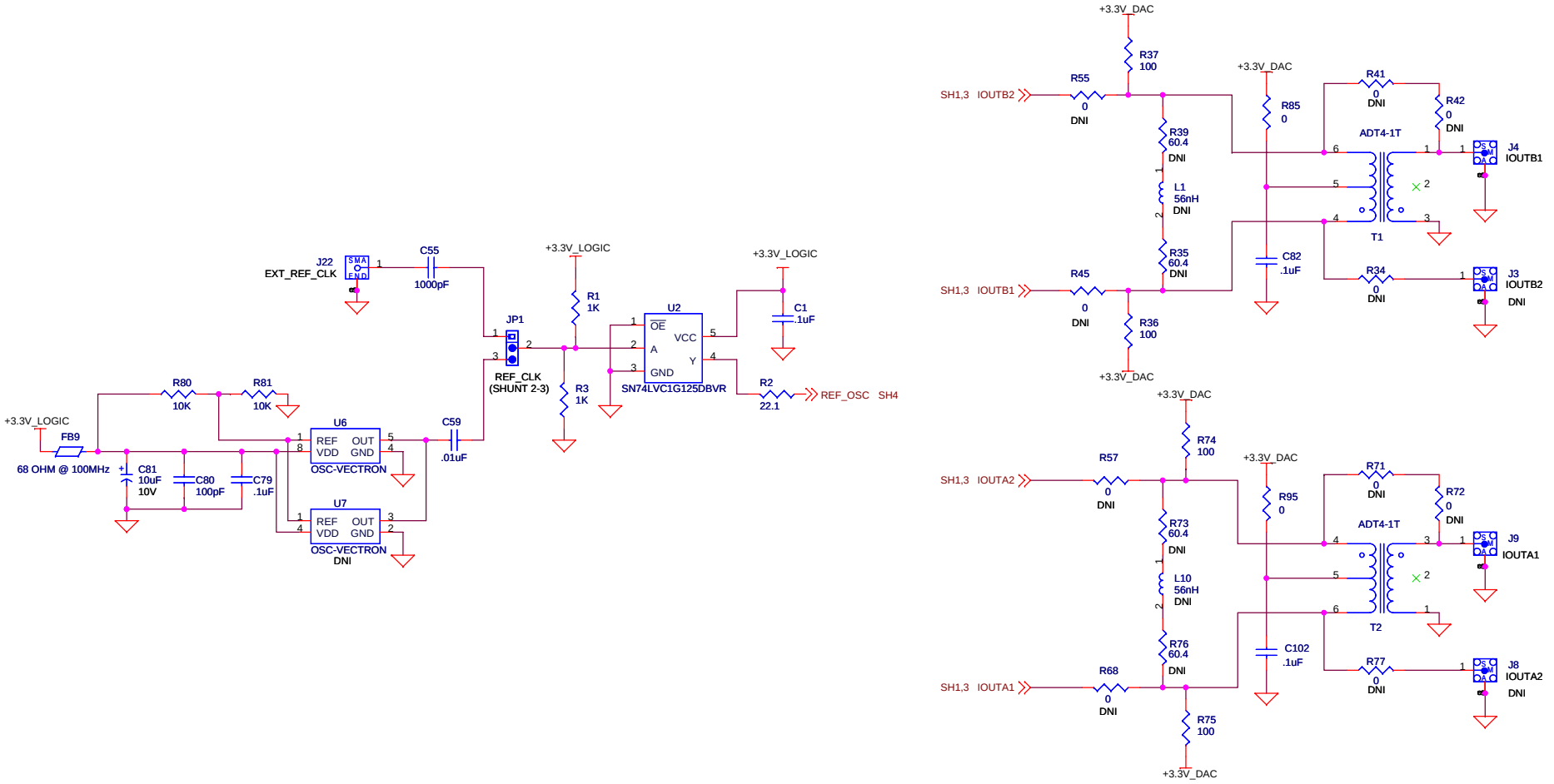
TEXAS INSTRUMENTS

Title	DAC5668/88/89 EVM	
Size B	Document Number	Rev D
Date: Wednesday, December 23, 2009	Sheet 5 of 7	



TEXAS INSTRUMENTS

Title	DAC5668/88/89 EVM	
Size: B	Document Number	Rev: D
Date: Wednesday, December 23, 2009	Sheet 6 of 7	



MECHANICAL PARTS FOR J24

x_SCREW1 SCREW PANHEAD 4-40 x 3/8
x_SCREW2 SCREW PANHEAD 4-40 x 3/8
x_SCREW3 SCREW PANHEAD 4-40 x 3/8
x_SCREW4 SCREW PANHEAD 4-40 x 3/8
x_SCREW5 SCREW PANHEAD 4-40 x 3/8
x_SCREW6 SCREW PANHEAD 4-40 x 3/8
x_STANDOFF1 STANDOFF ALUM HEX 4-40 x .500
x_STANDOFF2 STANDOFF ALUM HEX 4-40 x .500
x_STANDOFF3 STANDOFF ALUM HEX 4-40 x .500
x_STANDOFF4 STANDOFF ALUM HEX 4-40 x .500

TP1 GND Blk
TP8 GND Blk
TP10 GND Blk
TP4 GND Blk
TP2 GND Blk
TP6 GND Blk

TEXAS INSTRUMENTS

Title: DAC5668/88/89 EVM

Size	Document Number	Rev
B		D

Date: Wednesday, December 23, 2009 Sheet 7 of 7

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This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.8 V to 5 V and the output voltage range of 0 V to 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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