CY91460H Series

FR60 32-bit Microcontroller

CY91460H series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family of CPUs.

This series contains the LIN-USART and CAN controllers.

Features

FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)
- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

Internal peripheral resources

- General-purpose ports : Maximum 108 ports
- DMAC (DMA Controller)
  - Maximum of 5 channels able to operate simultaneously
  - 2 transfer sources (internal peripheral/software)
  - Activation source can be selected using software
  - Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  - Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  - Transfer data size selectable from 8/16/32-bit
  - Multi-byte transfer enabled (by software)
  - DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
  - 10-bit resolution: maximum 32 channels
  - Conversion time: minimum 1 µs
- External interrupt inputs : maximum 16 channels
  - 3 channels shared with CAN RX or I^2C pins
- Bit search module (for REALOS)
  - Function to search the first bit position of “1”, “0”, “changed” from the MSB (most significant bit) within one word
- LIN-USART (full duplex double buffer): 4 or 7 channels
  - Clock synchronous/asynchronous selectable
  - Sync-break detection
  - Internal dedicated baud rate generator
- I^2C bus interface (supports 400 kbps): 2 channels
  - Master/slave transmission and reception
  - Arbitration function, clock synchronization function
- CAN controller (C-CAN): 1 channel
  - Maximum transfer speed: 1 Mbps
  - 32 transmission/reception message buffers
- Sound generator : 1 channel
  - Tone frequency : PWM frequency divide-by-two (reload value + 1)
- Alarm comparator : 1 channel
  - Monitor external voltage
  - Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer : maximum 16 channels
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: maximum 8 channels (operates in conjunction with the free-run timer)
- Output compare: maximum 8 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 2 channels (2*8-bit or 1*16-bit)
- Watchdog timer
- Real-time clock
- Low-power consumption modes : Sleep/stop mode function
- Low voltage detection circuit
- Clock supervisor
  - Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
- Clock modulator
- Clock monitor

- Sub-clock calibration
  - Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
- Main oscillator stabilization timer
  - Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
- Sub-oscillator stabilization timer
  - Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

Package and technology

- Package: QFP-144
- CMOS 180 nm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between - 40 °C and + 125 °C

Contents

1. Product Lineup

Feature	CY91FV460B	CY91F464HB	CY91F466HA
Max. core frequency (CLKB)	100 MHz	100 MHz	96 MHz
Max. resource frequency (CLKP)	50 MHz	50 MHz	48 MHz
Max. external bus frequency (CLKT)	50 MHz	50 MHz	48 MHz
Max. CAN frequency (CLKCAN)	50 MHz	50 MHz	48 MHz
Technology	0.18 µm	0.18 µm	0.18 µm
Watchdog	yes	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes	yes
Bit Search	yes	yes	yes
Reset input (INITX)	yes	yes	yes
Clock Modulator	yes	yes	yes
Clock Monitor	yes	yes	yes
Low Power Mode	yes	yes	yes
DMA	5 ch	5 ch	5 ch
MMU/MPU	MPU (16 ch)*1	MPU (8 ch)*1	MPU (8 ch)*1
Flash memory	Internal Flash memory 2112 KB + external emulation SRAM with 64 bit read data	416 KByte	832 KByte
Flash Protection	yes	yes	yes
D-RAM	64 KByte	16 KByte	24 KByte
ID-RAM	64 KByte	16 KByte	16 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	16 KByte Boot Flash + 1 KB Boot ROM	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch
Free Running Timer	12 ch	8 ch*2	8 ch*2
ICU	10 ch	MD_3 = 0: 8 ch MD_3 = 1: 4 ch*3	MD_3 = 0: 8 ch MD_3 = 1: 4 ch*3
OCU	8 ch	MD_3 = 0: 8 ch MD_3 = 1: 4 ch*4	MD_3 = 0: 8 ch MD_3 = 1: 4 ch*4
Reload Timer	16 ch	8 ch*5	8 ch*5
PPG 16-bit	32 ch	MD_3 = 0: 16 ch MD_3 = 1: 8 ch*6	MD_3 = 0: 16 ch MD_3 = 1: 8 ch*6
Sound Generator	1 ch (old) + 1 ch (new)	1 ch (old)	1 ch (old)
Up/Down Counter (8/16 bit)	4 ch (8-bit) / 2 ch (16-bit)	MD_3 = 0: 2 ch (8-bit) / 1 ch (16-bit) MD_3 = 1: NA*7	MD_3 = 0: 2 ch (8-bit) / 1 ch (16-bit) MD_3 = 1: NA*7
C_CAN	6 ch (128 msg)	1 ch (32 msg)	1 ch (32 msg)
LIN-USART	16 ch (FIFO)	MD_3 = 0: 3 ch + 4 ch FIFO*8 MD_3 = 1: 4 ch FIFO	MD_3 = 0: 3 ch + 4 ch FIFO*8 MD_3 = 1: 4 ch FIFO
I^2C (400K)	8 ch	2 ch	2 ch
FR external bus	yes (32 bit addr, 32 bit data)	MD_3 = 0: no MD_3 = 1: yes (22 bit addr, 16 bit data)	MD_3 = 0: no MD_3 = 1: yes (22 bit addr, 16 bit data)

Feature	CY91FV460B	CY91F464HB	CY91F466HA
External Interrupts	32 ch	MD_3 = 0: 16 ch MD_3 = 1: 12 ch*9	MD_3 = 0: 16 ch MD_3 = 1: 12 ch*9
NMI Interrupts	1 ch	1 ch	1 ch
ADC (10-bit)	32 ch + 22 ch	MD_3 = 0: 32 ch MD_3 = 1: 16 ch	MD_3 = 0: 32 ch MD_3 = 1: 16 ch
Alarm Comparator	2 ch	1 ch	1 ch
Supply Supervisor (low voltage detection)	yes	yes	yes
Clock Supervisor	yes	yes	yes
Main clock oscillator	4 MHz	4 MHz	4 MHz
Sub clock oscillator	32 kHz	32 kHz	32 kHz
RC oscillator	100 kHz / 2 MHz	100 kHz / 2 MHz	100 kHz / 2 MHz
PLL	x 25	x 25	x 25
DSU4	yes	no	no
EDSU	yes (32 BP)*1	yes (16 BP)*1	yes (16 BP)*1
Supply voltage	1.8 V + 3 V/5 V	3 V/5 V	3 V/5 V
Regulator	no	yes	yes
Power consumption	1.5 W	< 1.3 W	< 1.3 W
Temperature Range (Ta)	0..70 C	-40..125 C	-40..125 C
Package	BGA-896	QFP-144	QFP-144
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	< 8 sec. typical	< 5 sec. typical	< 5 sec. typical

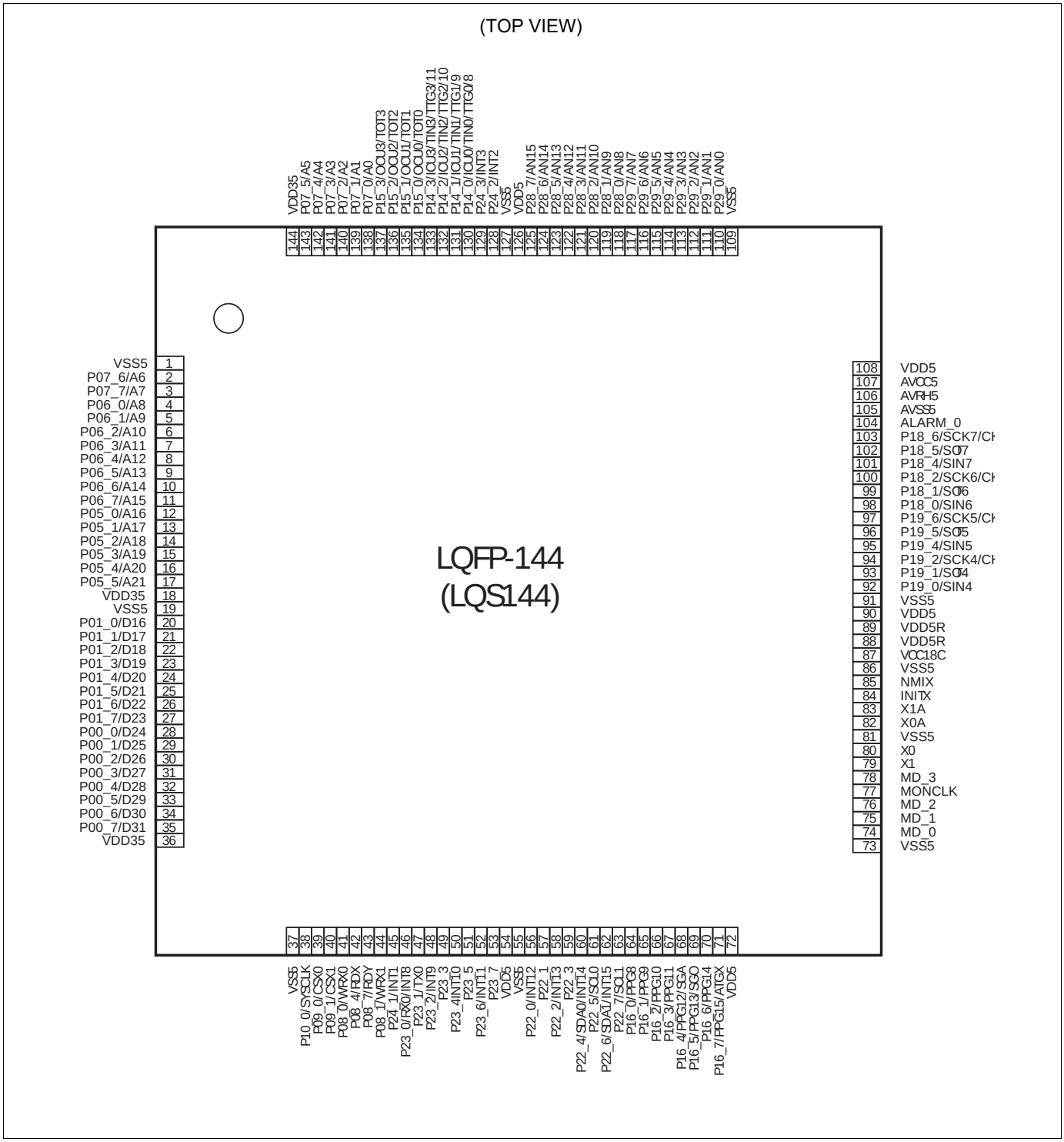
*1. MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

*2. Free Running Timer: MD3 = 0: CH 1 and 0 cannot select external clock (bit7 of TCCS1,0)
MD3 = 1: CH 3, 2, 1, and 0 cannot select external clock (bit7 of TCCS3,2,1,0)

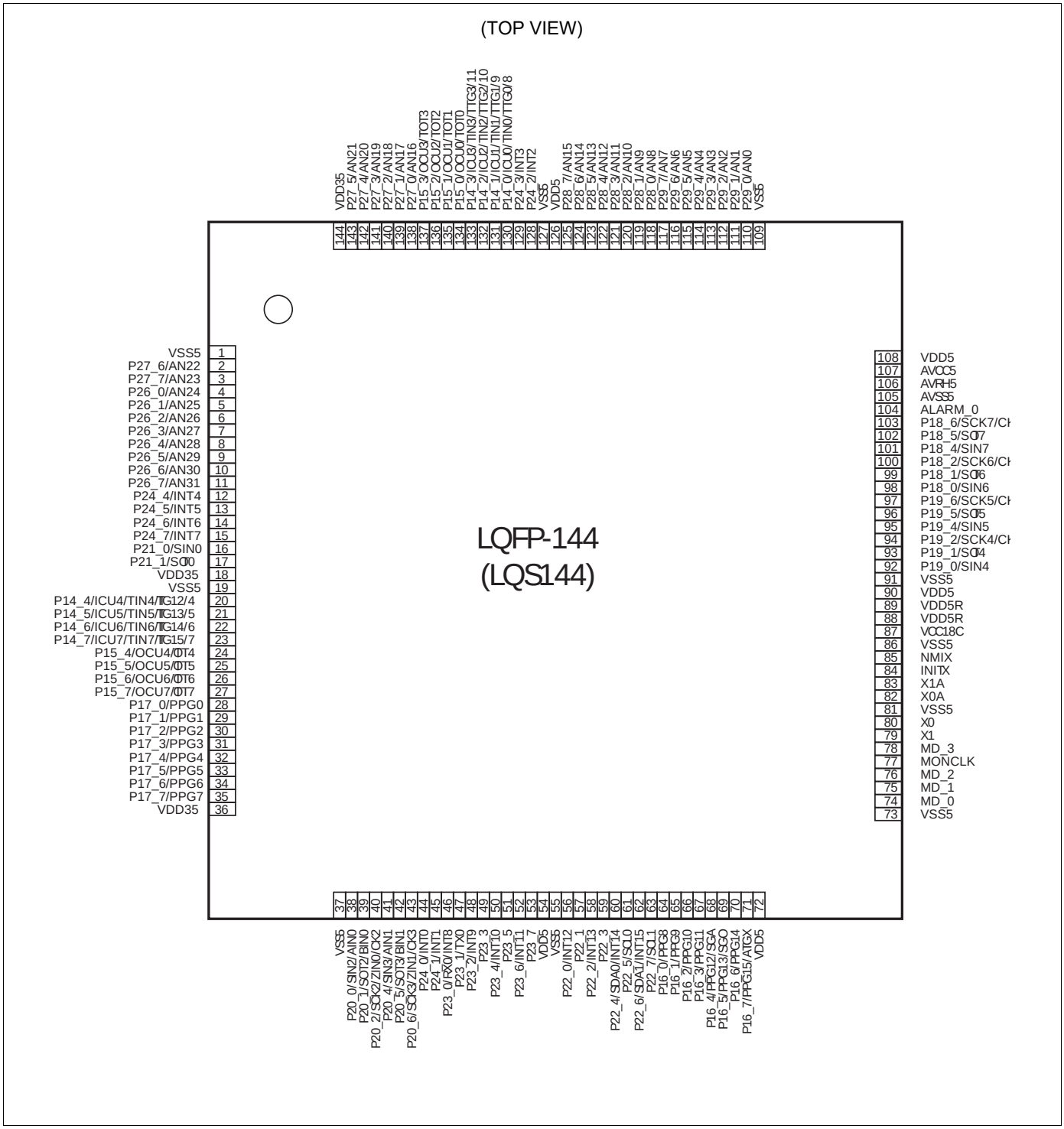
*3. ICU: MD3 = 1: Do not set PFR = 1 & EPFR = 1 (for LIN Synch Field detect).
*4. OCU: MD3 = 1: You cannot use external out-port (but, OCU-function is active.)
*5. Reload Timer: MD3 = 1: CH 7, 6, 5, and 4 cannot select external event
*6. PPG: MD3 = 1: You can use CH15 to 8 of PPG. CH15 to12 cannot select external trigger.
*7. Up/Down Counter: MD3 = 1: You can use Timer-mode only.
*8. LIN-USART CH 0 (shared with external bus) can be used for asynchronous mode only.
*9. External Interrupts: INT7 to INT4 (shared with external bus) can be used for MD3 = 0 mode only. INT0 (shared with external bus) can be used for MD3 = 0 mode only.

2. Pin Assignment

2.1 CY91F464HB, CY91F466HA with MD_3 = 1



2.2 CY91F464HB, CY91F466HA with MD_3 = 0



3. Pin Description

3.1 CY91F464HB, CY91F466HA with MD_3 = 1

Pin no.	Pin name	I/O	I/O circuit type*	Function
2, 3	P07_6, P07_7	I/O	B	General-purpose input/output port
	A6, A7			Signal pins of external address bus (bit6 to bit7)
4 to 11	P06_0 to P06_7	I/O	B	General-purpose input/output port
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
12 to 17	P05_0 to P05_5	I/O	A	General-purpose input/output port
	A16 to A21			Signal pins of external address bus (bit16 to bit21)
20 to 27	P01_0 to P01_7	I/O	A	General-purpose input/output port
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
28 to 35	P00_0 to P00_7	I/O	A	General-purpose input/output port
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
38	P10_0	I/O	A	General-purpose input/output port
	SYSCLK			External bus clock output pin
39	P09_0	I/O	A	General-purpose input/output port
	CSX0			Chip select output pins
40	P09_1	I/O	A	General-purpose input/output port
	CSX1			Chip select output pins
41	P08_0	I/O	A	General-purpose input/output port
	WRX0			External write strobe output pins
42	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
43	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
44	P08_1	I/O	A	General-purpose input/output port
	WRX1			External write strobe output pins
	INT0			External interrupt input, can only be used in general-purpose IO port mode
45	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pins
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0
48	P23_2	I/O	A	General-purpose input/output port
	INT9			External interrupt input pins
49	P23_3	I/O	A	General-purpose input/output port

Pin no.	Pin name	I/O	I/O circuit type*	Function
50	P23_4	I/O	A	General-purpose input/output port
	INT10			External interrupt input pin
51	P23_5	I/O	A	General-purpose input/output port
52	P23_6	I/O	A	General-purpose input/output port
	INT11			External interrupt input pin
53	P23_7	I/O	A	General-purpose input/output port
56	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
57	P22_1	I/O	A	General-purpose input/output port
58	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
59	P22_3	I/O	A	General-purpose input/output port
60	P22_4	I/O	C	General-purpose input/output port
	SDA0			I^2C bus DATA input/output pin (open drain)
	INT14			External interrupt input pin
61	P22_5	I/O	C	General-purpose input/output port
	SCL0			I^2C bus clock input/output pin (open drain)
62	P22_6	I/O	C	General-purpose input/output port
	SDA1			I^2C bus DATA input/output pin (open drain)
	INT15			External interrupt input pin
63	P22_7	I/O	C	General-purpose input/output port
	SCL1			I^2C bus clock input/output pin (open drain)
64	P16_0	I/O	A	General-purpose input/output port
	PPG8			Output pins of PPG timer
65	P16_1	I/O	A	General-purpose input/output port
	PPG9			Output pins of PPG timer
66	P16_2	I/O	A	General-purpose input/output port
	PPG10			Output pins of PPG timer
67	P16_3	I/O	A	General-purpose input/output port
	PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output port
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
69	P16_5	I/O	A	General-purpose input/output port
	PPG13			Output pins of PPG timer
	SGO			SGO output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output port
	PPG14			Output pins of PPG timer

Pin no.	Pin name	I/O	I/O circuit type*	Function
71	P16_7	I/O	A	General-purpose input/output port
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pin
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
95	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5
97	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
99	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6
100	P18_2	I/O	A	General-purpose input/output port
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output port
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output port
	SOT7			Data output pin of USART7

Pin no.	Pin name	I/O	I/O circuit type*	Function
103	P18_6	I/O	A	General-purpose input/output port
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	I	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output port
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output port
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output port
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output port
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output port
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output port
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P07_0 to P07_5	I/O	B	General-purpose input/output port
	A0 to A5			Signal pins of external address bus (bit0 to bit5)

[Power supply/Ground pins]

Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

3.2 CY91F464HB, CY91F466HA with MD_3 = 0

Pin no.	Pin name	I/O	I/O circuit type*	Function
2 to 3	P27_6 to P27_7	I/O	B	General-purpose input/output ports
	AN22 to AN23			Analog input pins of A/D converter
4 to 11	P26_0 to P26_7	I/O	B	General-purpose input/output ports
	AN24 to AN31			Analog input pins of A/D converter
12 to 15	P24_4 to P24_7	I/O	A	General-purpose input/output ports
	INT4 to INT7			External interrupt input pins
16	P21_0	I/O	A	General-purpose input/output ports
	SIN0			Data input pin of USART0
17	P21_1	I/O	A	General-purpose input/output ports
	SOT0			Data output pin of USART0
20 to 23	P14_4 to P14_7	I/O	A	General-purpose input/output ports
	ICU4 to ICU7			Input capture input pins
	TIN4 to TIN7			External trigger input pins of reload timer
	TTG4/12 to TTG7/15			External trigger input pins of PPG timer
24 to 27	P15_4 to P15_7	I/O	A	General-purpose input/output ports
	OCU4 to OCU7			Output compare output pins
	TOT4 to TOT7			Reload timer output pins
28 to 35	P17_0 to P17_7	I/O	A	General-purpose input/output ports
	PPG0 to PPG7			Output pins of PPG timer
38	P20_0	I/O	A	General-purpose input/output ports
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
39	P20_1	I/O	A	General-purpose input/output ports
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
40	P20_2	I/O	A	General-purpose input/output ports
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
41	P20_4	I/O	A	General-purpose input/output ports
	SIN3			Data input pin of USART3
	AIN1			Up/down counter input pin
42	P20_5	I/O	A	General-purpose input/output ports
	SOT3			Data output pin of USART3
	BIN1			Up/down counter input pin

Pin no.	Pin name	I/O	I/O circuit type*	Function
43	P20_6	I/O	A	General-purpose input/output ports
	SCK3			Clock input/output pin of USART3
	ZIN1			Up/down counter input pin
	CK3			External clock input pin of free-run timer 3
44	P24_0	I/O	A	General-purpose input/output ports
	INT0			External interrupt input pin
45	P24_1	I/O	A	General-purpose input/output ports
	INT1			External interrupt input pin
46	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input pin of CAN0
	INT8			External interrupt input pins
47	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0
48	P23_2	I/O	A	General-purpose input/output port
	INT9			External interrupt input pins
49	P23_3	I/O	A	General-purpose input/output port
50	P23_4	I/O	A	General-purpose input/output port
	INT10			External interrupt input pin
51	P23_5	I/O	A	General-purpose input/output port
52	P23_6	I/O	A	General-purpose input/output port
	INT11			External interrupt input pin
53	P23_7	I/O	A	General-purpose input/output port
56	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
57	P22_1	I/O	A	General-purpose input/output port
58	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
59	P22_3	I/O	A	General-purpose input/output port
60	P22_4	I/O	C	General-purpose input/output ports
	SDA0			I^2C bus DATA input/output pin (open drain)
	INT14			External interrupt input pin
61	P22_5	I/O	C	General-purpose input/output ports
	SCL0			I^2C bus clock input/output pin (open drain)
62	P22_6	I/O	C	General-purpose input/output ports
	SDA1			I^2C bus DATA input/output pin (open drain)
	INT15			External interrupt input pin
63	P22_7	I/O	C	General-purpose input/output ports
	SCL1			I^2C bus clock input/output pin (open drain)

Pin no.	Pin name	I/O	I/O circuit type*	Function
64 to 67	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			Output pins of PPG timer
68	P16_4	I/O	A	General-purpose input/output ports
	PPG12			Output pins of PPG timer
	SGA			SGA output pin of sound generator
69	P16_5	I/O	A	General-purpose input/output ports
	PPG13			Output pins of PPG timer
	SGO			SGO output pin of sound generator
70	P16_6	I/O	A	General-purpose input/output ports
	PPG14			Output pins of PPG timer
71	P16_7	I/O	A	General-purpose input/output ports
	PPG15			Output pins of PPG timer
	ATGX			A/D converter external trigger input pin
74 to 76	MD_0 to MD_2	I	G	Mode setting pins
77	MONCLK	O	M	Clock monitor pin
78	MD_3	I	H	Mode setting pins
79	X1	—	J1	Clock (oscillation) output
80	X0	—	J1	Clock (oscillation) input
82	X0A	—	J2	Sub clock (oscillation) input
83	X1A	—	J2	Sub clock (oscillation) output
84	INITX	I	H	External reset input pin
85	NMIX	I	H	Non-maskable interrupt input pin
92	P19_0	I/O	A	General-purpose input/output ports
	SIN4			Data input pin of USART4
93	P19_1	I/O	A	General-purpose input/output ports
	SOT4			Data output pin of USART4
94	P19_2	I/O	A	General-purpose input/output ports
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
95	P19_4	I/O	A	General-purpose input/output ports
	SIN5			Data input pin of USART5
96	P19_5	I/O	A	General-purpose input/output ports
	SOT5			Data output pin of USART5
97	P19_6	I/O	A	General-purpose input/output ports
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
98	P18_0	I/O	A	General-purpose input/output ports
	SIN6			Data input pin of USART6

Pin no.	Pin name	I/O	I/O circuit type*	Function
99	P18_1	I/O	A	General-purpose input/output ports
	SOT6			Data output pin of USART6
100	P18_2	I/O	A	General-purpose input/output ports
	SCK6			Clock input/output pin of USART6
	CK6			External clock input pin of free-run timer 6
101	P18_4	I/O	A	General-purpose input/output ports
	SIN7			Data input pin of USART7
102	P18_5	I/O	A	General-purpose input/output ports
	SOT7			Data output pin of USART7
103	P18_6	I/O	A	General-purpose input/output ports
	SCK7			Clock input/output pin of USART7
	CK7			External clock input pin of free-run timer 7
104	ALARM_0	I	N	Alarm comparator input pin
110 to 117	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
118 to 125	P28_0 to P28_7	I/O	B	General-purpose input/output ports
	AN8 to AN15			Analog input pins of A/D converter
128	P24_2	I/O	A	General-purpose input/output ports
	INT2			External interrupt input pin
129	P24_3	I/O	A	General-purpose input/output ports
	INT3			External interrupt input pin
130 to 133	P14_0 to P14_3	I/O	A	General-purpose input/output ports
	ICU0 to ICU3			Input capture input pins
	TIN0 to TIN3			External trigger input pins of reload timer
	TTG0/8 to TTG3/11			External trigger input pins of PPG timer
134 to 137	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
138 to 143	P27_0 to P27_5	I/O	B	General-purpose input/output ports
	AN16 to AN21			Analog input pins of A/D converter

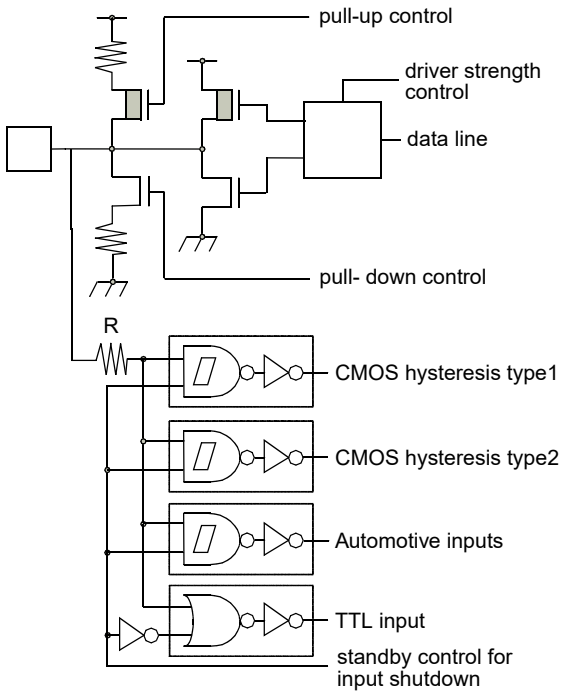
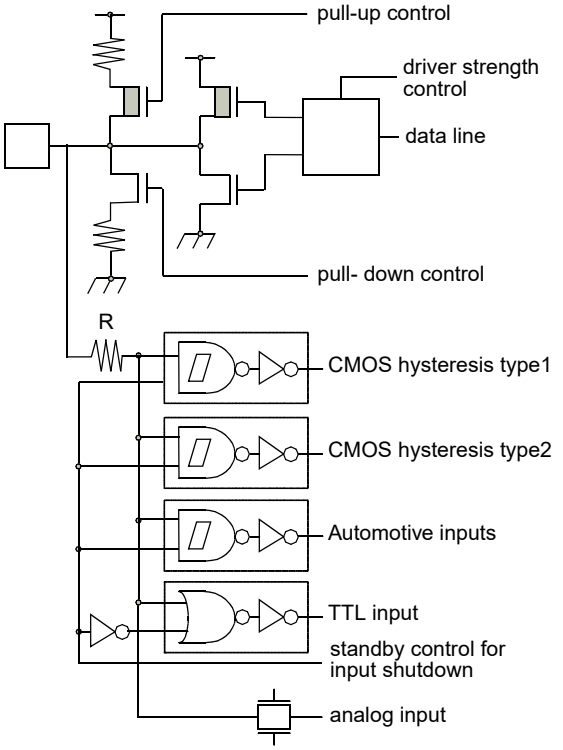
*: For information about the I/O circuit type, refer to 4.“I/O Circuit Types”.

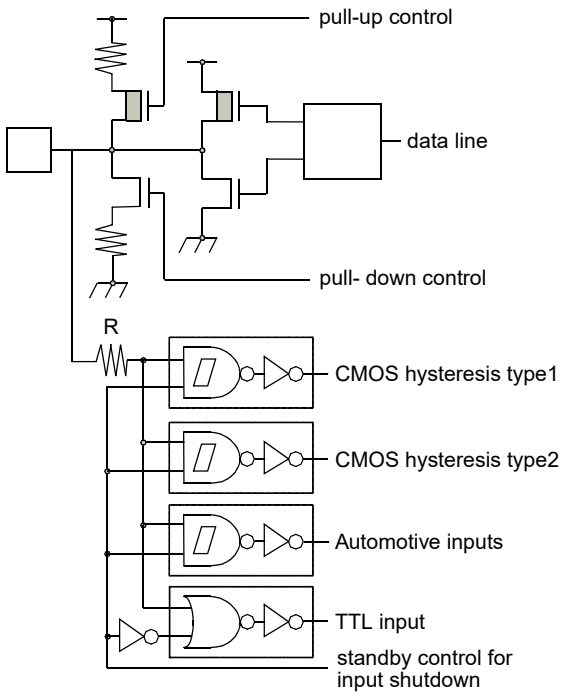
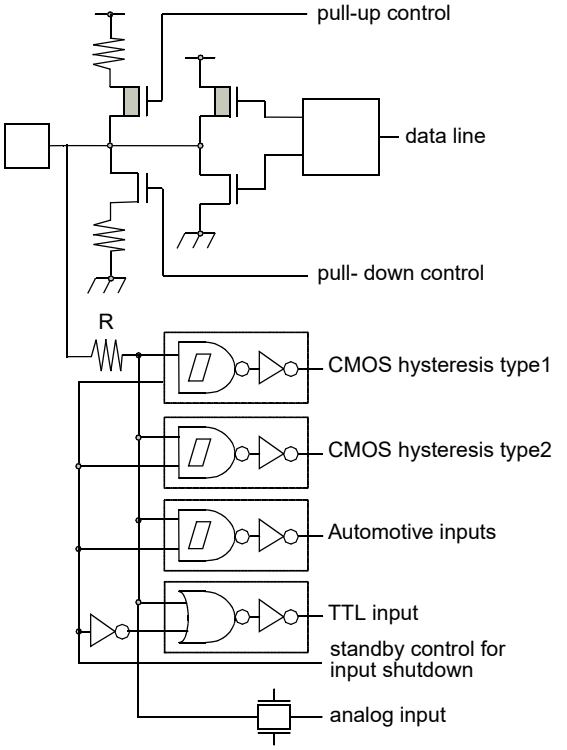
[Power supply/Ground pins]

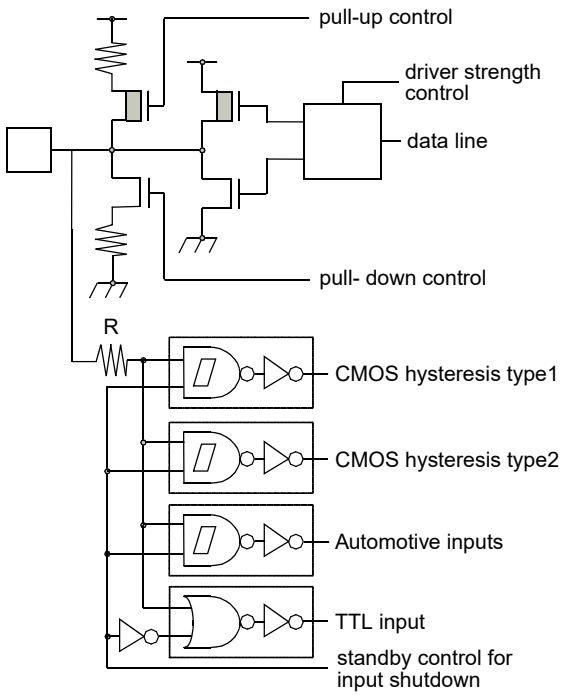
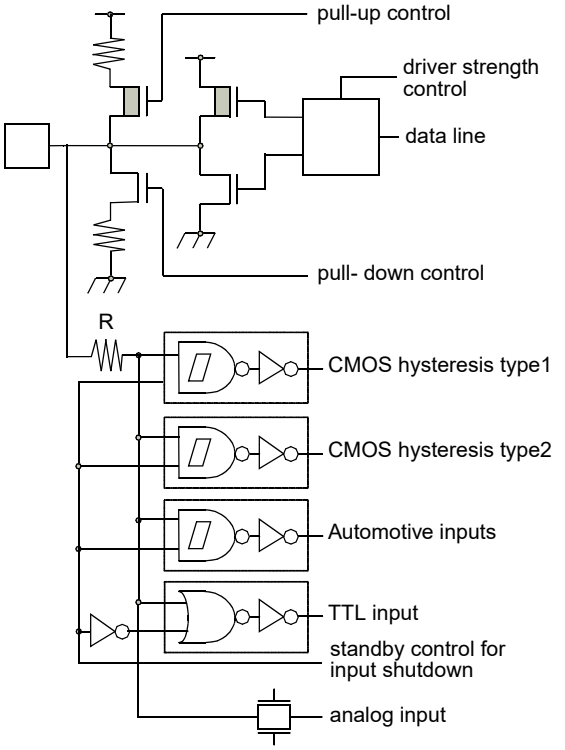
Pin no.	Pin name	I/O	Function
1, 19, 37, 55, 73, 81, 86, 91, 109, 127	VSS5	Supply	Ground pins
54, 72, 90, 108, 126	VDD5		Power supply pins
88, 89	VDD5R		Power supply pins for internal regulator
105	AVSS5		Analog ground pin for A/D converter
107	AVCC5		Power supply pin for A/D converter
106	AVRH5		Reference power supply pin for A/D converter
87	VCC18C		Capacitor connection pin for internal regulator
18, 36, 144	VDD35		Power supply pins for external bus part of I/O ring

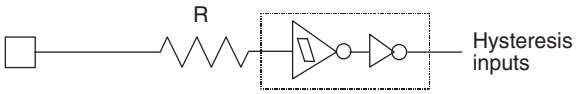
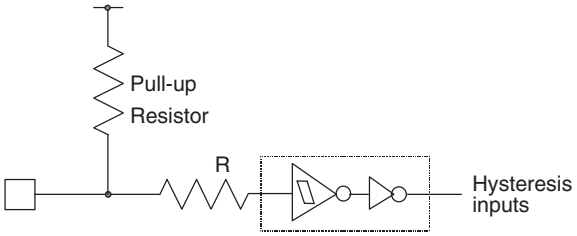
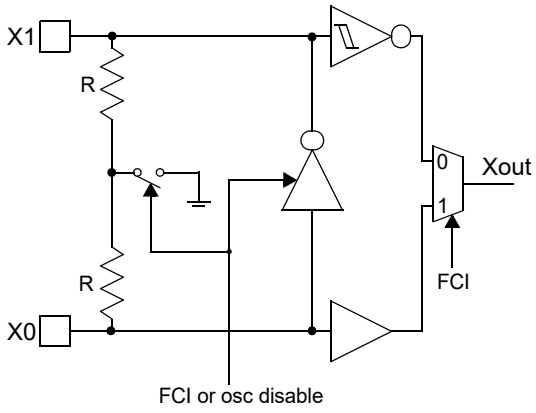
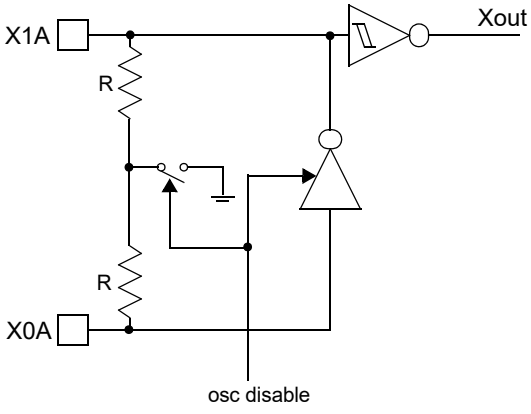
*: For information about the I/O circuit type, refer to 4.“I/O Circuit Types”.

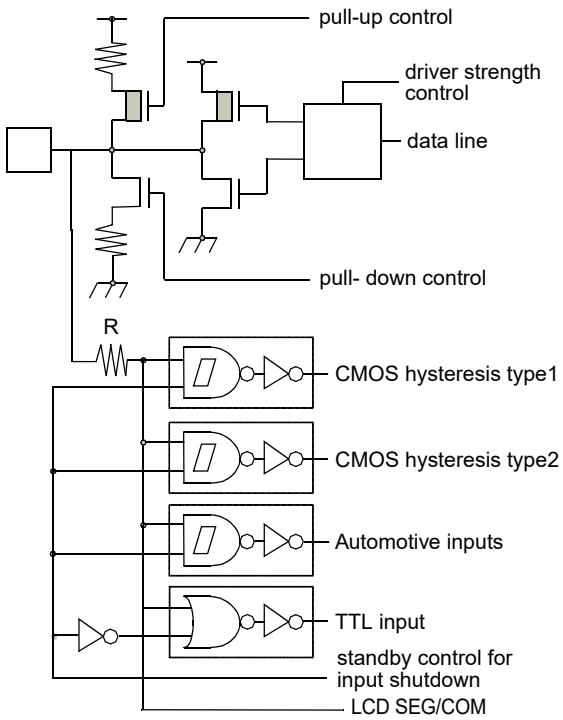
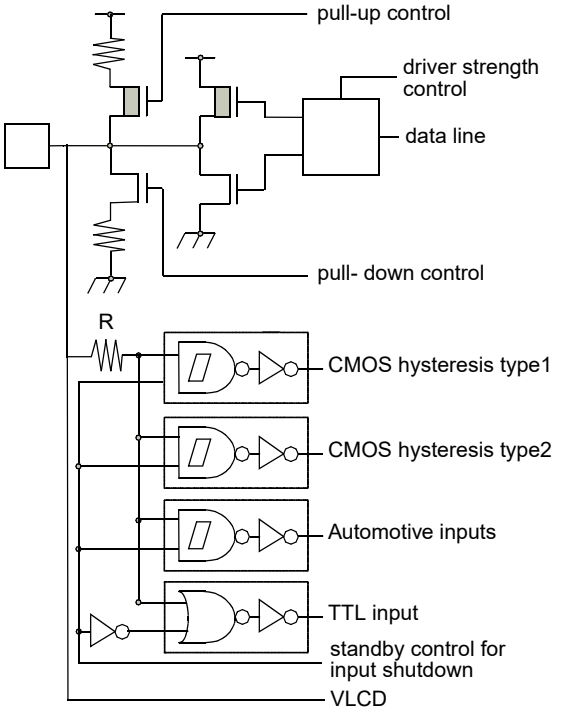
4. I/O Circuit Types

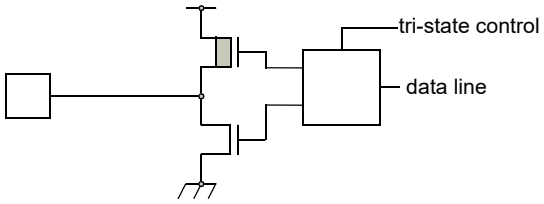
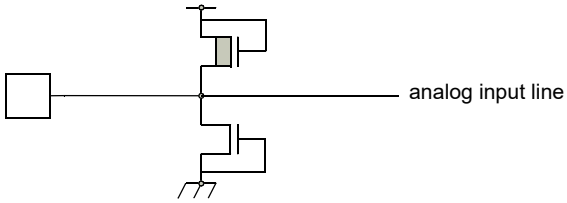
Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx.
B		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. Analog input

Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3 mA, I_{OH} = -3 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx.
D		CMOS level output (I_{OL} = 3 mA, I_{OH} = -3 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. Analog input

Type	Circuit	Remarks
E		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA, and I_{OL} = 30 mA, I_{OH} = -30 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx.
F		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA, and I_{OL} = 30 mA, I_{OH} = -30 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. Analog input

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: • Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. LCD SEG/COM output
L		CMOS level output (programmable I_{OL} = 5 mA, I_{OH} = -5 mA and I_{OL} = 2 mA, I_{OH} = -2 mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50 kΩ approx. Analog input LCD Voltage input

Type	Circuit	Remarks
M		CMOS level tri-state output (I_{OL} = 5 mA, I_{OH} = -5 mA)
N		Analog input pin with protection

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$ *1) or less than ($V_{SS}5$ or $HV_{SS}5$ *1) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

Note *1: $HV_{DD}5$, $HV_{SS}5$ are available only on devices having Stepper Motor Controller.

5.2 Handling of Unused Input Pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2 kΩ to 10 kΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

5.3 Power Supply Pins

In CY91460 series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the CY91460 series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 µF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

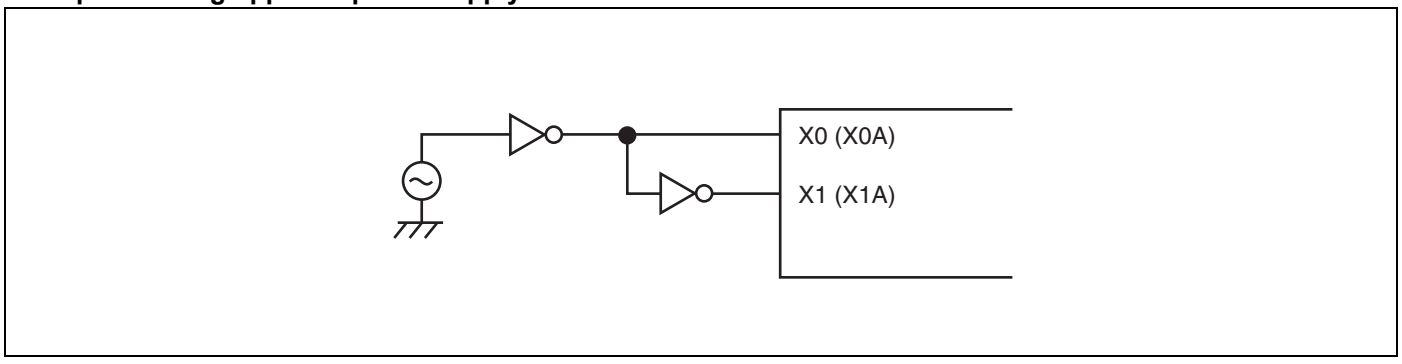
5.4 Crystal Oscillator Circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5.5 Notes on Using External Clock

When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

Example of using opposite phase supply



5.6 Mode Pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

5.7 Notes on Operating in PLL Clock Mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

5.8 Pull-up Control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

6. Notes on Debugger

6.1 Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

6.2 Break Function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

6.3 Operand Break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

6.4 Notes on PS Register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event,
the operation before and after the EIT always proceeds according to specification.

The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:

(a) a user interrupt or NMI is accepted;
(b) single-step execution is performed;
(c) execution breaks due to a data event or from the emulator menu.

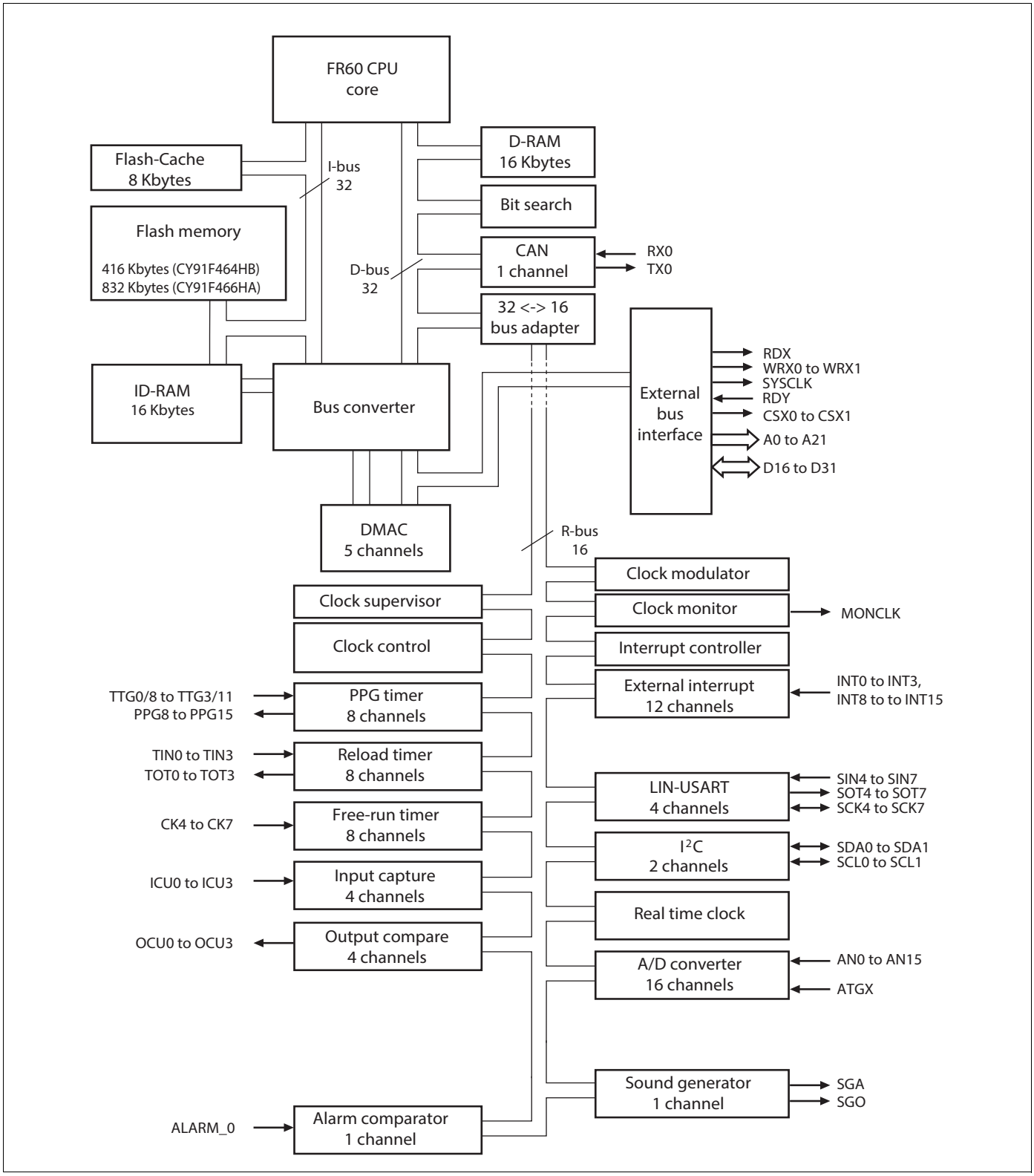
1. D0 and D1 flags are updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1.

The following behavior occurs when an ORCCR, STILM, MOV Ri,PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.

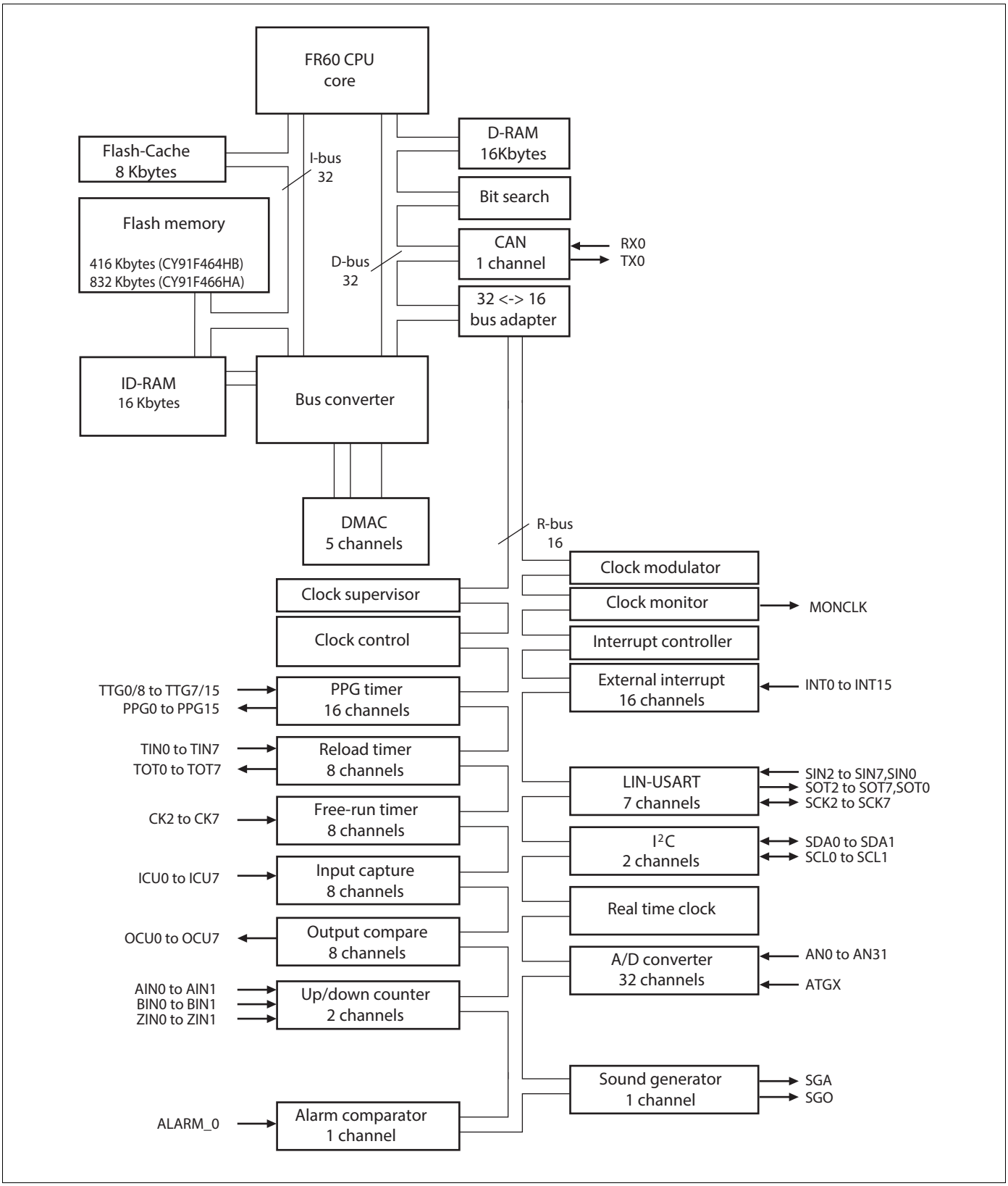
1. The PS register is updated in advance.
2. An EIT handling routine (user interrupt/NMI or emulator) is executed.
3. Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1.

7. Block Diagram

7.1 CY91F464HB, CY91F466HA with MD_3 = 1



7.2 CY91F464HB, CY91F466HA with MD_3 = 0



8. CPU and Control Unit

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

8.1 Features

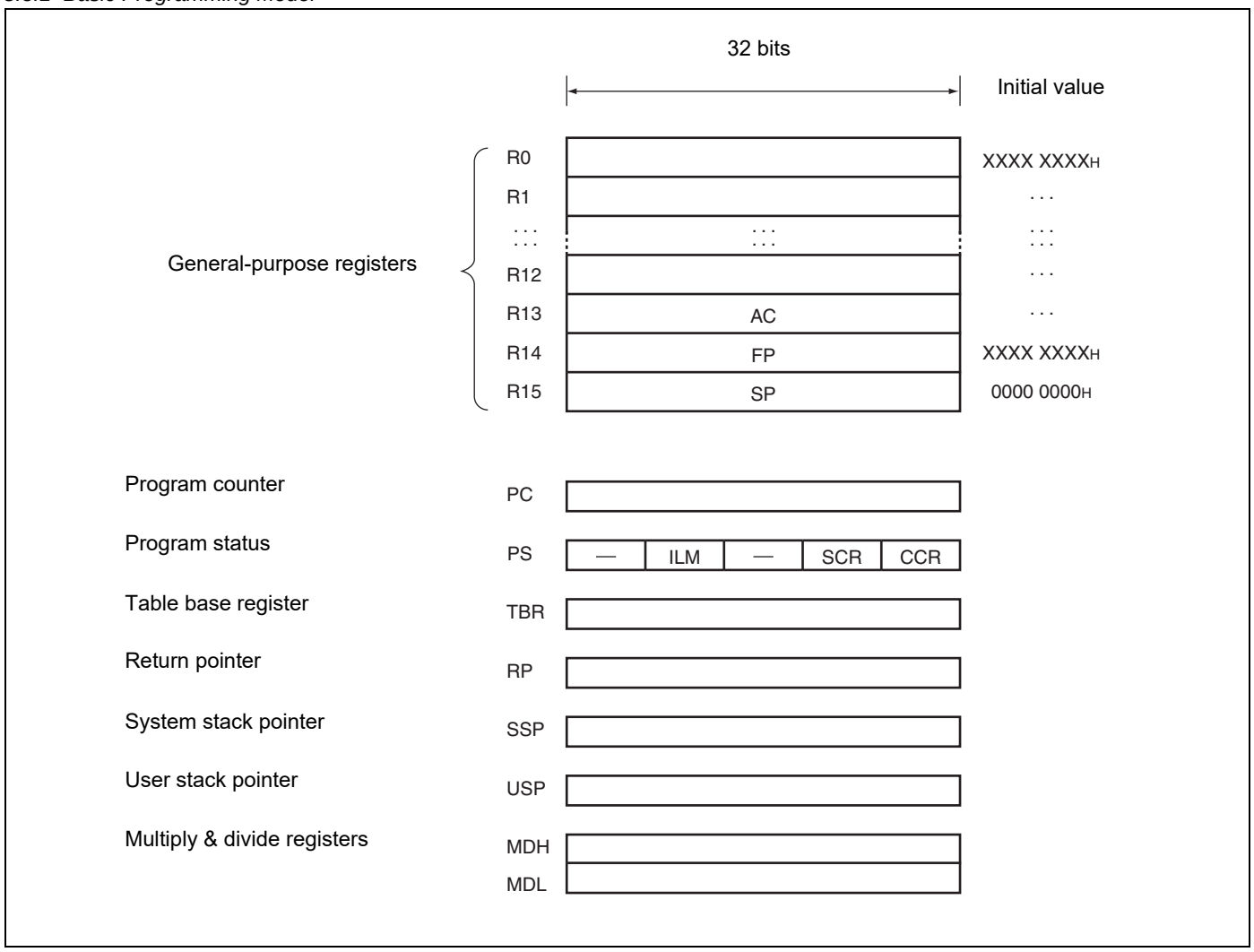
- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit × 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit × 32-bit multiplication: 5 cycles
  16-bit × 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

8.2 Internal Architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

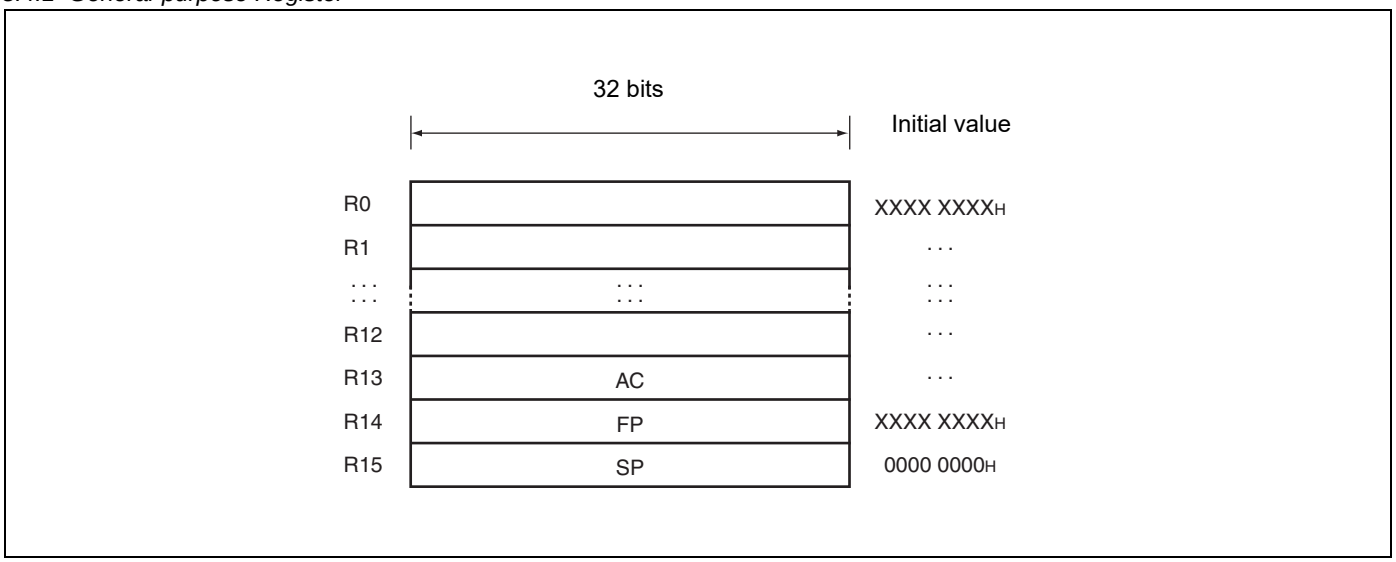
8.3 Programming Model

8.3.1 Basic Programming Model



8.4 Registers

8.4.1 General-purpose Register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13: Virtual accumulator

R14: Frame pointer

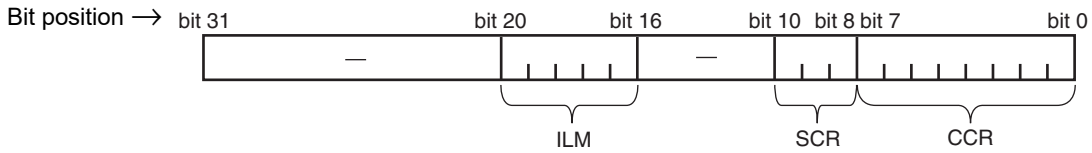
R15: Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000_H (SSP value).

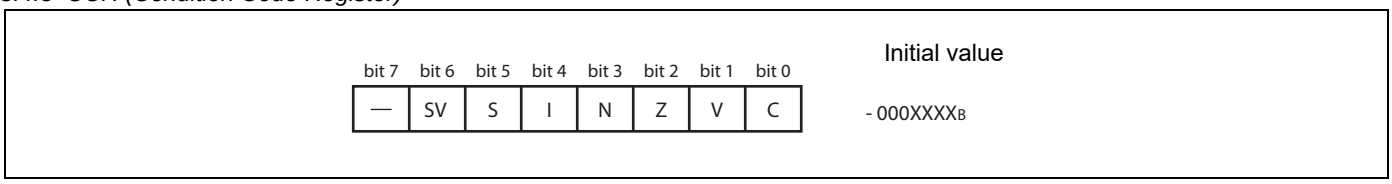
8.4.2 PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.

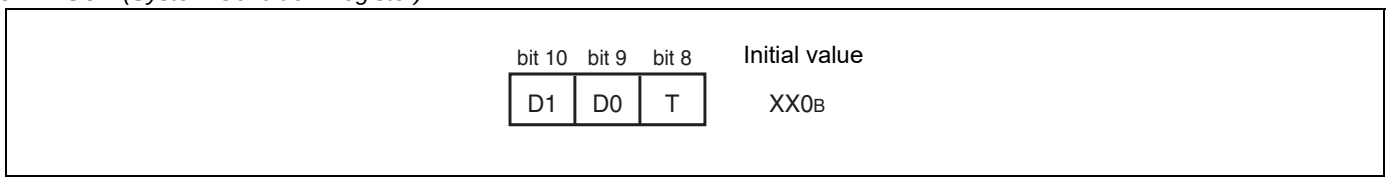


8.4.3 CCR (Condition Code Register)



SV: Supervisor flag
S: Stack flag
I: Interrupt enable flag
N: Negative enable flag
Z: Zero flag
V: Overflow flag
C: Carry flag

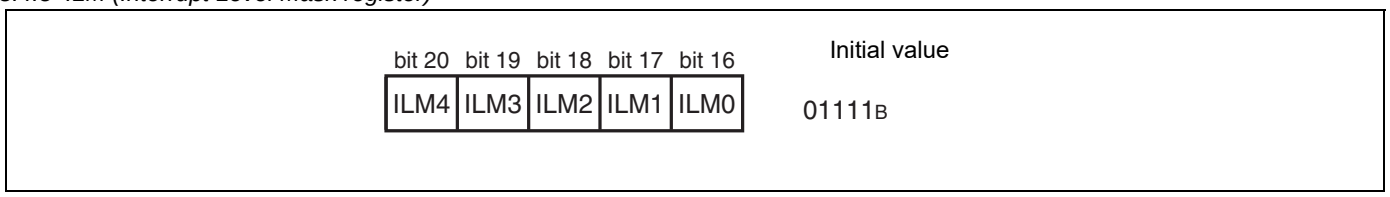
8.4.4 SCR (System Condition Register)



Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

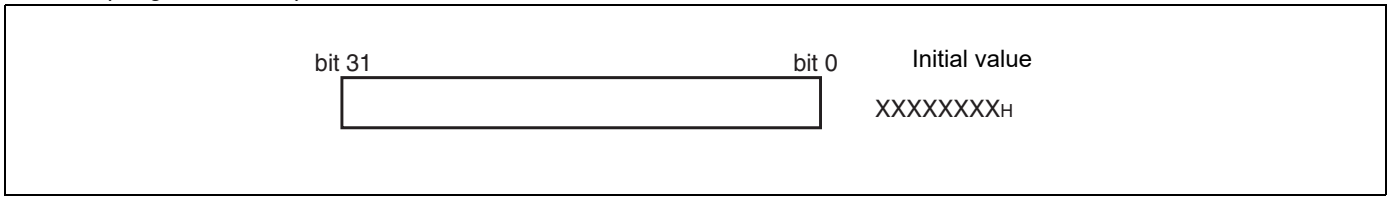
Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

8.4.5 ILM (Interrupt Level Mask register)



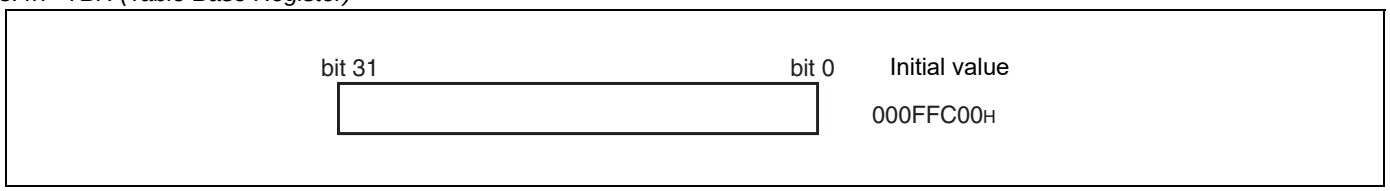
This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.
The register is initialized to value "01111_B" at reset.

8.4.6 PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.
The initial value at reset is undefined.

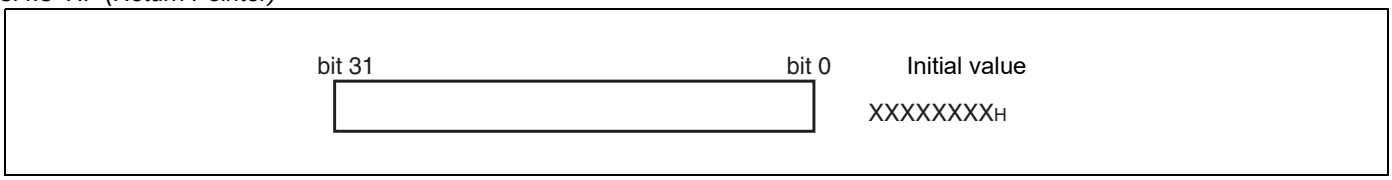
8.4.7 TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is $000FFC00_H$.

8.4.8 RP (Return Pointer)



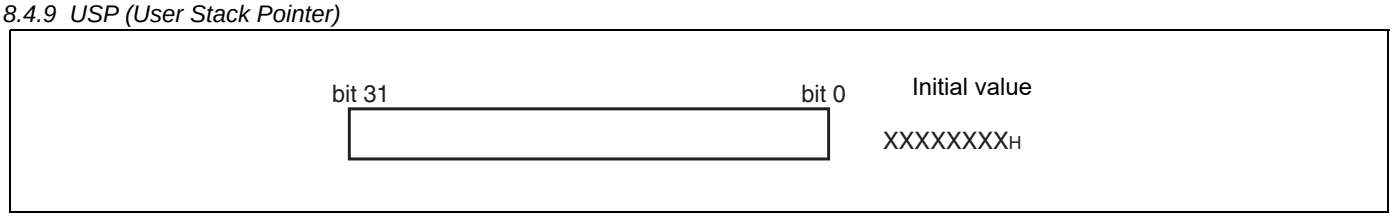
The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

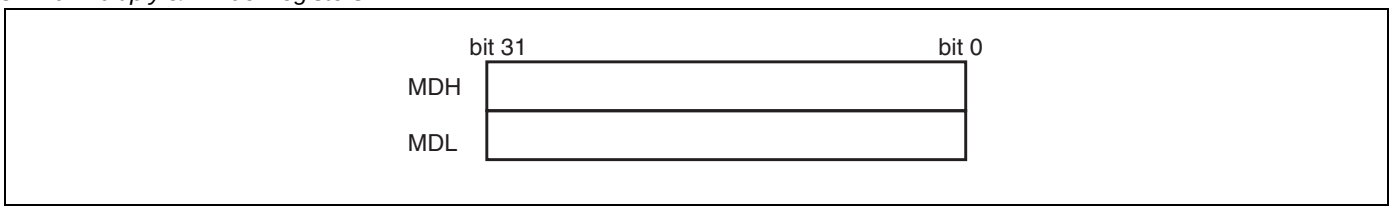
8.4.9 USP (User Stack Pointer)



The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.
  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

8.4.10 Multiply & Divide Registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

9. Embedded Program/Data Memory (Flash)

9.1 Flash Features

- CY91F464HB: 416 Kbytes (6 × 64 Kbytes + 4 × 8 Kbytes = 3.25 Mbits)
- CY91F466HA: 832 Kbytes (12 × 64 Kbytes + 8 × 8 Kbytes = 6.5 Mbits)
- Programmable wait states for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

9.2 Operation Modes:

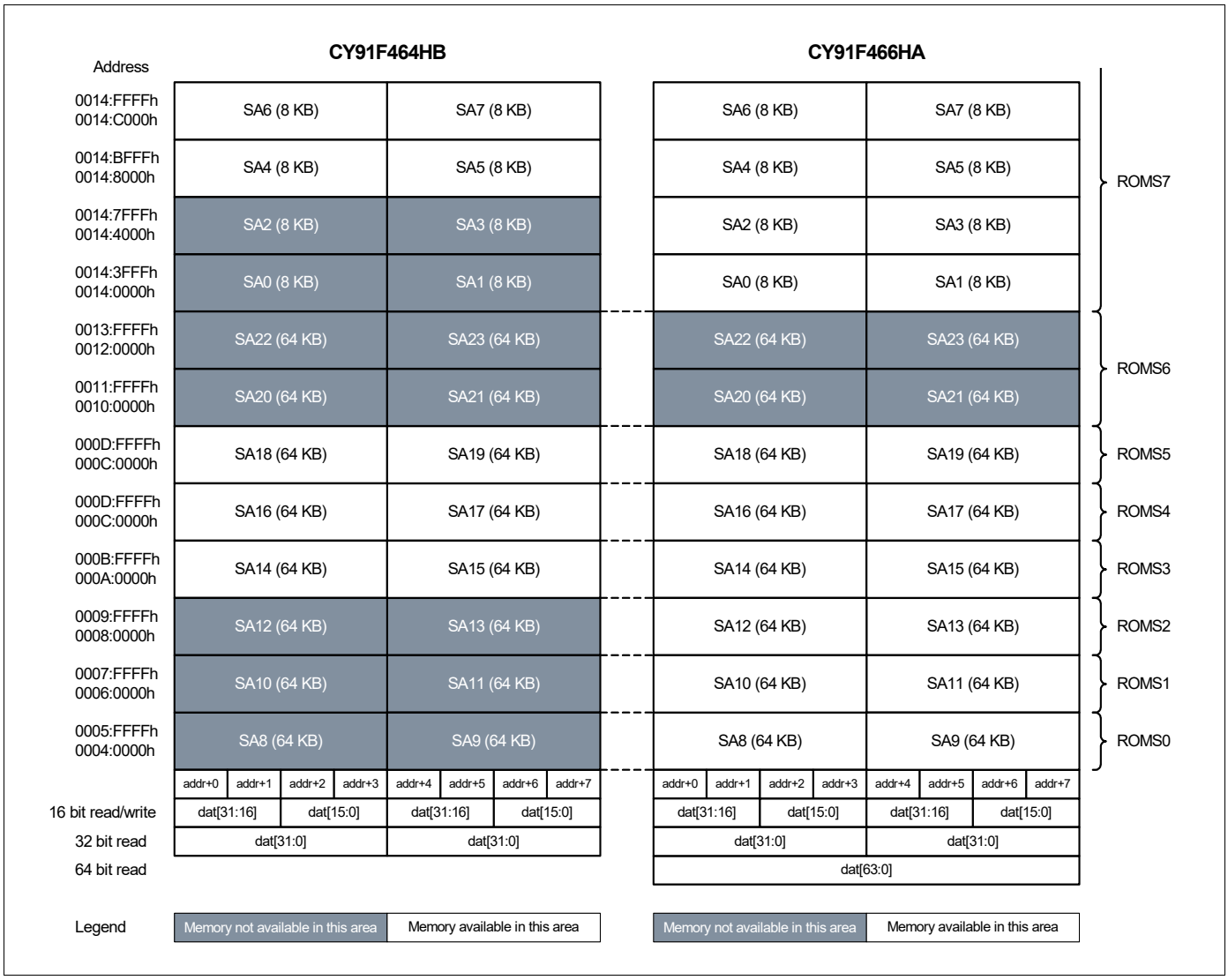
1. 64-bit CPU mode (available on CY91F466HA only):
   - CPU reads and executes programs in word (32-bit) length units.
   - Flash writing is not possible.
   - Actual Flash Memory access is performed in d-word (64-bit) length units.
2. 32-bit CPU mode:
   - CPU reads and executes programs in word (32-bit) length units.
   - Actual Flash Memory access is performed in word (32-bit) length units.
3. 16-bit CPU mode:
   - CPU reads and writes in half-word (16-bit) length units.
   - Program execution from the Flash is not possible.
   - Actual Flash Memory access is performed in word (16-bit) length units.
4. Flash memory mode (external access to Flash memory enabled)

Note: The operation mode of the flash memory can be selected using a Boot-ROM function. The function start address is 0xBF60. The parameter description is given in the Hardware Manual in chapter 54.6 “Flash Access Mode Switching”.

9.3 Flash Access in CPU Mode

9.3.1 Flash Configuration

Flash memory map CY91F464HB, CY91F466HA



9.3.2 Flash Access Timing Settings in CPU Mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 96 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	not available on CY91F466HA

Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 16 MHz	0	-	-	0	3	
to 32 MHz	0	-	-	0	4	
to 48 MHz	0	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	not available on CY91F466HA

9.3.3 Address Mapping from CPU to Parallel Programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

Address mapping CY91F464HB

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 0D:0000h
0A:0000h to 0F:FFFFh	addr[2]==0	SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4
0A:0000h to 0F:FFFFh	addr[2]==1	SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4

Note: FA result is without 20:0000h offset for parallel Flash programming.
Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

Address mapping CY91F466HA

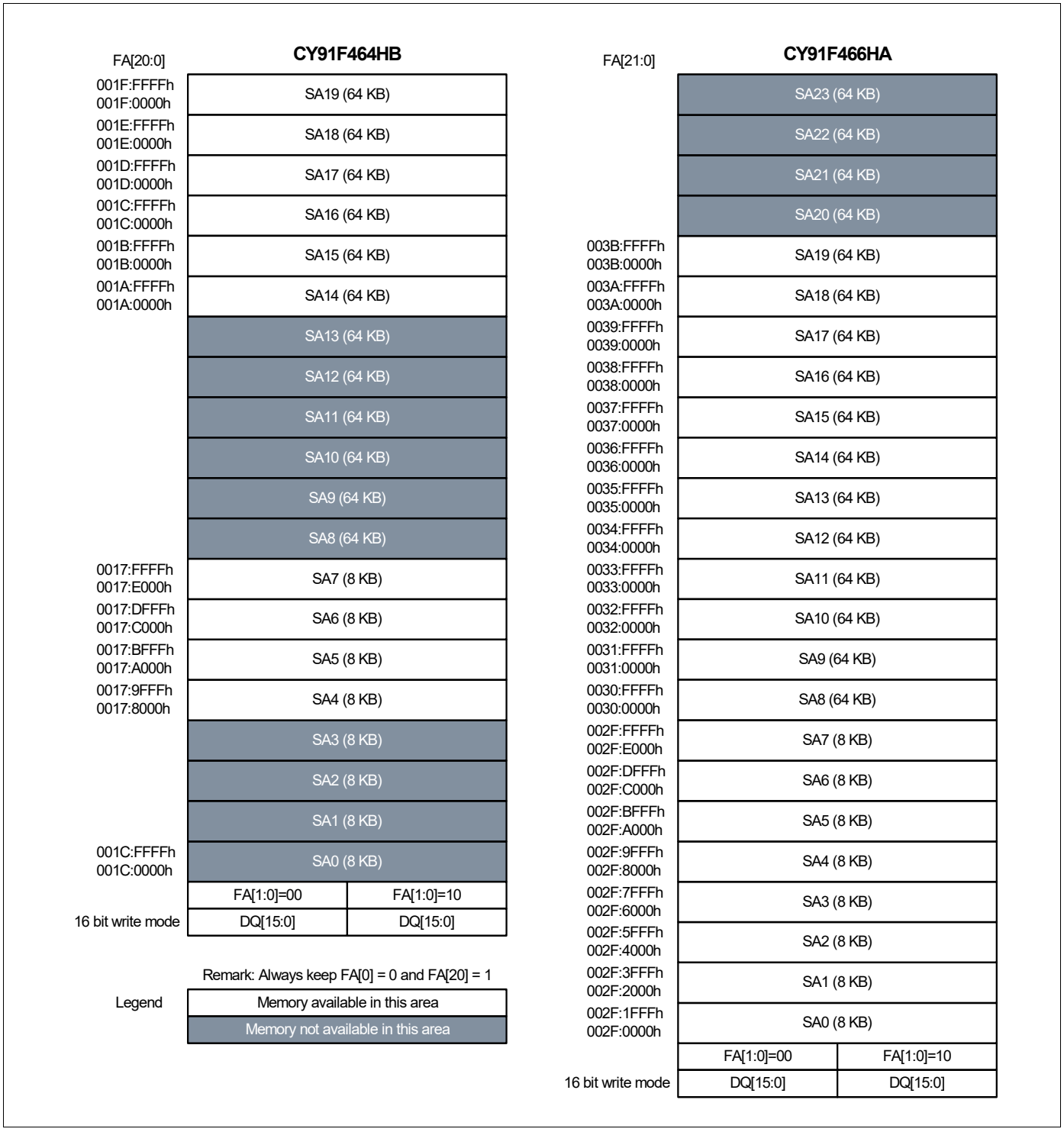
CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 + 00:2000h - (addr/2)%4 + addr%4 - 05:0000h
04:0000h to 0F:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 0F:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 + 01:0000h - (addr/2)%4 + addr%4 + 0C:0000h

Note: FA result is without 20:0000h offset for parallel Flash programming.
Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

9.4 Parallel Flash Programming Mode

9.4.1 Flash Configuration in Parallel Flash Programming Mode

Parallel Flash programming mode (MD[2:0] = 111)



9.4.2 Pin connections in Parallel Programming Mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to GP-Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	CY91F464HB, CY91F466HA external pins			Comment
		Flash memory mode	Normal function	Pin number	
-	INITX	-	INITX	84	
RESET	-	FRSTX	P16_6	70	
-	-	MD2	MD2	76	Set to ‘1’
-	-	MD1	MD1	75	Set to ‘1’
-	-	MD0	MD0	74	Set to ‘1’
RY/BY	FMCS:RDY bit	RY/BYX	P18_2	100	
BYTE	Internally fixed to ‘H’	BYTEX	P16_4	68	
WE	Internal control signal + control via interface circuit	WEX	P16_7	71	
OE		OEX	P07_7	3	
CE		CEX	P07_6	2	
-		ATDIN	P18_6	103	Set to ‘0’
-		EQIN	P18_5	102	Set to ‘0’
-		TESTX	P16_5	69	Set to ‘1’
-		RDYI	P18_4	101	Set to ‘0’
A-1	Internal address bus	FA0	P05_5	17	Set to ‘0’
A0 to A3		FA1 to FA4	P19_0 to P19_2, P19_4	92 to 95	
A4 to A7		FA5 to FA8	P19_5 to P19_6, P18_0 to P18_1	96 to 99	
A8 to A11		FA9 to FA12	P06_0 to P06_3	4 to 7	
A12 to A15		FA13 to FA16	P06_4 to P06_7	8 to 11	
A16 to A18		FA17 to FA19	P05_0 to P05_2	12 to 14	
A19		FA20	P05_3	15	*1
-		FA21	P05_4	16	*2
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	P00_0 to P00_7	28 to 35	
DQ8 to DQ15		DQ8 to DQ15	P01_0 to P01_7	20 to 27	

*1. A19 is used as address bit on CY91F466HA. For CY91F464HB, set this pin to ‘1’.

*2. For CY91F466HA, set this pin to ‘1’. For CY91F464HB, this pin can be left open.

9.5 Poweron Sequence in Parallel Programming Mode

The flash memory can be accessed in programming mode after a certain wait time, which is needed for Security Vector fetch:

- Minimum wait time after VDD5/VDD5R power on: 2.76 ms
- Minimum wait time after INITX rising: 1.0 ms

9.6 Flash Security

9.6.1 Vector Addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

9.6.2 Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 KBytes sectors.

9.6.3 FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1[31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to ‘0’	set to ‘0’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘0’	Write Protection (all device modes, without exception)
set all to ‘0’	set to ‘0’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes)
set all to ‘0’	set to ‘1’	set to ‘0’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘0’	Write Protection (all device modes, except INTVEC mode MD[2:0]=”000”)
set all to ‘0’	set to ‘1’	set to ‘1’	set to ‘1’	Read Protection (all device modes, except INTVEC mode MD[2:0]=”000”) and Write Protection (all device modes except INTVEC mode MD[2:0]=”000”)

FSV1 (bit15 to bit0) CY91F464HB

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 KBytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[3:0]	—	—	—	not available
FSV1[4]	SA4	set to “0”	—	Write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	
FSV1[6]	SA6	set to “0”	set to “1”	
FSV1[7]	SA7	set to “0”	set to “1”	
FSV1[15:8]	—	—	—	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

FSV1 (bit15 to bit0) CY91F466HA

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 KBytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1[15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0	set to “0”	set to “1”	
FSV1[1]	SA1	set to “0”	set to “1”	
FSV1[2]	SA2	set to “0”	set to “1”	
FSV1[3]	SA3	set to “0”	set to “1”	
FSV1[4]	SA4	set to “0”	—	Write protection is mandatory!
FSV1[5]	SA5	set to “0”	set to “1”	
FSV1[6]	SA6	set to “0”	set to “1”	
FSV1[7]	SA7	set to “0”	set to “1”	
FSV1[15:8]	—	—	—	not available

Note: It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

9.6.4 Security Vector FSV2 CY91F464HB

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[5:0]	—	—	—	not available
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[31:12]	—	—	—	not available

Note : See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

9.6.5 Security Vector FSV2 CY91F466HA

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 KByte sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV2 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8	set to “0”	set to “1”	
FSV2[1]	SA9	set to “0”	set to “1”	
FSV2[2]	SA10	set to “0”	set to “1”	
FSV2[3]	SA11	set to “0”	set to “1”	
FSV2[4]	SA12	set to “0”	set to “1”	
FSV2[5]	SA13	set to “0”	set to “1”	
FSV2[6]	SA14	set to “0”	set to “1”	
FSV2[7]	SA15	set to “0”	set to “1”	
FSV2[8]	SA16	set to “0”	set to “1”	
FSV2[9]	SA17	set to “0”	set to “1”	
FSV2[10]	SA18	set to “0”	set to “1”	
FSV2[11]	SA19	set to “0”	set to “1”	
FSV2[31:12]	—	—	—	not available

Note : See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

10. Memory Space

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

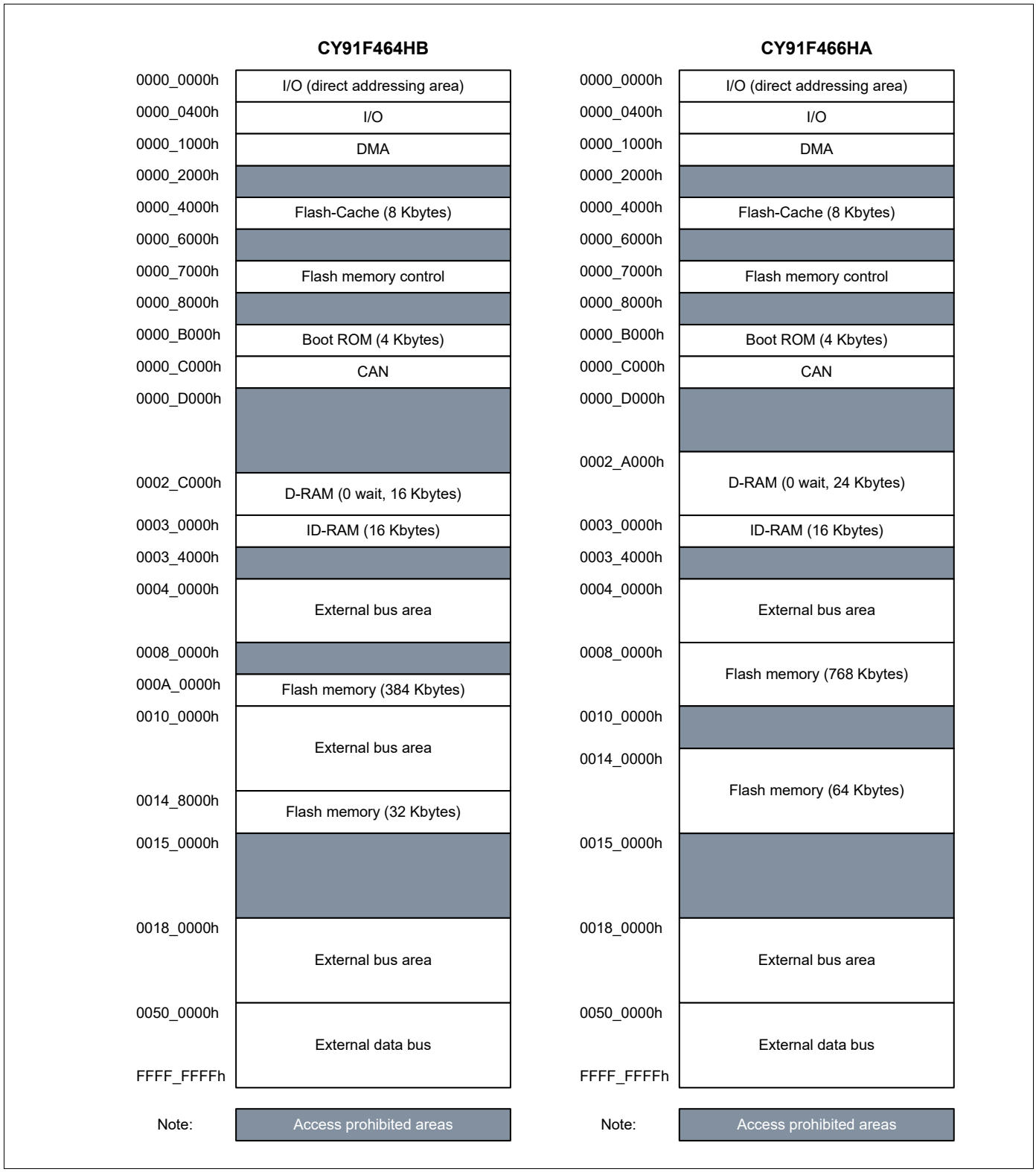
Byte data access : 000_H to $0FF_H$

Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

11. Memory Maps

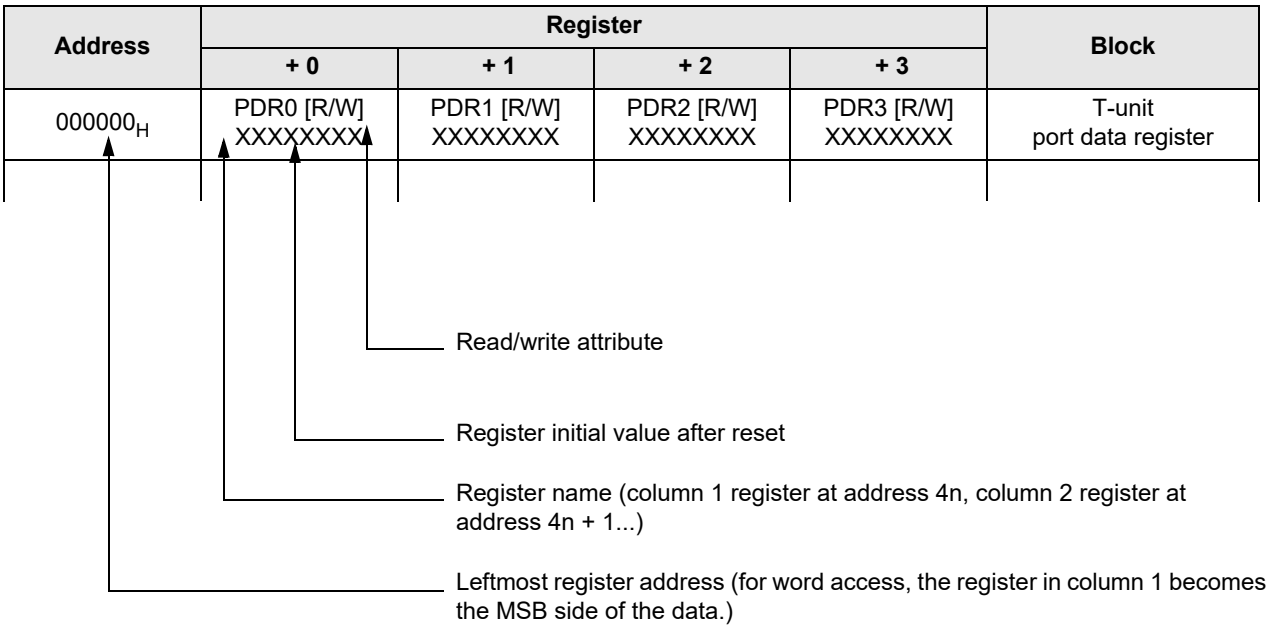
11.1 CY91F464HB, CY91466HA



12. I/O Map

12.1 CY91F464HB, CY91F466HA

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000_H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note : Initial values of register bits are represented as follows:
" 1 " : Initial value " 1 "
" 0 " : Initial value " 0 "
" X " : Initial value " undefined "
" - " : No physical register at this location
Access is barred with an undefined data access attribute.

Address	Register				Block
	+0	+1	+2	+3	
000000_H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved	Reserved	R-bus Port Data Register
000004_H	Reserved	PDR05 [R/W] - - XXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008_H	PDR08 [R/W] X - - X - - - X	PDR09 [R/W] - - - - - - XX	PDR10 [R/W] - - - - - - - X	Reserved	
$00000C_H$	Reserved	Reserved	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] XXXXXXXX	
000010_H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014_H	PDR20 [R/W] - XXX - XXX	PDR21 [R/W] - - - - - - XX	PDR22 [R/W] XXXXXXXX	PDR23 [R/W] XXXXXXXX	
000018_H	PDR24 [R/W] XXXXXXXX	Reserved	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
$00001C_H$	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved	Reserved	

Address	Register				Block
	+0	+1	+2	+3	
000020_H to $00002C_H$	Reserved				
000030_H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034_H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 15)
000038_H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	RBSYNC		Delay interrupt
$00003C_H$	Reserved				Reserved
000040_H	SCR00 [R/W,W] 00000000	SMR00 [R/W,W] 00000000	SSR00 [R/W,R] 00001000	RDR00/TDR00 [R/W] 00000000	LIN-USART 0
000044_H	ESCR00 [R/W] 00000X00	ECCR00 [R/W,R,W] -00000XX	Reserved		
000048_H $00004C_H$	Reserved				Reserved
000050_H	SCR02 [R/W,W] 00000000	SMR02 [R/W,W] 00000000	SSR02 [R/W,R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054_H	ESCR02 [R/W] 00000X00	ECCR02 [R/W,R,W] -00000XX	Reserved		
000058_H	SCR03 [R/W,W] 00000000	SMR03 [R/W,W] 00000000	SSR03 [R/W,R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
$00005C_H$	ESCR03 [R/W] 00000X00	ECCR03 [R/W,R,W] -00000XX	Reserved		
000060_H	SCR04 [R/W,W] 00000000	SMR04 [R/W,W] 00000000	SSR04 [R/W,R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064_H	ESCR04 [R/W] 00000X00	ECCR04 [R/W,R,W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068_H	SCR05 [R/W,W] 00000000	SMR05 [R/W,W] 00000000	SSR05 [R/W,R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
$00006C_H$	ESCR05 [R/W] 00000X00	ECCR05 [R/W,R,W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070_H	SCR06 [R/W,W] 00000000	SMR06 [R/W,W] 00000000	SSR06 [R/W,R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074_H	ESCR06 [R/W] 00000X00	ECCR06 [R/W,R,W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078_H	SCR07 [R/W,W] 00000000	SMR07 [R/W,W] 00000000	SSR07 [R/W,R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
$00007C_H$	ESCR07 [R/W] 00000X00	ECCR07 [R/W,R,W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	

Address	Register				Block
	+0	+1	+2	+3	
000080_H	BGR100 [R/W] 00000000	BGR000 [R/W] 00000000	Reserved	Reserved	Baud rate Generator LIN-USART 0 to 7
000084_H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	
000088_H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
$00008C_H$	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090_H to $0000CC_H$	Reserved				Reserved
$0000D0_H$	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I^2C 0
$0000D4_H$	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
$0000D8_H$	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	Reserved	
$0000DC_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1 [R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I^2C 1
$0000E0_H$	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
$0000E4_H$	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] - 0011111	Reserved	
$0000E8_H$ to $0000FC_H$	Reserved				Reserved
000100_H	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104_H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108_H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
000110_H	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114_H	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118_H	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
$00011C_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120_H	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG 2
000124_H	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000128_H	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG 3
$00012C_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130_H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134_H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138_H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
$00013C_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140_H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144_H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148_H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
$00014C_H$	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150_H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154_H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158_H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
$00015C_H$	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160_H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164_H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168_H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
$00016C_H$	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170_H to $00017C_H$	Reserved				Reserved
000180_H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184_H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188_H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		

Address	Register				Block
	+0	+1	+2	+3	
$00018C_H$	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190_H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194_H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198_H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
$00019C_H$	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
$0001A0_H$	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
$0001A8_H$	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
$0001AC_H$	Reserved	ACSR0 [R/W] -11XXX00	Reserved	Reserved	Alarm Comparator 0 to 1
$0001B0_H$	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
$0001B4_H$	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
$0001B8_H$	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
$0001BC_H$	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
$0001C0_H$	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
$0001C4_H$	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
$0001C8_H$	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
$0001CC_H$	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
$0001D0_H$	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
$0001D4_H$	Reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	

Address	Register				Block
	+0	+1	+2	+3	
$0001D8_H$	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
$0001DC_H$	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
$0001E0_H$	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
$0001E4_H$	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
$0001E8_H$	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
$0001EC_H$	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
$0001F0_H$	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
$0001F4_H$	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
$0001F8_H$	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
$0001FC_H$	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)
000200_H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204_H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208_H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00020C_H$	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210_H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214_H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218_H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
$00021C_H$	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
000220_H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000224_H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228_H to $00023C_H$	Reserved				
000240_H	DMACR [R/W] 00 - - 0000	Reserved			
000244_H to $0002CC_H$	Reserved				Reserved
$0002D0_H$	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
$0002D4_H$	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
$0002D8_H$	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
$0002DC_H$	OCS45 [R/W] - - - 0 - - 00 0000 - - 00		OCS67 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 4 to 7
$0002E0_H$	OCCP4 [R/W] XXXXXXXX XXXXXXXX		OCCP5 [R/W] XXXXXXXX XXXXXXXX		
$0002E4_H$	OCCP6 [R/W] XXXXXXXX XXXXXXXX		OCCP7 [R/W] XXXXXXXX XXXXXXXX		
$0002E8_H$ to $0002EC_H$	Reserved				Reserved
$0002F0_H$	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4, ICU 5)
$0002F4_H$	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6, ICU 7)
$0002F8_H$	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6 (OCU 4, OCU 5)
$0002FC_H$	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7 (OCU 6, OCU 7)
000300_H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0 to 1
000304_H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308_H	UDCCH1 [R/W] 00000000	UDCCL1 [R/W] 00001000	Reserved	UDCS1 [R/W] 00000000	
$00030C_H$ to $00031C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000320_H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] - - - - 0000	PPG Control 12 to 15
000324_H to $00032C_H$	Reserved				Reserved
000330_H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334_H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338_H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
$00033C_H$	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340_H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344_H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	
000348_H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
$00034C_H$	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350_H to $00038C_H$	Reserved				Reserved
000390_H	ROMS [R] 11111111 01000011		Reserved		ROM Select Register
000394_H to $0003EC_H$	Reserved				Reserved
$0003F0_H$	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
$0003F4_H$	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003F8_H$	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0003FC_H$	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400_H to $00043C_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444_H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448_H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
$00044C_H$	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450_H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454_H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458_H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
$00045C_H$	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460_H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34[R/W] ---11111	ICR35 [R/W] ---11111	
000464_H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468_H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
$00046C_H$	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470_H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474_H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478_H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
$00047C_H$	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	Interrupt Controller
000480_H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control
000484_H	CLKR [R/W] - - - - 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488_H	Reserved				Reserved
$00048C_H$	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [R/W] 00000000	PLL Interface
000490_H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494_H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control (Reserved)

Address	Register				Block
	+0	+1	+2	+3	
000498_H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control
$0004A0_H$	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
$0004A4_H$	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
$0004A8_H$	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
$0004AC_H$	CSVTR [R/W] - - - 00010	CSVCR [R/W] - 011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor /Selector/ Monitor
$0004B0_H$	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
$0004B4_H$	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
$0004B8_H$	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulator
$0004BC_H$	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
$0004C0_H$	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - - - - - - 0	Reserved		CAN Clock Control
$0004C4_H$	LVSEL [R/W] 00000111	LVDET [R/W] 00000 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W,W] 00011000	Low Voltage Detection/ Hardware Watchdog
$0004C8_H$	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 000 - - 001	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilisation Timer
$0004CC_H$	OSCCR [R/W] - - - - - - 00	Reserved	REGSEL [R/W] - - 000110	REGCTR [R/W] - - - 0 - - 00	Main- Oscillation Standby Control / Main/Sub Regulator Control
$0004D0_H$ to $00063C_H$	Reserved				Reserved
000640_H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00000000*2		External Bus Unit
000644_H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648_H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
$00064C_H$	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650_H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654_H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		

Address	Register				Block
	+0	+1	+2	+3	
000658_H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		External Bus Unit
$00065C_H$	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660_H	AWR0 [R/W] 01111111 11111*11		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664_H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668_H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
$00066C_H$	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670_H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674_H	Reserved				
000678_H	IOWR0 [R/W] XXXXXXXX	IOWR1 [R/W] XXXXXXXX	IOWR2 [R/W] XXXXXXXX	IOWR3 [R/W] XXXXXXXX	
$00067C_H$	Reserved				
000680_H	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** *3	
000684_H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688_H to $0007F8_H$	Reserved				
$0007FC_H$	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register
000800_H to $000CFC_H$	Reserved				Reserved
$000D00_H$	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		R-bus Port Data Direct Read Register
$000D04_H$	Reserved	PDRD05 [R] - - XXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
$000D08_H$	PDRD08 [R] X - - X - - -X	PDRD09 [R] - - - - - - XX	PDRD10 [R] - - - - - - - X	Reserved	
$000D0C_H$	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] XXXXXXXX	
$000D10_H$	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
$000D14_H$	PDRD20 [R] - XXX - XXX	PDRD21 [R] - - - - - - - X	PDRD22 [R] XXXXXXXX	PDRD23 [R] XXXXXXXX	
$000D18_H$	PDRD24 [R] XXXXXXXX	Reserved	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
$000D1C_H$	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		

Address	Register				Block
	+0	+1	+2	+3	
$000D20_H$ to $000D3C_H$	Reserved				
$000D40_H$	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		R-bus Port Direction Register
$000D44_H$	Reserved	DDR05 [R/W] - - 000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
$000D48_H$	DDR08 [R/W] 0 - - 0 - - -0	DDR09 [R/W] - - - - - - 00	DDR10 [R/W] - - - - - - - -0	Reserved	
$000D4C_H$	Reserved		DDR14 [R/W] 00000000	DDR15 [R/W] 00000000	
$000D50_H$	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
$000D54_H$	DDR20 [R/W] - 000 - 000	DDR21 [R/W] - - - - - - 00	DDR22 [R/W] 00000000	DDR23 [R/W] 00000000	
$000D58_H$	DDR24 [R/W] 00000000	Reserved	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
$000D5C_H$	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		
$000D60_H$ to $000D7C_H$	Reserved				Reserved
$000D80_H$	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	Reserved		R-bus Port Function Register
$000D84_H$	Reserved	PFR05 [R/W] - - 111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
$000D88_H$	PFR08 [R/W] 1 - - 1 - - 11	PFR09 [R/W] - - - - - - 11	PFR10 [R/W] - - - - - - - -1	Reserved	
$000D8C_H$	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] 00000000	
$000D90_H$	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
$000D94_H$	PFR20 [R/W] - 000 - 000	PFR21 [R/W] - - - - - - 00	PFR22 [R/W] 0000-0-0	PFR23 [R/W] -0000000	
$000D98_H$	PFR24 [R/W] 00000000	Reserved	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
$000D9C_H$	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	Reserved		
$000DA0_H$ to $000DC4_H$	Reserved				

Address	Register				Block
	+0	+1	+2	+3	
$000DC8_H$	Reserved		EPFR10 [R/W] - - - - - - - 0	Reserved	R-bus Port Extra Function Register
$000DCC_H$	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] 00000000	
$000DD0_H$	EPFR16 [R/W] 0 - 00 - - - -	Reserved	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0- - - 0- -	
$000DD4_H$	EPFR20 [R/W] - 000 - 000	EPFR21 [R/W] - - - - - - - -	Reserved		
$000DD8_H$	Reserved		EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
$000DDC_H$ to $000DFC_H$	Reserved				Reserved
$000E00_H$	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	Reserved		R-bus Port Output Drive Select Register
$000E04_H$	Reserved	PODR05 [R/W] - - 000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
$000E08_H$	PODR08 [R/W] 0 - - 0 - - - 0	PODR09 [R/W] - - - - - - 00	PODR10 [R/W] - - - - - - - 0	Reserved	
$000E0C_H$	Reserved		PODR14 [R/W] 00000000	PODR15 [R/W] 00000000	
$000E10_H$	PODR16 [R/W] 00000000	PODR17 [R/W] 00000000	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
$000E14_H$	PODR20 [R/W] - 000 - 000	PODR21 [R/W] - - - - - - 00	PODR22 [R/W] 00000000	PODR23 [R/W] 00000000	
$000E18_H$	PODR24 [R/W] 00000000	Reserved	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
$000E1C_H$	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	Reserved		
$000E20_H$ to $000E3C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000E40_H$	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		R-bus Port Input Level Select Register
$000E44_H$	Reserved	PILR05 [R/W] - - 000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
$000E48_H$	PILR08 [R/W] 0 - - 0 - - - 0	PILR09 [R/W] - - - - - - 00	PILR10 [R/W] - - - - - - - 0	Reserved	
$000E4C_H$	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] 00000000	
$000E50_H$	PILR16 [R/W] 00000000	PILR17 [R/W] 00000000	PILR18 [R/W] - - - - - 000	PILR19 [R/W] - 000 - 000	
$000E54_H$	PILR20 [R/W] - 000 - 000	PILR21 [R/W] - - - - - - 00	PILR22 [R/W] 00000000	PILR23 [R/W] 00000000	
$000E58_H$	PILR24 [R/W] 00000000	Reserved	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
$000E5C_H$	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
$000E60_H$ to $000E7C_H$	Reserved				Reserved
$000E80_H$	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved		R-bus Port Extra Input Level Select Register
$000E84_H$	Reserved	EPILR05 [R/W] - - 000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
$000E88_H$	EPILR08 [R/W] 0 - - 0- - - 0	EPILR09 [R/W] - - - - - - 00	EPILR10 [R/W] - - - - - - - 0	Reserved	
$000E8C_H$	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] 00000000	
$000E90_H$	EPILR16 [R/W] 00000000	EPILR17 [R/W] 00000000	EPILR18 [R/W] - - - - - 000	EPILR19 [R/W] - 000 - 000	
$000E94_H$	EPILR20 [R/W] - 000 - 000	EPILR21 [R/W] - - - - - - 00	EPILR22 [R/W] 00000000	EPILR23 [R/W] 00000000	
$000E98_H$	EPILR24 [R/W] 00000000	Reserved	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
$000E9C_H$	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
$000EA0_H$ to $000EBC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$000EC0_H$	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		R-bus Port Pull-Up/Down Enable Register
$000EC4_H$	Reserved	PPER05 [R/W] - - 000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
$000EC8_H$	PPER08 [R/W] 0 - - 0 - - - 0	PPER09 [R/W] - - - - - - 00	PPER10 [R/W] - - - - - - - 0	Reserved	
$000ECC_H$	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] 00000000	
$000ED0_H$	PPER16 [R/W] 00000000	PPER17 [R/W] 00000000	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
$000ED4_H$	PPER20 [R/W] - 000 - 000	PPER21 [R/W] - - - - - - 00	PPER22 [R/W] 00000000	PPER23 [R/W] 00000000	
$000ED8_H$	PPER24 [R/W] 00000000	Reserved	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
$000EDC_H$	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
$000EE0_H$ to $000EFC_H$	Reserved				Reserved
$000F00_H$	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		R-bus Port Pull-Up/Down Control Register
$000F04_H$	Reserved	PPCR05 [R/W] - - 111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
$000F08_H$	PPCR08 [R/W] 1 - - 1 - - - 1	PPCR09 [R/W] - - - - - - 11	PPCR10 [R/W] - - - - - - - 1	Reserved	
$000F0C_H$	Reserved		PPCR14 [R/W] 00000000	PPCR15 [R/W] 11111111	
$000F10_H$	PPCR16 [R/W] 00000000	PPCR17 [R/W] 00000000	PPCR18 [R/W] - 111- 111	PPCR19 [R/W] - 111- 111	
$000F14_H$	PPCR20 [R/W] - 111- 111	PPCR21 [R/W] - - - - - - 11	PPCR22 [R/W] 11111111	PPCR23 [R/W] 11111111	
$000F18_H$	PPCR24 [R/W] 11111111	Reserved	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
$000F1C_H$	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
$000F20_H$ to $000F3C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
001000_H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004_H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008_H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00100C_H$	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010_H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014_H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018_H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00101C_H$	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020_H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024_H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028_H to $003FFC_H$	Reserved				Reserved
002000_H to $006FFC_H$	Flash-cache size is 8 Kbytes: 004000_H to $005FFC_H$				Flash-cache / I-RAM area
007000_H	FMCS [R/W] 01101000	FMCR [R/W] - - - - 0000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ I-Cache Control Register
007004_H	FMWT [R/W] 11111111 11111111		Reserved	FMPS [R/W] - - - - - 000	
007008_H	FMAC [R] 00000000 00000000 00000000 00000000				
$00700C_H$	FCHA0 [R/W] - - - - - - - - - - 000000 00000000 00000000				I-Cache Non-cacheable area setting Register
007010_H	FCHA1 [R/W] - - - - - - - - - - 000000 00000000 00000000				
007014_H to $007FFC_H$	Reserved				Reserved
008000_H to $00BFFC_H$	Boot-ROM size is 4 Kbytes: $00B000_H$ to $00BFFC_H$ (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area

Address	Register				Block
	+0	+1	+2	+3	
$00C000_H$	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
$00C004_H$	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
$00C008_H$	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
$00C00C_H$	BRPE0 [R/W] 00000000 00000000		CBSYNC0		
$00C010_H$	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
$00C014_H$	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
$00C018_H$	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
$00C01C_H$	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
$00C020_H$	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		
$00C024_H$	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
$00C028_H$ to $00C02C_H$	Reserved				
$00C030_H$	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
$00C034_H$	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
$00C038_H$ to $00C03C_H$	Reserved				
$00C040_H$	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
$00C044_H$	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
$00C048_H$	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		

Address	Register				Block
	+0	+1	+2	+3	
$00C04C_H$	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
$00C050_H$	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
$00C054_H$	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
$00C058_H$ to $00C05C_H$	Reserved				
$00C060_H$	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
$00C064_H$	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
$00C068_H$ to $00C07C_H$	Reserved				
$00C080_H$	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
$00C084_H$ to $00C08C_H$	Reserved		Reserved		
$00C090_H$	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
$00C094_H$ to $00C09C_H$	Reserved		Reserved		
$00C0A0_H$	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
$00C0A4_H$ to $00C0AC_H$	Reserved		Reserved		
$00C0B0_H$	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
$00C0B4_H$ to $00C0FC_H$	Reserved		Reserved		
$00C100_H$ to $00EFFC_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$00F000_H$	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
$00F004_H$	BSTAT [R/W] -------- -----000 00000000 10--000000				
$00F008_H$	BIAC [R] -------- -------- 00000000 00000000				
$00F00C_H$	BOAC [R] -------- -------- 00000000 00000000				
$00F010_H$	BIRQ [R/W] -------- -------- 00000000 00000000				
$00F014_H$ to $00F01C_H$	Reserved				
$00F020_H$	BCR0 [R/W] -------- 00000000 00000000 00000000				
$00F024_H$	BCR1 [R/W] -------- 00000000 00000000 00000000				
$00F028_H$	BCR2 [R/W] -------- 00000000 00000000 00000000				
$00F02C_H$	BCR3 [R/W] -------- 00000000 00000000 00000000				
$00F030_H$ to $00F07C_H$	Reserved				Reserved

Address	Register				Block
	+0	+1	+2	+3	
$00F080_H$	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
$00F084_H$	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F088_H$	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F08C_H$	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F090_H$	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F094_H$	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F098_H$	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F09C_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A0_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A4_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0A8_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0AC_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B0_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B4_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0B8_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0BC_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00F0C0_H$ to $01FFFC_H$	Reserved				
020000_H to $02FFFC_H$	CY91F466HA D-RAM size is 24 Kbytes: 02A000H - 02FFFCH CY91F464HB D-RAM size is 16 Kbytes: 02C000H - 02FFFCH (data access is 0 wait cycles)				D-RAM area
030000_H to $03FFFC_H$	ID-RAM size is 16 Kbytes: 030000_H - $033FFC_H$ (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

*1: depends on the number of available CAN channels

*2: ACR0 [11 : 10] depends on Mode vector fetch information on bus width

*3: TCR [3 : 0] INIT value = 0000, keeps value after RST

12.2 Flash Memory and External Bus Area

12.2.1 CY91F464HB, CY91F466HA

CY91F464HB

32 bit read	dat[31:0]				dat[31:0]				
16 bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+0	+1	+2	+3	+4	+5	+6	+7	
040000h to 05FFF8h	Reserved				Reserved				ROMS0
060000h to 07FFF8h	Reserved				Reserved				ROMS1
080000h to 09FFF8h	Reserved				Reserved				ROMS2
0A0000h to 0BFFF8h	SA14 (64 KB)				SA15 (64 KB)				ROMS3
0C0000h to 0DFFF8h	SA16 (64 KB)				SA17 (64 KB)				ROMS4
0E0000h to 0FFFF0h	SA18 (64 KB)				SA19 (64 KB)				ROMS5
0FFFF8h	FMV [R] 06 00 00 00h				FMV [R] 00 00 BF F8h				
100000h to 11FFF8h	External Bus Area								ROMS6
120000h to 13FFF8h									
140000h to 143FF8h	External Bus Area								ROMS7
144000h to 147FF8h									
148000h to 14BFF8h	SA4 (8 KB)				SA5 (8 KB)				
14C000h to 14FFF8h	SA6 (8 KB)				SA7 (8 KB)				
150000h to 17FFF8h	Reserved								
180000h to 1BFFF8h	External Bus Area								ROMS8
1C0000h to 1FFFF8h									ROMS9
200000h to 27FFF8h									ROMS10
280000h to 2FFFF8h									ROMS11
300000h to 37FFF8h									ROMS12
380000h to 3FFFF8h									ROMS13
400000h to 47FFF8h									ROMS14
480000h to 4FFFF8h									ROMS15

CY91F466HA

64 bit read	dat[63:0]								
32 bit read/write	dat[31:0]				dat[31:0]				
16 bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+0	+1	+2	+3	+4	+5	+6	+7	
040000h to 05FFF8h	SA8 (64 KB)				SA9 (64 KB)				ROMS0
060000h to 07FFF8h	SA10 (64 KB)				SA11 (64 KB)				ROMS1
080000h to 09FFF8h	SA12 (64 KB)				SA13 (64 KB)				ROMS2
0A0000h to 0BFFF8h	SA14 (64 KB)				SA15 (64 KB)				ROMS3
0C0000h to 0DFFF8h	SA16 (64 KB)				SA17 (64 KB)				ROMS4
0E0000h to 0FFFF0h	SA18 (64 KB)				SA19 (64 KB)				ROMS5
0FFFF8h	FMV [R] 06 00 00 00h				FMV [R] 00 00 BF F8h				
100000h to 11FFF8h	External Bus Area								ROMS6
120000h to 13FFF8h									
140000h to 143FF8h	SA0 (8 KB)				SA1 (8 KB)				ROMS7
144000h to 147FF8h	SA2 (8 KB)				SA3 (8 KB)				
148000h to 14BFF8h	SA4 (8 KB)				SA5 (8 KB)				
14C000h to 14FFF8h	SA6 (8 KB)				SA7 (8 KB)				
150000h to 17FFF8h	Reserved								
180000h to 1BFFF8h	External Bus Area								ROMS8
1C0000h to 1FFFF8h									ROMS9
200000h to 27FFF8h									ROMS10
280000h to 2FFFF8h									ROMS11
300000h to 37FFF8h									ROMS12
380000h to 3FFFF8h									ROMS13
400000h to 47FFF8h									ROMS14
480000h to 4FFFF8h									ROMS15

Note: Write operations to address 0FFFF8h and 0FFFFCh are not possible. When reading these addresses, the values shown above will be read.

13. Interrupt Vector Table

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reset	0	00	—	—	$3FC_H$	$000FFFFC_H$	—
Mode vector	1	01	—	—	$3F8_H$	$000FFFF8_H$	—
System reserved	2	02	—	—	$3F4_H$	$000FFFF4_H$	—
System reserved	3	03	—	—	$3F0_H$	$000FFFF0_H$	—
System reserved	4	04	—	—	$3EC_H$	$000FFFEC_H$	—
CPU supervisor mode (INT #5 instruction) *5	5	05	—	—	$3E8_H$	$000FFFE8_H$	—
Memory Protection exception *5	6	06	—	—	$3E4_H$	$000FFFE4_H$	—
System reserved	7	07	—	—	$3E0_H$	$000FFFE0_H$	—
System reserved	8	08	—	—	$3DC_H$	$000FFFDC_H$	—
System reserved	9	09	—	—	$3D8_H$	$000FFFD8_H$	—
System reserved	10	0A	—	—	$3D4_H$	$000FFFD4_H$	—
System reserved	11	0B	—	—	$3D0_H$	$000FFFD0_H$	—
System reserved	12	0C	—	—	$3CC_H$	$000FFFCC_H$	—
System reserved	13	0D	—	—	$3C8_H$	$000FFFC8_H$	—
Undefined instruction exception	14	0E	—	—	$3C4_H$	$000FFFC4_H$	—
NMI request	15	0F	F_H fixed		$3C0_H$	$000FFFC0_H$	—
External Interrupt 0	16	10	ICR00	440_H	$3BC_H$	$000FFFBC_H$	0, 16
External Interrupt 1	17	11			$3B8_H$	$000FFFB8_H$	1, 17
External Interrupt 2	18	12	ICR01	441_H	$3B4_H$	$000FFFB4_H$	2, 18
External Interrupt 3	19	13			$3B0_H$	$000FFFB0_H$	3, 19
External Interrupt 4	20	14	ICR02	442_H	$3AC_H$	$000FFFAC_H$	20
External Interrupt 5	21	15			$3A8_H$	$000FFFA8_H$	21
External Interrupt 6	22	16	ICR03	443_H	$3A4_H$	$000FFFA4_H$	22
External Interrupt 7	23	17			$3A0_H$	$000FFFA0_H$	23
External Interrupt 8	24	18	ICR04	444_H	$39C_H$	$000FFF9C_H$	—
External Interrupt 9	25	19			398_H	$000FFF98_H$	—
External Interrupt 10	26	1A	ICR05	445_H	394_H	$000FFF94_H$	—
External Interrupt 11	27	1B			390_H	$000FFF90_H$	—
External Interrupt 12	28	1C	ICR06	446_H	$38C_H$	$000FFF8C_H$	—
External Interrupt 13	29	1D			388_H	$000FFF88_H$	—
External Interrupt 14	30	1E	ICR07	447_H	384_H	$000FFF84_H$	—
External Interrupt 15	31	1F			380_H	$000FFF80_H$	—
Reload Timer 0	32	20	ICR08	448_H	$37C_H$	$000FFF7C_H$	4, 32
Reload Timer 1	33	21			378_H	$000FFF78_H$	5, 33

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Reload Timer 2	34	22	ICR09	449_H	374_H	$000FFF74_H$	34
Reload Timer 3	35	23			370_H	$000FFF70_H$	35
Reload Timer 4	36	24	ICR10	$44A_H$	$36C_H$	$000FFF6C_H$	36
Reload Timer 5	37	25			368_H	$000FFF68_H$	37
Reload Timer 6	38	26	ICR11	$44B_H$	364_H	$000FFF64_H$	38
Reload Timer 7	39	27			360_H	$000FFF60_H$	39
Free Run Timer 0	40	28	ICR12	$44C_H$	$35C_H$	$000FFF5C_H$	40
Free Run Timer 1	41	29			358_H	$000FFF58_H$	41
Free Run Timer 2	42	2A	ICR13	$44D_H$	354_H	$000FFF54_H$	42
Free Run Timer 3	43	2B			350_H	$000FFF50_H$	43
Free Run Timer 4	44	2C	ICR14	$44E_H$	$34C_H$	$000FFF4C_H$	44
Free Run Timer 5	45	2D			348_H	$000FFF48_H$	45
Free Run Timer 6	46	2E	ICR15	$44F_H$	344_H	$000FFF44_H$	46
Free Run Timer 7	47	2F			340_H	$000FFF40_H$	47
CAN 0	48	30	ICR16	450_H	$33C_H$	$000FFF3C_H$	—
Reserved	49	31			338_H	$000FFF38_H$	—
Reserved	50	32	ICR17	451_H	334_H	$000FFF34_H$	—
Reserved	51	33			330_H	$000FFF30_H$	—
Reserved	52	34	ICR18	452_H	$32C_H$	$000FFF2C_H$	—
Reserved	53	35			328_H	$000FFF28_H$	—
LIN-USART 0 RX	54	36	ICR19	453_H	324_H	$000FFF24_H$	6, 48
LIN-USART 0 TX	55	37			320_H	$000FFF20_H$	7, 49
Reserved	56	38	ICR20	454_H	$31C_H$	$000FFF1C_H$	8, 50
Reserved	57	39			318_H	$000FFF18_H$	9, 51
LIN-USART 2 RX	58	3A	ICR21	455_H	314_H	$000FFF14_H$	52
LIN-USART 2 TX	59	3B			310_H	$000FFF10_H$	53
LIN-USART 3 RX	60	3C	ICR22	456_H	$30C_H$	$000FFF0C_H$	54
LIN-USART 3 TX	61	3D			308_H	$000FFF08_H$	55
System Reserved	62	3E	ICR23 *3	457_H	304_H	$000FFF04_H$	—
Delayed Interrupt	63	3F			300_H	$000FFF00_H$	—
System Reserved *4	64	40	ICR24	458_H	$2FC_H$	$000FFEFC_H$	—
System Reserved *4	65	41			$2F8_H$	$000FFEF8_H$	—
LIN-USART (FIFO) 4 RX	66	42	ICR25	459_H	$2F4_H$	$000FFEF4_H$	10, 56
LIN-USART (FIFO) 4 TX	67	43			$2F0_H$	$000FFEF0_H$	11, 57
LIN-USART (FIFO) 5 RX	68	44	ICR26	$45A_H$	$2EC_H$	$000FFEEC_H$	12, 58
LIN-USART (FIFO) 5 TX	69	45			$2E8_H$	$000FFEE8_H$	13, 59

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
LIN-USART (FIFO) 6 RX	70	46	ICR27	$45B_H$	$2E4_H$	$000FFEE4_H$	60
LIN-USART (FIFO) 6 TX	71	47			$2E0_H$	$000FFEE0_H$	61
LIN-USART (FIFO) 7 RX	72	48	ICR28	$45C_H$	$2DC_H$	$000FFEDC_H$	62
LIN-USART (FIFO) 7 TX	73	49			$2D8_H$	$000FFED8_H$	63
I^2C 0	74	4A	ICR29	$45D_H$	$2D4_H$	$000FFED4_H$	—
I^2C 1	75	4B			$2D0_H$	$000FFED0_H$	—
Reserved	76	4C	ICR30	$45E_H$	$2CC_H$	$000FFECC_H$	64
Reserved	77	4D			$2C8_H$	$000FFEC8_H$	65
Reserved	78	4E	ICR31	$45F_H$	$2C4_H$	$000FFEC4_H$	66
Reserved	79	4F			$2C0_H$	$000FFEC0_H$	67
Reserved	80	50	ICR32	460_H	$2BC_H$	$000FFEBC_H$	68
Reserved	81	51			$2B8_H$	$000FFEB8_H$	69
Reserved	82	52	ICR33	461_H	$2B4_H$	$000FFEB4_H$	70
Reserved	83	53			$2B0_H$	$000FFEB0_H$	71
Reserved	84	54	ICR34	462_H	$2AC_H$	$000FFEAC_H$	72
Reserved	85	55			$2A8_H$	$000FFEA8_H$	73
Reserved	86	56	ICR35	463_H	$2A4_H$	$000FFEA4_H$	74
Reserved	87	57			$2A0_H$	$000FFEA0_H$	75
Reserved	88	58	ICR36	464_H	$29C_H$	$000FFE9C_H$	76
Reserved	89	59			298_H	$000FFE98_H$	77
Reserved	90	5A	ICR37	465_H	294_H	$000FFE94_H$	78
Reserved	91	5B			290_H	$000FFE90_H$	79
Input Capture 0	92	5C	ICR38	466_H	$28C_H$	$000FFE8C_H$	80
Input Capture 1	93	5D			288_H	$000FFE88_H$	81
Input Capture 2	94	5E	ICR39	467_H	284_H	$000FFE84_H$	82
Input Capture 3	95	5F			280_H	$000FFE80_H$	83
Input Capture 4	96	60	ICR40	468_H	$27C_H$	$000FFE7C_H$	84
Input Capture 5	97	61			278_H	$000FFE78_H$	85
Input Capture 6	98	62	ICR41	469_H	274_H	$000FFE74_H$	86
Input Capture 7	99	63			270_H	$000FFE70_H$	87
Output Compare 0	100	64	ICR42	$46A_H$	$26C_H$	$000FFE6C_H$	88
Output Compare 1	101	65			268_H	$000FFE68_H$	89
Output Compare 2	102	66	ICR43	$46B_H$	264_H	$000FFE64_H$	90
Output Compare 3	103	67			260_H	$000FFE60_H$	91
Output Compare 4	104	68	ICR44	$46C_H$	$25C_H$	$000FFE5C_H$	92
Output Compare 5	105	69			258_H	$000FFE58_H$	93

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
Output Compare 6	106	6A	ICR45	$46D_H$	254_H	$000FFE54_H$	94
Output Compare 7	107	6B			250_H	$000FFE50_H$	95
Sound Generator	108	6C	ICR46	$46E_H$	$24C_H$	$000FFE4C_H$	—
Reserved	109	6D			248_H	$000FFE48_H$	—
System Reserved	110	6E	ICR47 *3	$46F_H$	244_H	$000FFE44_H$	—
System Reserved	111	6F			240_H	$000FFE40_H$	—
PPG 0	112	70	ICR48	470_H	$23C_H$	$000FFE3C_H$	15, 96
PPG 1	113	71			238_H	$000FFE38_H$	97
PPG 2	114	72	ICR49	471_H	234_H	$000FFE34_H$	98
PPG 3	115	73			230_H	$000FFE30_H$	99
PPG 4	116	74	ICR50	472_H	$22C_H$	$000FFE2C_H$	100
PPG 5	117	75			228_H	$000FFE28_H$	101
PPG 6	118	76	ICR51	473_H	224_H	$000FFE24_H$	102
PPG 7	119	77			220_H	$000FFE20_H$	103
PPG 8	120	78	ICR52	474_H	$21C_H$	$000FFE1C_H$	104
PPG 9	121	79			218_H	$000FFE18_H$	105
PPG 10	122	7A	ICR53	475_H	214_H	$000FFE14_H$	106
PPG 11	123	7B			210_H	$000FFE10_H$	107
PPG 12	124	7C	ICR54	476_H	$20C_H$	$000FFE0C_H$	108
PPG 13	125	7D			208_H	$000FFE08_H$	109
PPG 14	126	7E	ICR55	477_H	204_H	$000FFE04_H$	110
PPG 15	127	7F			200_H	$000FFE00_H$	111
Up/Down Counter 0	128	80	ICR56	478_H	$1FC_H$	$000FFDFC_H$	—
Up/Down Counter 1	129	81			$1F8_H$	$000FFDF8_H$	—
Reserved	130	82	ICR57	479_H	$1F4_H$	$000FFDF4_H$	—
Reserved	131	83			$1F0_H$	$000FFDF0_H$	—
Real Time Clock	132	84	ICR58	$47A_H$	$1EC_H$	$000FFDEC_H$	—
Calibration Unit	133	85			$1E8_H$	$000FFDE8_H$	—
A/D Converter 0	134	86	ICR59	$47B_H$	$1E4_H$	$000FFDE4_H$	14, 112
System reserved	135	87			$1E0_H$	$000FFDE0_H$	—
Alarm Comparator 0	136	88	ICR60	$47C_H$	$1DC_H$	$000FFDDC_H$	—
Reserved	137	89			$1D8_H$	$000FFDD8_H$	—
Low Voltage Detection	138	8A	ICR61	$47D_H$	$1D4_H$	$000FFDD4_H$	—
Reserved	139	8B			$1D0_H$	$000FFDD0_H$	—
Time base Overflow	140	8C	ICR62	$47E_H$	$1CC_H$	$000FFDCC_H$	—
PLL Clock Gear	141	8D			$1C8_H$	$000FFDC8_H$	—

Interrupt	Interrupt number		Interrupt level *1		Interrupt vector *2		DMA Resource number
	Decimal	Hexa-decimal	Setting Register	Register address	Offset	Default vector address	
DMA Controller	142	8E	ICR63	$47F_H$	$1C4_H$	$000FFDC4_H$	—
Main/Sub OSC stability wait	143	8F			$1C0_H$	$000FFDC0_H$	—
Security vector	144	90	—	—	$1BC_H$	$000FFDBC_H$	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	$1B8_H$ to 000_H	$000FFDB8_H$ to $000FFC00_H$	—

*1 : The Interrupt Control Registers (ICRs) are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value ($000FFC00_H$) . The TBR is initialized to this value by a reset. The TBR is set to $000FFC00_H$ after the internal boot ROM is executed.

*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr $0C03_H$: IOS[0])

*4 : Used by REALOS

*5 : Memory Protection Unit (MPU) support

14. Recommended Settings

14.1 PLL and Clockgear Settings

Please note that for CY91F464HB the core base clock frequencies are valid in the 1.8 V operation mode of the Main regulator and Flash.

Please refer to “Absolute maximum ratings” on page 77 to find the maximum allowed frequency of Core Base Clock (f_{CLKB}) at high temperature.

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	*1
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

*1. This setting is not possible at CY91F466HA.

14.2 Clock Modulator Settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32 MHz up to 88 MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Please refer to “Absolute maximum ratings” on page 77 to find the maximum allowed frequency of Fmax (f_{CLKB}) at high temperature.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	88	79.5	98.5	*1
1	3	026F	84	76.1	93.8	
1	3	026F	80	72.6	89.1	
1	5	02AE	80	68.7	95.8	
2	3	046E	80	68.7	95.8	
1	3	026F	76	69.1	84.5	
1	5	02AE	76	65.3	90.8	
1	7	02ED	76	62	98.1	*1
2	3	046E	76	65.3	90.8	
3	3	066D	76	62	98.1	*1
1	3	026F	72	65.5	79.9	
1	5	02AE	72	62	85.8	
1	7	02ED	72	58.8	92.7	
2	3	046E	72	62	85.8	
3	3	066D	72	58.8	92.7	
1	3	026F	68	62	75.3	
1	5	02AE	68	58.7	80.9	
1	7	02ED	68	55.7	87.3	
1	9	032C	68	53	95	
2	3	046E	68	58.7	80.9	
2	5	04AC	68	53	95	
3	3	066D	68	55.7	87.3	
4	3	086C	68	53	95	
1	3	026F	64	58.5	70.7	
1	5	02AE	64	55.3	75.9	
1	7	02ED	64	52.5	82	
1	9	032C	64	49.9	89.1	
1	11	036B	64	47.6	97.6	*1
2	3	046E	64	55.3	75.9	
2	5	04AC	64	49.9	89.1	
3	3	066D	64	52.5	82	
4	3	086C	64	49.9	89.1	
5	3	0A6B	64	47.6	97.6	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	60	54.9	66.1	
1	5	02AE	60	51.9	71	
1	7	02ED	60	49.3	76.7	
1	9	032C	60	46.9	83.3	
1	11	036B	60	44.7	91.3	
2	3	046E	60	51.9	71	
2	5	04AC	60	46.9	83.3	
3	3	066D	60	49.3	76.7	
4	3	086C	60	46.9	83.3	
5	3	0A6B	60	44.7	91.3	
1	3	026F	56	51.4	61.6	
1	5	02AE	56	48.6	66.1	
1	7	02ED	56	46.1	71.4	
1	9	032C	56	43.8	77.6	
1	11	036B	56	41.8	84.9	
1	13	03AA	56	39.9	93.8	
2	3	046E	56	48.6	66.1	
2	5	04AC	56	43.8	77.6	
2	7	04EA	56	39.9	93.8	
3	3	066D	56	46.1	71.4	
3	5	06AA	56	39.9	93.8	
4	3	086C	56	43.8	77.6	
5	3	0A6B	56	41.8	84.9	
6	3	0C6A	56	39.9	93.8	
1	3	026F	52	47.8	57	
1	5	02AE	52	45.2	61.2	
1	7	02ED	52	42.9	66.1	
1	9	032C	52	40.8	71.8	
1	11	036B	52	38.8	78.6	
1	13	03AA	52	37.1	86.8	
1	15	03E9	52	35.5	96.9	*1
2	3	046E	52	45.2	61.2	
2	5	04AC	52	40.8	71.8	
2	7	04EA	52	37.1	86.8	
3	3	066D	52	42.9	66.1	
3	5	06AA	52	37.1	86.8	
4	3	086C	52	40.8	71.8	
5	3	0A6B	52	38.8	78.6	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
6	3	0C6A	52	37.1	86.8	
7	3	0E69	52	35.5	96.9	*1
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	
1	15	03E9	48	32.8	89.1	
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	
2	7	04EA	44	31.5	73	
2	9	0528	44	28.9	92.1	
3	3	066D	44	36.4	55.7	
3	5	06AA	44	31.5	73	
4	3	086C	44	34.6	60.4	
4	5	08A8	44	28.9	92.1	
5	3	0A6B	44	33	66.1	
6	3	0C6A	44	31.5	73	
7	3	0E69	44	30.1	81.4	
8	3	1068	44	28.9	92.1	
1	3	026F	40	37	43.6	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	5	02AE	40	34.9	46.8	
1	7	02ED	40	33.1	50.5	
1	9	032C	40	31.5	54.8	
1	11	036B	40	30	59.9	
1	13	03AA	40	28.7	66.1	
1	15	03E9	40	27.4	73.7	
2	3	046E	40	34.9	46.8	
2	5	04AC	40	31.5	54.8	
2	7	04EA	40	28.7	66.1	
2	9	0528	40	26.3	83.3	
3	3	066D	40	33.1	50.5	
3	5	06AA	40	28.7	66.1	
3	7	06E7	40	25.3	95.8	
4	3	086C	40	31.5	54.8	
4	5	08A8	40	26.3	83.3	
5	3	0A6B	40	30	59.9	
6	3	0C6A	40	28.7	66.1	
7	3	0E69	40	27.4	73.7	
8	3	1068	40	26.3	83.3	
9	3	1267	40	25.3	95.8	
1	3	026F	36	33.3	39.2	
1	5	02AE	36	31.5	42	
1	7	02ED	36	29.9	45.3	
1	9	032C	36	28.4	49.2	
1	11	036B	36	27.1	53.8	
1	13	03AA	36	25.8	59.3	
1	15	03E9	36	24.7	66.1	
2	3	046E	36	31.5	42	
2	5	04AC	36	28.4	49.2	
2	7	04EA	36	25.8	59.3	
2	9	0528	36	23.7	74.7	
3	3	066D	36	29.9	45.3	
3	5	06AA	36	25.8	59.3	
3	7	06E7	36	22.8	85.8	
4	3	086C	36	28.4	49.2	
4	5	08A8	36	23.7	74.7	
5	3	0A6B	36	27.1	53.8	
6	3	0C6A	36	25.8	59.3	

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
7	3	0E69	36	24.7	66.1	
8	3	1068	36	23.7	74.7	
9	3	1267	36	22.8	85.8	
1	3	026F	32	29.7	34.7	
1	5	02AE	32	28	37.3	
1	7	02ED	32	26.6	40.2	
1	9	032C	32	25.3	43.6	
1	11	036B	32	24.1	47.7	
1	13	03AA	32	23	52.5	
1	15	03E9	32	22	58.6	
2	3	046E	32	28	37.3	
2	5	04AC	32	25.3	43.6	
2	7	04EA	32	23	52.5	
2	9	0528	32	21.1	66.1	
2	11	0566	32	19.5	89.1	
3	3	066D	32	26.6	40.2	
3	5	06AA	32	23	52.5	
3	7	06E7	32	20.3	75.9	
4	3	086C	32	25.3	43.6	
4	5	08A8	32	21.1	66.1	
5	3	0A6B	32	24.1	47.7	
5	5	0AA6	32	19.5	89.1	
6	3	0C6A	32	23	52.5	
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	

*1. These settings are not possible at CY91F466HA.

15. Electrical Characteristics

15.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	—	—	50	V/ms	
Power supply voltage 1 *1	$V_{DD}5R$	- 0.3	+ 6.0	V	
Power supply voltage 2 *1	$V_{DD}5$	- 0.3	+ 6.0	V	
Relationship of the supply voltages	$AV_{CC}5$	$V_{DD}5$-0.3 $V_{DD}35$-0.3	$V_{DD}5$+0.3 $V_{DD}35$+0.3	V	At least one pin of the Ports 26 to 29 (ANn) is used as digital input or output.
		$V_{SS}5$-0.3 $V_{DD}35$-0.3	$V_{DD}5$+0.3 $V_{DD}35$+0.3	V	All pins of the Ports 26 to 29 (ANn) follow the condition of V_{IA}
Analog power supply voltage *1	$AV_{CC}5$	- 0.3	+ 6.0	V	*2
Analog reference power supply voltage *1	AVRH	- 0.3	+ 6.0	V	*2
Input voltage 1 *1	V_{I1}	Vss5 - 0.3	$V_{DD}5$ + 0.3	V	
Analog pin input voltage *1	V_{IA}	AVss5 - 0.3	AVcc5 + 0.3	V	
Output voltage 1 *1	V_{O1}	Vss5 - 0.3	$V_{DD}5$ + 0.3	V	
Maximum clamp current	I_{CLAMP}	- 4.0	+ 4.0	mA	*3
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*3
“L” level maximum output current *4	I_{OL}	—	10	mA	
“L” level average output current *5	I_{OLAV}	—	8	mA	
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current *6	ΣI_{OLAV}	—	50	mA	
“H” level maximum output current *4	I_{OH}	—	- 10	mA	
“H” level average output current *5	I_{OHAV}	—	- 4	mA	
“H” level total maximum output current	ΣI_{OH}	—	- 100	mA	
“H” level total average output current *6	ΣI_{OHAV}	—	- 25	mA	
Permitted operating frequency CY91F464HB	$f_{max, CLKB}$	—	100	MHz	$T_A \leq 105$ °C
	$f_{max, CLKP}$	—	50		
	$f_{max, CLKT}$	—	50		
	$f_{max, CLKCAN}$	—	50		
	$f_{max, CLKB}$	—	96	MHz	$T_A \leq 125$ °C
	$f_{max, CLKP}$	—	48		
	$f_{max, CLKT}$	—	48		
	$f_{max, CLKCAN}$	—	48		

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Permitted operating frequency CY91F466HA	$f_{max, CLKB}$	—	96	MHz	$T_A \leq 105$ °C
	$f_{max, CLKP}$	—	48		
	$f_{max, CLKT}$	—	48		
	$f_{max, CLKCAN}$	—	48		
	$f_{max, CLKB}$	—	92	MHz	$T_A \leq 125$ °C
	$f_{max, CLKP}$	—	46		
	$f_{max, CLKT}$	—	46		
	$f_{max, CLKCAN}$	—	46		
Permitted power dissipation *7	P_D	—	1200 *8	mW	$T_A \leq 85$ °C
		—	600 *8		$T_A \leq 105$ °C
		—	1300 *8		$T_A \leq 105$ °C, no Flash program/erase *9
		—	1000 *8		$T_A \leq 115$ °C, no Flash program/erase *9
		—	750 *8		$T_A \leq 125$ °C, no Flash program/erase *9
Operating temperature	T_A	- 40	+ 125	°C	
Storage temperature	Tstg	- 55	+ 150	°C	

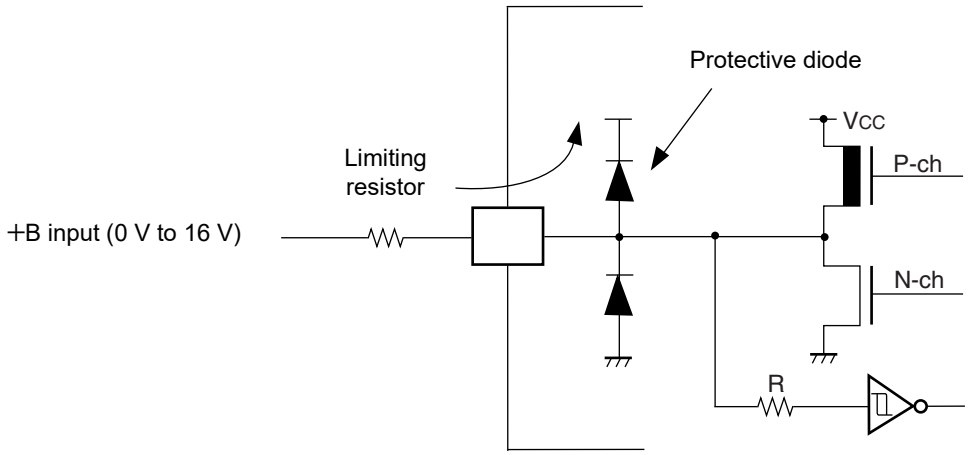
*1 : The parameter is based on $V_{SS}5 = AV_{SS}5 = 0.0$ V.

*2 : $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V.

*3 :
- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time, either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.

• Do not leave +B input pins open.
• Example of recommended circuit :

Input/output equivalent circuit



*4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.

*6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

*7 : The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} * I_{OL} + V_{OH} * I_{OH})$ (IO load power dissipation, sum is performed on all IO ports)
$P_{INT} = V_{DD}5R * I_{CC} + AV_{CC}5 * IA + AVRH5 * IR$ (internal power dissipation)

*8 : Worst case value for the QFP package mounted on a 4-layer PCB at specified TA without air flow.

*9 : Please contact Fujitsu for reliability limitations when using under these conditions.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

15.2 Recommended Operating Conditions

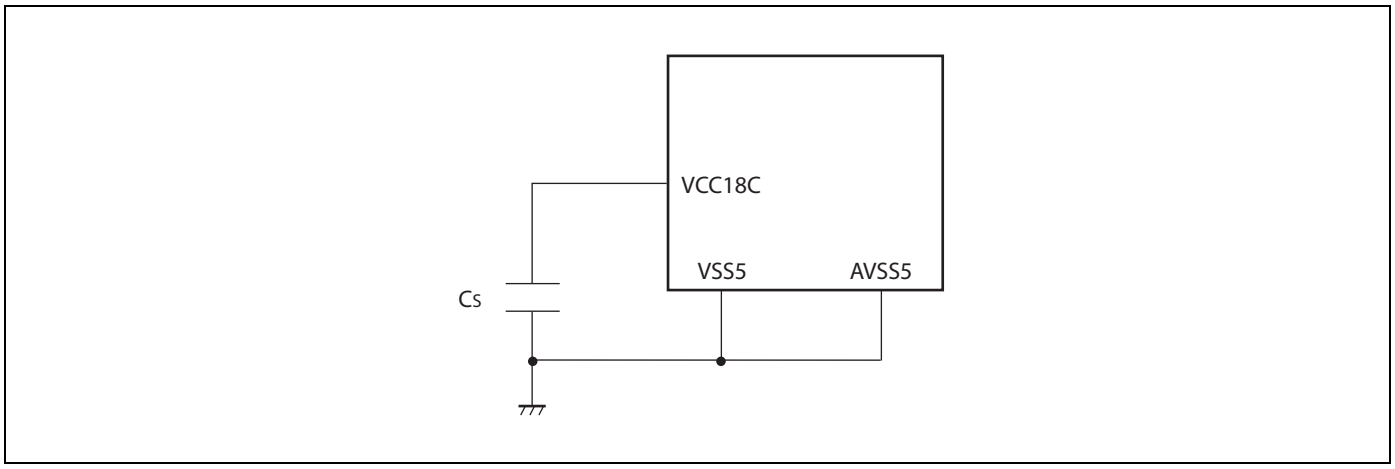
($V_{SS}5 = AV_{SS}5 = 0.0$ V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0	—	5.5	V	
	$V_{DD}5R$	3.0	—	5.5	V	Internal regulator
	$AV_{CC}5$	3.0	—	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	—	4.7	—	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		—	—	50	V/ms	
Operating temperature	T_A	- 40	—	+ 125	°C	
Main Oscillation stabilisation time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	Vsurge	2			kV	$R_{discharge}$ = 1.5 kΩ $C_{discharge}$ = 100 pF
RC Oscillator	$f_{RC100kHz}$ f_{RC2MHz}	50 1	100 2	200 4	kHz MHz	$VDD_{CORE} \geq 1.65$ V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.



15.3 DC Characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	0.8 × V_{DD}	—	V_{DD} + 0.3	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	0.7 × V_{DD}	—	V_{DD} + 0.3	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				0.74 × V_{DD}	—	V_{DD} + 0.3	V	3 V ≤ V_{DD} < 4.5 V
		—	AUTOMOTIVE Hysteresis input is selected	0.8 × V_{DD}	—	V_{DD} + 0.3	V	
		—	Port inputs if TTL input is selected	2.0	—	V_{DD} + 0.3	V	
	V_{IHR}	INITX	—	0.8 × V_{DD}	—	V_{DD} + 0.3	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_3 to MD_0	—	V_{DD} - 0.3	—	V_{DD} + 0.3	V	Mode input pins
	V_{IHX0S}	X0, X0A	—	2.5	—	V_{DD} + 0.3	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	—	0.8 × V_{DD}	—	V_{DD} + 0.3	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	V_{SS} - 0.3	—	0.2 × V_{DD}	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	V_{SS} - 0.3	—	0.3 × V_{DD}	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	V_{SS} - 0.3	—	0.5 × V_{DD}	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				V_{SS} - 0.3	—	0.46 × V_{DD}	V	3 V ≤ V_{DD} < 4.5 V
		—	Port inputs if TTL input is selected	V_{SS} - 0.3	—	0.8	V	
	V_{ILR}	INITX	—	V_{SS} - 0.3	—	0.2 × V_{DD}	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_3 to MD_0	—	V_{SS} - 0.3	—	V_{SS} + 0.3	V	Mode input pins
	V_{ILXDS}	X0, X0A	—	V_{SS} - 0.3	—	0.5	V	External clock in "Oscillation mode"
Input "L" voltage	V_{ILXDF}	X0	—	V_{SS} - 0.3	—	0.2 × V_{DD}	V	External clock in "Fast Clock Input mode"

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output “H” voltage	V_{OH2}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, I_{OH} = - 2mA	V_{DD} - 0.5	—	—	V	Driving strength set to 2 mA
			$3.0V \le V_{DD} < 4.5V$, I_{OH} = - 1.6mA					
	V_{OH5}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, I_{OH} = - 5mA	V_{DD} - 0.5	—	—	V	Driving strength set to 5 mA
			$3.0V \le V_{DD} < 4.5V$, I_{OH} = - 3mA					
	V_{OH3}	I^2C outputs	$3.0V \le V_{DD} \le 5.5V$, I_{OH} = - 3mA	V_{DD} - 0.5	—	—	V	
Output “L” voltage	V_{OL2}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, I_{OL} = + 2mA	—	—	0.4	V	Driving strength set to 2 mA
			$3.0V \le V_{DD} < 4.5V$, I_{OL} = + 1.6mA					
	V_{OL5}	Normal outputs	$4.5V \le V_{DD} \le 5.5V$, I_{OL} = + 5mA	—	—	0.4	V	Driving strength set to 5 mA
			$3.0V \le V_{DD} < 4.5V$, I_{OL} = + 3mA					
	V_{OL3}	I^2C outputs	$3.0V \le V_{DD} \le 5.5V$, I_{OL} = + 3mA	—	—	0.4	V	
Input leakage current	I_{IL}	Pnn_m[*1]	$3.0V \le V_{DD} \le 5.5V$ $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	- 1	—	+ 1	µA	
			$3.0V \le V_{DD} \le 5.5V$ $V_{SS}5 < V_I < V_{DD}$ T_A=125 °C	- 3	—	+ 3		
Analog input leakage current	I_{AIN}	ANn[*2]	$3.0V \le V_{DD} \le 5.5V$ T_A=25 °C	- 1	—	+ 1	µA	
			$3.0V \le V_{DD} \le 5.5V$ T_A=125 °C	- 3	—	+ 3	µA	
Pull-up resistance	R_{UP}	Pnn_m[*3] INITX	$3.0V \le V_{DD} \le 3.6V$	40	100	160	kΩ	
			$4.5V \le V_{DD} \le 5.5V$	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m[*4]	$3.0V \le V_{DD} \le 3.6V$	40	100	180	kΩ	
			$4.5V \le V_{DD} \le 5.5V$	25	50	100		
Input capacitance	C_{IN}	All except $V_{DD}5$, $V_{DD}5R$, $V_{SS}5$, $AV_{CC}5$, $AV_{SS}5$, AVRH5	f = 1 MHz	—	5	15	pF	

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current CY91F464HB	I_{CC}	$V_{DD}5R$	CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	—	100	130	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	T_A = + 25 °C T_A = + 105 °C T_A = + 125 °C	— — —	30 0.3 0.75	150 2.0 5.0	µA mA mA	At stop mode*5
			T_A = + 25 °C T_A = + 105 °C T_A = + 125 °C	— — —	100 0.5 0.85	500 2.4 5.4	µA mA mA	RTC : 4 MHz mode*5
			T_A = + 25 °C T_A = + 105 °C T_A = + 125 °C	— — —	50 0.4 0.8	250 2.2 5.2	µA mA mA	RTC : 100 kHz mode*5
	I_{LVI}	$V_{DD}5R$	—	—	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	—	—	250	500	µA	Main clock (4 MHz)
			—	—	20	40	µA	Sub clock (32 kHz)
Power supply current CY91F466HA	I_{CC}	$V_{DD}5R$	CLKB: 96 MHz CLKP: 48 MHz CLKT: 48 MHz CLKCAN: 48 MHz	—	110	140	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	T_A = + 25 °C T_A = + 105 °C T_A = + 125 °C	— — —	30 0.4 1.0	150 2.0 5.0	µA mA mA	At stop mode*5
			T_A = + 25 °C T_A = + 105 °C T_A = + 125 °C	— — —	100 0.5 1.1	500 2.4 5.4	µA mA mA	RTC : 4 MHz mode*5
			T_A = + 25 °C T_A = + 105 °C T_A = + 125 °C	— — —	50 0.45 1.05	250 2.2 5.2	µA mA mA	RTC : 100 kHz mode*5
	I_{LVE}	$V_{DD}5$	—	—	70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD}5R$	—	—	50	100	µA	Internal low voltage detection
	I_{OSC}	$V_{DD}5$	—	—	250	500	µA	Main clock (4 MHz)
			—	—	20	40	µA	Sub clock (32 kHz)

*1. Pnn_m includes all GPIO pins. Analog (AN) channels and PullUp/PullDown are disabled.
*2. ANn includes all pins where AN channels are enabled.
*3. Pnn_m includes all GPIO pins. The pull up resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
*4. Pnn_m includes all GPIO pins. The pull down resistors must be enabled by PPER/PPCR setting and the pins must be in input direction.
*5. Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.

15.4 A/D Converter Characteristics

($V_{DD}5$ = $AV_{CC}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40°C to + 125°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	- 3	—	+ 3	LSB	
Nonlinearity error	—	—	- 2.5	—	+ 2.5	LSB	
Differential nonlinearity error	—	—	- 1.9	—	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL–1.5	AVRL + 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	ANn	AVRH–3.5	AVRH–1.5	AVRH + 0.5	LSB	
Compare time	T_{comp}	—	0.6	—	16,500	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	—	0.4	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	—	1.0	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	—	—	11	pF	
Input resistance	R_{IN}	ANn	—	—	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			—	—	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	- 1	—	+ 1	µA	T_A = + 25°C
			- 3	—	+ 3	µA	T_A = + 125°C
Analog input voltage range	V_{AIN}	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	4	LSB	
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$	—	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	—	$AV_{CC}5$ × 0.25	V	
Power supply current per ADC macro *3	I_A	$AV_{CC}5$	—	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	—	—	5	µA	A/D Converter not operated *1
Reference voltage current per ADC macro *3	I_R	AVRH5	—	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	—	—	5	µA	A/D Converter not operated *2

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

*1 : Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5$ = $AV_{CC}5$ = AVRH = 5.0 V)

*2 : Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5$ = $AV_{CC}5$ = AVRH = 5.0 V)

*3 : The current consumption per ADC macro is given here. On devices having more then one A/D converter, the current values have to be multiplied by the number of macros.

Sampling Time Calculation
T_{samp} = (2.6 kOhm + R_{EXT}) × 11pF × 7; for 4.5V ≤ $AV_{CC}5$ ≤ 5.5V
T_{samp} = (12.1 kOhm + R_{EXT}) × 11pF × 7; for 3.0V ≤ $AV_{CC}5$ < 4.5V

Conversion Time Calculation
$T_{conv} = T_{samp} + T_{comp}$

Definition of A/D converter terms

■ Resolution

Analog variation that is recognizable by the A/D converter.

■ Nonlinearity error

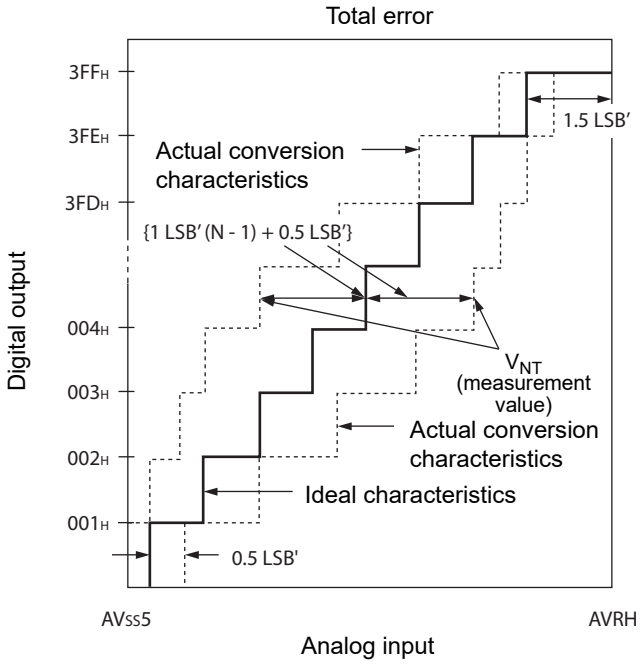
Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).

■ Differential nonlinearity error

Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

■ Total error

This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.



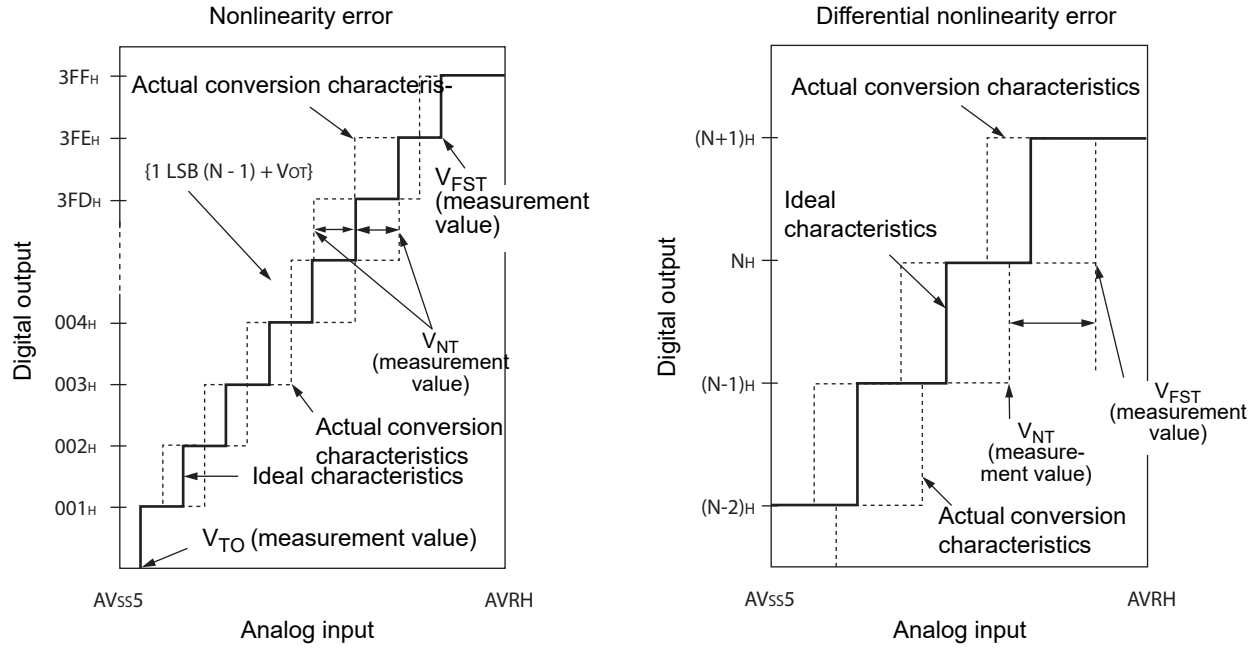
$$1LSB'\ (\text{ideal value}) = \frac{AVRH - AV_{SS}5}{1024}\ [V]$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$$

N : A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5 + 0.5\ LSB'$ [V]
V_{FST}' (ideal value) = $AVRH - 1.5\ LSB'$ [V]
V_{NT} : Voltage at which the digital output changes from $(N + 1)_H$ to N_H

(Continued)

(Continued)



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

15.5 Alarm Comparator Characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	$AV_{CC}5$	—	25	40	µA	Alarm comparator enabled in fast mode (per channel) *1
	I_{A5ALMS}		—	7	10	µA	Alarm comparator enabled in normal mode (per channel) *1
	I_{A5ALMH}		—	—	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM_n	- 1	—	+ 1	µA	T_A=25 °C
			- 3	—	+ 3	µA	T_A=125 °C
ALARM pin input voltage range	V_{ALIN}		0	—	$AV_{CC}5$	V	
Alarm upper limit voltage	V_{IAH}		$AV_{CC}5 \times 0.78$ - 3%	$AV_{CC}5 \times 0.78$	$AV_{CC}5 \times 0.78$ + 3%	V	
Alarm lower limit voltage	V_{IAL}		$AV_{CC}5 \times 0.36$ - 5%	$AV_{CC}5 \times 0.36$	$AV_{CC}5 \times 0.36$ + 5%	V	
Alarm hysteresis voltage	V_{IAHYS}		50	—	250	mV	
Alarm input resistance	R_{IN}		5	—	—	MΩ	
Comparison time	t_{COMPF}		—	0.1	0.2	µs	Alarm comparator enabled in fast mode *1
	t_{COMPS}		—	1	2	µs	Alarm comparator enabled in normal mode *1

Note: *1: The fast Alarm Comparator mode is enabled by setting ACSR.MD=1
Setting ACSR.MD=0 sets the normal mode.

15.6 FLASH Memory Program/Erase Characteristics

15.6.1 CY91F464HB

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{DD}5R$ = 3.0 V to 5.5 V, $V_{SS}5$ = 0 V, T_A = -40 °C to +105 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit or 32-bit width) programming time	-	23	370	µs	System overhead time not included
Program/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1. This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85 °C)

15.6.2 CY91F466HA

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{DD}5R$ = 3.0 V to 5.5 V, $V_{SS}5$ = 0 V, T_A = -40 °C to +105 °C)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
Chip erase time	-	n*0.5	n*2.0	s	n is the number of Flash sector of the device
Word (16-bit or 32-bit width) programming time	-	6	100	µs	System overhead time not included
Program/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1. This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85 °C)

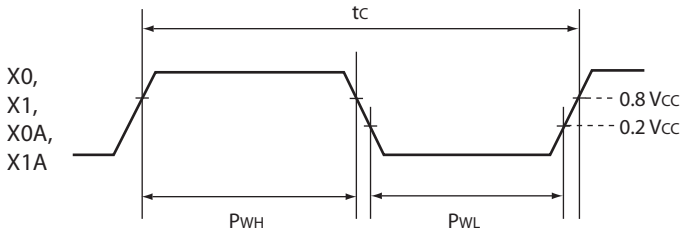
15.7 AC Characteristics

15.7.1 Clock Timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

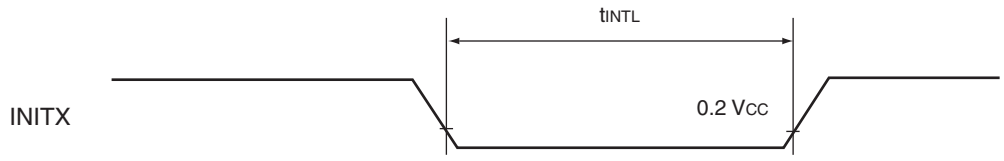
Clock timing condition



15.7.2 Reset Input Ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	8	—	ms
INITX input time (other than the above)				20	—	µs



15.7.3 LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements

  All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - T_a = -40 °C to +125 °C
  - C_l = 50 pF (load capacity value of pins when testing)
  - VOL = 0.2 x $V_{DD}5$
  - VOH = 0.8 x $V_{DD}5$
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

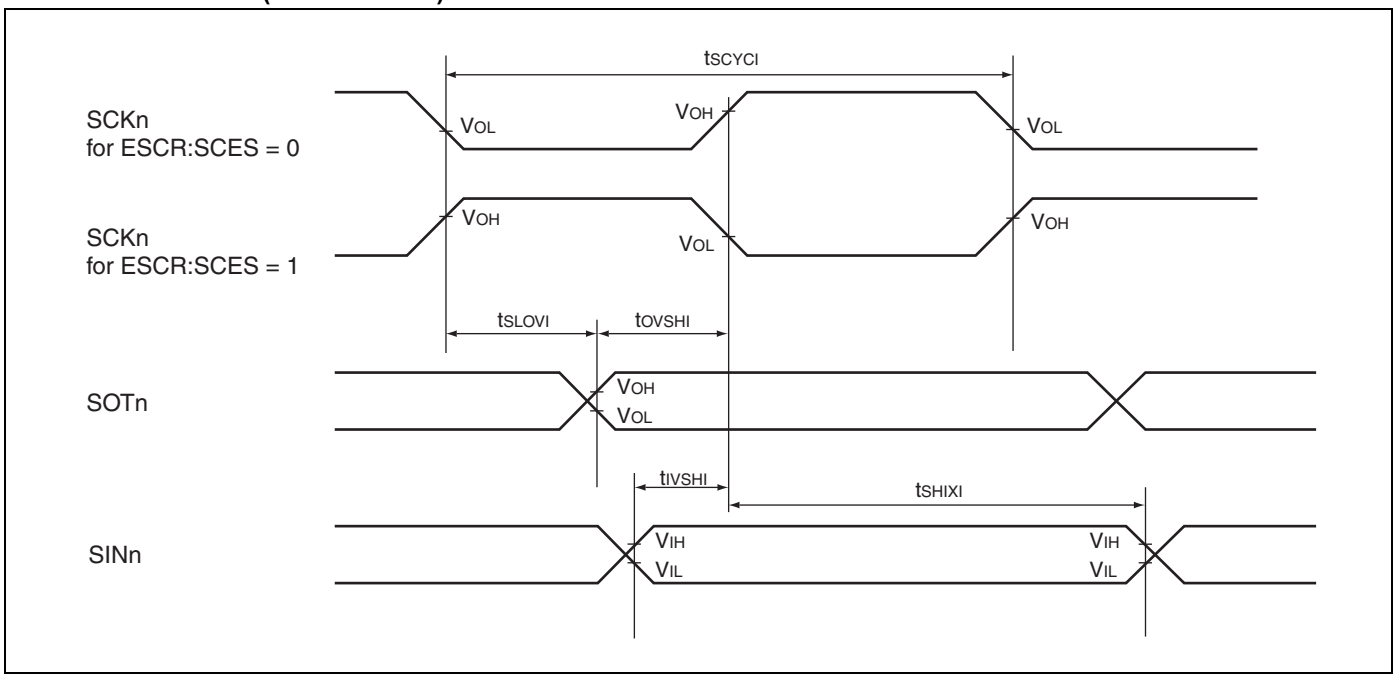
Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	—	4 t_{CLKP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		- 30	30	- 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} - 30*	—	m × t_{CLKP} - 20*	—	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	—	t_{CLKP} + 45	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	—	0	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		—	2 t_{CLKP} + 55	—	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	—	10	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK rising time	t_{FE}	SCKn		—	20	—	20	ns
SCK falling time	t_{RE}	SCKn		—	20	—	20	ns

* : Parameter m depends on t_{SCYCI} and can be calculated as :

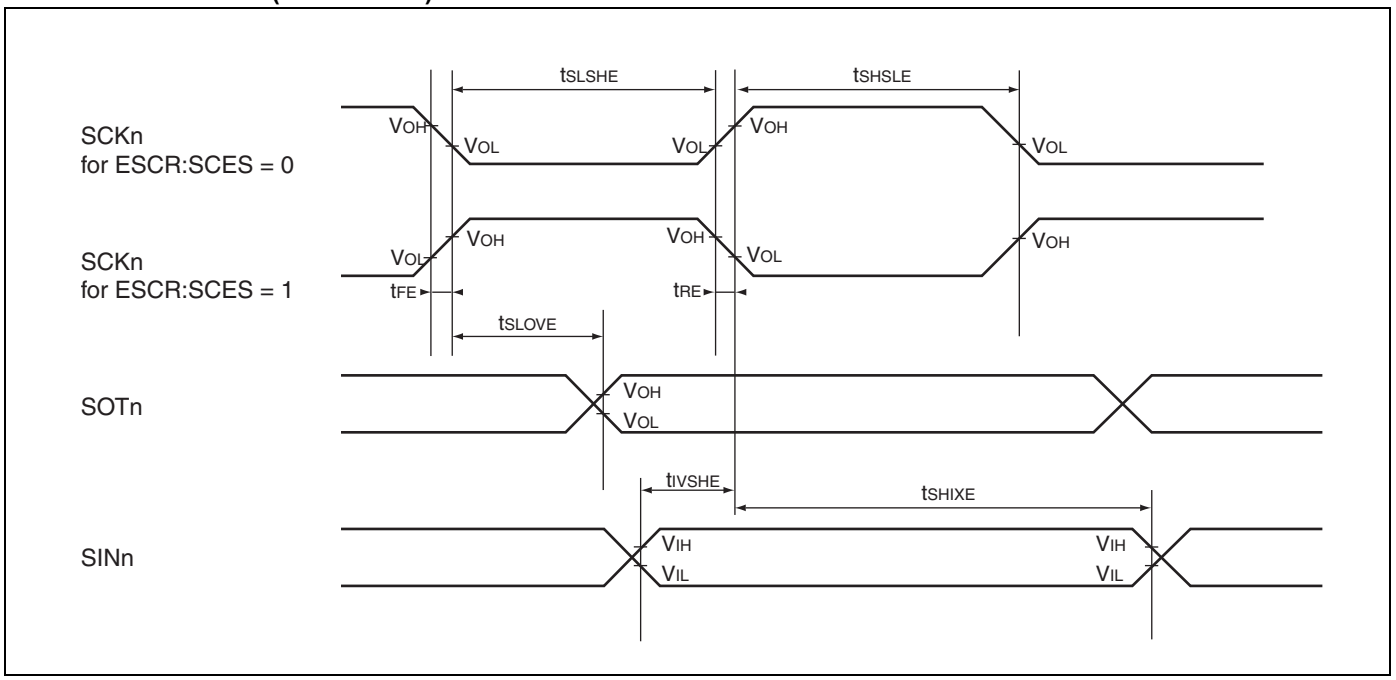
- if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2
- if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

Notes :
- The above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

Internal clock mode (master mode)



External clock mode (slave mode)



15.7.4 I^2C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements

  All AC tests were measured under the following conditions:
  - IO_{drive} = 3 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = - 40 °C to + 125 °C
  - C_l = 50 pF
  - VOL = 0.3 × $V_{DD}5$
  - VOH = 0.7 × $V_{DD}5$
  - EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

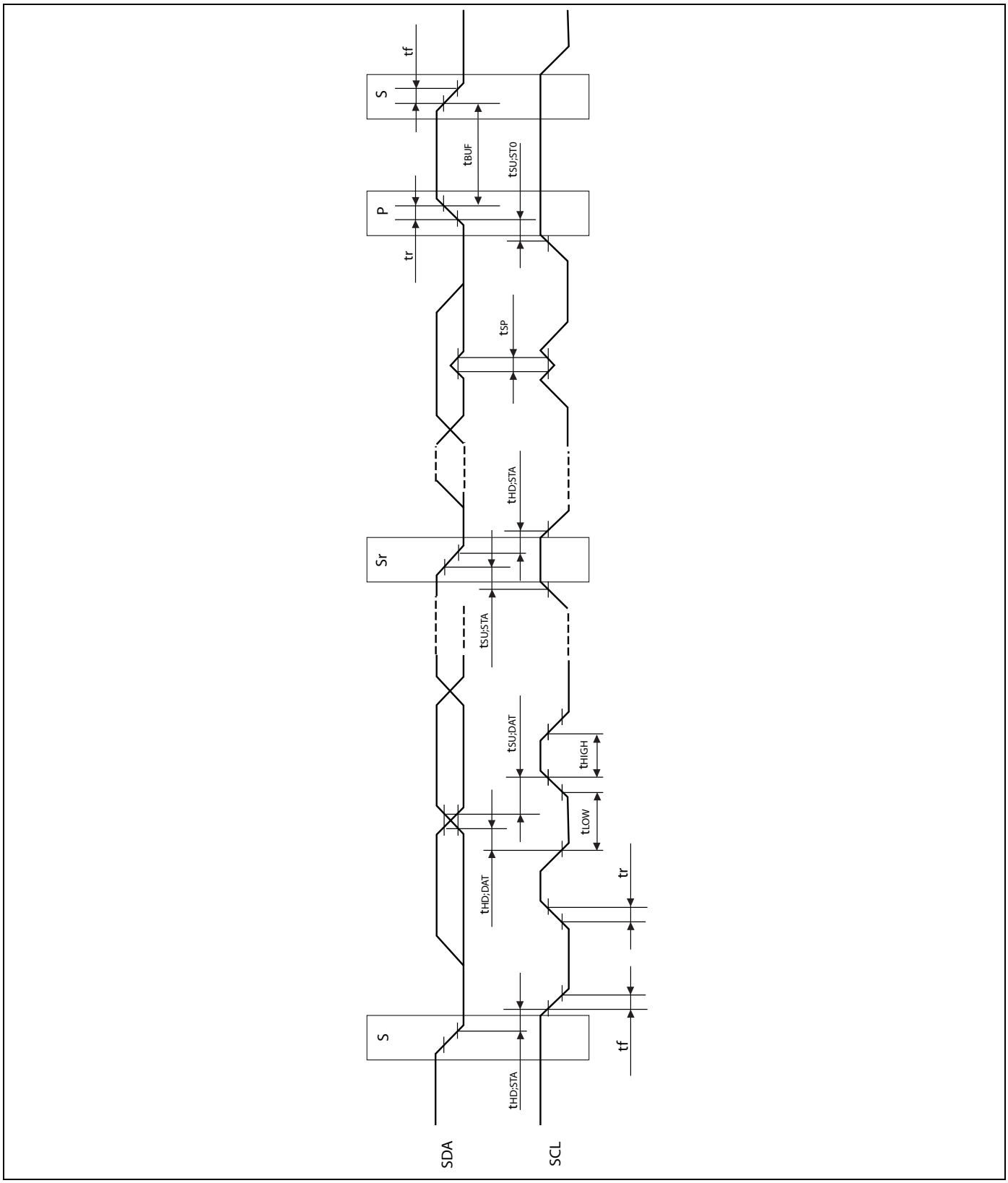
Fast mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	—	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	—	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	—	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	—	µs	
Data hold time for I^2C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	—	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	—	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*1

*1: The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I^2C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

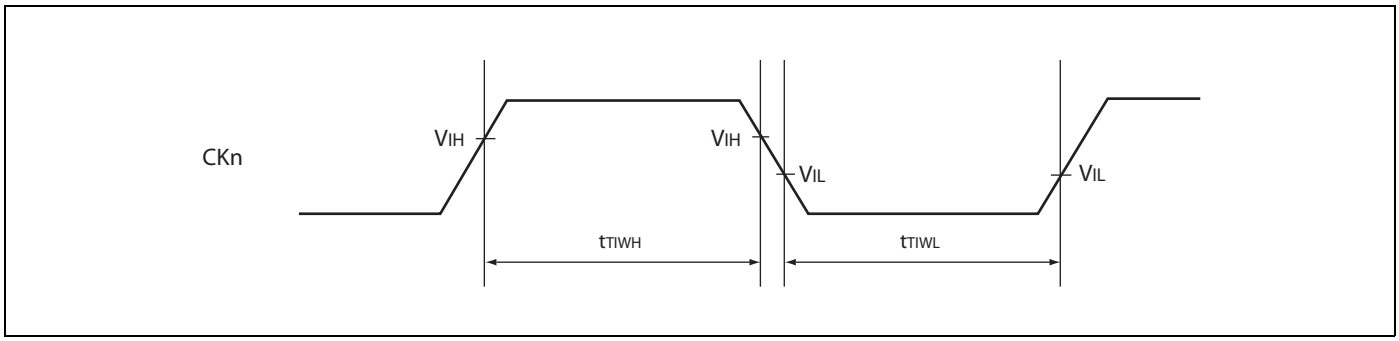

tf
S
tBUF
tSU;STO
P
tr
tSP
tHD;STA
Sr
tSU;STA
tSU;DAT
tHIGH
tLOW
tHD;DAT
tr
S
tf
tHD;STA
SDA
SCL

15.7.5 Free-run Timer Clock

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	—	$4t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.

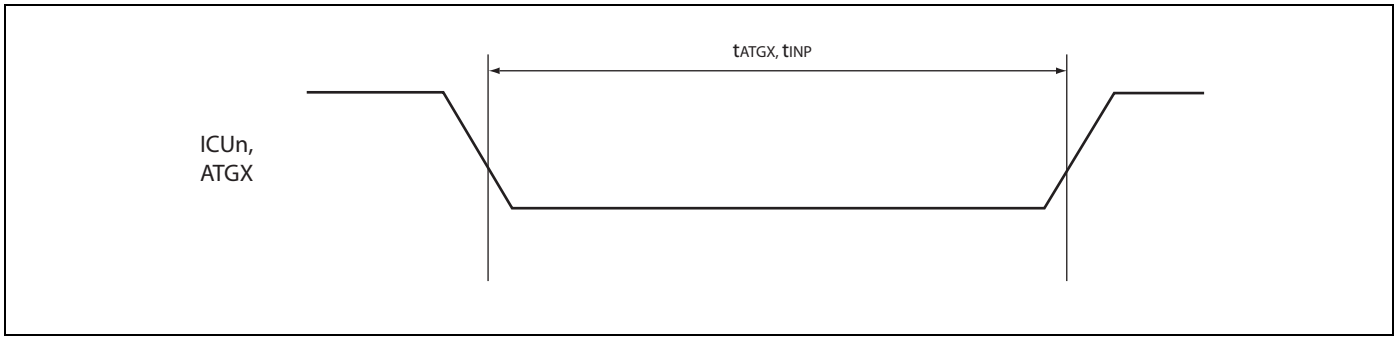


15.7.6 Trigger Input Timing

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	t_{ATGX}	ATGX	—	$5t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.



15.7.7 External Bus AC Timings at $V_{DD}35$ = 3.0 to 5.5 V

- Conditions during AC measurements

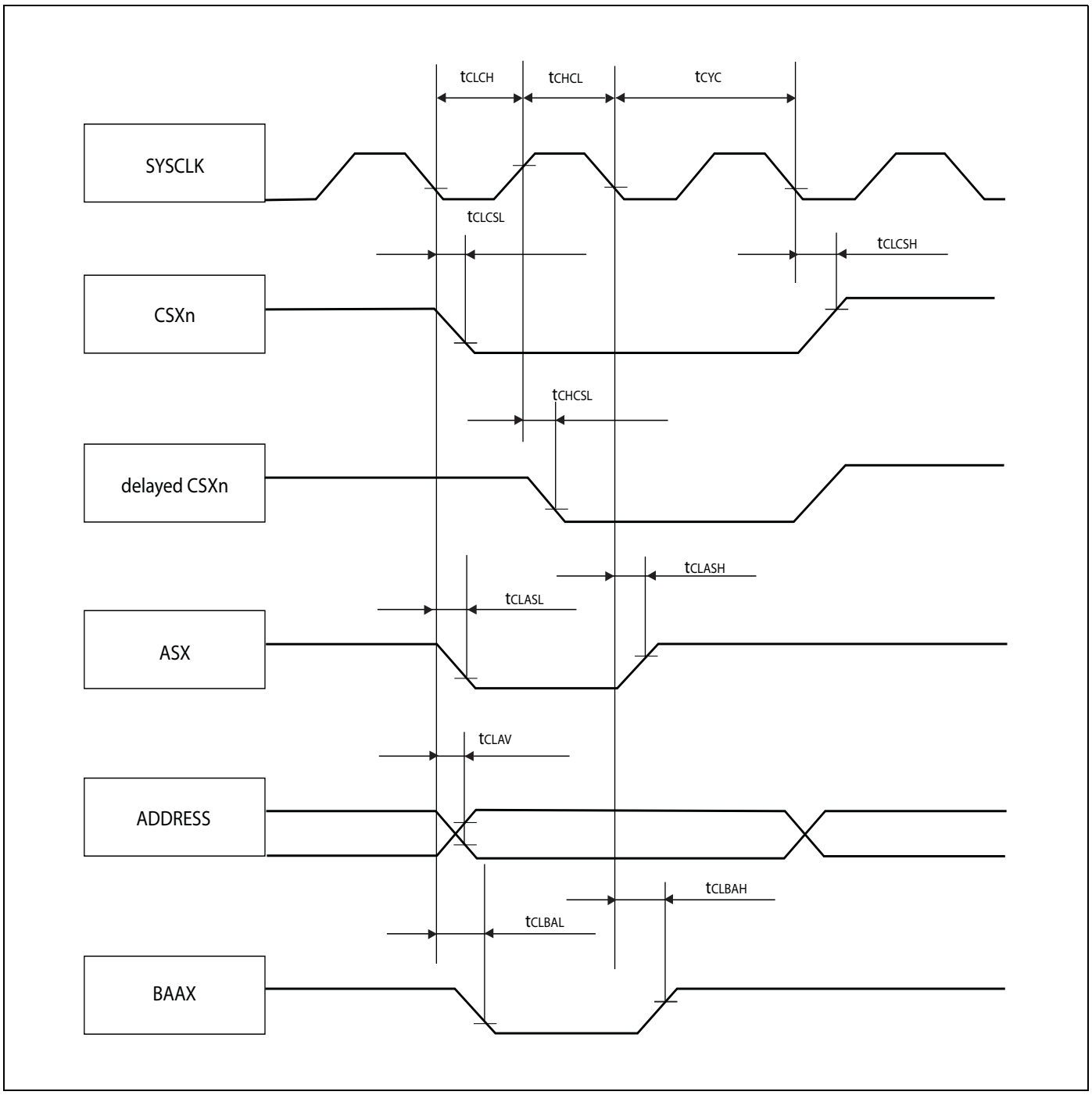
  All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = - 40 °C to + 125 °C
  - C_l = 50 pF
  - VOL = 0.5 × $V_{DD}35$
  - VOH = 0.5 × $V_{DD}35$
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

Basic Timing

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	t_{CLCH}	SYSCLK	1/2 × t_{CLKT} - 1	1/2 × t_{CLKT} + 9	ns
	t_{CHCL}		1/2 × t_{CLKT} - 9	1/2 × t_{CLKT} + 1	ns
SYSCLK ↓ to CSXn delay time	t_{CLCSL}	SYSCLK CSXn	—	8	ns
	t_{CLCSH}		—	12	ns
SYSCLK ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		- 6	+ 1	ns
SYSCLK ↓ to Address valid delay time	t_{CLAV}	SYSCLK A21 to A0	—	13	ns

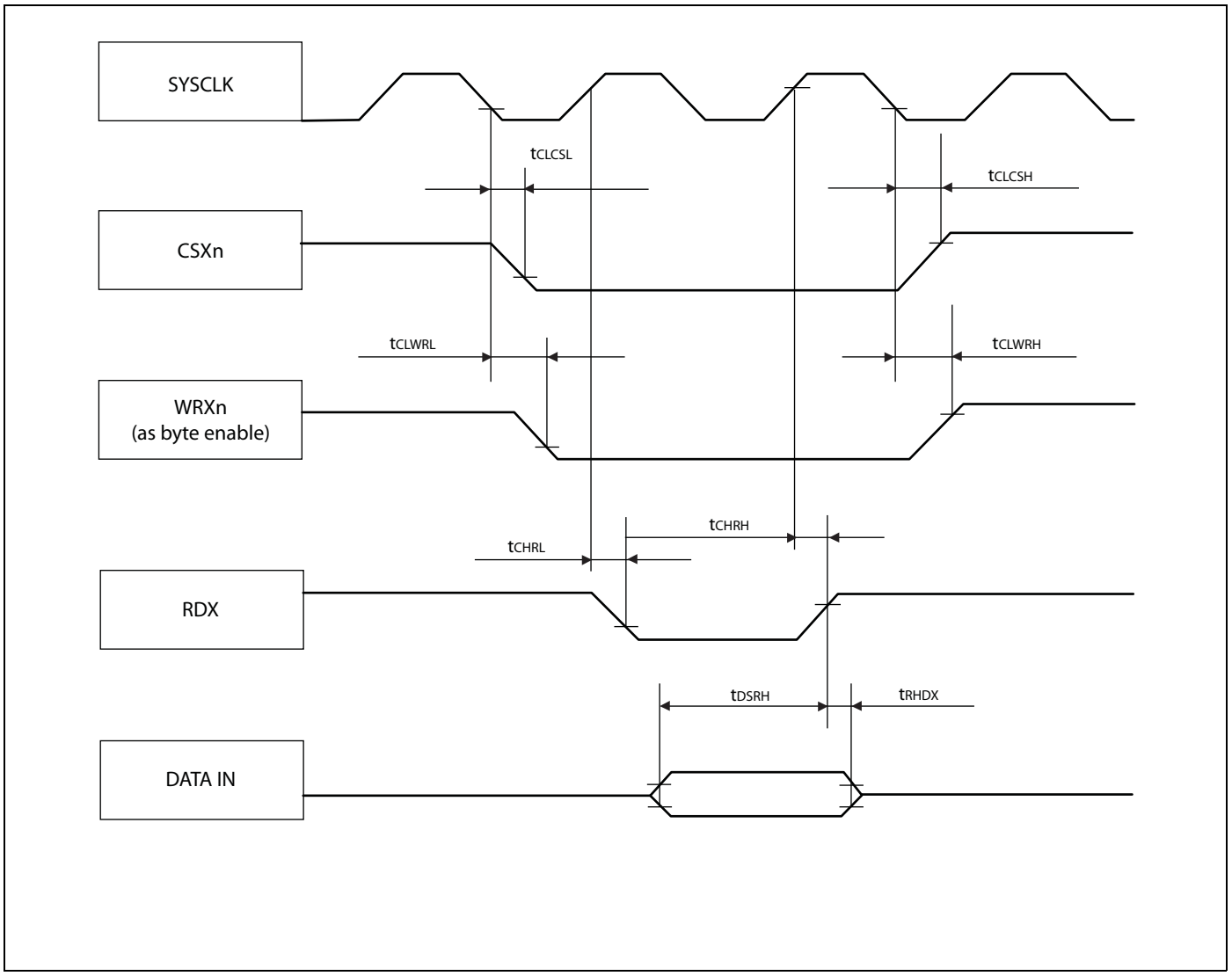
Note : t_{CLKT} is the cycle time of the external bus clock.


tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS
tCLBAH
tCLBAL
BAAX

Synchronous/Asynchronous read access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

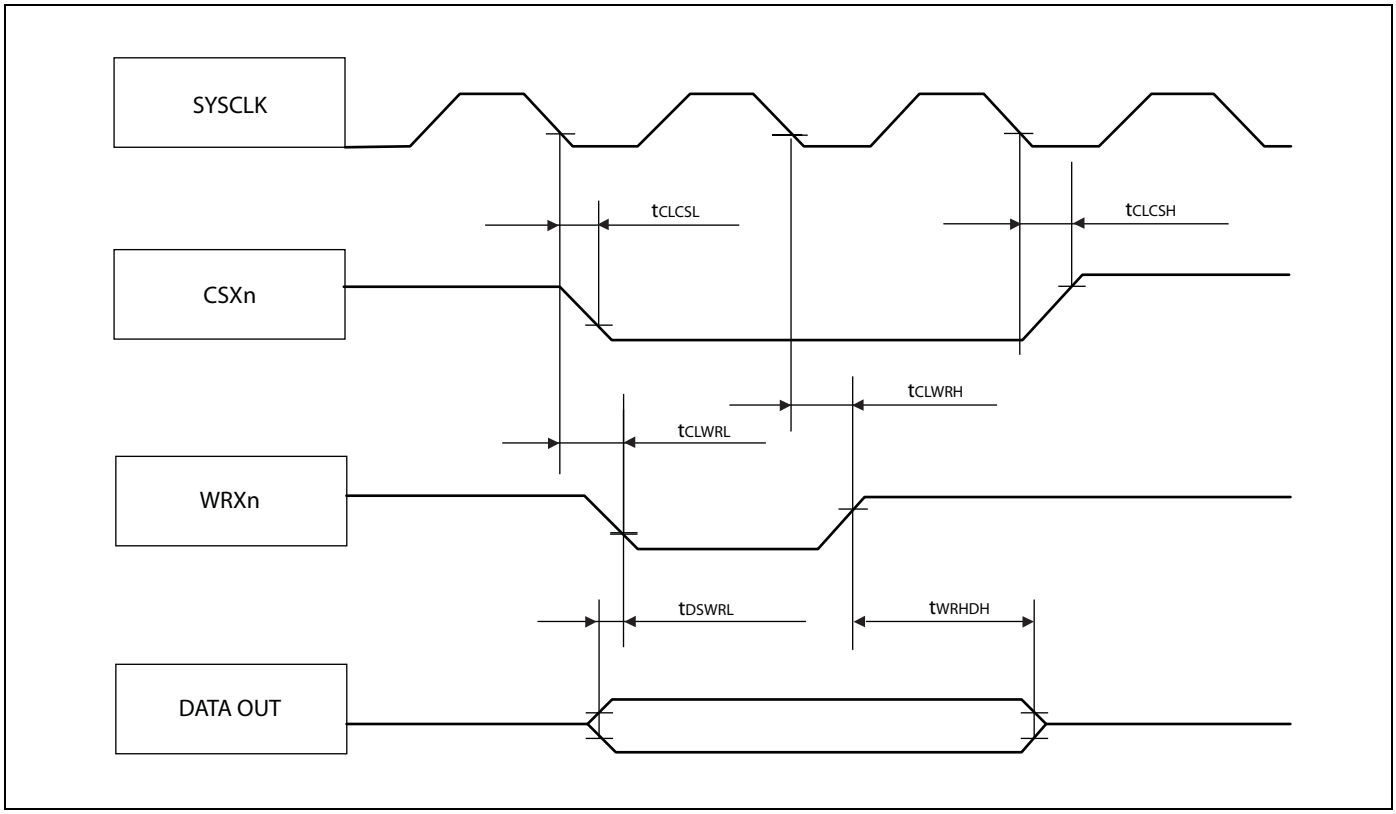
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↑ to RDX delay time	TCHRL	SYSCLK RDX	- 7	1	ns
	TCHRH		- 4	2	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D16	33	—	ns
RDX ↑ to Data valid hold time	TRHDX	RDX D31 to D16	0	—	ns
SYSCLK ↓ to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn	—	8	ns
	TCLWRH		0	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	12	ns



Synchronous write access

($V_{DD}35$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

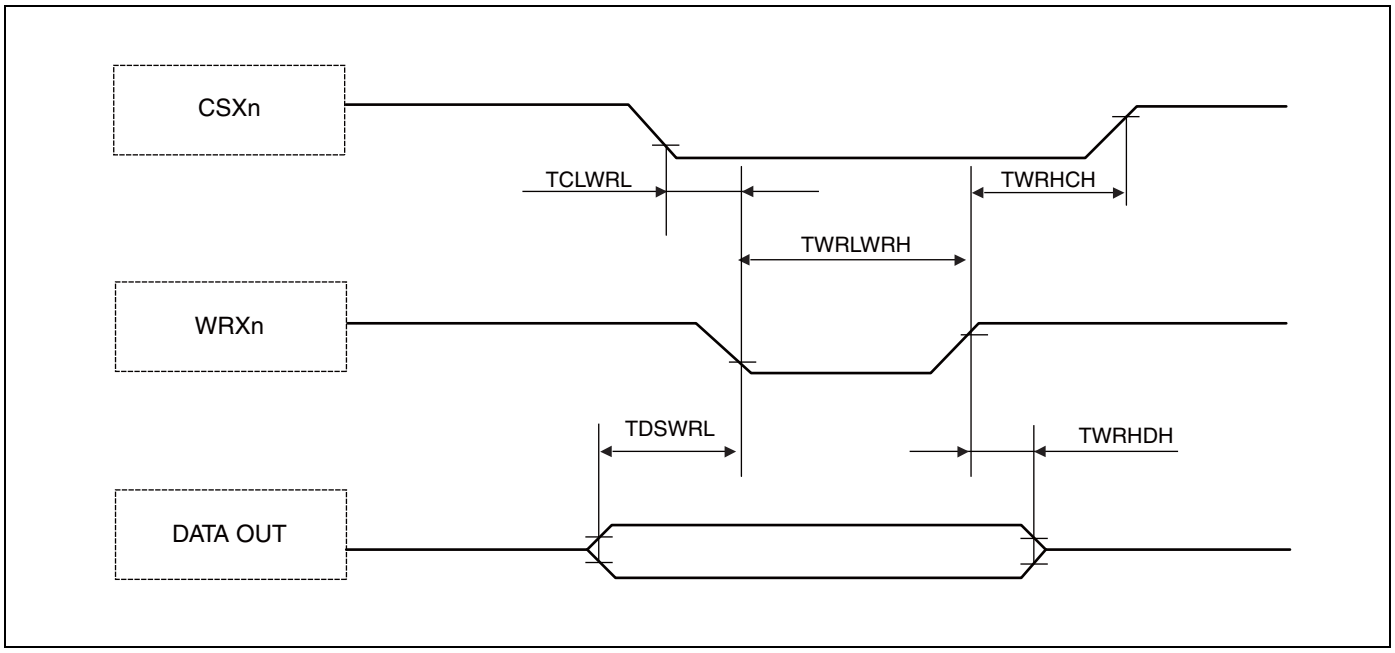
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK ↓ to WRXn delay time	TCLWRL	SYSCLK WRXn	—	8	ns
	TCLWRH		0	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	- 7	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} - 20	—	ns
SYSCLK ↓ to CSXn delay time	TCLCSL	SYSCLK CSXn	—	8	ns
	TCLCSH		—	12	ns



Asynchronous write access

(V_{DD}35 = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

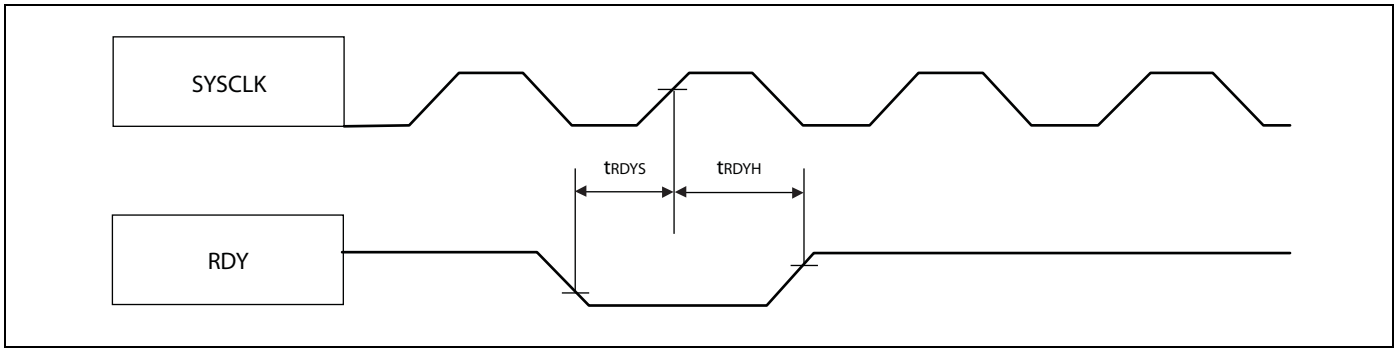
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	t_{CLKT}	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D16	1/2 × t_{CLKT} - 10	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D16	1/2 × t_{CLKT} - 19	—	ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn	—	1/2 × t_{CLKT}	ns
	TWRHCH		1/2 × t_{CLKT}	—	ns



RDY waitcycle insertion

(V_{DD}35 = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 125 °C)

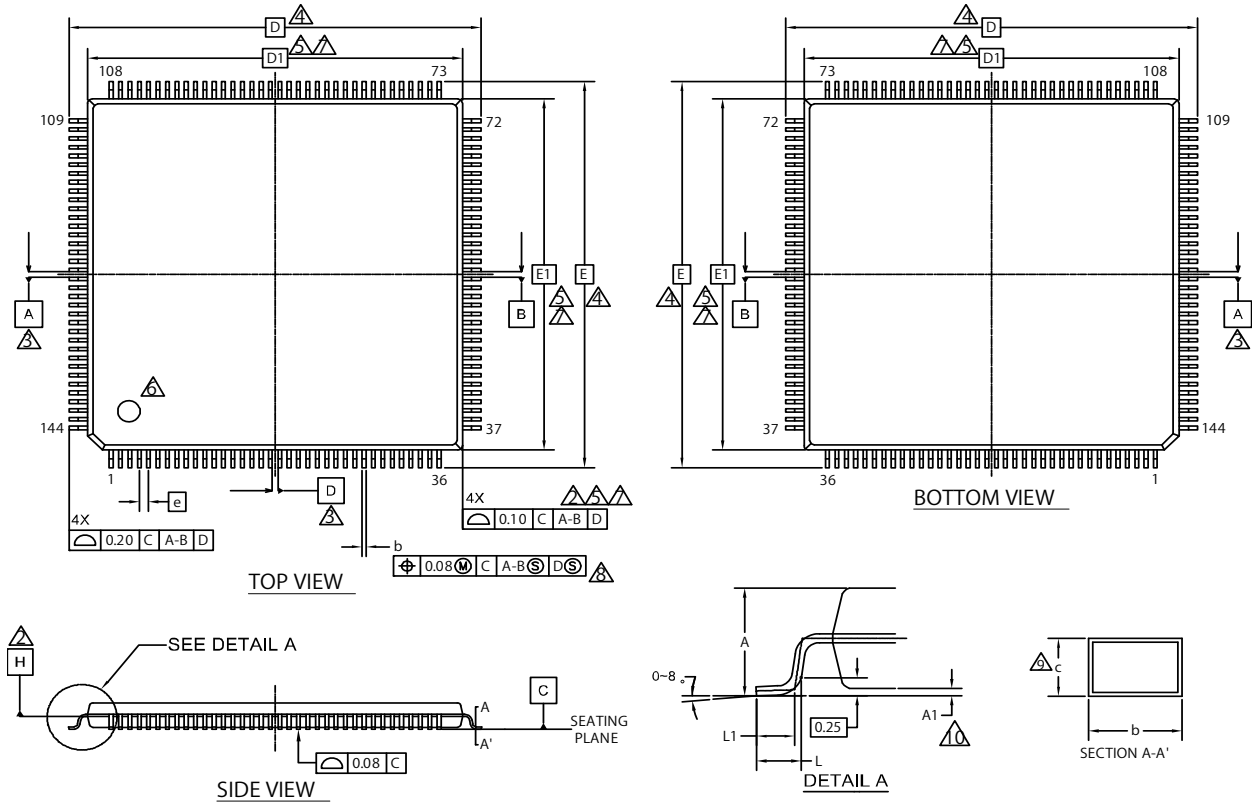
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	SYSCLK RDY	34	—	ns
RDY hold time	TRDYH	SYSCLK RDY	0	—	ns



16. Ordering Information

Part Number	Package	Remarks
CY91F466HAPMC-GS-UJE2	144-pin plastic LQFP (LQS144)	Lead-free package

17. Package Dimension



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
b	0.17	0.22	0.27
c	0.09	——	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 *A

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 REV*A

18. Revision History

Version	Date	Remark
2.0	2009-01-07	Initial version

19. Major Changes

Spansion Publication Number: DS07-16616-1E

Page	Section	Change Results
87	4. A/D converter characteristics	Corrected “Zero reading voltage” and “Full scale reading voltage”.

NOTE: Please see “Document History” about later revised information.

Page	Section	Change Results
Rev. *B		
—	Marketing Part Numbers changed from a prefix MB to a prefix CY.	
—	1. Product Lineup 2. Pin Assignment 3. Pin Description 7. Block Diagram 9. Embedded Program/Data Memory (Flash) 11. Memory Maps 12. I/O Map 14. Recommended Settings 15. Electrical Characteristics	- Added device CY91F466HA - Added Ta=125 °C characteristics - Product Lineup: CY91F464HB has 16KB D-Bus RAM (not 24KB) - Flash memory and external bus area: Changed table formatting for CY91F464HB - IO-Map: Corrected CANCKD register (only bit 0 applicable)
6, 7 102 103	2.Pin Assignment 16.Ordering Information 17.Package Dimension	Package description modified to JEDEC description.
102	16.Ordering Information	Deleted Marketing Part Number as follows: MB91F464HBPMC-GSE2 Added Marketing Part Number as follows: CY91F466HAPMC-GS-UJE2

Document History

Document Title: CY91460H Series FR60 32-bit Microcontroller Document Number: 002-04621				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	08/27/2009	Migrated to Cypress and assigned document number 002-04621. No change to document contents or format.
*A	5221965	AKIH	04/15/2016	Updated to Cypress format.
*B	6459657	SHUS	01/25/2019	- Added device CY91F466HA - Added Ta=125 °C characteristics - Product Lineup: CY91F464HB has 16KB D-Bus RAM (not 24KB) - Flash memory and external bus area: Changed table formatting for CY91F464HB - IO-Map: Corrected CANCKD register (only bit 0 applicable) - Package description modified to JEDEC description. - Updated the ordering information For details, please see 19. Major Changes.

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