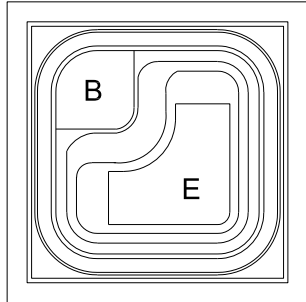


CP388X-BC546B

NPN - Low Noise Transistor Die

The CP388X-BC546B is a silicon NPN transistor designed for low noise amplifier applications.



BACKSIDE COLLECTOR R0

MECHANICAL SPECIFICATIONS:

Die Size	13 x 13 MILS
Die Thickness	5.9 MILS
Base Bonding Pad Size	3.9 x 3.9 MILS
Emitter Bonding Pad Size	5.4 x 5.4 MILS
Top Side Metalization	Al-Si – 17,000Å
Back Side Metalization	Au – 9,000Å
Scribe Alley Width	1.8 MILS
Wafer Diameter	5 INCHES
Gross Die Per Wafer	102,852

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

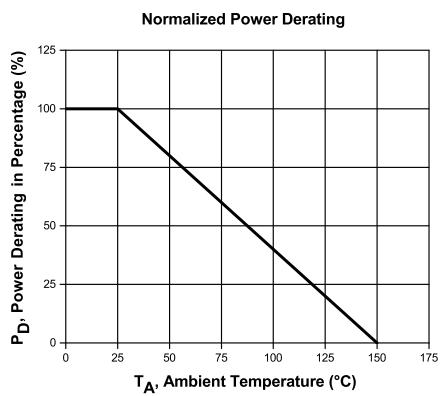
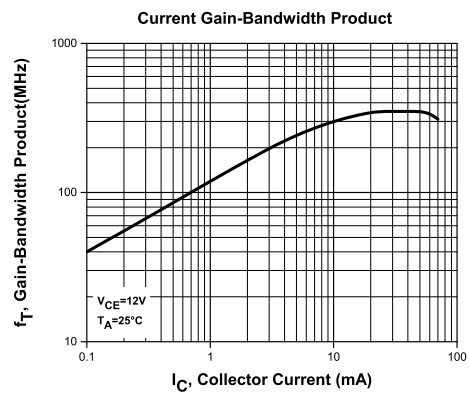
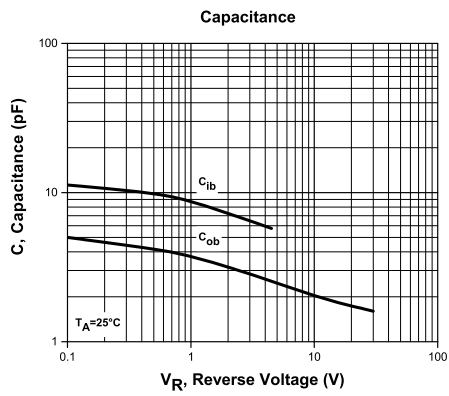
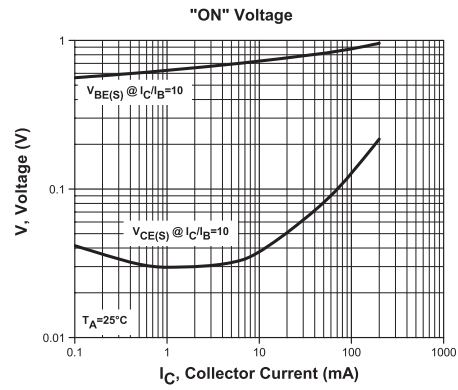
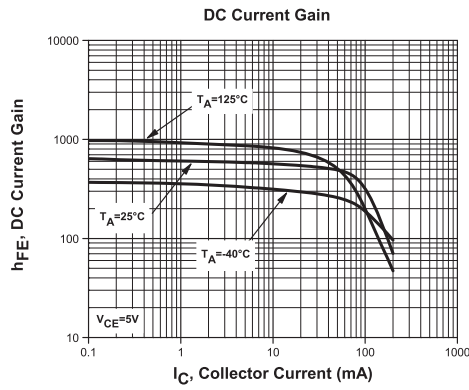
	SYMBOL		UNITS
Collector-Base Voltage	V_{CB0}	80	V
Collector-Emitter Voltage	V_{CES}	80	V
Collector-Emitter Voltage	V_{CEO}	65	V
Emitter-Base Voltage	V_{EBO}	6.0	V
Continuous Collector Current	I_C	100	mA
Peak Collector Current	I_{CM}	200	mA
Peak Base Current	I_{BM}	200	mA
Peak Emitter Current	I_{EM}	200	mA
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{CB0}	$V_{CB}=30\text{V}$			15	nA
$V_{CE(SAT)}$	$I_C=10\text{mA}, I_B=0.5\text{mA}$			250	mV
$V_{CE(SAT)}$	$I_C=100\text{mA}, I_B=5.0\text{mA}$			600	mV
$V_{BE(SAT)}$	$I_C=10\text{mA}, I_B=0.5\text{mA}$		700		mV
$V_{BE(SAT)}$	$I_C=100\text{mA}, I_B=5.0\text{mA}$		900		mV
$V_{BE(ON)}$	$V_{CE}=5.0\text{V}, I_C=2.0\text{mA}$	580		700	mV
$V_{BE(ON)}$	$V_{CE}=5.0\text{V}, I_C=10\text{mA}$			770	mV
h_{FE}	$V_{CE}=5.0\text{V}, I_C=2.0\text{mA}$	200			
h_{fe}	$V_{CE}=5.0\text{V}, I_C=2.0\text{mA}, f=1.0\text{kHz}$	125		900	
f_T	$V_{CE}=5.0\text{V}, I_C=10\text{mA}, f=35\text{MHz}$		300		MHz
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=1.0\text{MHz}$		2.5		pF
C_{ib}	$V_{EB}=0.5\text{V}, I_C=0, f=1.0\text{MHz}$		9.0		pF
NF	$V_{CE}=5.0\text{V}, I_C=0.2\text{mA}, R_G=2.0\text{k}\Omega, f=1.0\text{kHz}, BW=200\text{Hz}$		2.0	10	dB

CP388X-BC546B

Typical Electrical Characteristics



BARE DIE PACKING OPTIONS



BARE DIE IN TRAY (WAFFLE) PACK

CT: Singulated die in tray (waffle) pack.
(example: CP211-PART NUMBER-CT)

CM: Singulated die in tray (waffle) pack 100% visually inspected as per MIL-STD-750, (method 2072 transistors, method 2073 diodes).
(example: CP211-PART NUMBER-CM)



UNSAWN WAFER

WN: Full wafer, unsawn, 100% tested with reject die inked.
(example: CP211-PART NUMBER-WN)



SAWN WAFER ON PLASTIC RING

WR: Full wafer, sawn and mounted on plastic ring,
100% tested with reject die inked.
(example: CP211-PART NUMBER-WR)

Please note: Sawn Wafer on Metal Frame (WS) is possible as a special order. Please contact your Central Sales Representative at 631-435-1110.



Visit the Central website for a complete listing of specifications:
www.centrasemi.com/bdspecs

OUTSTANDING SUPPORT AND SUPERIOR SERVICES



PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2nd day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

REQUESTING PRODUCT PLATING

1. If requesting Tin/Lead plated devices, add the suffix "TIN/LEAD" to the part number when ordering (example: 2N2222A TIN/LEAD).
2. If requesting Lead (Pb) Free plated devices, add the suffix "PBFREE" to the part number when ordering (example: 2N2222A PBFREE).

CONTACT US

Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.
145 Adams Avenue
Hauppauge, NY 11788 USA
Main Tel: (631) 435-1110
Main Fax: (631) 435-1824
Support Team Fax: (631) 435-3388
www.centrasemi.com

Worldwide Field Representatives:
www.centrasemi.com/wwreps

Worldwide Distributors:
www.centrasemi.com/wwdistributors

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