CAB500M17HM3

1700 V, 500 A, Silicon Carbide, Half-Bridge Module

V_{DS}	**1700 V**
I_{DS}	**500 A**

Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation
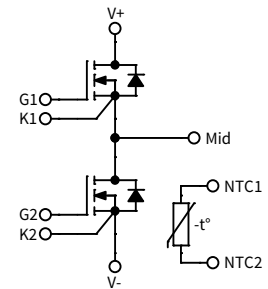
Applications

- Railway, Traction, and Motor Drives
- EV Chargers
- High-Efficiency Converters / Inverters
- Renewable Energy
- Smart-Grid / Grid-Tied Distributed Generation

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Maximum Parameters (Verified by Design)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	V_{DS}			1700	V		
Gate-Source Voltage, Maximum Value	$V_{GS\,max}$	-8		+19		Transient, <100 ns	Fig. 33
Gate-Source Voltage, Recommended	$V_{GS\,op}$	-4		+15		Static	
DC Continuous Drain Current	I_D		653		A	V_{GS} = 15 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	Fig. 20
			494			V_{GS} = 15 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	
DC Source-Drain Current (Body Diode)	$I_{SD\,BD}$		446			V_{GS} = - 4 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	
			284			V_{GS} = - 4 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	
Pulsed Drain Current	$I_{D\,(pulsed)}$			1000		t_{Pmax} limited by T_{VJmax} V_{GS} = 15 V, T_C = 25 °C	
Virtual Junction Temperature	$T_{VJ\,op}$	-40		175	°C	Operation	

MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1700				V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_D = 203 mA	
			2.0			V_{DS} = V_{GS}, I_D = 203 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		8	325	µA	V_{GS} = 0 V, V_{DS} = 1700 V	
Gate-Source Leakage Current	I_{GSS}		0.008	2		V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		2.16	2.60	mΩ	V_{GS} = 15 V, I_D = 500 A	Fig. 2 Fig. 3
			4.97			V_{GS} = 15 V, I_D = 500 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		369		S	V_{DS} = 20 V, I_D = 500 A	Fig. 4
			374			V_{DS} = 20 V, I_D = 500 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{On}		25.0 27.9 32.5		mJ	V_{DD} = 900 V I_D = 500 A, V_{GS} = -4 V/15 V, $R_{G(OFF)}$ = 1.5 Ω, $R_{G(ON)}$ = 1.5 Ω, L = 14 µH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{Off}		15.4 15.4 15.6				
Internal Gate Resistance	$R_{G(int)}$		0.93		Ω	f = 1 MHz, V_{AC} = 25 mV	
Input Capacitance	C_{iss}		64.9		nF	V_{GS} = 0 V, V_{DS} = 1200 V V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		1.5				
Reverse Transfer Capacitance	C_{rss}		42		pF		
Gate to Source Charge	Q_{GS}		640		nC	V_{DS} = 1200 V, V_{GS} = -4 V/15 V I_D = 735 A Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		560				
Total Gate Charge	Q_G		1992				
FET Thermal Resistance, Junction to Case	$R_{th\,JC}$		0.070		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Body Diode Forward Voltage	V_{SD}		5.5		V	V_{GS} = -4 V, I_{SD} = 500 A	Fig. 7
			4.8			V_{GS} = -4 V, I_{SD} = 500 A, T_{VJ} = 175 °C	
Reverse Recovery Time	t_{RR}		67		ns	V_{GS} = -4 V, I_{SD} = 500 A, V_R = 900 V di/dt = 13 A/ns, T_{VJ} = 175 °C	Fig. 32
Reverse Recovery Charge	Q_{RR}		24		µC		
Peak Reverse Recovery Current	I_{RRM}		350		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{RR}		0.6 3.3 6.3		mJ	V_{DD} = 900 V, I_D = 500 A, V_{GS} = -4 V/15 V, $R_{G(ON)}$ = 1.5 Ω, L = 14 µH	Fig. 14

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Package Resistance, M1 (High-Side)	R_{1-2}		106.5		µΩ	T_C = 125°C, Note 1
Package Resistance, M2 (Low-Side)	R_{2-3}		126.3			T_C = 125°C, Note 1
Stray Inductance	L_{Stray}		4.9		nH	Between DC- and DC+, f = 10 MHz
Case Temperature	T_C	-40		125	°C	
Mounting Torque	M_S	3	4.5	5	N-m	Baseplate, M6 bolts
		0.9	1.1	1.3		Power Terminals, M4 bolts
Weight	W		167		g	
Case Isolation Voltage	V_{isol}	4			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	600				
Clearance Distance		13.07			mm	Terminal to Terminal
		6.00				Terminal to Heatsink
Creepage Distance		14.27				Terminal to Terminal
		12.34				Terminal to Heatsink

Note:

[1] Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

NTC Characteristics (T_{NTC} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Resistance at 25°C	R_{25}		4700		Ω	
Tolerance of R_{25}			±1		%	
Beta Value for 25°C to 85°C	$B_{25/85}$		3435		K	
Beta Value for 0°C to 100°C	$B_{0/100}$		3399		K	
Tolerance of $B_{25/85}$			±1		%	
Maximum Power Dissipation	P_{Max}		50		mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A	B	C	D	A_1	B_1	C_1	D_1
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06	3.354E-03	3.001E-04	5.085E-06	2.188E-07

Typical Performance
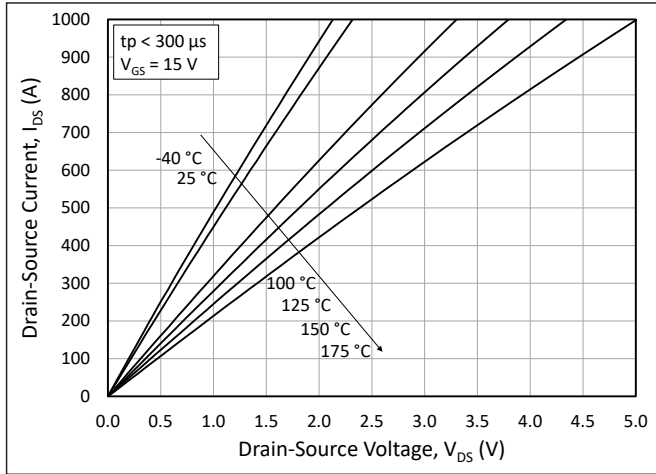
Figure 1. Output Characteristics for Various Junction Temperatures
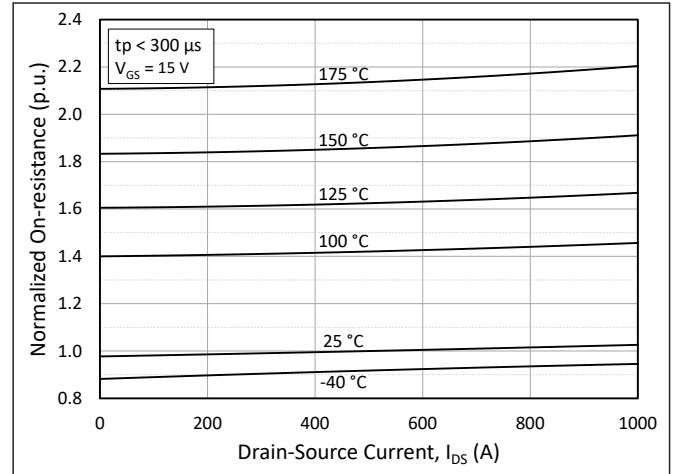

Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures
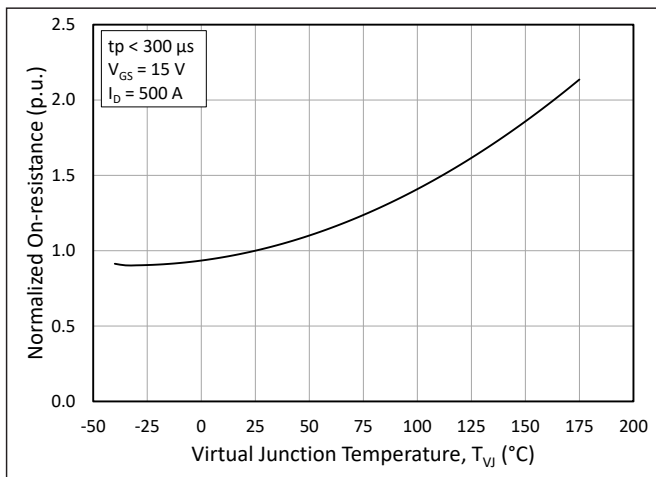

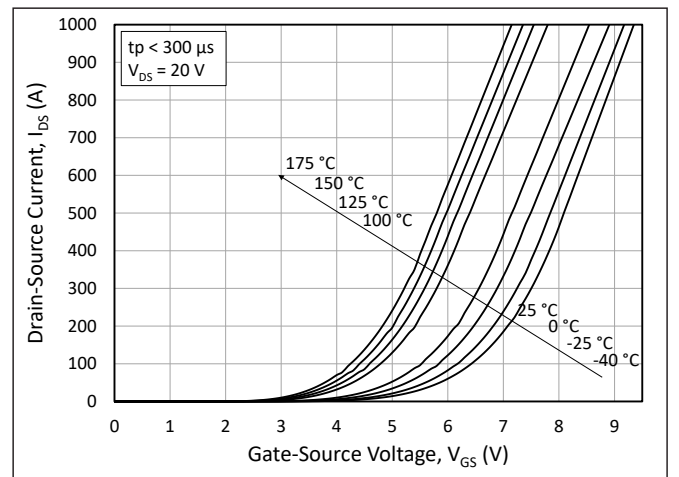**Figure 3.** Normalized On-State Resistance vs. Junction Temperature

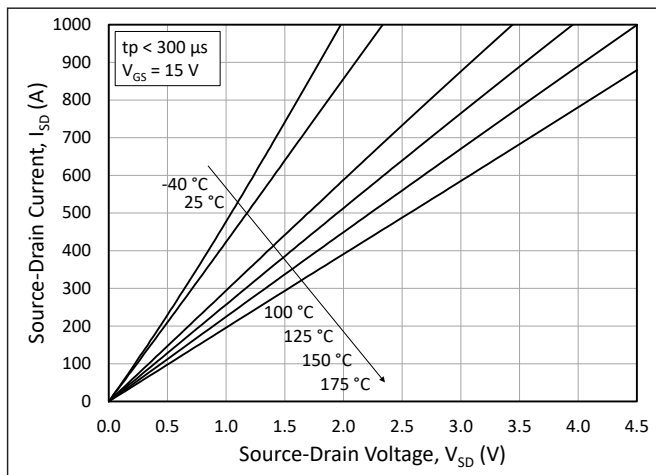**Figure 4.** Transfer Characteristic for Various Junction Temperatures

Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V
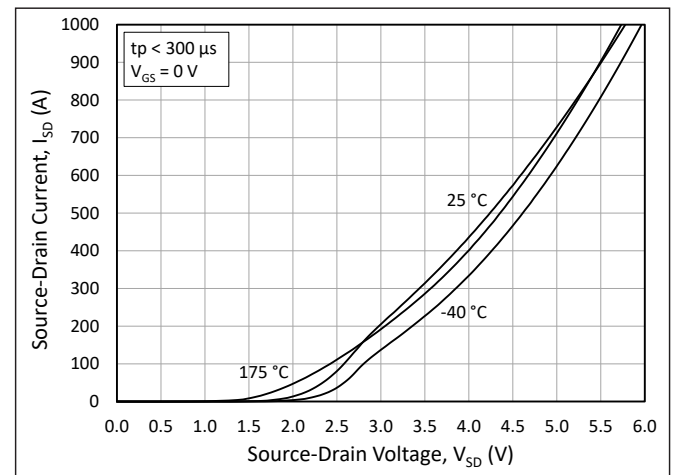

Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

Typical Performance
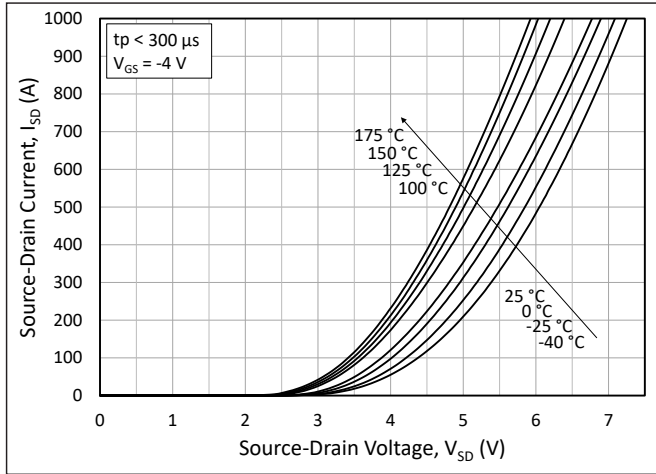
Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Body Diode)
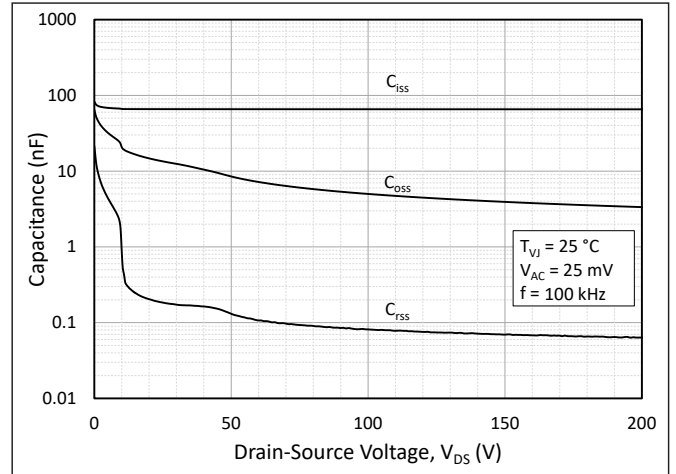
Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)
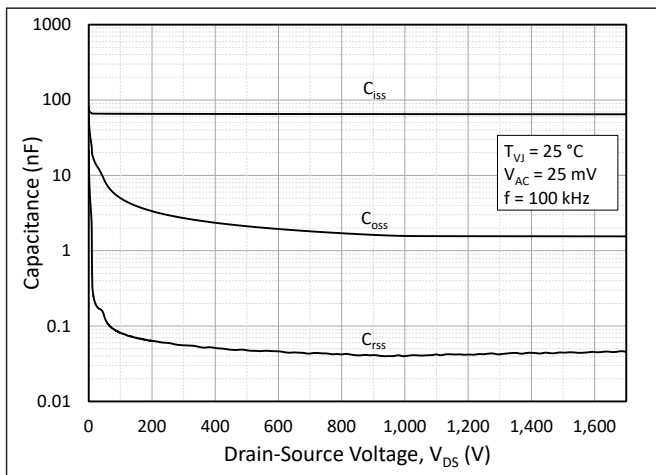
Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)
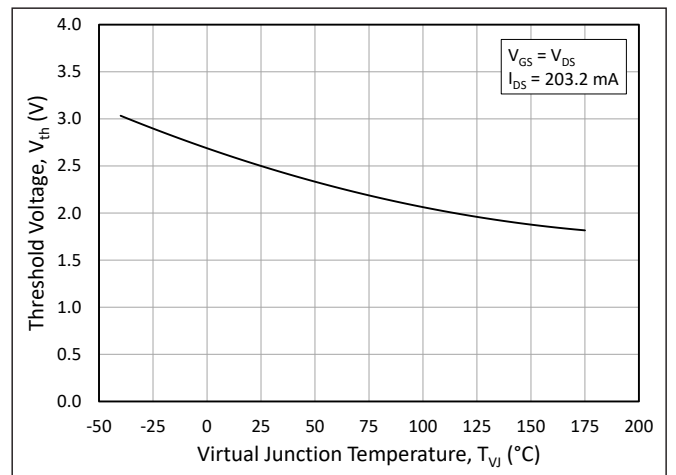
Figure 10. Threshold Voltage vs. Junction Temperature
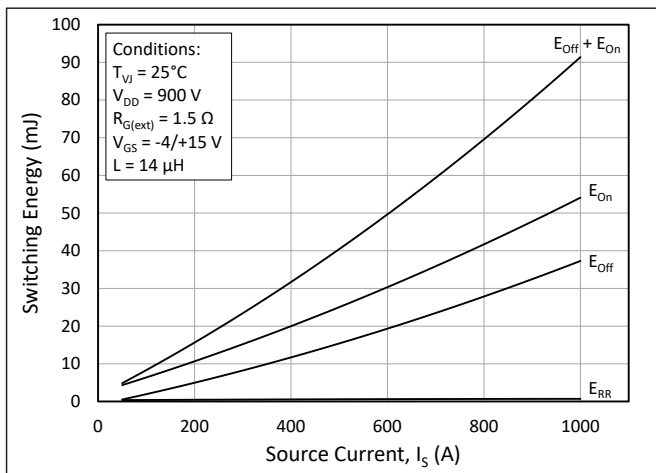
Figure 11. Switching Energy vs. Drain Current (V_{DD} = 900 V)
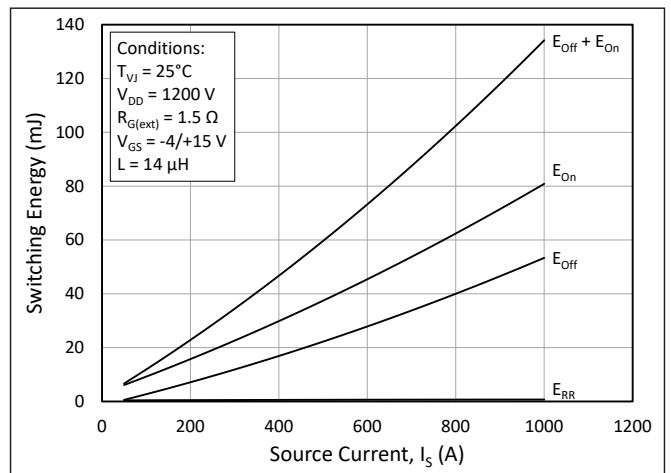
Figure 12. Switching Energy vs. Drain Current (V_{DD} = 1200 V)

Typical Performance
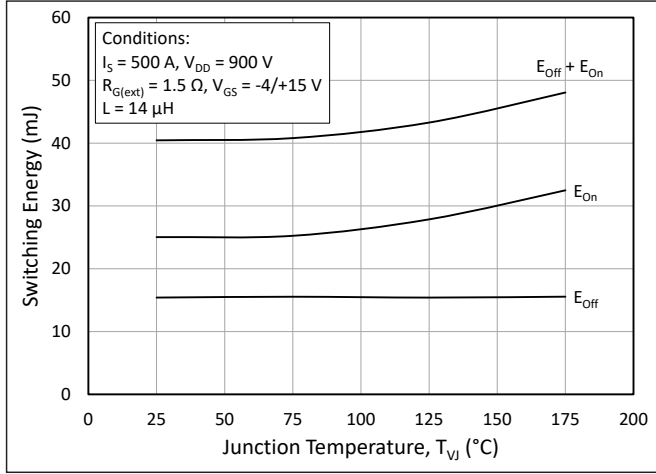
Figure 13. MOSFET Switching Energy vs. Junction Temperature
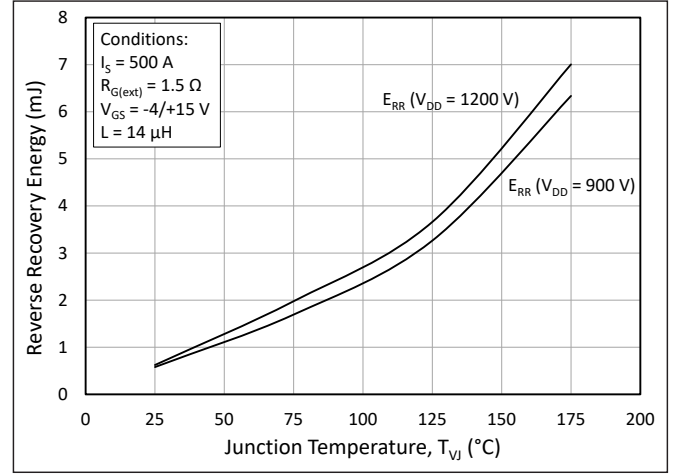
Figure 14. Reverse Recovery Energy vs. Junction Temperature
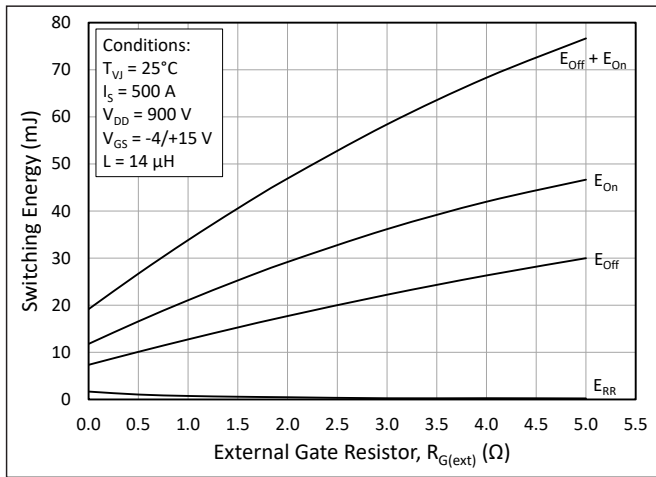
Figure 15. MOSFET Switching Energy vs. External Gate Resistance
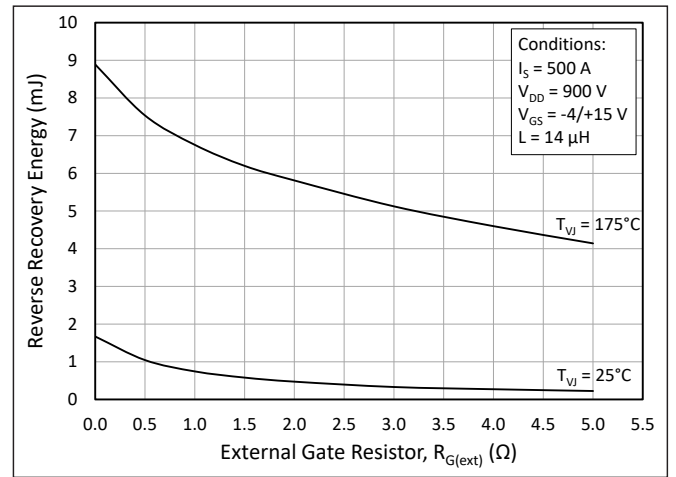
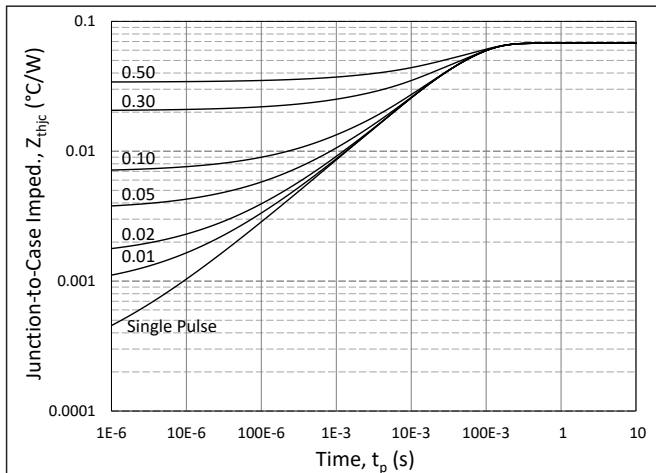**Figure 16.** Reverse Recovery Energy vs. External Gate Resistance

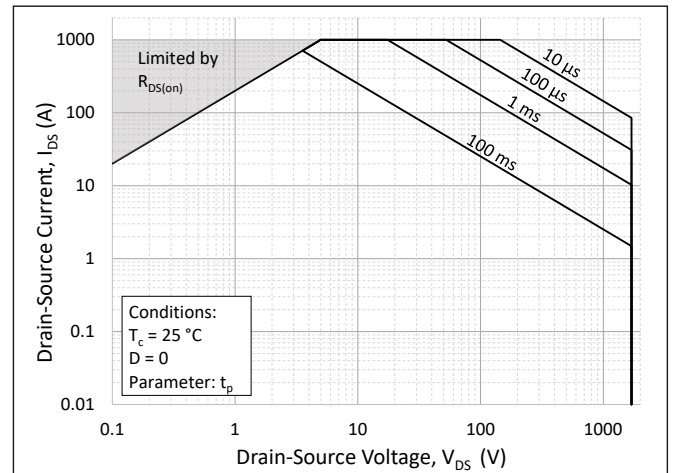**Figure 17.** MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

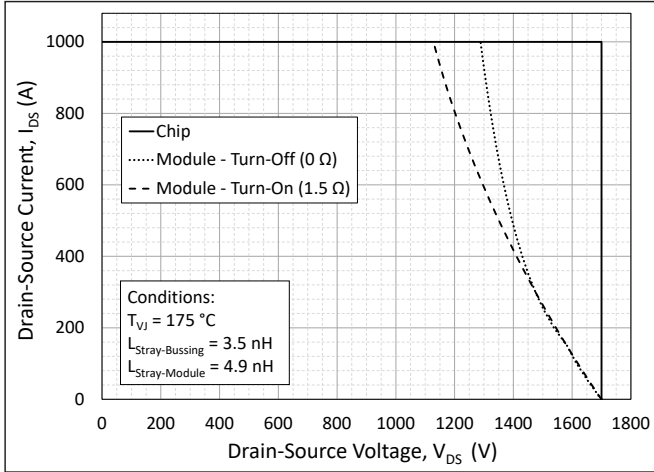**Figure 18.** Forward Bias Safe Operating Area (FBSOA)

Typical Performance

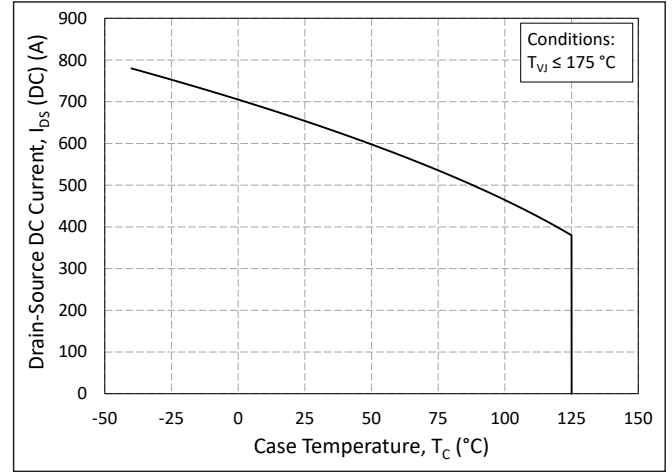**Figure 19.** Reverse Bias Safe Operating Area (RBSOA)

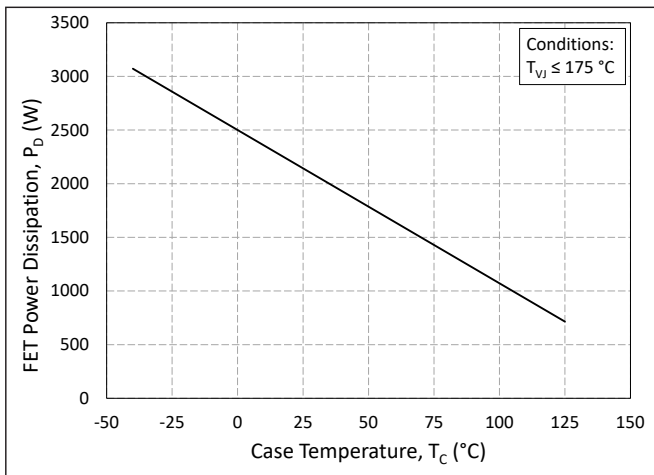**Figure 20.** Continuous Drain Current Derating vs. Case Temperature

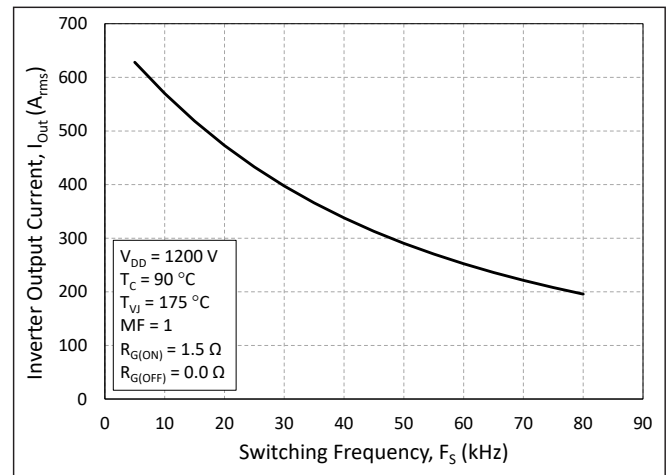**Figure 21.** Maximum Power Dissipation Derating vs. Case Temperature

Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)
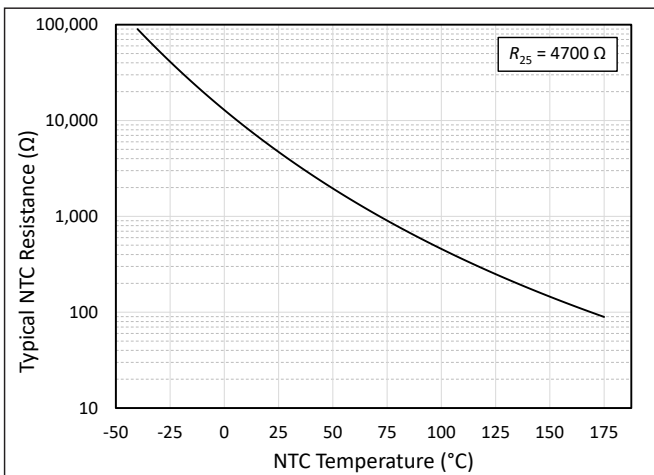

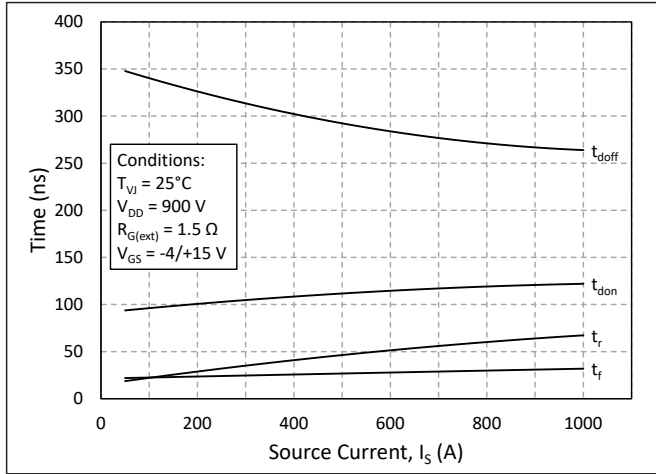**Figure 23.** NTC Resistance vs. NTC Temperature

Timing Characteristics

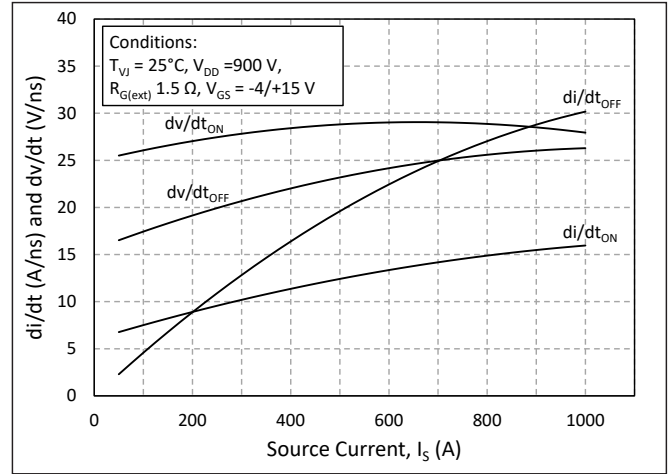**Figure 24.** Timing vs. Source Current

Figure 25. dv/dt and di/dt vs. Source Current

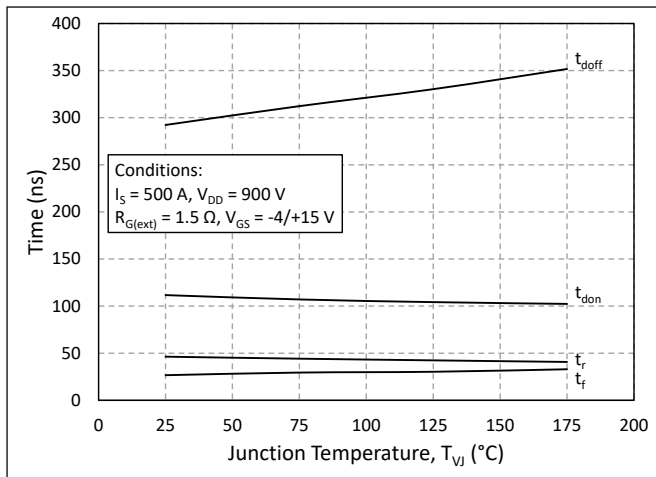**Figure 26.** Timing vs. Junction Temperature

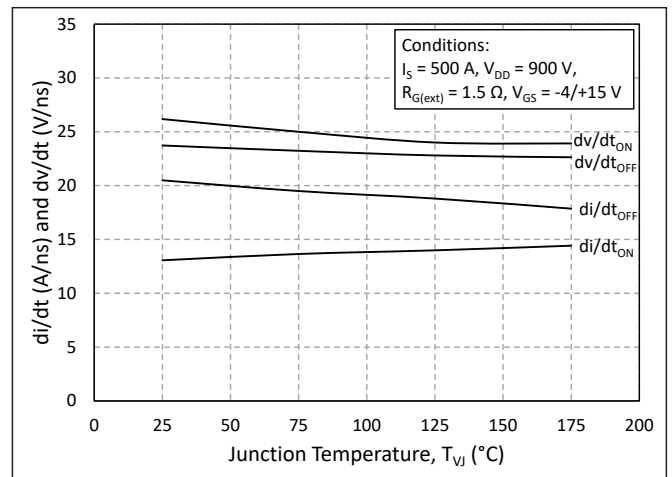**Figure 27.** dv/dt and di/dt vs. Junction Temperature
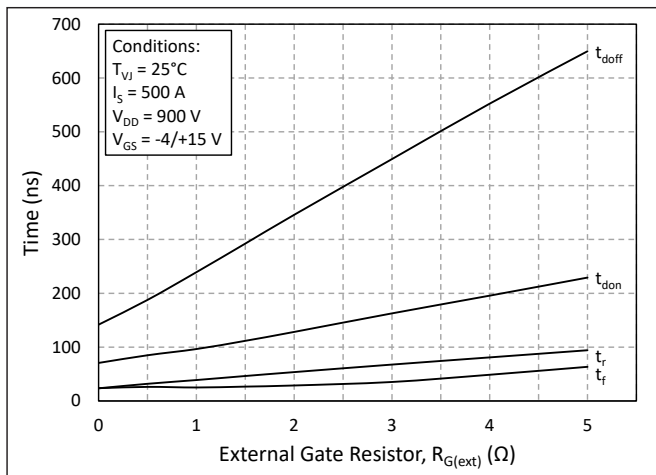

Figure 28. Timing vs. External Gate Resistance
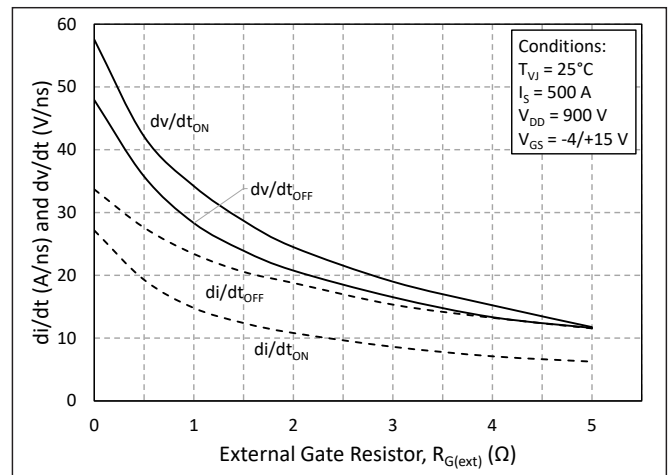

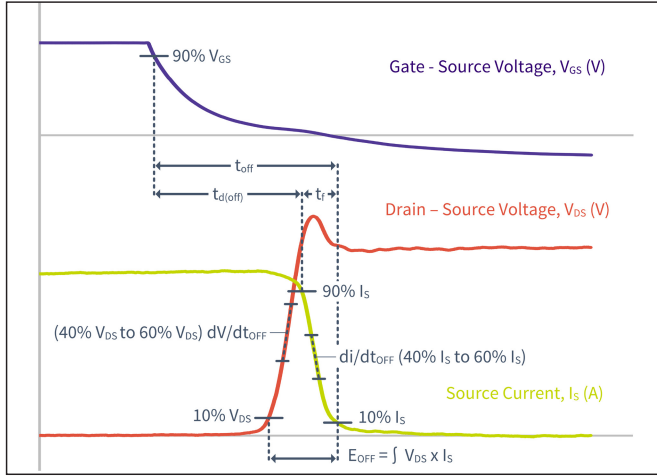**Figure 29.** dv/dt and di/dt vs. External Gate Resistance

Definitions

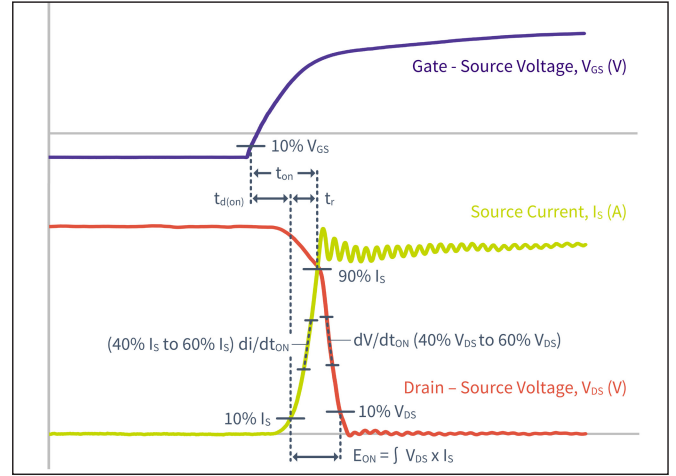**Figure 30.** Turn-off Transient Definitions

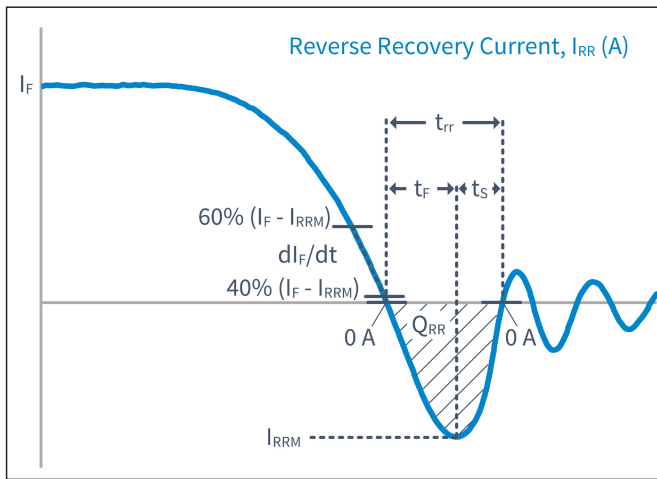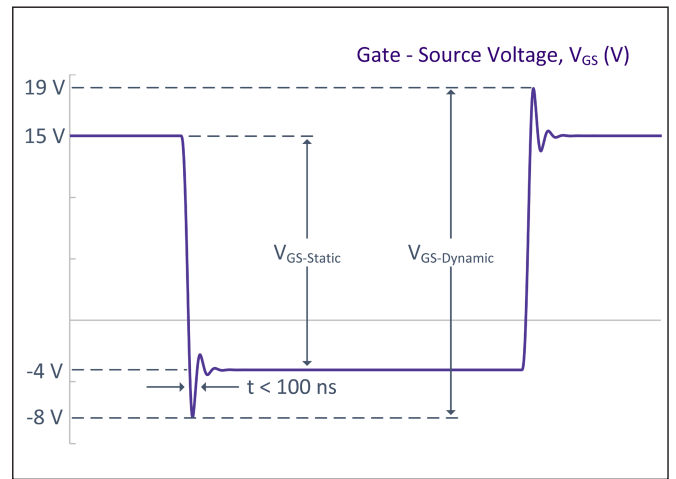**Figure 31.** Turn-on Transient Definitions
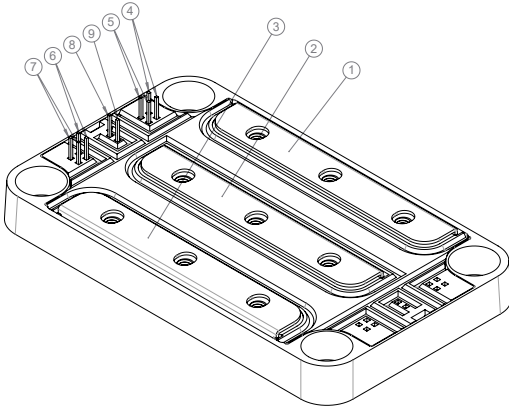

Figure 32. Reverse Recovery Definitions

Figure 33. V_{GS} Transient Definitions

Schematic and Pin Out

PIN OUT SCHEME	
PIN	LABEL
1	V+
2	Mid
3	V-
4	G1, Top row pins (2)
5	K1, Bottom row pins (2)
6	G2, Top row pins (2)
7	K2, Bottom row pins (2)
8	NTC1
9	NTC2
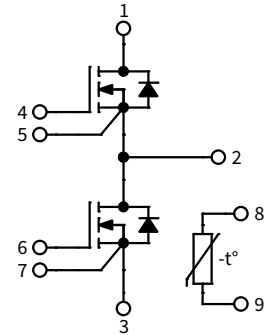
Package Dimension (mm)
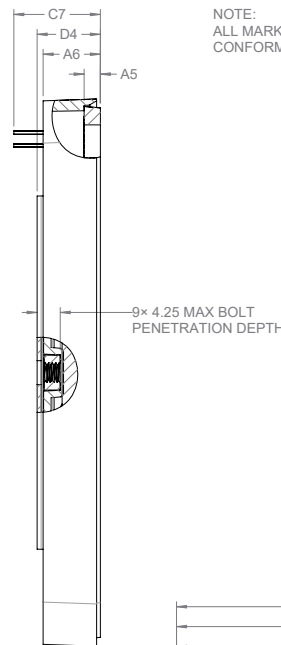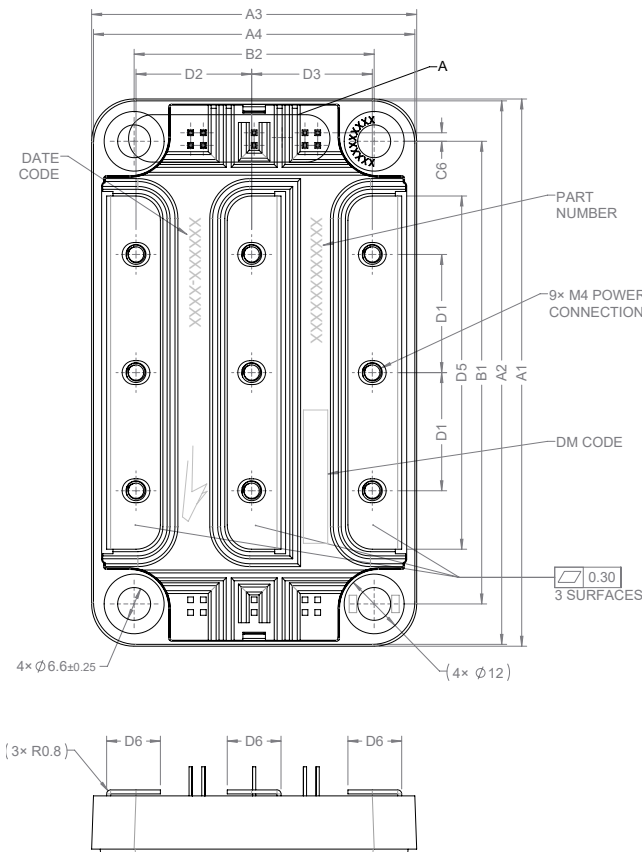
NOTE:
ALL MARKINGS SHALL CONFORM TO PRC-00786.

DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	110.00	±0.60
A2	109.25	±0.60
A3	65.00	±0.60
A4	64.25	±0.60
A5	3.25	±0.30
A6	11.45	±0.60
B1	93.00	±0.30
B2	48.00	±0.30
C1	11.30	±0.40
C2	13.84	±0.40
C3	24.00	±0.40
C4	34.16	±0.40
C5	36.70	±0.40
C6	1.71	±0.40
C7	17.30	±0.50
C8	2.54	±0.30
C9	0.64	±0.30
C10	10.16	±0.40
D1	23.75	±0.50
D2	23.13	±0.50
D3	24.13	±0.50
D4	12.20	±0.50
D5	71.00	±0.30
D6	10.75	±0.30

DETAIL A
SCALE: 4:1

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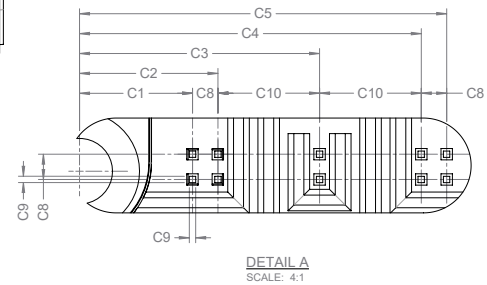
Supporting Links & Tools

Evaluation Tools & Support

- CAB500M17HM3 PLECS Model
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- Dynamic Characterization Evaluation Tool for the High Performance 62mm (HM) Module Platform

Dual-Channel Gate Driver Board

- CGD1700HB3P-HM3: Wolfspeed Gate Driver Board
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- CPWR-AN35: 62mm Thermal Interface Material Application Note
- CPWR-AN39: KIT-CRD-CIL12N-HM User Guide
- PRD-04814: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies

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REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Cree representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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