

C3M0120065L

Silicon Carbide Power MOSFET

C3M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

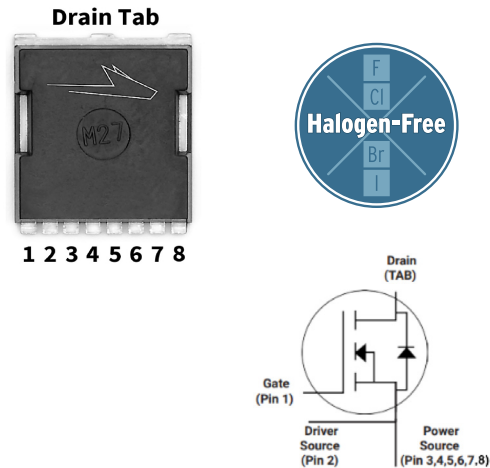
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Datacenter Power Supplies
- Telecom Power Supplies
- Energy Storage Systems
- Solar (PV) inverters
- High Voltage DC/DC converters

Package



Orderable Part Number	Package	Marking
C3M0120065L-TR	TOLL	C3M0120065L

Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Note	
V_{DSmax}	Drain - Source Voltage	650	V		
V_{GSmax}	Gate - Source Voltage	-8/+19	V	Note: 1	
I_D	Continuous Drain Current, $V_{GS} = 15\text{ V}$	$T_c = 25^\circ\text{C}$	21	A	Fig. 19 Note: 2
		$T_c = 100^\circ\text{C}$	14		
$I_{D(pulse)}$	Pulsed Drain Current, Pulse width t_p limited by T_{jmax}	51	A	Fig. 22	
P_D	Power Dissipation, $T_c=25^\circ\text{C}$, $T_j = 175^\circ\text{C}$	86	W	Fig. 20 Note: 2	
T_j	Junction Temperature	-40 to +175	$^\circ\text{C}$		
T_c, T_{stg}	Case Temperature and Storage Temperature	-40 to +150	$^\circ\text{C}$		
T_L	Solder Temperature, 1.6mm (0.063") from case for 10s	260	$^\circ\text{C}$		

Note (1): Recommended turn off / turn on gate voltage $V_{GS} = -4V..0V / +15V$

Note (2): Verified by design


Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	650			V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.3	3.6	V	$V_{DS} = V_{GS}, I_D = 1.86\ \text{mA}$	Fig. 11
			1.9		V	$V_{DS} = V_{GS}, I_D = 1.86\ \text{mA}, T_J = 175^\circ\text{C}$	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	$V_{DS} = 650\ \text{V}, V_{GS} = 0\ \text{V}$	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	$V_{GS} = 15\ \text{V}, V_{DS} = 0\ \text{V}$	
$R_{DS(on)}$	Drain-Source On-State Resistance		120	157	m Ω	$V_{GS} = 15\ \text{V}, I_D = 6.76\ \text{A}$	Fig. 4, 5, 6
			168			$V_{GS} = 15\ \text{V}, I_D = 6.76\ \text{A}, T_J = 175^\circ\text{C}$	
g_{fs}	Transconductance		5		S	$V_{DS} = 20\ \text{V}, I_{DS} = 6.76\ \text{A}$	Fig. 7
			5			$V_{DS} = 20\ \text{V}, I_{DS} = 6.76\ \text{A}, T_J = 175^\circ\text{C}$	
C_{iss}	Input Capacitance		640		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 400\ \text{V}$ $F = 1\ \text{MHz}$ $V_{AC} = 25\ \text{mV}$	Fig. 17, 18
C_{oss}	Output Capacitance		45				
C_{rss}	Reverse Transfer Capacitance		2.3				
E_{oss}	C_{oss} Stored Energy		9		μJ	$V_{DS} = 600\ \text{V}, F = 1\ \text{MHz}$	Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		57		pF	$V_{GS} = 0\ \text{V}, V_{DS} = 0\dots 400\ \text{V}$	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		79				
E_{oN}	Turn-On Switching Energy (Body Diode FWD)		27		μJ	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}, I_D = 6.76\ \text{A},$ $R_{G(ext)} = 10\ \Omega, L = 237\ \mu\text{H}, T_J = 25^\circ\text{C}$ FWD = Internal Body Diode	Fig. 23
E_{oFF}	Turn-Off Switching Energy (Body Diode FWD)		7				
$t_{d(on)}$	Turn-On Delay Time		5		ns	$V_{DD} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 6.76\ \text{A}, R_{G(ext)} = 10\ \Omega,$ Timing relative to V_{DS} Inductive load	Fig. 26
t_r	Rise Time		10				
$t_{d(off)}$	Turn-Off Delay Time		18				
t_f	Fall Time		9				
$R_{G(int)}$	Internal Gate Resistance		6		Ω	$f = 1\ \text{MHz}, V_{AC} = 25\ \text{mV}$	
Q_{gs}	Gate to Source Charge		8		nC	$V_{DS} = 400\ \text{V}, V_{GS} = -4\ \text{V}/15\ \text{V}$ $I_D = 6.76\ \text{A}$ Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		7				
Q_g	Total Gate Charge		26				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{ds} is rising from 0 to 400V
 $C_{o(tr)}$, a lumped capacitance that gives same charging time as C_{oss} while V_{ds} is rising from 0 to 400V


Reverse Diode Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.5		V	$V_{GS} = -4\text{ V}, I_{SD} = 3.4\text{ A}, T_J = 25^\circ\text{C}$	Fig. 8, 9, 10
		4.0		V	$V_{GS} = -4\text{ V}, I_{SD} = 3.4\text{ A}, T_J = 175^\circ\text{C}$	
I_S	Continuous Diode Forward Current		14	A	$V_{GS} = -4\text{ V}, T_c = 25^\circ\text{C}$	
$I_{S, pulse}$	Diode pulse Current		51	A	$V_{GS} = -4\text{ V}$, pulse width t_p limited by T_{Jmax}	
t_{rr}	Reverse Recover time	7		ns	$V_{GS} = -4\text{ V}, I_{SD} = 6.76\text{ A}, V_R = 400\text{ V}$ $dif/dt = 7880\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	93		nC		
I_{rrm}	Peak Reverse Recovery Current	23		A		
t_{rr}	Reverse Recover time	8		ns	$V_{GS} = -4\text{ V}, I_{SD} = 6.76\text{ A}, V_R = 400\text{ V}$ $dif/dt = 2320\text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$	
Q_{rr}	Reverse Recovery Charge	45		nC		
I_{rrm}	Peak Reverse Recovery Current	9		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.38	$^\circ\text{C}/\text{W}$		Fig. 21



Typical Performance

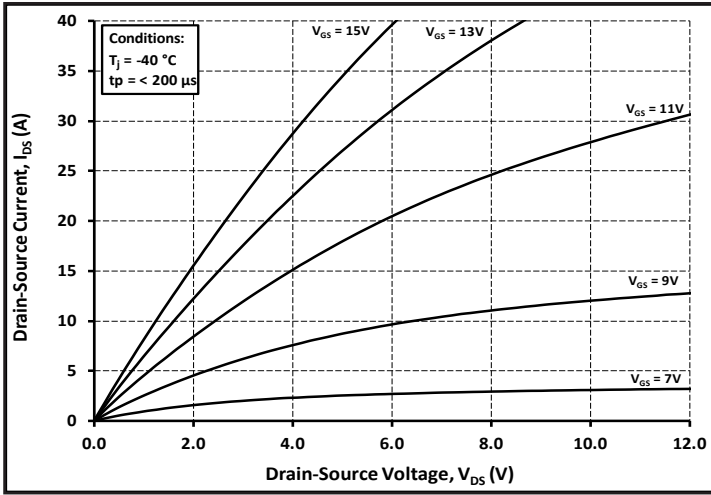


Figure 1. Output Characteristics $T_J = -40\text{ }^\circ\text{C}$

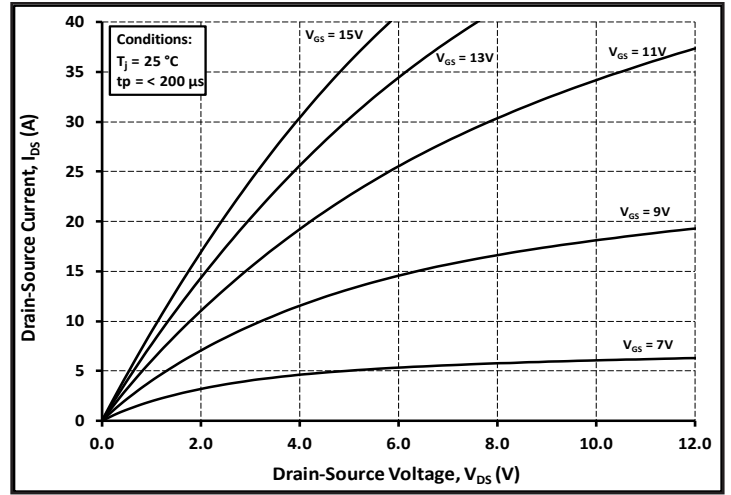


Figure 2. Output Characteristics $T_J = 25\text{ }^\circ\text{C}$

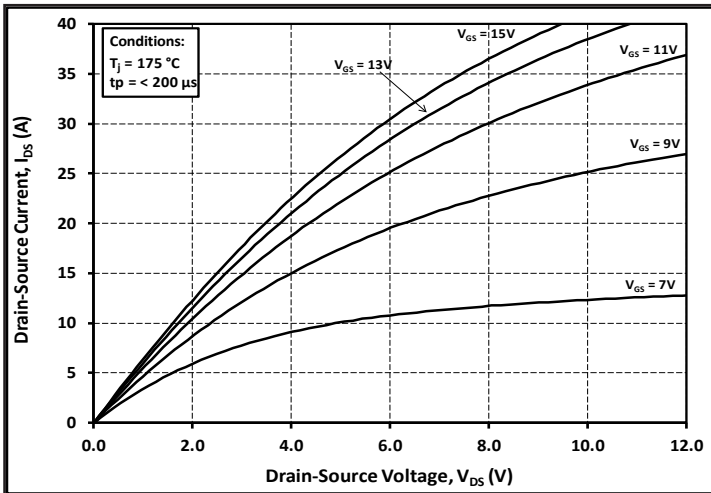


Figure 3. Output Characteristics $T_J = 175\text{ }^\circ\text{C}$

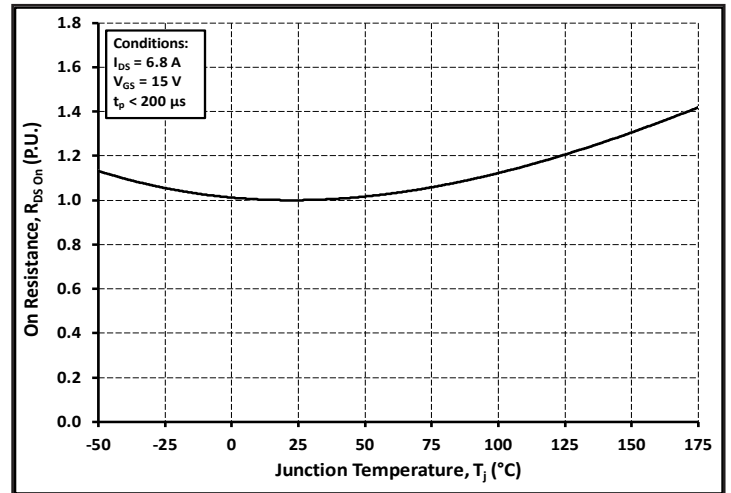


Figure 4. Normalized On-Resistance vs. Temperature

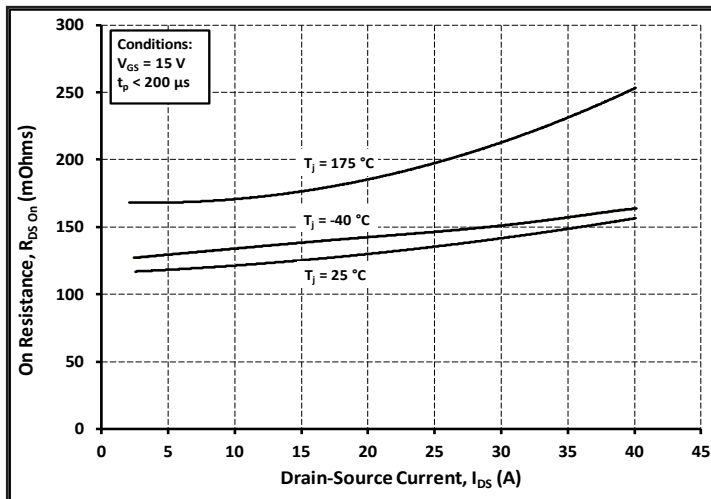


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

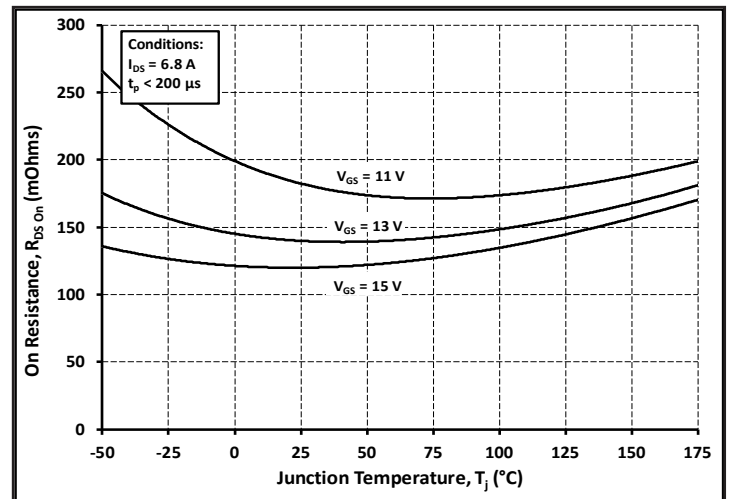


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage



Typical Performance

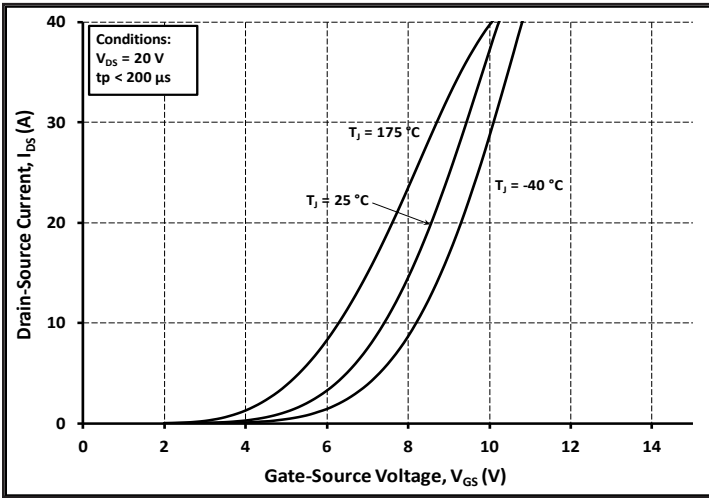


Figure 7. Transfer Characteristic for Various Junction Temperatures

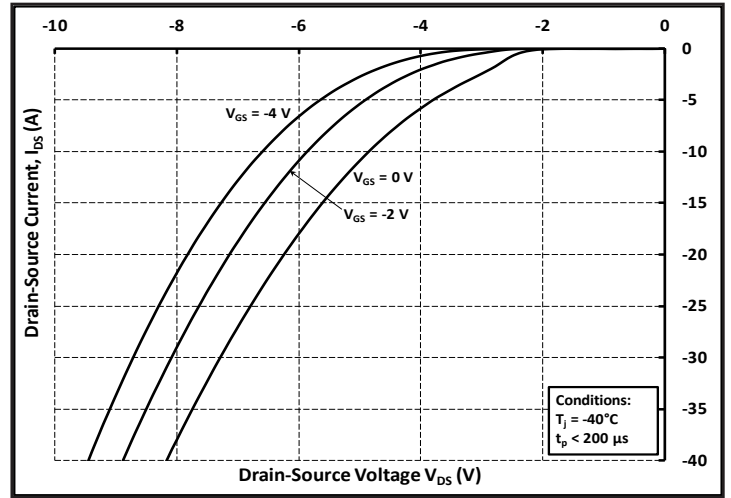


Figure 8. Body Diode Characteristic at -40 °C

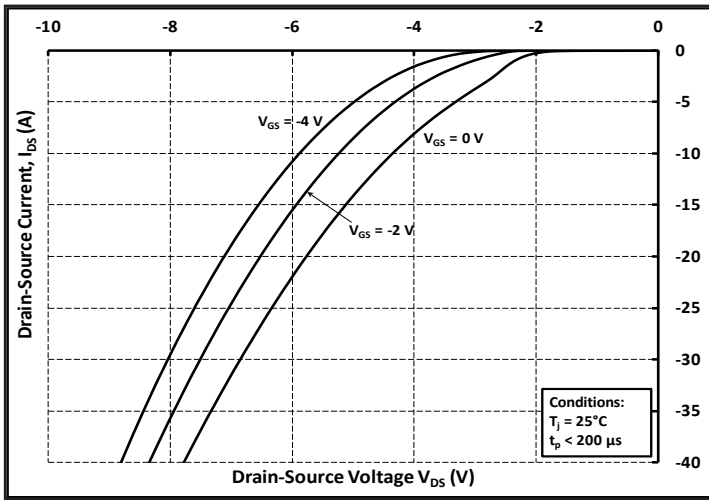


Figure 9. Body Diode Characteristic at 25 °C

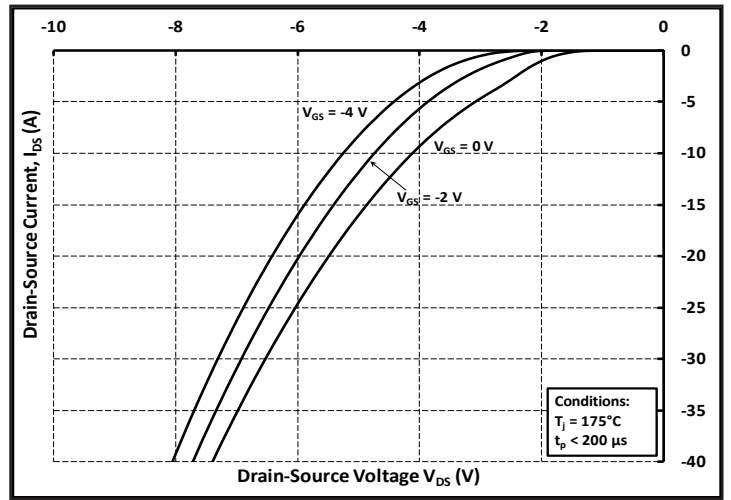


Figure 10. Body Diode Characteristic at 175 °C

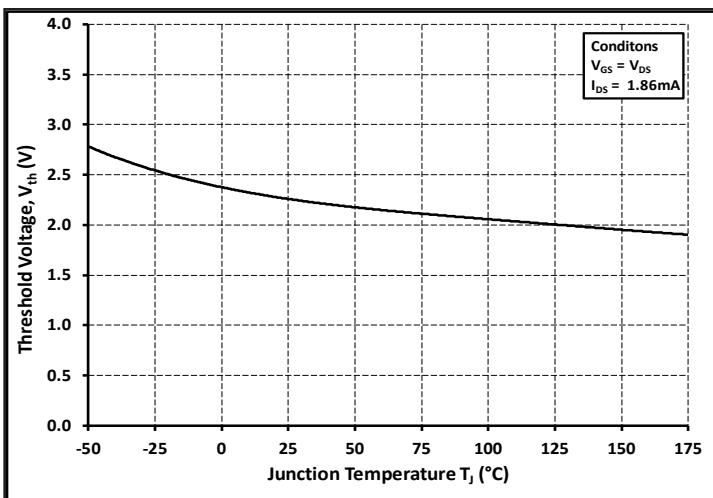


Figure 11. Threshold Voltage vs. Temperature

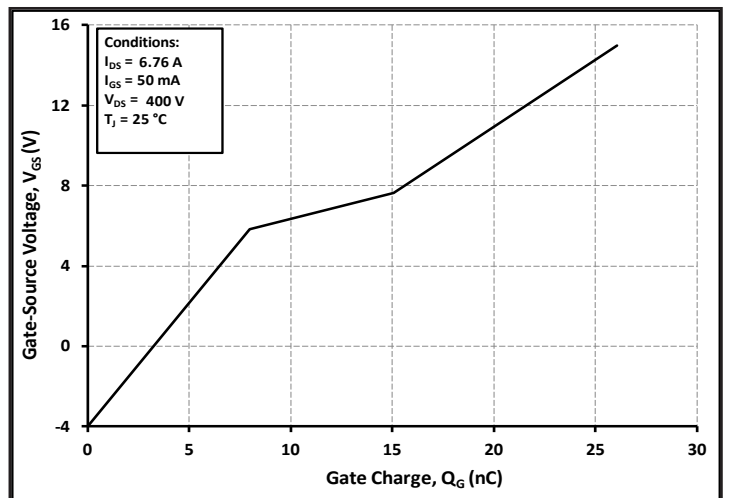


Figure 12. Gate Charge Characteristics



Typical Performance

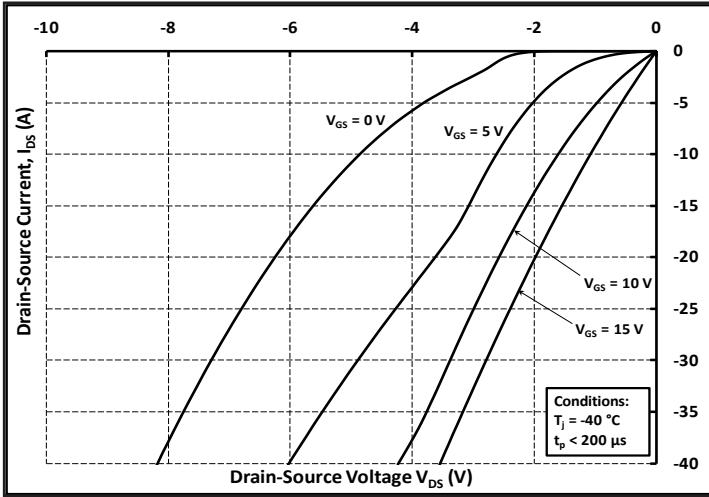


Figure 13. 3rd Quadrant Characteristic at -40 °C

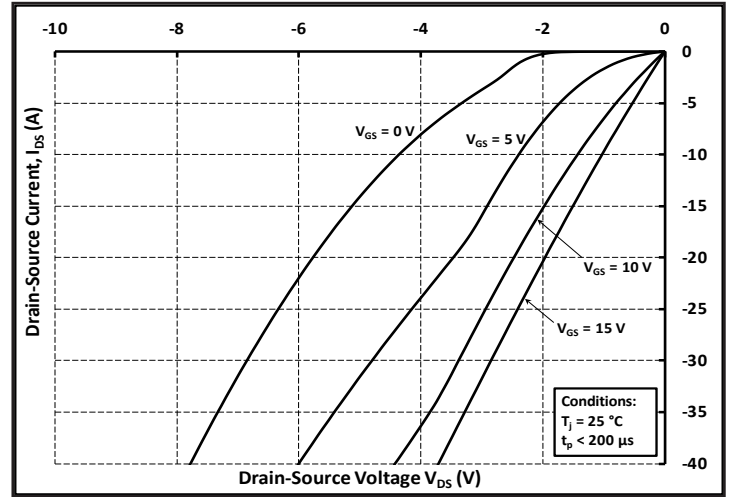


Figure 14. 3rd Quadrant Characteristic at 25 °C

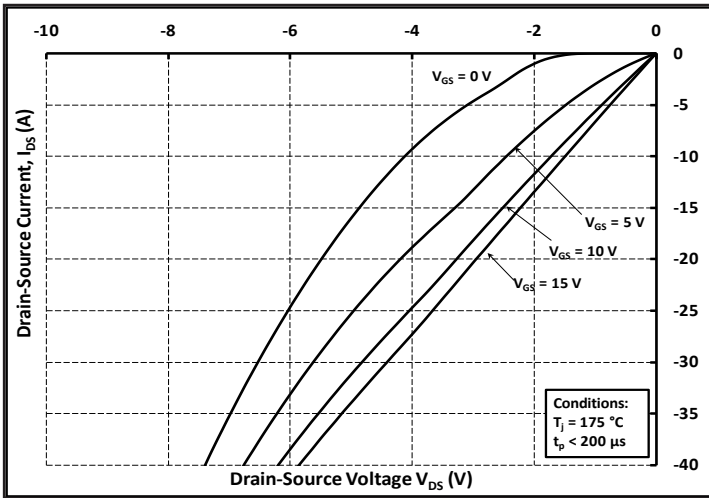


Figure 15. 3rd Quadrant Characteristic at 175 °C

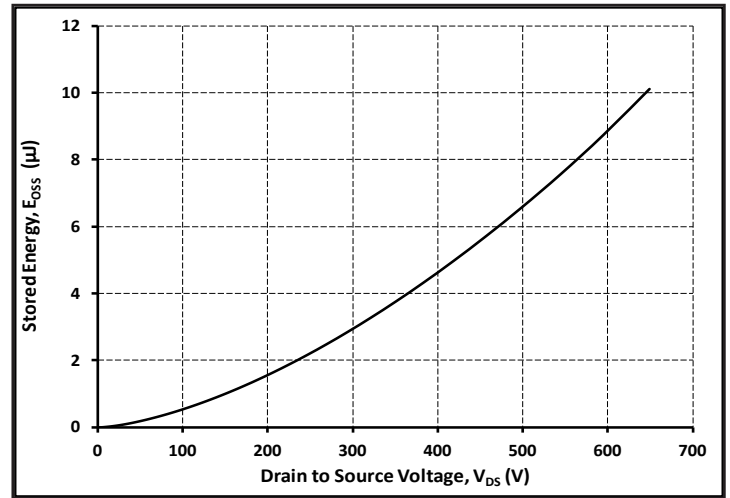


Figure 16. Output Capacitor Stored Energy

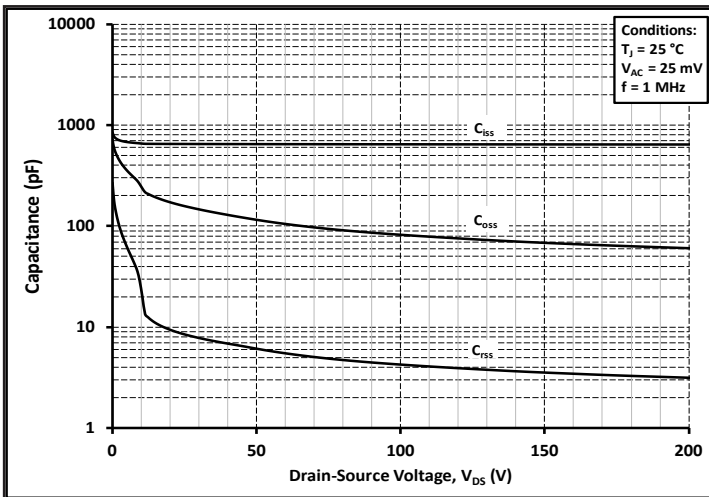


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

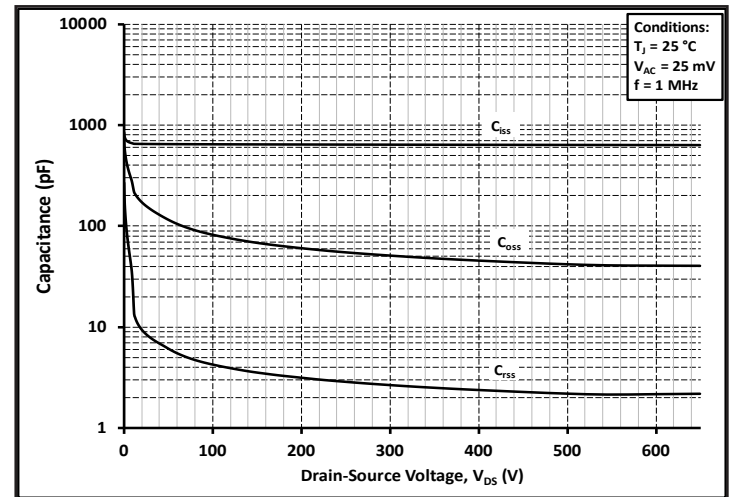


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650V)



Typical Performance

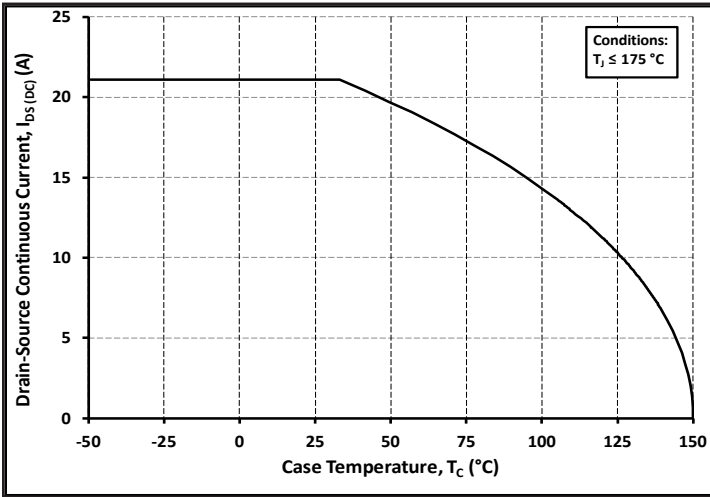


Figure 19. Continuous Drain Current Derating vs. Case Temperature

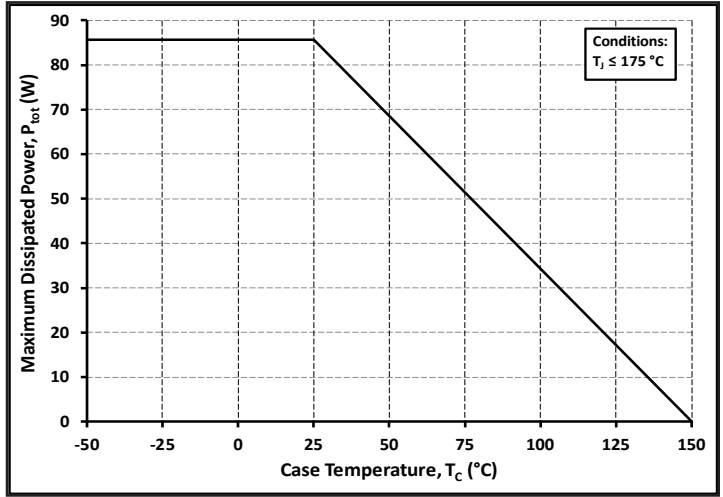


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

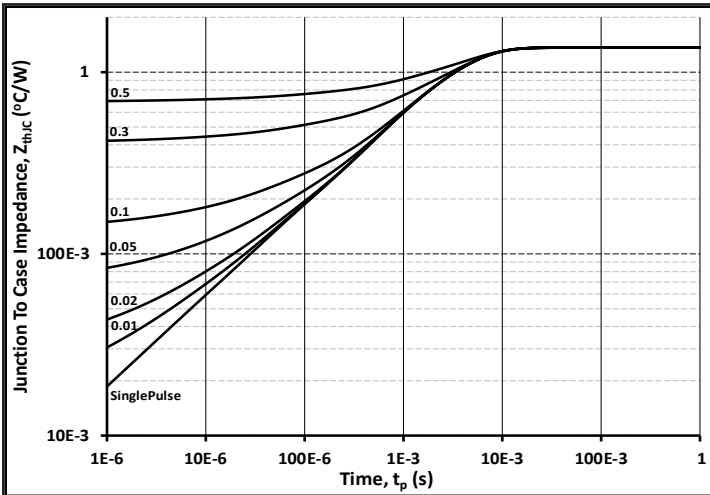


Figure 21. Transient Thermal Impedance (Junction - Case)

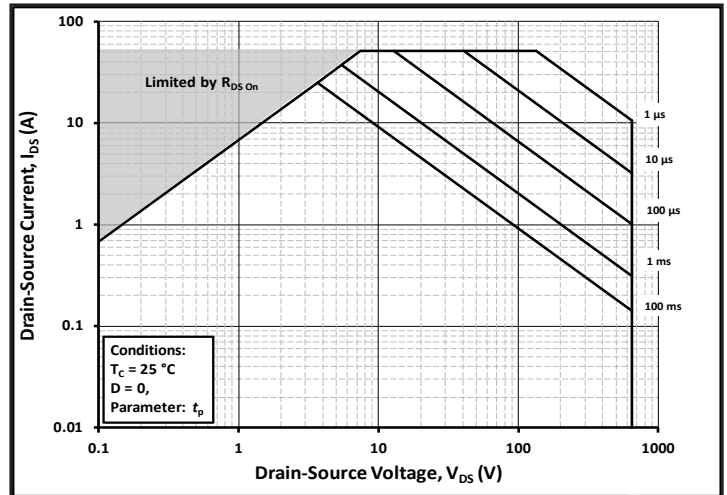


Figure 22. Safe Operating Area

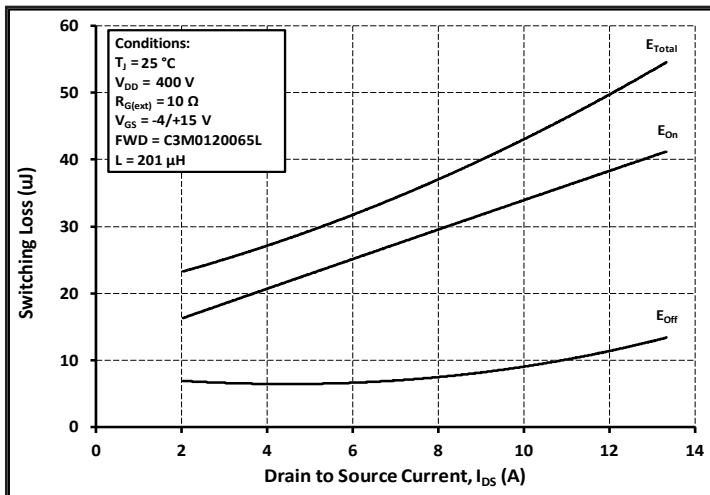


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ($V_{DD} = 400V$)

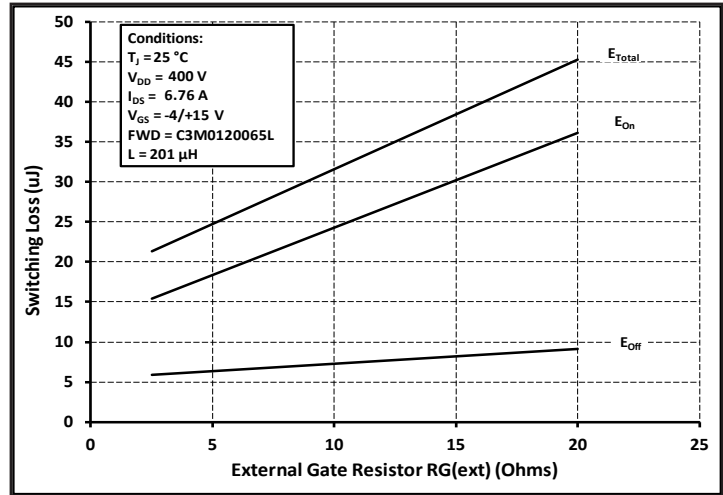


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$



Typical Performance

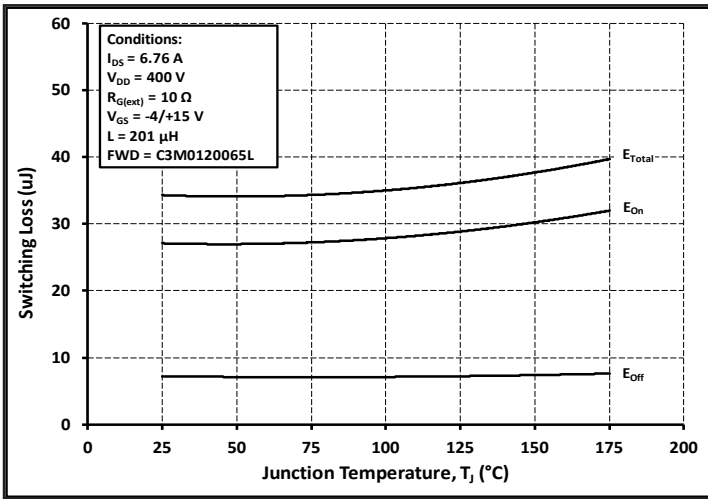


Figure 25. Clamped Inductive Switching Energy vs. Temperature

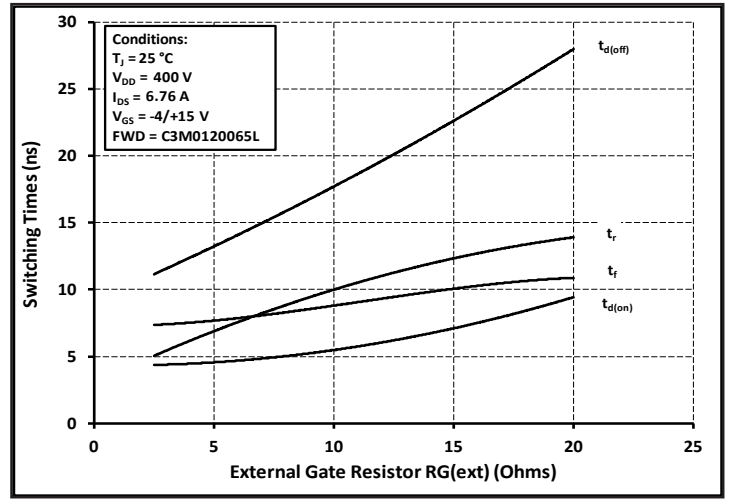


Figure 26. Switching Times vs. $R_{G(ext)}$

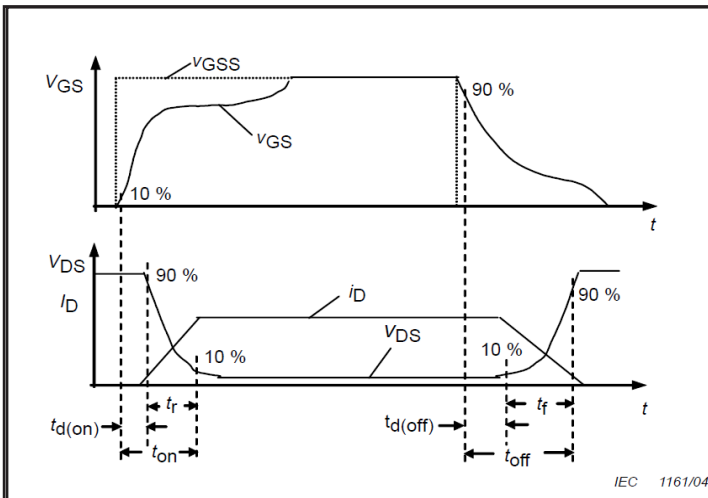


Figure 27. Switching Times Definition

Test Circuit Schematic

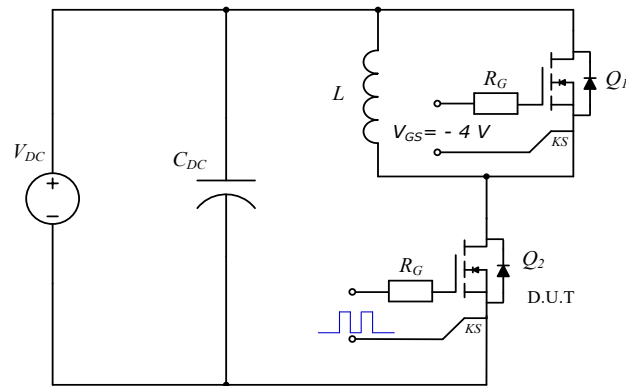
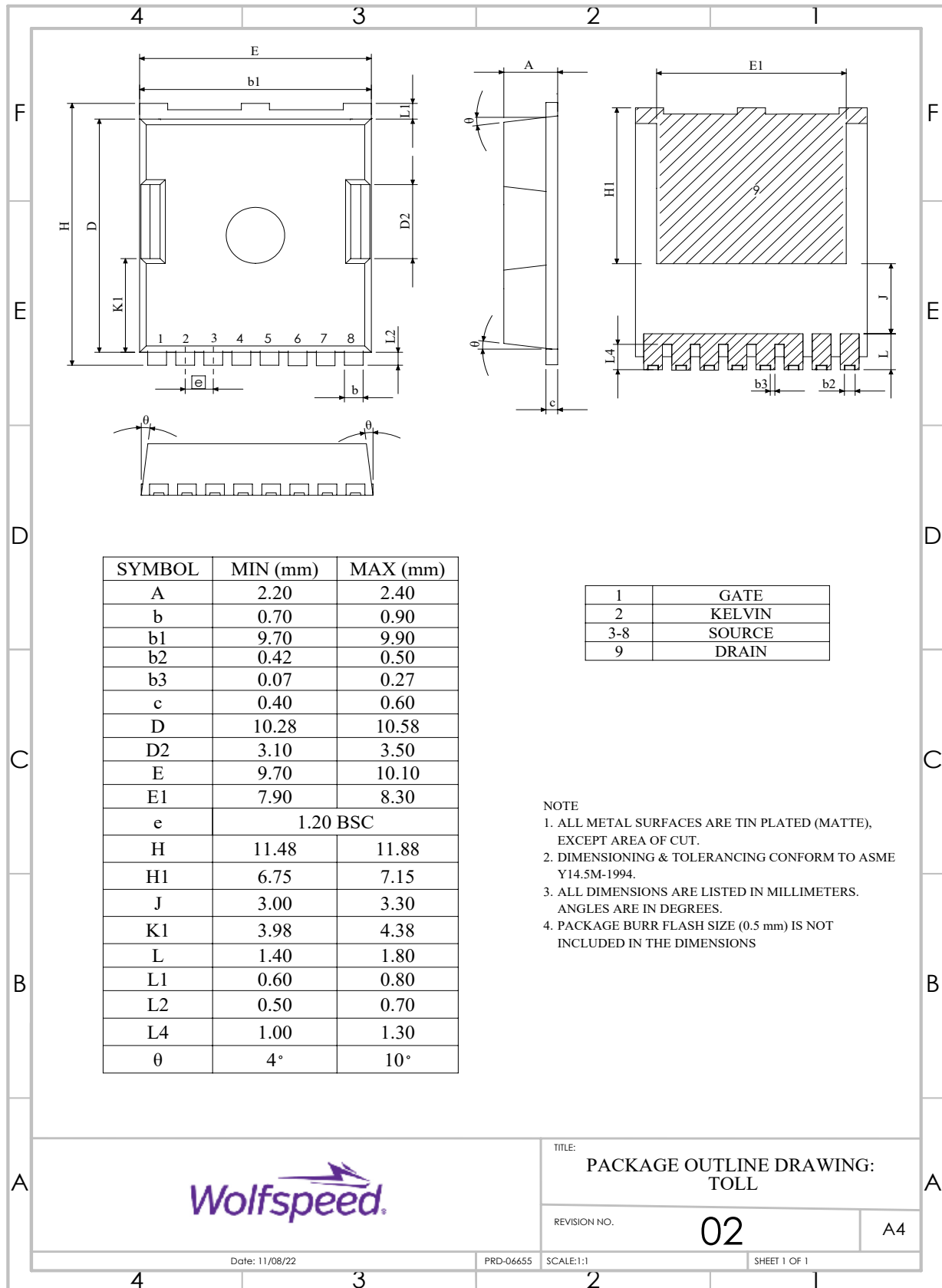


Figure 28. Clamped Inductive Switching Waveform Test Circuit

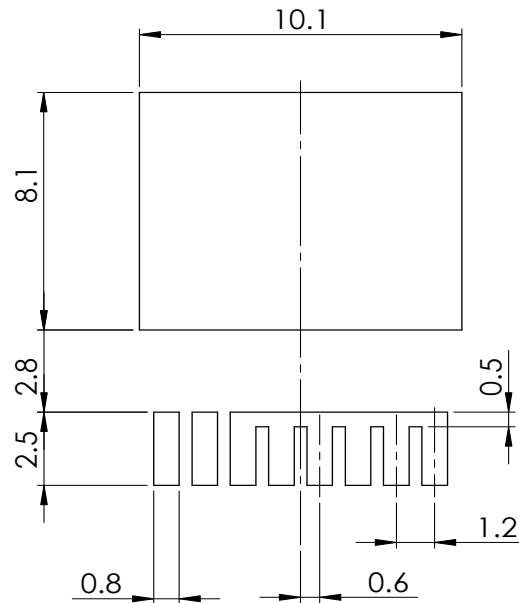
Package Dimensions





Recommended Solder Pad Layout

(Note: All Dimensions are listed in Millimeters)





Revision history

Document Version	Date of release	Description of changes
1.0	September-2022	Initial datasheet
2.0	November-2022	Correction in the placement of "E1" package dimension Orderable part number information added



Notes & Disclaimer

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