BVA3144

Medium Power Digital Variable Gain Amplifier

4400MHz – 5000MHz

Product Description

The BVA3144 is a digitally controlled variable gain amplifier (DVGA) in a 6mm x 6mm LGA package, with a frequency range of 4400 to 5000 MHz and an operating VDD of 5.0V.

BVA3144 is high performance and high dynamic range makes it ideally suited for use in 5G/LTE wireless infrastructure and other high performance wireless RF applications.

The BVA3144 is an integration of a high performance digital 7bit step attenuator (DSA) that provides a 31.75 dB attenuation range in 0.25 dB steps, and high linearity broadband gain block amplifiers featuring high ACP and P1dB.

The BVA3144 digital control interface supports serial programming of the attenuator, and includes the reference gain (max gain, bypass) state on the Parallel programing .

The BVA3144 is integrated of two gain blocks (AMP1, AMP2), a digital step attenuator (DSA) and high linearity amplifier (AMP3).

Implementation requires only a few external components, such as matching capacitors on the Input and Output pins. (Don't need DC Blocking Capacitor)

Figure 1. Functional Block Diagram

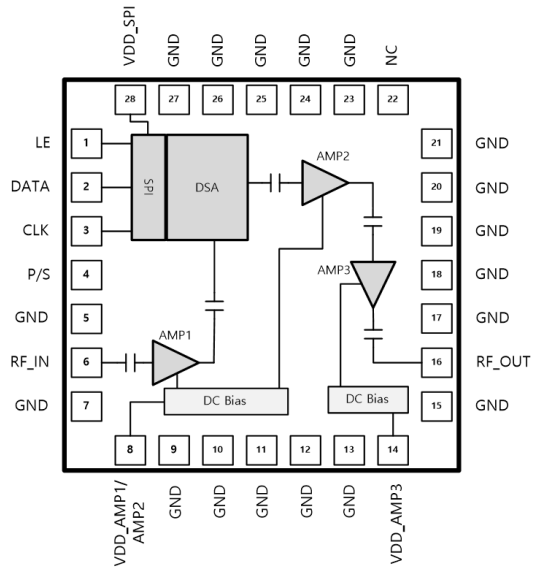


Figure 2. Package Type

28-Pin 6mm x 6mm x 0.95mm LGA

Device Features

- 28-Pin 6mm x 6mm x 0.95mm LGA Package
- Integrated Amp1 + DSA + Amp2 + Amp3
- A Single +5.0V supply
- 4300-5000MHz Frequency Range
- 36.3dB Gain @ 4.65GHz
- 4.0dB Noise Figure at max gain setting @ 4.65GHz
- 26.2dBm Output P1dB @ 4.65GHz
- 41dBm Output IP3 @ 4.65GHz
- ACP at 4.65GHz, 50dBc
  - Pre5G 100MBW (±100MHz offset) ≥ 14.5dBm
  - LTE 20MBW(FDD E-TM3.1, 100RB, ±20MHz offset) ≥16.0dBm
- Attenuation: 0.25 dB step up to 31.75 dB
- Glitch-less attenuation state transitions
- High attenuation accuracy
  ±(0.5dB + 6% x Atten) @ 4.4-5.0GHz
- Programming Interface
  - Serial / Parallel (Bypass Mode)
- Lead-free/RoHS2-compliant SiP LGA SMT Package

Application

- 5G/4G/3G wireless Infrastructure
- Small Cells
- Repeaters

Table 1. Electrical Specifications[1]

Typical Performance Data @ 25°and VDD = 5.0V, ATT=0dB state (Max. gain) unless otherwise noted.
(De-embedded PCB and connector Loss)

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			4400		5000	MHz
Gain		Attenuation = 0dB, at 4650MHz	33.8	36.3	38.8	dB
Attenuation Control range		0.25dB step		0 - 31.75		dB
Attenuation Step				0.25		dB
Attenuation Accuracy	4.4GHz—5GHz	Any bit or bit combination	−(0.5 +6% of ATT. setting)		+ (0.5 +6% of ATT. setting)	dB
Return loss	Input Return Loss	Attenuation = 0dB		10		dB
	Output Return Loss			15		
Output Power for 1dB Compression		Attenuation = 0dB , at 4650MHz		26		dBm
Output Third Order Intercept Point		Attenuation = 0dB, at 4650MHz	36	41		dBm
		Pout= +5dBm/tone △f = 1 MHz.				
Noise Figure		Attenuation = 0dB, at 4650MHz		4.0		dB
Switching time		50% CTRL to 90% or 10% RF		275		ns
Supply voltage (VDD)		DSA	3.3	5	5.5	V
		AMP	4.85	5	5.15	V
Supply Current		AMP1+DSA+AMP2+AMP3	270	310	350	mA
Control Interface		Serial mode		8		Bit
Control Voltage		Digital input high	1.17		3.6	V
		Digital input low	-0.3		0.63	V
Impedance				50		Ω

Table 2. Typical RF Performance[1]

Parameter	Frequency			Unit
Frequency	**4450**	**4650**	**4950**	**MHz**
Gain	36	36.3	35.8	dB
S11	-8	-10	-14	dB
S22	-15.5	-16	-18	dB
OIP3[2]	41	41	40	dBm
P1dB	26.8	26.1	25.9	dBm
LTE20M ACP[3]	63	64	62	dBc
Pre5G 100M ACP[4]	57	56.5	56	dBc
N.F	3.8	4	4.2	dB

[1] Device performance _ measured on a BeRex evaluation board at 25°C, Vcc=+5.0V, 50 Ω system. measure on Evaluation Board De-embedded PCB and Connector Loss.

[2] OIP3 _ measured with two tones at an output of +5 dBm per tone separated by 1 MHz.

[3] LTE set-up: 3GPP LTE, FDD E-TM3.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. Output power 7dBm. Applied the Noise correlation function of Instrument.

[4] 5G set-up: 3GPP Pre5G, 100MHz BW, ±100MHz offset. Output Power 7dBm. Applied the Noise correlation function of Instrument.

Table 3. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Unit
Supply Voltage(VCC)	-0.3		5.5	V
Supply Current			580	mA
Digital input voltage	-0.3		3.6	V
Maximum input power			+20	dBm
Storage Temperature	-55		+150	℃

[1] Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions[1]

Parameter	Min	Typ	Max	Unit
Bandwidth	4400		5000	MHz
Supply Voltage(VCC)	4.85	5	5.15	V
Operating Temperature	-40		+105	˚C
Thermal Resistance (θ_{JC})		21.77		˚C/W

[1] Operation of this device above any of these parameters may result in permanent damage.

Programming mode

Serial / Parallel (Bypass) Selection

Either a Serial or Parallel interface can be used to control the P/S Pin. The P/S bit provides the selection, with P/S = HIGH or floating selecting the Serial interface and P/S = LOW selecting the Parallel interface (Bypass Mode, Max Gain State).

Serial Interface

The Serial interface is an 8-bit Serial-In, Parallel-Out shift register buffered by a transparent latch. The 8-bits make up the Attenuation Word that controls the DSA. **Figure 4** illustrates an example timing diagram for programming a state.

The Serial interface is controlled using three CMOS compatible signals: SI, Clock (CLK) and LE. The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. The Attenuation Word truth table is listed in **Table 5**. A programming example of the serial register is illustrated in **Figure 3**. The Serial timing diagram is illustrated in **Figure 4**.

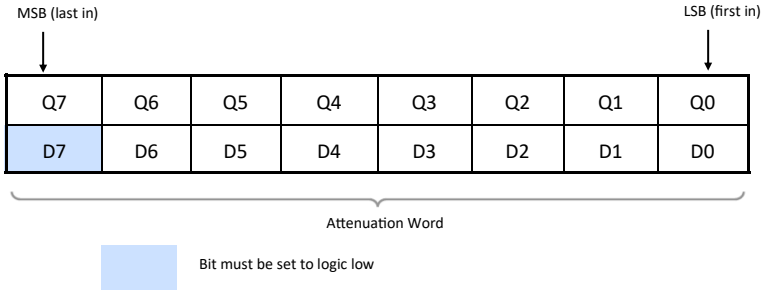
Table 5. Serial Attenuation word Truth Table

Attenuation Word								Attenuation setting
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Max. Gain
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

Power-up Control Settings

The BVA3144 will always initialize to the maximum attenuation setting (Atten=31.75dB) on power-up for the Serial mode and will remain in this setting until the user latches in the next programming word.

Figure 3. Serial Register Map



The attenuation word is derived directly from the value of the attenuation state. To find the attenuation word, multiply the value of the state by four, then convert to binary.

For example, to program the 12.5dB state;

4 x 12.5 = 50
50 → 00110010

Serial Input : 00110010

Figure 4. Serial Interface Timing Diagram

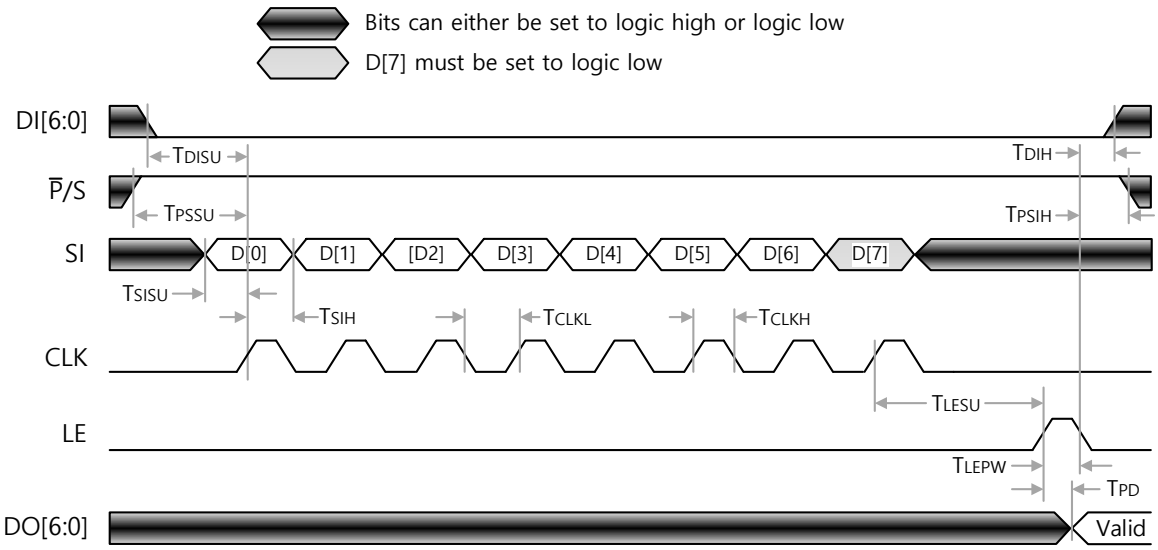


Table 6. Serial Interface AC Characteristics

VDD= 5.0V with DSA only, -40°C ≤ TA ≤ 105°C, unless otherwise specified

Symbol	Parameter	Min	Max	Unit
F_{CLK}	Serial data clock frequency		10	MHz
T_{CLKH}	Serial clock HIGH time	30		ns
T_{CLKL}	Serial clock LOW time	30		ns
T_{LESU}	Last Serial clock rising edge setup time to Latch Enable rising edge	10		ns
T_{LEPW}	Latch Enable minimum pulse width	30		ns
T_{SISU}	Serial data setup time	10		ns
T_{SIH}	Serial data hold time	10		ns
T_{DISU}	Parallel data setup time	100		ns
T_{DIH}	Parallel data hold time	100		ns
T_{PSSU}	Parallel / Serial setup time	100		ns
T_{PSIH}	Parallel / Serial hold time	100		ns
T_{ASU}	Address setup time	100		ns
T_{AH}	Address hold time	100		ns
T_{PD}	Digital register delay (internal)		10	ns

Figure 5. Pin Configuration

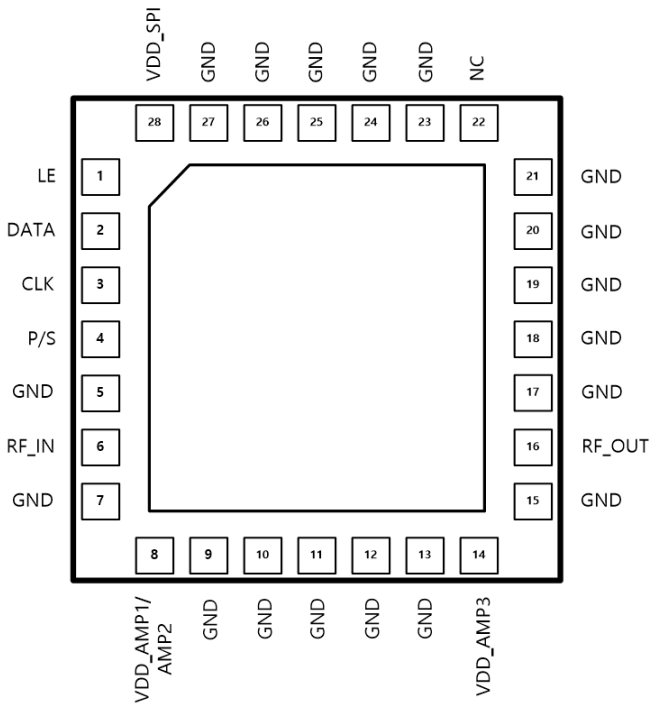


Table 7. Pin Description

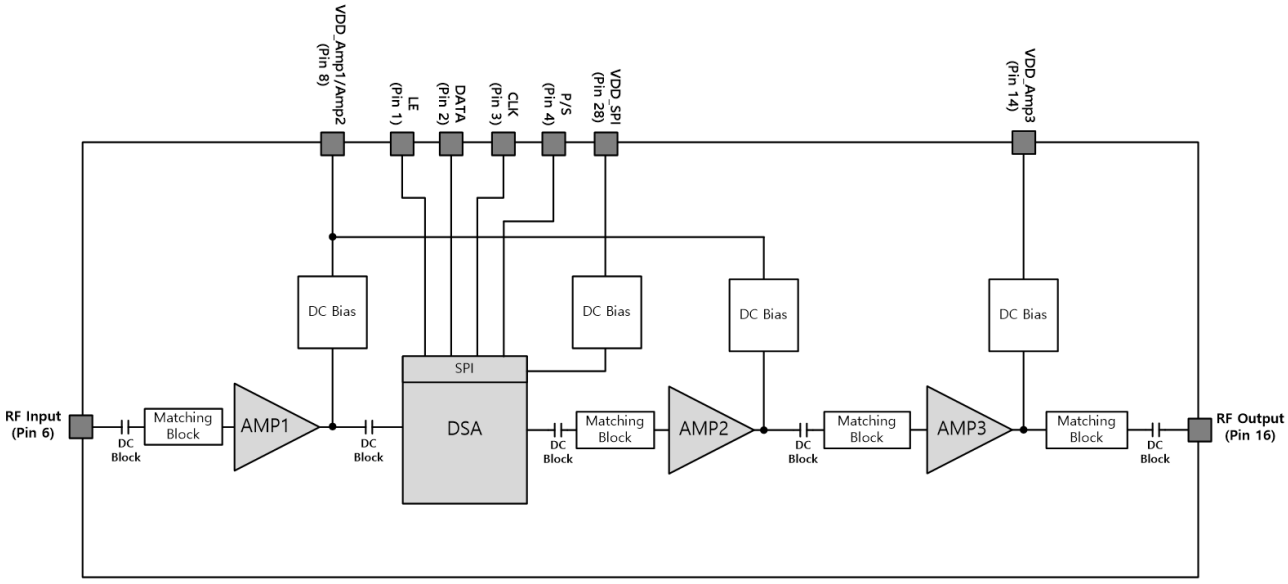
Pin	Pin name	Description
1	LE[1]	Serial Latch Enable Input. When LE is high, latch is clear and content of SPI control the attenuator. When LE is low, data in SPI is latched.
2	DATA	Serial Data Input. The data and clock pins allow the data to be entered serially into SPI and is independent of Latch state.
3	CLK	Serial Clock Input.
4	P/S	The P/S bit provides this selection, P/S=Low selecting the Parallel Interface which is the Max. Gain state (Bypass Mode, ATT=0dB) and either P/S=High selecting or floating for the Serial Interface.
6	RF IN	RF Input, matched to 50 ohm. Internally DC blocked.
8	VDD_AMP1/AMP2	Supply Voltage to AMP1 and AMP2. This pin is connected internally to bypass capacitors followed by inductor inside the module.
14	VDD_AMP3	Supply Voltage to AMP3. This pin is connected internally to bypass capacitors followed by inductor inside the module.
16	RF OUT	RF output, matched to 50 ohm. Internally DC blocked.
22	N/C	No connect or open. This pin is not connected.
28	VDD_SPI	SPI and DSA DC supply. This pin is connected to bypass capacitor internally.
5, 7, 9-13, 15 17-21,23-27	GND	RF/DC Ground
Backside Pad	GND	RF/DC Ground

Note: 1. LE must be Pulled-up to 1.17V—3.6V to use the Bypass Mode when P/S = Low (Bypass mode, ATT=0dB)

Figure 6. Internal Function Block Diagram

The BVA3144 is integrated of two gain block (AMP1, AMP2), a digital step attenuator (DSA) and high linearity amplifier (AMP3). Additionally, the BVA3144 includes an internal bias and RF matching circuits to improve the RF performance at 4.4GHz - 5.0GHz.

The Internal structure of the Package is shown below.

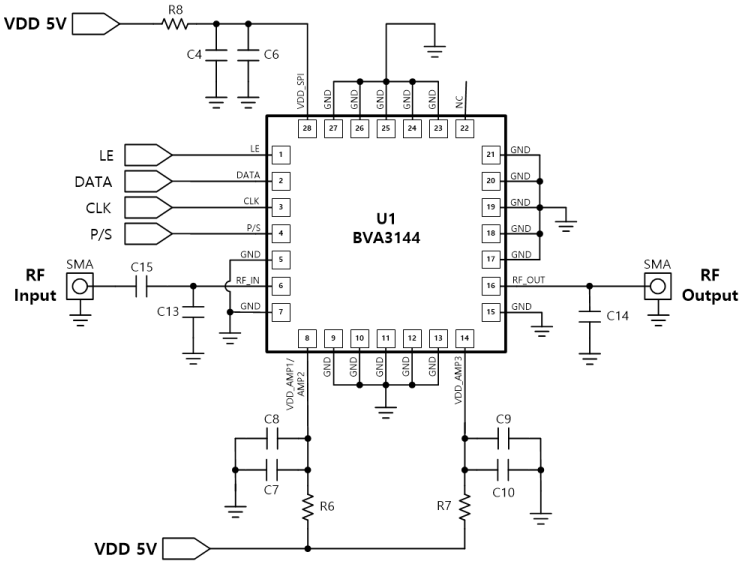


Typical RF Performance Plot - BVA3144 EVK - PCB

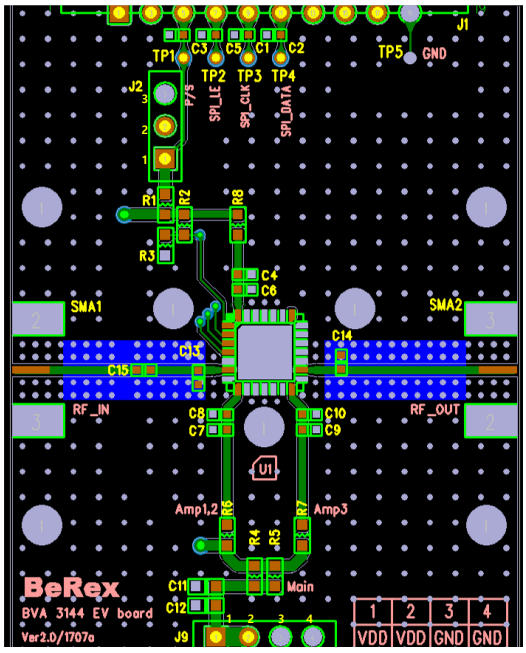
Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted and RF Circuit

Table 8. Application Circuit

Schematic Diagram



BOM			Remark
Ref	Size	Value	
C4	0402	1 uF	
C6	0402	100 pF	
C7	0402	1 uF	
C8	0402	100 pF	
C9	0402	1 uF	
C11	0402	100 pF	
C13	0402	0.3 pF	
C14	0402	0.5 pF	
C15	0402	1.2pF	
R6	0603	0 Ω	
R7	0603	0 Ω	
R8	0603	0 Ω	



NOTE

1. C1, C2, C3, C5, R1 are NC
2. R2 = 100 KΩ, R3=200 KΩ
3. R4, R5 = 0 Ω
4. C11 = 100pF, C12=1uF
5. J2 Information
   - Not connected (Floating) : Serial Mode
   - Connected 1-2 : Serial Mode
   - Connected 2-3 : Bypass mode (Max Gain State)
6. J9 Information
   - Pin 1, 2 : 5Vdc
   - Pin 3, 4 : Ground

Typical RF Performance Plot - BVA3144 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Table 9. Typical Performance : 4650MHz

parameter		Typical Values		Units
Frequency	**4650**	**4650**	**4650**	**MHz**
VDD	4.85	5	5.15	Vdc
Current	290	310	330	mA
Gain	36.2	36.3	36.4	dB
S11	-10	-10	-10	dB
S22	-16	-16	-16	dB
OIP3[1]	40	41	41.5	dBm
P1dB	25.8	26.1	26.3	dBm
Noise Figure	4.1	4.1	4.1	dB
LTE20MHz ACP[2]	63.5	64	64.5	dBc
Pre5G 100MHz ACP[3]	56.5	56.5	56.6	dBc

[1] OIP3 _ measured with two tones at an output of 5 dBm per tone separated by 1 MHz.

[2] LTE set-up: 3GPP LTE, FDD E-TM3.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. Output Power 7dBm. Applied the Noise correlation function of Instrument.

[3] Pre5G set-up: 3GPP Pre5G, 100MHz BW, ±100MHz offset. Output Power 7dBm. Applied the Noise correlation function of Instrument.

Figure 7. Gain vs Frequency @Max Gain state

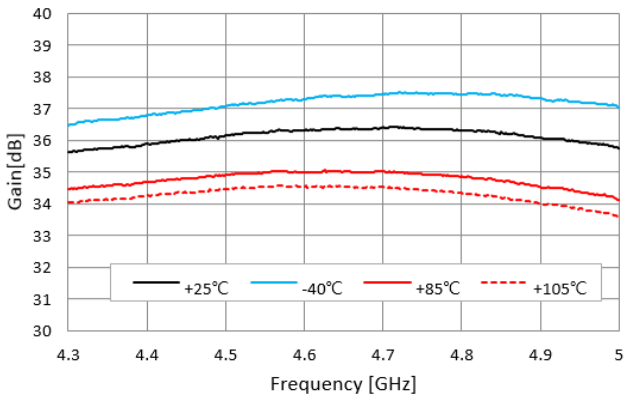


Figure 8. Gain vs Frequency @Min Gain state

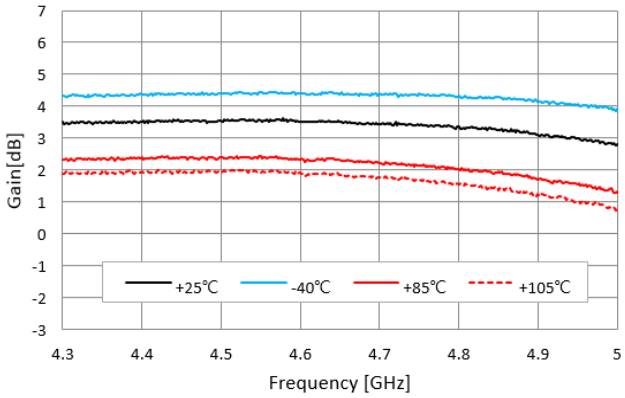


Figure 9. Gain vs VDD @Max Gain state

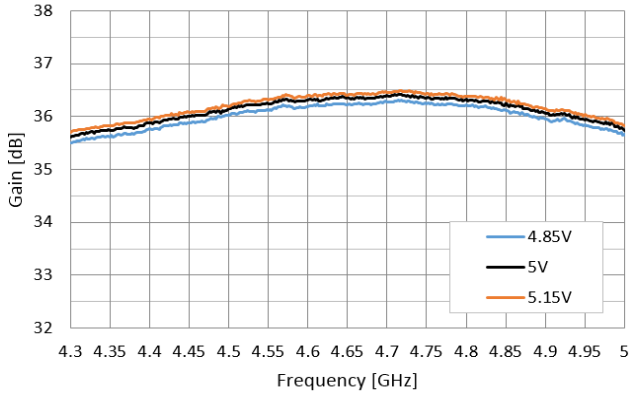
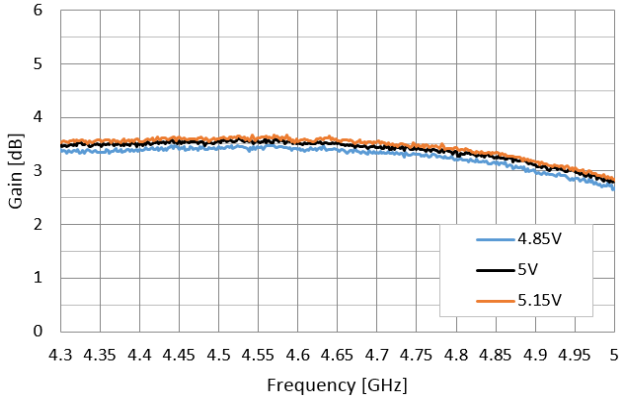


Figure 10. Gain vs VDD @Min Gain state



Typical RF Performance Plot - BVA3144 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 11. Input Return Loss vs Frequency @Max Gain State

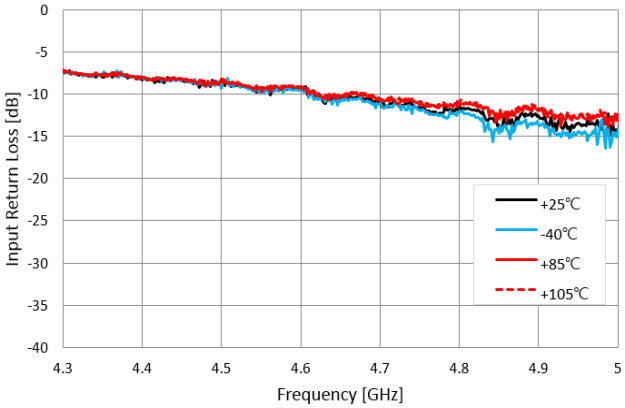


Figure 12. Input Return Loss vs Frequency @Min Gain State

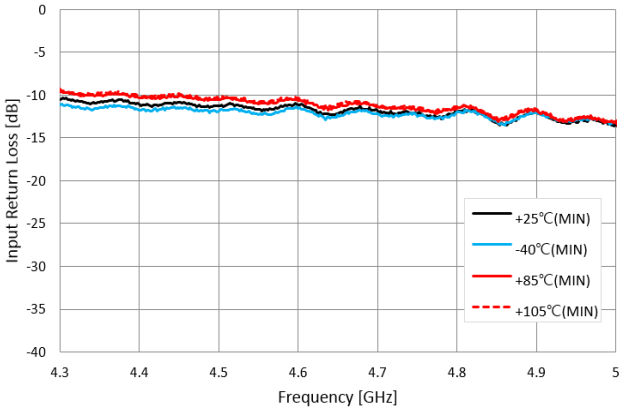


Figure 13. Output Return Loss vs Frequency @Max Gain State

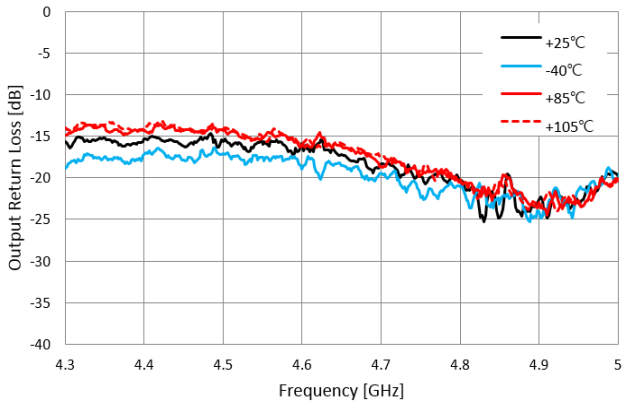


Figure 14. Output Return Loss vs Frequency @Min Gain State

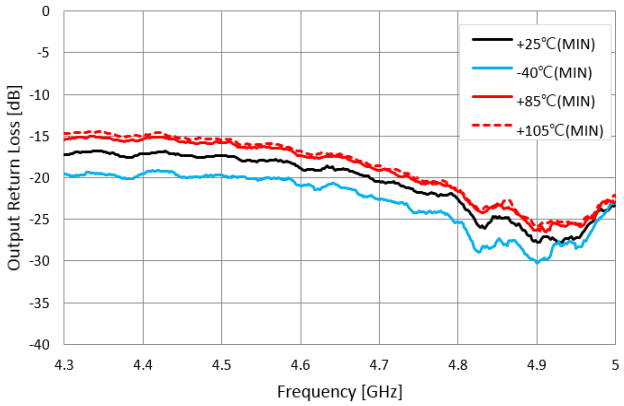


Figure 15. Gain vs Attenuation Settings

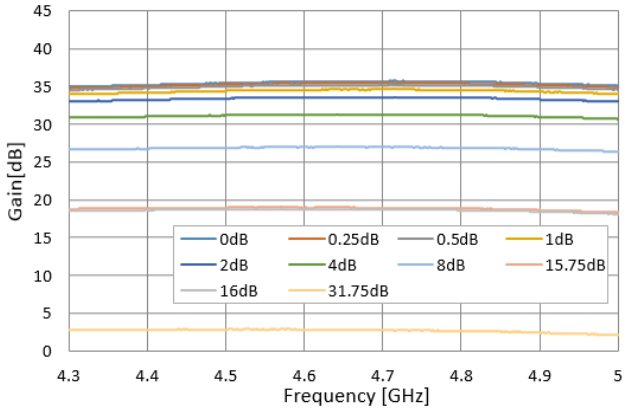
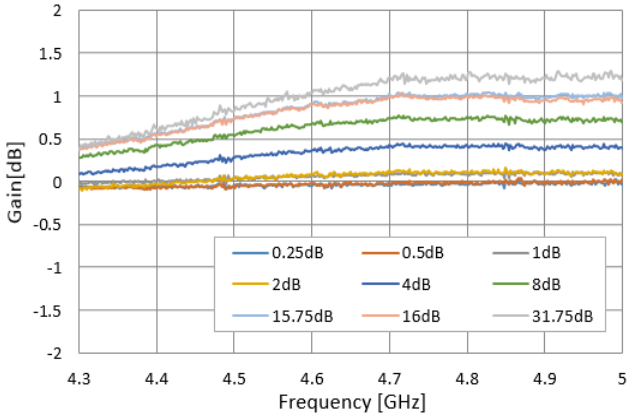


Figure 16. Attenuation Error vs Frequency



Typical RF Performance Plot - BVA3144 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 17. Attenuation Error vs Temp vs Attenuation Settings @ 4650MHz

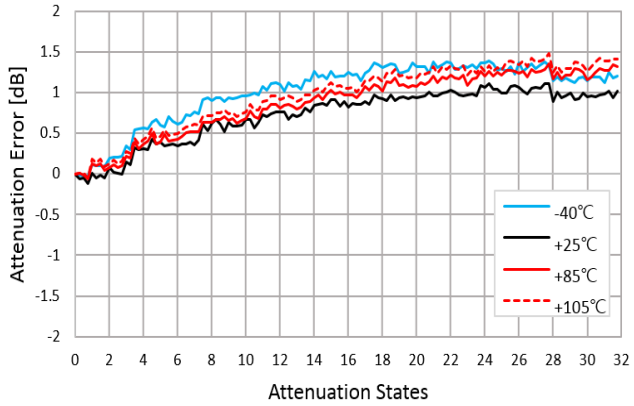


Figure 18. Attenuation Error vs Frequency vs Attenuation Settings

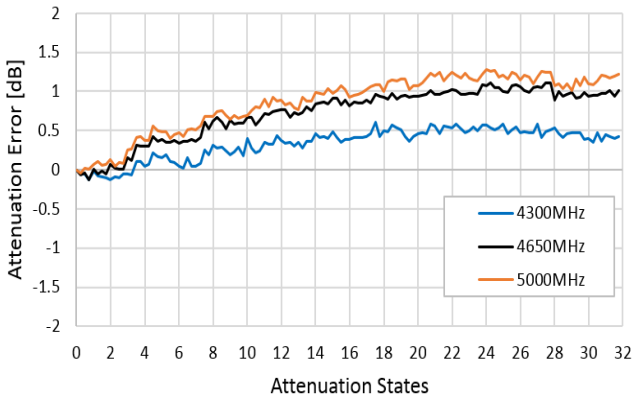


Figure 19. OIP3 vs Frequency vs Output Power
ATT=0dB (Max Gain) , 1MHz interval

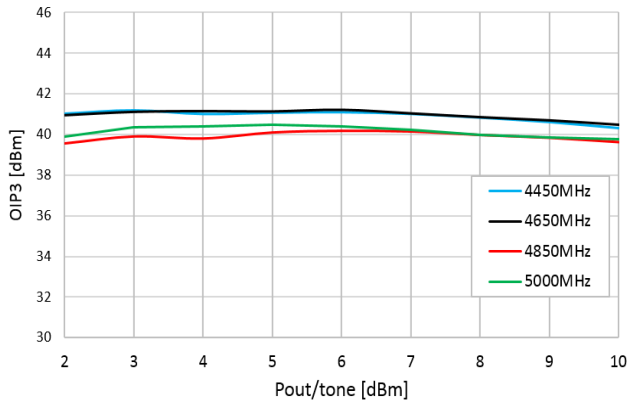


Figure 20. OIP3 vs Frequency vs Output Power
ATT = 15dB , 1MHz interval

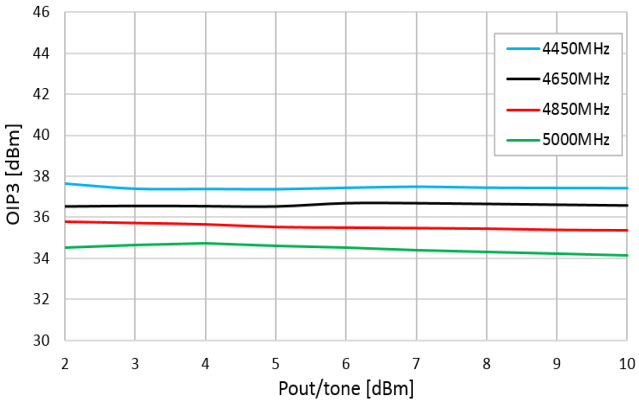


Figure 21. OIP3 vs VDD vs Output Power
Fo = 4650MHz, ATT=0dB (Max Gain) , 1MHz interval

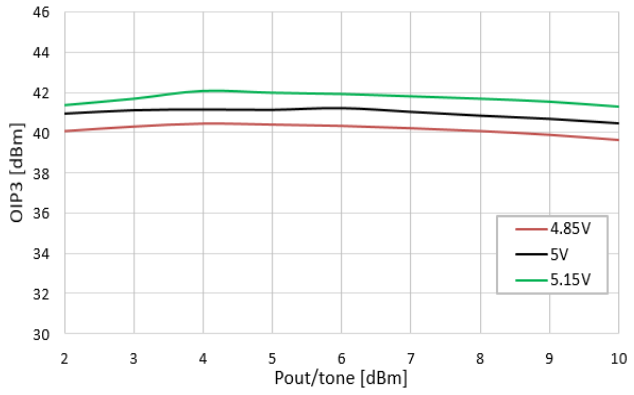
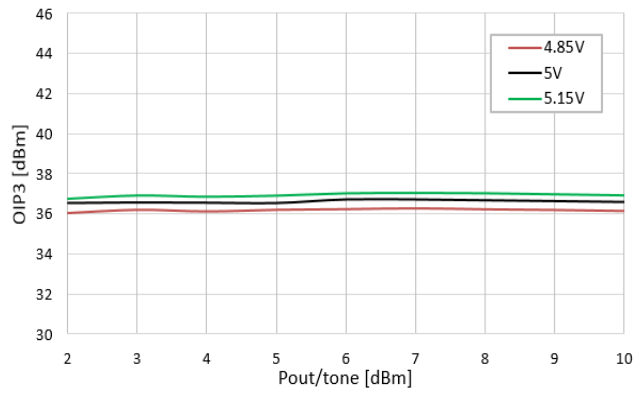


Figure 22. OIP3 vs VDD vs Output Power
Fo = 4650MHz, ATT=15dB, 1MHz interval



Typical RF Performance Plot - BVA3144 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 23. OIP3 vs Temp. vs Output Power

Fo = 4650MHz, ATT=0dB (Max Gain) , 1MHz interval

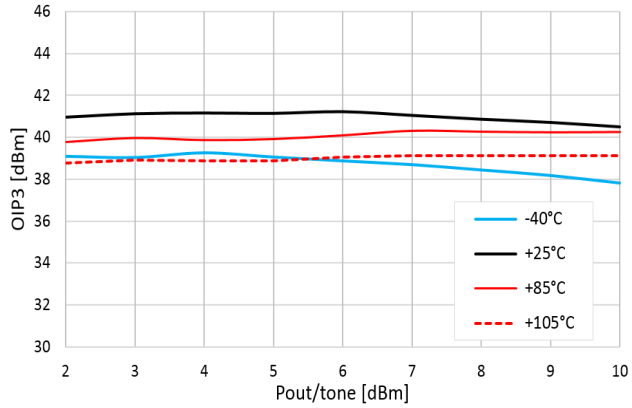


Figure 24. Pin-Pout-Gain (OP1dB)

@ 4650MHz

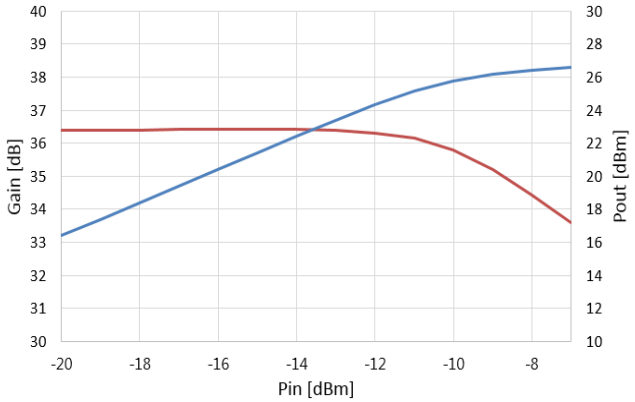


Figure 25. OP1dB vs Temp vs Frequency

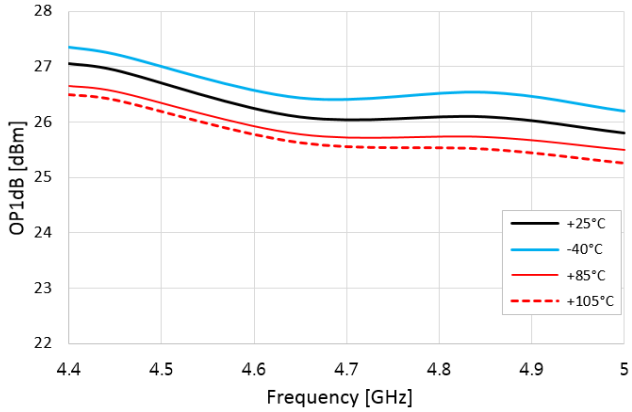


Figure 26. OP1dB vs VDD vs Frequency

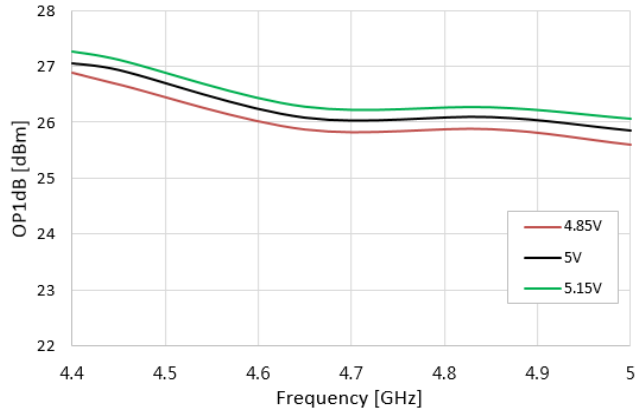


Figure 27. ACP vs Frequency vs Pout

ATT=0dB (Max Gain), Pre5G 100MBW

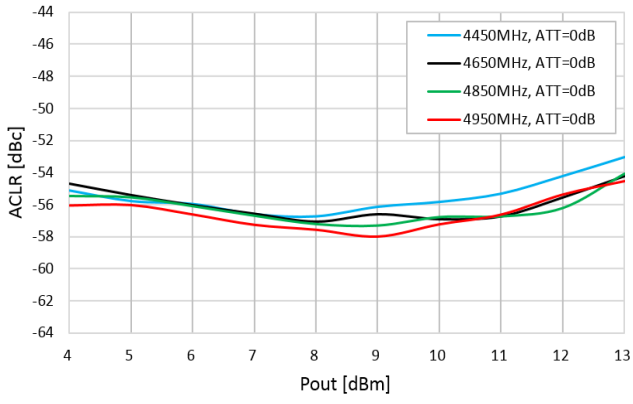
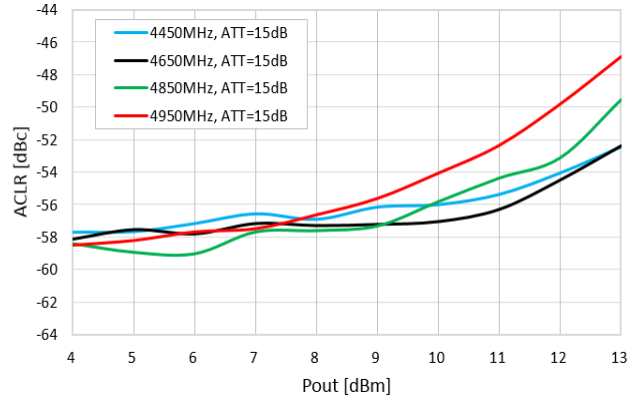


Figure 28. ACP vs Frequency vs Pout

ATT=15dB, Pre5G 100MBW



Typical RF Performance Plot - BVA3144 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 29. ACP vs VDD vs Pout

F0=4650MHz, ATT=0dB (Max Gain), Pre5G 100MBW

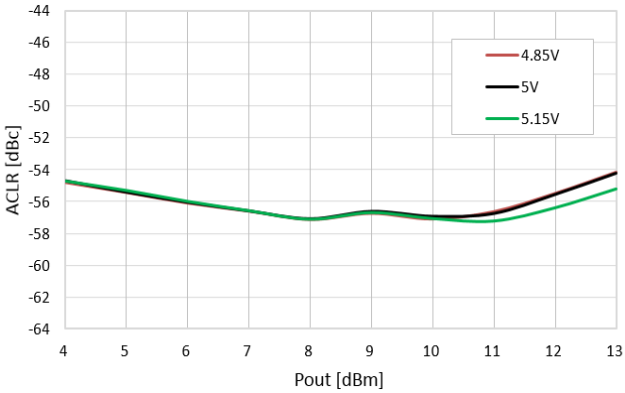


Figure 30. ACP vs VDD vs Pout

F0=4650MHz, ATT=15dB, Pre5G 100MBW

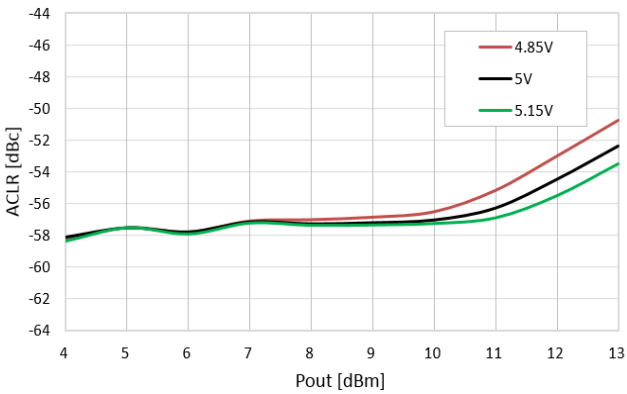


Figure 31. ACP vs Temp. vs Pout

Fo = 4650MHz, ATT=0dB (Max Gain), Pre5G 100MBW

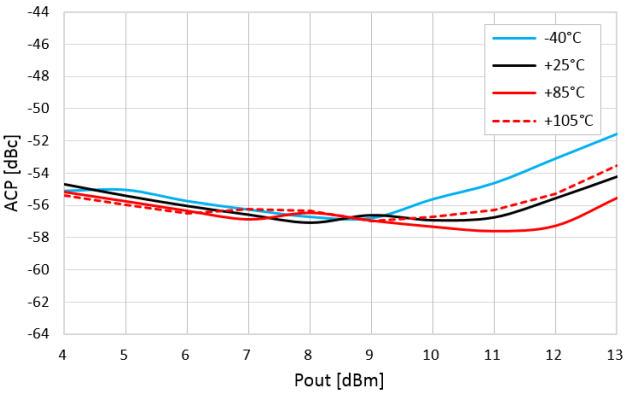
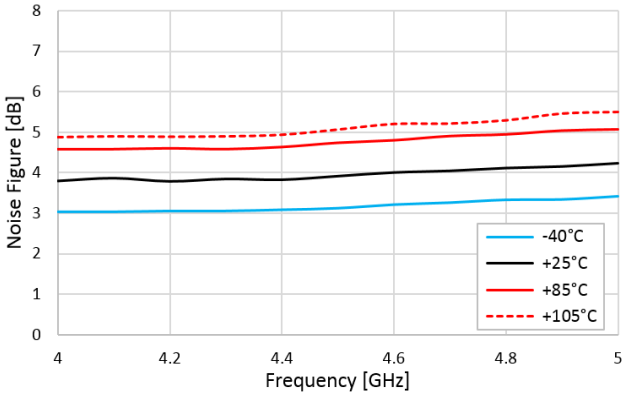


Figure 32. Noise Figure vs Temp vs Frequency @ Max Gain State

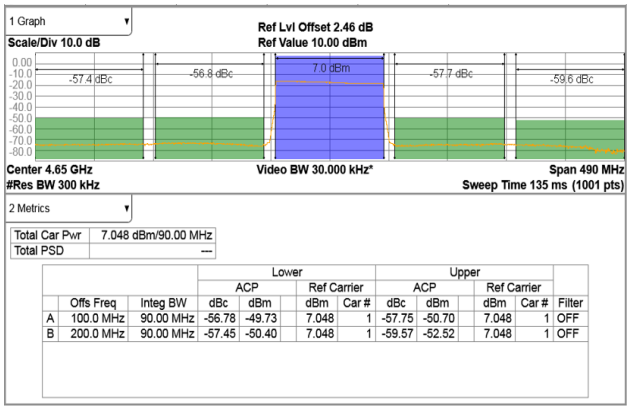


Typical RF Performance Plot - BVA3144 EVK

Typical Performance Data @ 25°and VDD = 5.0V unless otherwise noted. (All data de-embedded PCB and Connector Loss)

Figure 33. ACP Plot

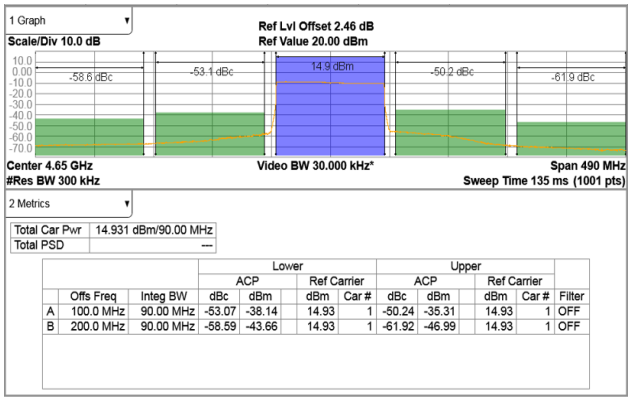
@ 4650MHz, 7dBm, Pre5G 100MBW



			Lower ACP		Lower Ref Carrier		Upper ACP		Upper Ref Carrier		
	Offs Freq	Integ BW	dBc	dBm	dBm	Car #	dBc	dBm	dBm	Car #	Filter
A	100.0 MHz	90.00 MHz	-56.78	-49.73	7.048	1	-57.75	-50.70	7.048	1	OFF
B	200.0 MHz	90.00 MHz	-57.45	-50.40	7.048	1	-59.57	-52.52	7.048	1	OFF

Figure 34. ACP Plot

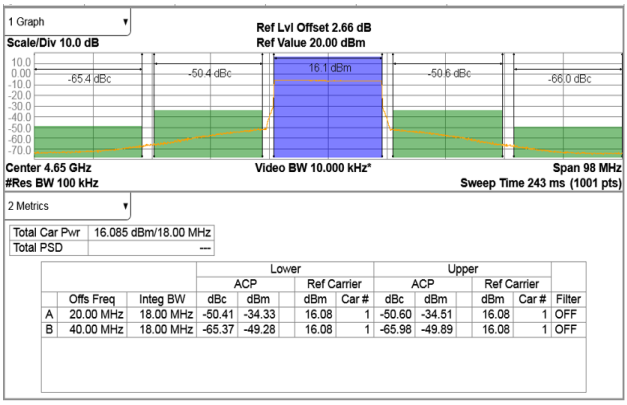
@ 4650MHz, 50dBc, Pre5G 100MBW



			Lower ACP		Lower Ref Carrier		Upper ACP		Upper Ref Carrier		
	Offs Freq	Integ BW	dBc	dBm	dBm	Car #	dBc	dBm	dBm	Car #	Filter
A	100.0 MHz	90.00 MHz	-53.07	-38.14	14.93	1	-50.24	-35.31	14.93	1	OFF
B	200.0 MHz	90.00 MHz	-58.59	-43.66	14.93	1	-61.92	-46.99	14.93	1	OFF

Figure 35. ACP Plot

@ 4650MHz, 50dBc, LTE20MHz (E-TM1.1 100RB)



			Lower ACP		Lower Ref Carrier		Upper ACP		Upper Ref Carrier		
	Offs Freq	Integ BW	dBc	dBm	dBm	Car #	dBc	dBm	dBm	Car #	Filter
A	20.00 MHz	18.00 MHz	-50.41	-34.33	16.08	1	-50.60	-34.51	16.08	1	OFF
B	40.00 MHz	18.00 MHz	-65.37	-49.28	16.08	1	-65.98	-49.89	16.08	1	OFF

Figure 36. Evaluation Board Schematic

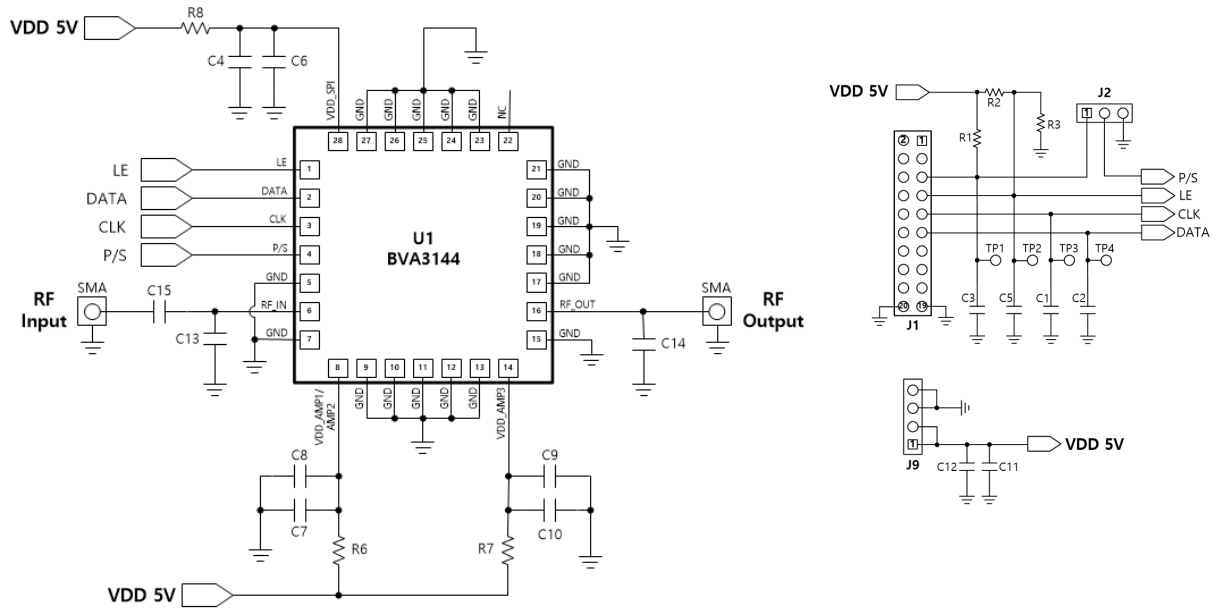
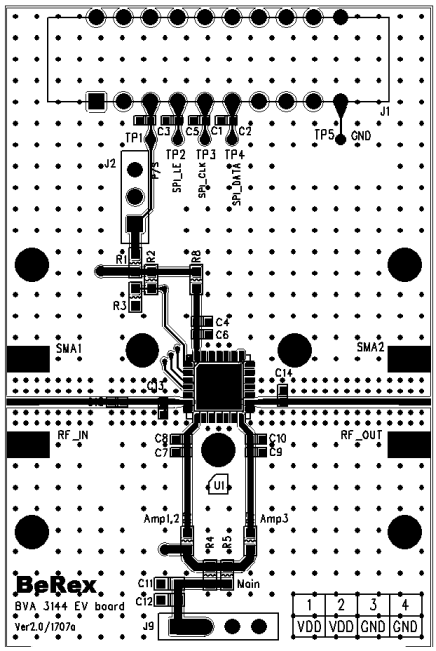


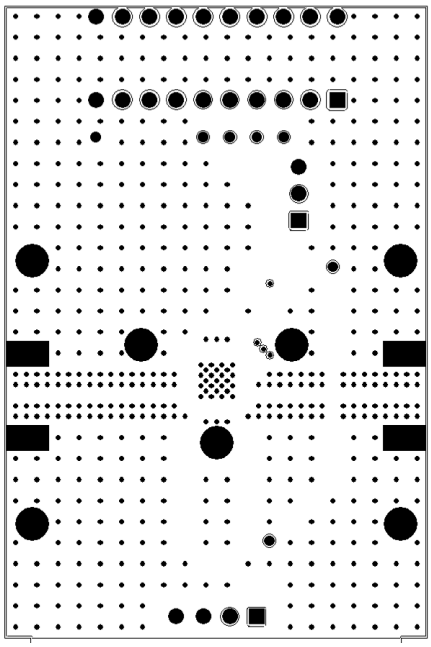
Table 10. Bill of material

No.	Ref. Number	Value	Description	Manufacturer
1	R2	100KΩ	Resistor, 0603, Chip, 5%	KOA Speer
2	R3	200KΩ	Resistor, 0603, Chip, 5%	KOA Speer
3	R6	0Ω	Jumper Resistor, 0603, Chip	KOA Speer
4	R7	0Ω	Jumper Resistor, 0603, Chip	KOA Speer
5	R8	0Ω	Jumper Resistor, 0603, Chip	KOA Speer
6	C4	100nF	Capacitor, 0402, Chip, 5%	Murata
7	C6	100pF	Capacitor, 0402, Chip, 5%	Murata
8	C7	100nF	Capacitor, 0402, Chip, 5%	Murata
9	C8	100pF	Capacitor, 0402, Chip, 5%	Murata
10	C9	100pF	Capacitor, 0402, Chip, 5%	Murata
11	C10	100nF	Capacitor, 0402, Chip, 5%	Murata
12	C11	1uF	Capacitor, 0603, Chip, 5%	Murata
13	C12	1nF	Capacitor, 0603, Chip, 5%	Murata
14	C13	0.3pF	Capacitor, 0402, Chip, ±0.1pF	Murata
15	C14	0.5pF	Capacitor, 0402, Chip, ±0.1pF	Murata
16	C15	1.2pF	Capacitor, 0402, Chip, ±0.2pF	Murata
17	SMA1	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
18	SAM2	SMA	SMA(F) Connector, PCB Mount, PSF-S01-007	Gigalane
19	J1	20pin	Receptacle Connector, 5-532955-3, Female,RT/A Dual	AMP Connectors
20	J2	3pin	2.54mm Breakaway Male Header, Straight, Black	
21	J9	4pin	2.54mm Breakaway Male Header, Straight, Black	
22	R1,C1,C2,C3,C5	NC	Not connected	

Figure 37. Evaluation Board Layout



[Top View]



[Bottom View]

Figure 38. Evaluation Board PCB Layer Information

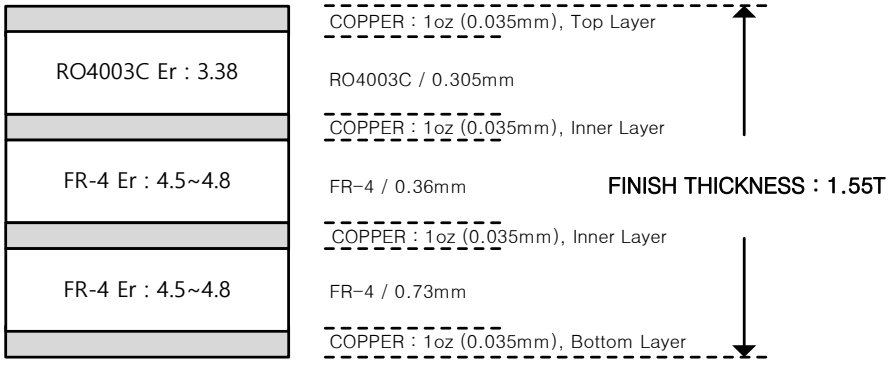


Figure 39. Suggested PCB Land Pattern and PAD Layout

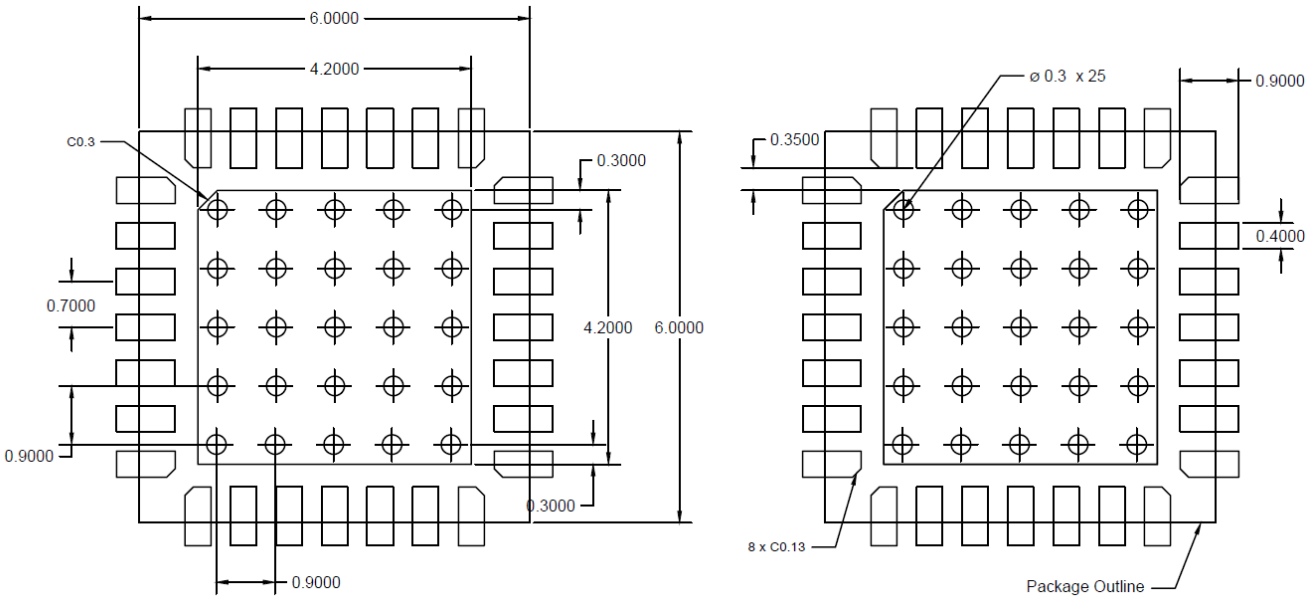
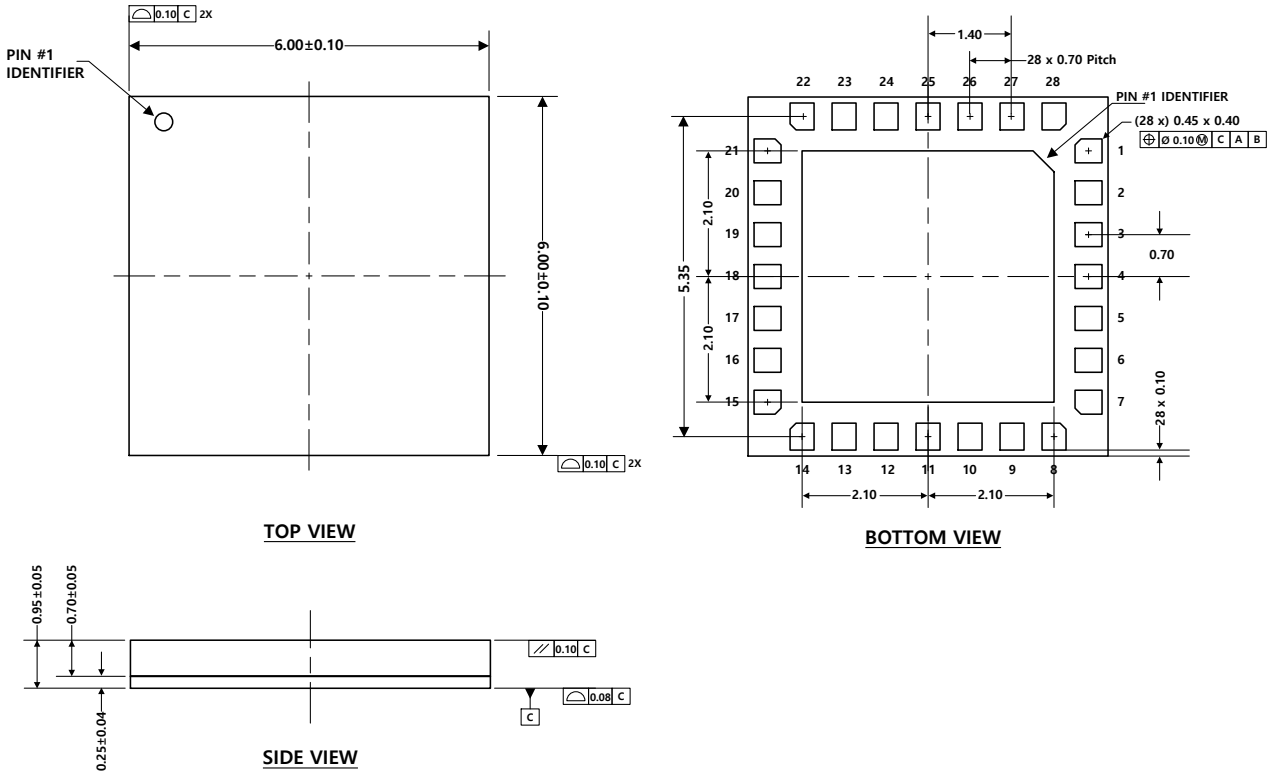


Figure 40. Packing Outline Dimension



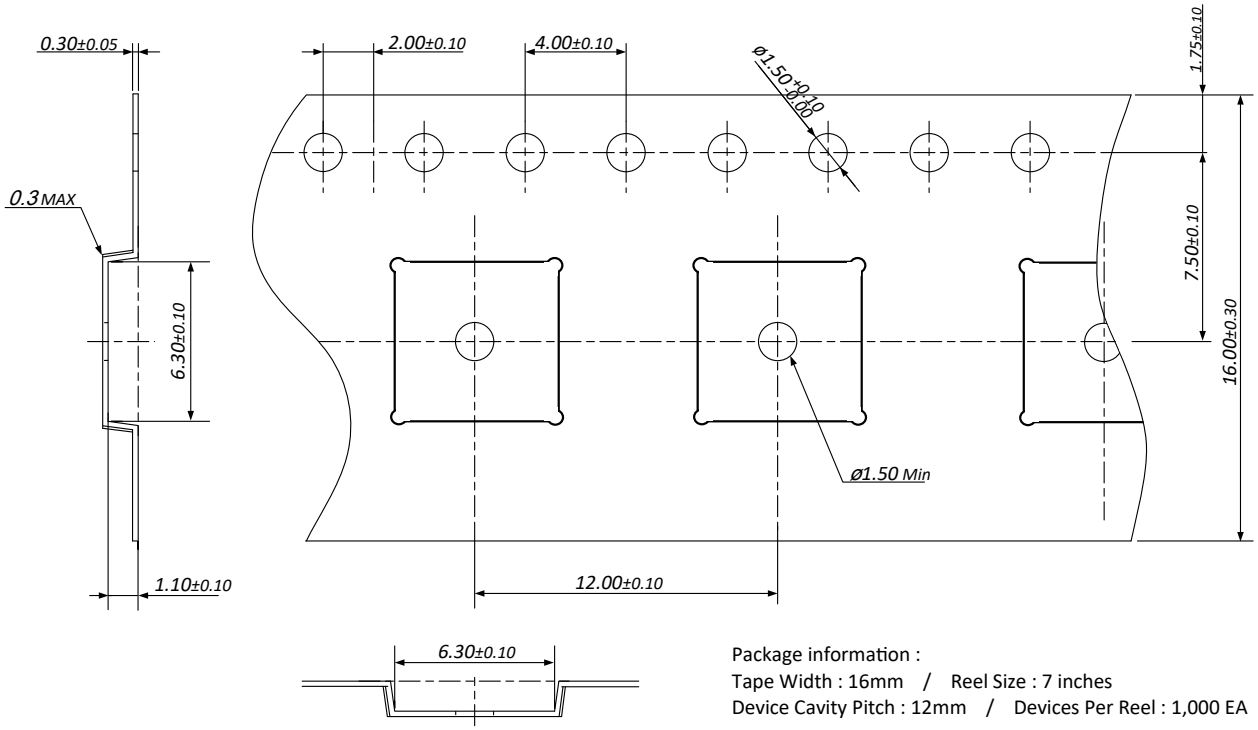
Notes

1. All dimensions are in millimeters. Angles are in degrees
2. Dimension and tolerancing conform to ASME Y14.5M-1994.

Figure 41. Package Marking Information

YY = Year
WW = Working Week
XXX = Wafer Lot Number

Figure 42. Tape and Reel



Package information :
Tape Width : 16mm / Reel Size : 7 inches
Device Cavity Pitch : 12mm / Devices Per Reel : 1,000 EA

Lead Plating Finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating :	Class1C
Value :	Passes > 1000V
Test :	Human Body Model (HBM)
Standard :	JEDEC Standard JS-001-2017
ESD Rating :	ClassC3
Value :	Passes > 1000V
Test :	Charged Device Model (CDM)
Standard :	JEDEC Standard JESD22-C101F
MSL Rating :	MSL3 at +260°C convection reflow
Standard :	JEDEC Standard J-STD-020

Caution : ESD Sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Proper ESD procedures should be followed when handling the device.

RoHS Compliance

This part is compliant with Restrictions on the use of certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO GAGE Code :

2	N	9	6	F