BVA2140B

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Device Features

- Small 24-Pin 4 x 4 x 0.9mm QFN Package
- Integrates Amp1(Gain Block), DSA and Amp2(1/4-watt) Functionality
- Wide Power supply range of +2.7~5.5V(DSA)
- Single Fixed +5.0V supply (Amp)
- 700-4000MHz Broadband Performance
- 30.4dB Gain at 2.14GHz (Matching Circuit)
- 2.7dB Noise Figure at max gain setting at 2.14GHz(Matching Circuit)
- 25.6dBm P1dB at 2.14GHz (Matching Circuit)
- 40.2dBm OIP3 at 2.14GHz(10dBm per tone, Matching Circuit)
- LTE 20MHz Channel Power 15.5dBm at 2.14GHz (-50dBc ACLR)
- Attenuation: 0.5 dB steps to 31.5 dB
- Safe attenuation state transitions
- Monotonicity: 0.5 dB up to 4 GHz
- High attenuation accuracy (DSA to Amp)
  ±(0.3dB + 6% x Atten setting) @ 0.7~4GHz
- 1.8V control logic compatible
- Programming modes
  - Serial
- Unique power-up state selection
- Lead-free/RoHS2-compliant 24-lead 4mm x 4mm x 0.9mm QFN SMT package

24-lead 4mm x 4mm x 0.9mm QFN

Figure 1. Package Type

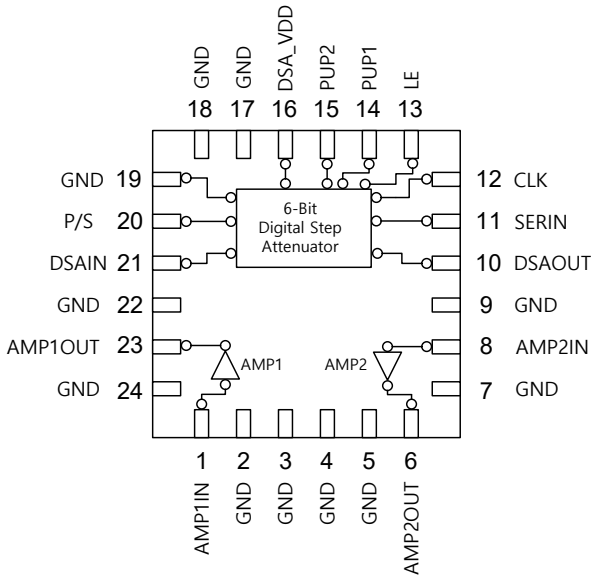

Figure 2. Functional Block Diagram

Product Description

The BVA2140B is a digitally controlled variable gain amplifier (DVGA) in a small 4x4mm QFN package, with a broadband frequency range of 700 to 4000 MHz and an operating V_{DD} of 5.0V at 150mA.

BVA2140B is high performance and high dynamic range makes it ideally suited for use in WCDMA/LTE wireless infrastructure point-to-point and other demanding wireless applications.

The BVA2140B is an integration of a high performance digital 6-step attenuator (DSA) that provides a 31.5 dB attenuation range in 0.5 dB steps, and high linearity broadband gain block amplifiers featuring high ACLR and P1.

The BVA2140B digital control interface supports serial programming of the attenuator, and includes the ability to define the initial attenuation state at power-up.

Implementation requires only a few external components, such as DC blocking capacitors on the Input and Output pins, plus a bypass capacitor and a RF choke for the Output port.

Application

- Base station/Repeater Infrastructure
- LTE/WCDMA/CDMA Wireless infrastructure and other high performance RF application
- Commercial/Industrial/Military Wireless system
- General purpose Wireless

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Table 1. Electrical Specifications[1]

Parameter		Condition	Min	Typ	Max	Unit
Operational Frequency Range			700		4000	MHz
Gain		Attenuation = 0dB, at 2140MHz		30.4		dB
Attenuation Control range		0.5dB step				dB
Attenuation Step				31.5		dB
Attenuation Accuracy	>0.7GHz-4GHz	Any bit or bit combination	±(0.3 + 6% of atten setting)			dB
Return loss (input or output port)	Input Return Loss	Attenuation = 0dB		23.6		dB
	Output Return Loss			12.2		
Output Power for 1dB Compression		Attenuation = 0dB , at 2140MHz		25.6		dBm
Output Third Order Intercept Point		Attenuation = 0dB, at 2140MHz		40.2		dBm
		Pout= +10dBm/tone △f = 1 MHz.				
Noise Figure		Attenuation = 0dB, at 2140MHz		2.7		dB
Switching time		50% CTRL to 90% or 10% RF		500	800	ns
Supply voltage		DSA	2.7		5.5	V
		AMP		5		V
Supply Current		MCM(AMP1+DSA+AMP2)		150		mA
Control Interface		Serial mode		6		Bit
Impedance				50		Ω

1. Device performance _ measured on a BeRex Evaluation board at 25°C, 50 Ω system, VDD=+5.0V, measure on Evaluation Board (AMP1 to DSA and AMP2)

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Table 2. Typical RF Performance[1]

Parameter	Frequency						Unit
	700	900	1900	2140	2650	3500	MHz
Gain	41.6	40.3	31.1	30.4	28.6	24.2	dB
S11	-17.5	-17.6	-22.2	-23.6	-19.5	-21.1	dB
S22	-7.8	-13.0	-13.4	-12.2	-12.1	-15.3	dB
OIP3[2]	40.7	46.9	41.6	40.2	38.3	36.8	dBm
P1dB	27.0	27.3	26.8	25.6	24.9	24.4	dBm
LTE 20M ACLR[3]	15.1	16.2	16.5	15.5	15.3	14.9	dBm
N.F	2.4	2.6	2.7	2.7	2.9	3.4	dB

1. Device performance _ measured on a BeRex evaluation board at 25°C, VDD=+5.0V,50 Ω system. measure on Evaluation Board (DSA to AMP)
2. OIP3 measured with two tones at an output of +10 dBm per tone separated by 1 MHz.
3. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. *ACLR Channel Power measured at –50dBc

Table 3. Absolute Maximum Ratings

Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage(V_{DD})	MCM(AMP1+DSA+AMP2)	-0.3		5.5	V
Supply Current	MCM(AMP1+DSA+AMP2)			440	mA
Digital input voltage	DSA	-0.3		3.6	V
Maximum input power	MCM(AMP1+DSA+AMP2)			+12	dBm
Storage Temperature	MCM(AMP1+DSA+AMP2)	-55		150	℃
Junction Temperature	MCM(AMP1+DSA+AMP2)			220	℃

Operation of this device above any of these parameters may result in permanent damage.

Table 4. Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
Bandwidth	MCM(AMP1+DSA+AMP2)	700		4000	MHz
Supply Voltage(V_{DD})	MCM(AMP1,AMP2)		5		V
	MCM(DSA)	2.7		5.5	V
Control Voltage	Digital input high	1.17		3.6	V
	Digital input low	-0.3		0.6	V
Ic @(V_{DD} =5V)	MCM(AMP1+DSA+AMP2)		150		mA
Operating Temperature	MCM(AMP1+DSA+AMP2)	-40		105	˚C

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Programming Options

BVA2140B can be programmed using either the parallel or serial interface, which is selectable via P/S pin(Pin20).
Serial mode is selected by floating P/S or pulling it to a voltage logic High and parallel mode is selected by setting P/S to logic low

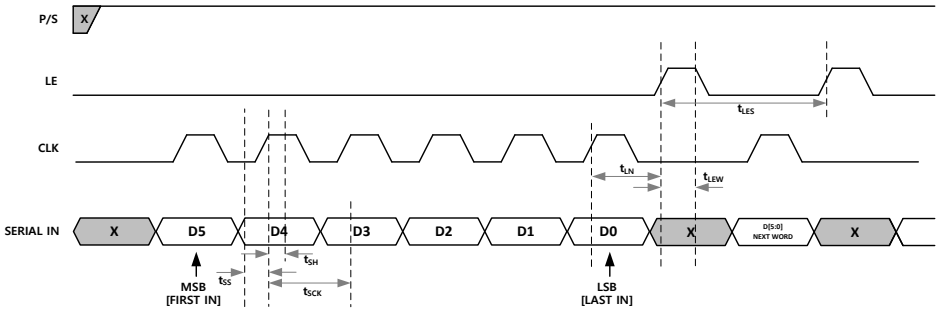
Serial Control Mode

The serial interface is a 6 bit shift register to shift in the data MSB (D5) first. It is controlled by three CMOS-compatible signals: SERIN, Clock, and Latch Enable (LE).

Table 5. 6-Bit Serial Word Sequence

D5	**Attenuation 16dB Control Bit**
D4	**Attenuation 8dB Control Bit**
D3	**Attenuation 4dB Control Bit**
D2	**Attenuation 2dB Control Bit**
D1	**Attenuation 1dB Control Bit**
D0	**Attenuation 0.5dB Control Bit**

Figure 3. Serial Mode Resister Timing Diagram



The BVA2140B has a 3-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when P/S is set to HIGH.
In serial mode, the 6-bit Data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggledHigh to latch the new attenuation state into the device. LE must be set to low to clock new 6-bit data into the shift register because CLK is masked to prevent the attenuator value from changing if LE is kept High (see Figure 3 and Table 8).

Table 6. Mode Selection

P/S	Control Mode
LOW	**Parallel**
HIGH	**Serial**

Table 7. Serial Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
fClk	Serial data clock frequency			10	MHz
t_{SCK}	Minimum serial period	70			
t_{SS}	Serial Data setup time	10			
t_{SH}	Serial Data hold time	10			
t_{LN}	LE setup time	10			
t_{LEW}	Minimum LE pulse width	30			
t_{LES}	Minimum LE pulse spacing		600		

Table 8. Truth Table for Serial Control Word

Digital Control Input						Attenuation
D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	(dB)
LOW	LOW	LOW	LOW	LOW	LOW	0 (Reference)
LOW	LOW	LOW	LOW	LOW	HIGH	0.5
LOW	LOW	LOW	LOW	HIGH	LOW	1
LOW	LOW	LOW	HIGH	LOW	LOW	2
LOW	LOW	HIGH	LOW	LOW	LOW	4
LOW	HIGH	LOW	LOW	LOW	LOW	8
HIGH	LOW	LOW	LOW	LOW	LOW	16
HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	31.5

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Power-UP Interface

The BVA2140B uses the PUP1 and PUP2 control voltage inputs to set the attenuation value to a known value at power-up before the initial control data word is provided in parallel mode. When the attenuator powers up with LE set to low, the state of PUP1 and PUP2 determines the power-up state of the device per the truth table shown in Table 9. The attenuator latches in the desired power-up state approximately 200 ms after power-up.

But BVA2140B can be use the PUP, when user is only able to control the P/S pin.

Table 9. PUP Truth Table

Attenuation state	P/S	LE	PUP1	PUP2
31.5 dB	LOW	LOW	HIGH	HIGH
16 dB	LOW	LOW	HIGH	LOW
8 dB	LOW	LOW	LOW	HIGH
Reference Loss	LOW	LOW	LOW	LOW

Figure 4. Pin Configuration(Top View)

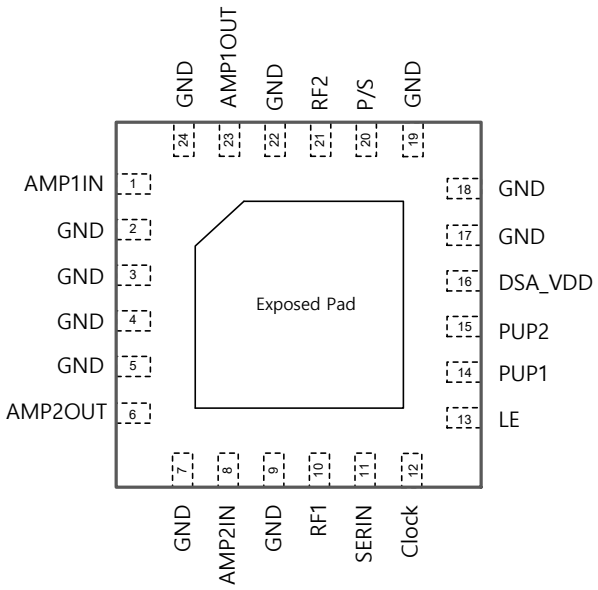

Table 10. Pin Description

Pin	Pin name	Description
2,3,4,5,7,9,17, 18,19,22,24	GND	Ground
1	AMP1IN	RF Amp1 in Port
6	AMP2OUT	RF Amp2 out Port
8	AMP2IN	RF Amp in Port
10	RF1[1]	RF port(DSA output)
11	SERIN	Serial interface data input
12	Clock	Serial interface clock input
13	LE	Latch Enable input
14	PUP1	Power-up selection bit 1
15	PUP2	Power-up selection bit 2
16	DSA_V_{DD}	DSA Supply voltage (nominal 3.3V)
20	P/S[2]	Parallel/Serial mode select
21	RF2[1]	RF port(DSA input)
23	AMP1OUT	RF Amp1 out Port

Note: 1. RF pins 10 and 21 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper Operation if the 0V DC requirement is met
2. P/S pin must be applied 1.17~3.6V, when use the serial mode.

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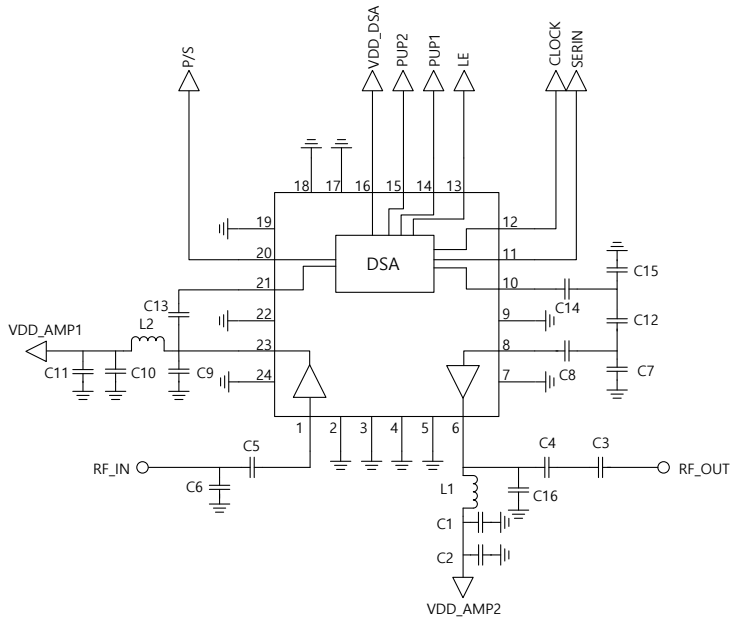
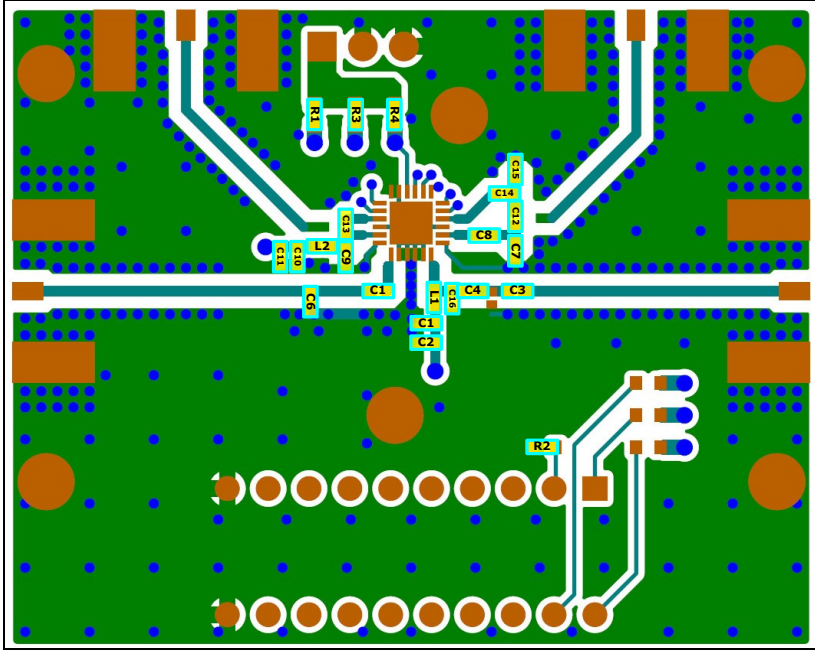
Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 700MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 11

Table 11. Application Circuit : 700MHz

Schematic Diagram	BOM(700MHz)			Remark
	Ref	Size	Value	
	C6	0402	NC	
	C5	0402	100pF	
	C9	0402	NC	
	L2	0402	22nH	
	C10	0402	22pF	
	C11	0402	1nF	
	C13	0402	10pF	
	C14	0402	0ohm	
	C15	0402	NC	
	C12	0402	9pF	
	C7	0402	6.8pF	
	C8	0402	2.7nH	
	L1	0402	22nH	
	C1	0402	100pF	
	C2	0402	1uF	
	C4	0402	6.8nH	
	C3	0402	10pF	
	C16	0402	3.3pF	
	NOTE: BOM's Information refer to table 23.			
	NOTE 1. R1, R2, R3, R4 is 0ohm(0805)			

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Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 700MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 11

Table 12. Typical RF Performance

parameter	Typical Values	Units
Frequency	**700**	**MHz**
Gain	41.6	dB
S11	-17.5	dB
S22	-7.8	dB
OIP3[1]	40.7	dBm
P1dB	27.0	dBm
Noise Figure	2.4	dB
LTE20MHz ACLR[2]	15.1	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 5. Gain vs. Frequency
over Temperature

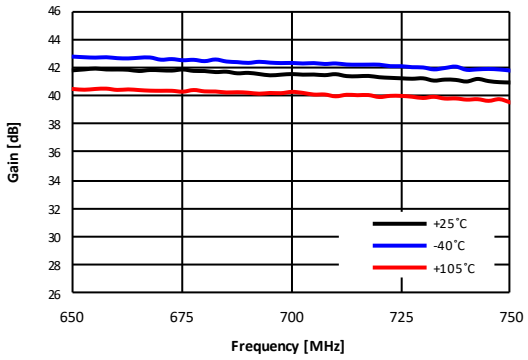


Figure 6. Input Return Loss vs. Frequency
over Major Attenuation States

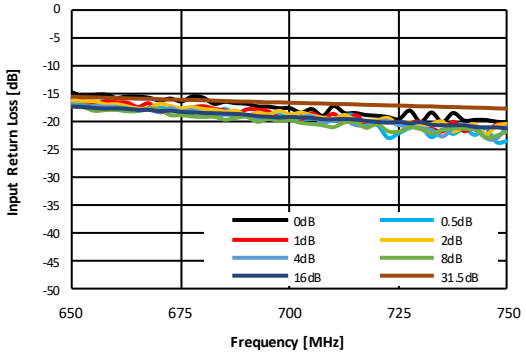


Figure 7. Input Return Loss vs. Frequency
over Temperature (Min,Max Gain State)

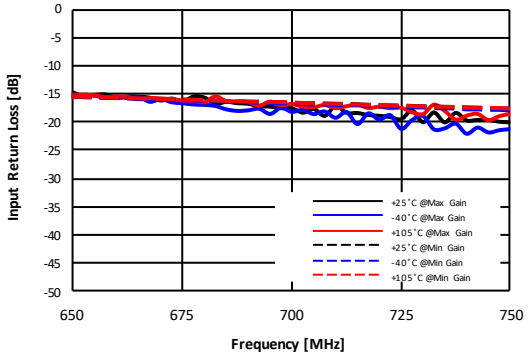


Figure 8. Output Return Loss vs. Frequency
over Major Attenuation States

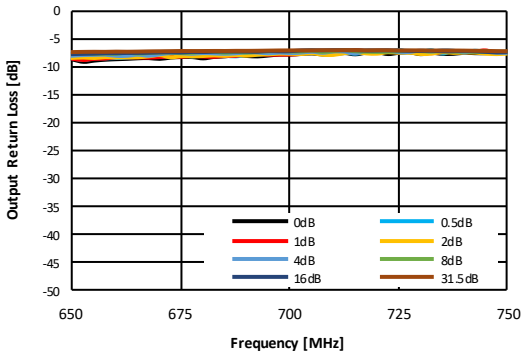
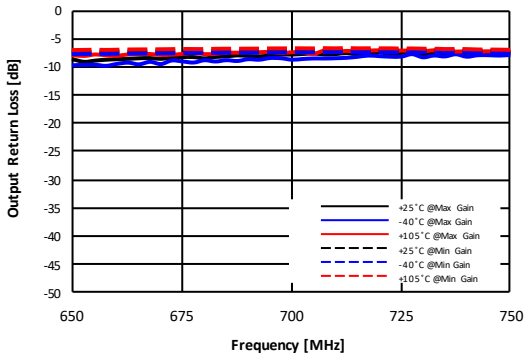


Figure 9. Output Return Loss vs. Frequency
over Temperature (Min,Max Gain State)



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Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 700MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 10. Gain vs. Frequency
over Major Attenuation States

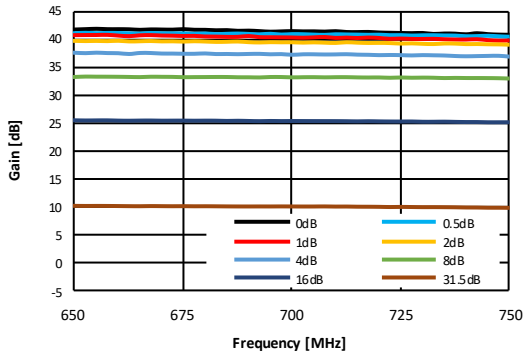


Figure 11. Attenuation Error vs Frequency
over Major Attenuation Steps

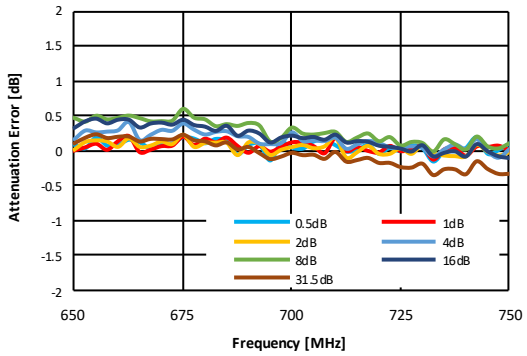


Figure 12. Attenuation Error vs Attenuation Setting
over Major Frequency(Max Gain State)

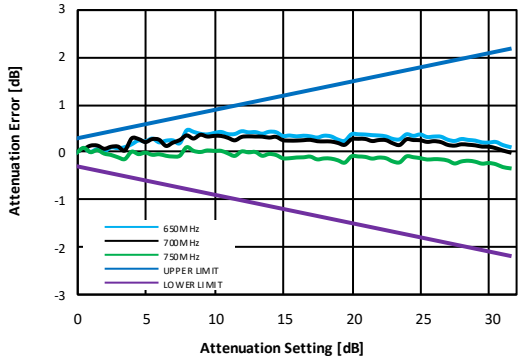


Figure 13. 0.5dB Step Attenuation vs Attenuation Setting
over Temperature @700MHz

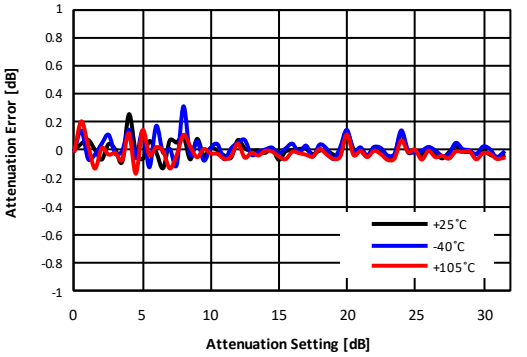


Figure 14. Attenuation Error vs Temperature @700MHz
over All Attenuation States

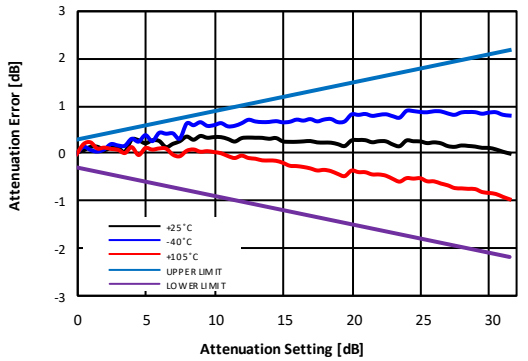
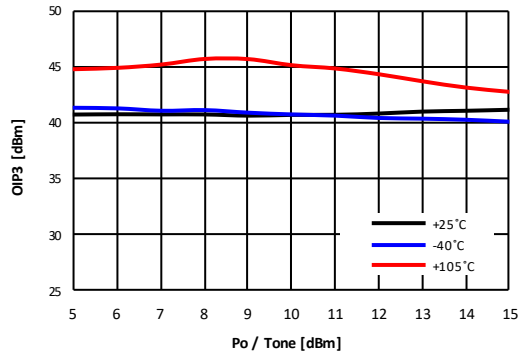


Figure 15. OIP3 vs Output Power @700MHz
over Temperature (Max Gain State)



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Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 700MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 11

Figure 16. Device Performance Pin-Pout-Gain @700MHz

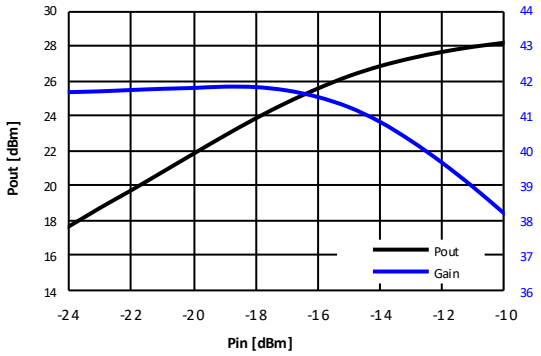


Figure 17. Noise Figure vs Frequency
over Temperature

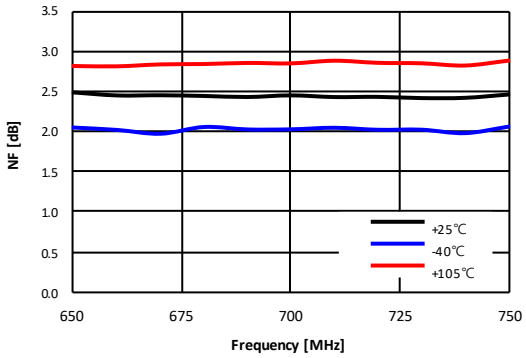


Figure 18. 3GPP LTE 20MHz ACLR vs Output Power
over Temperature @700MHz

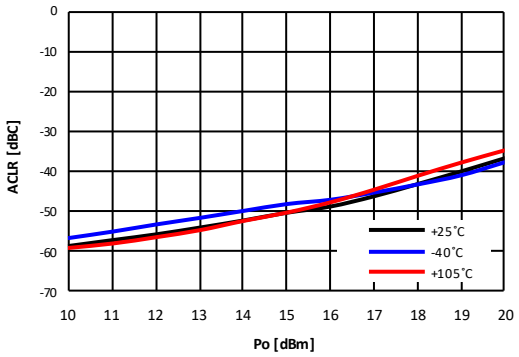
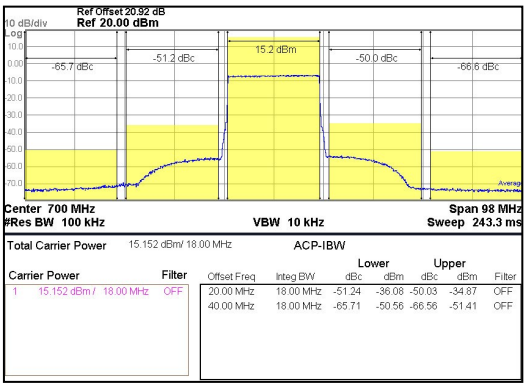


Figure 19. ACLR @700MHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

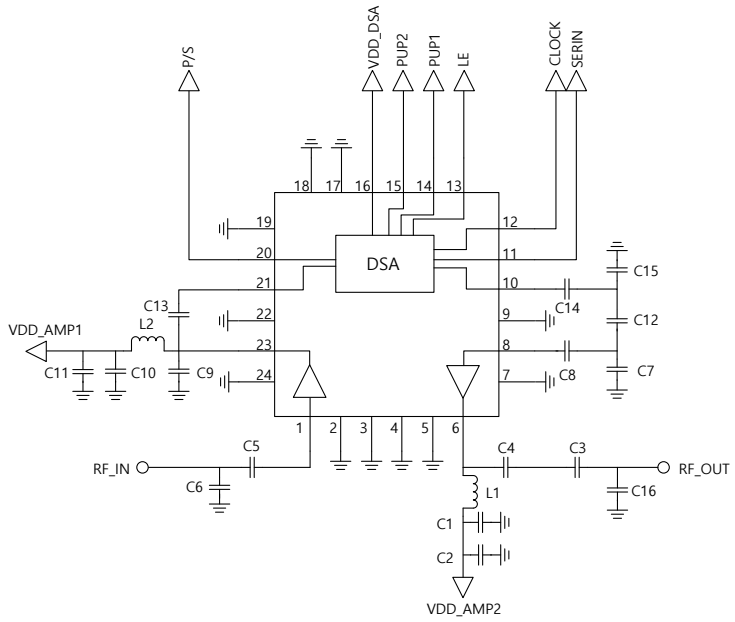
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 900MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 13

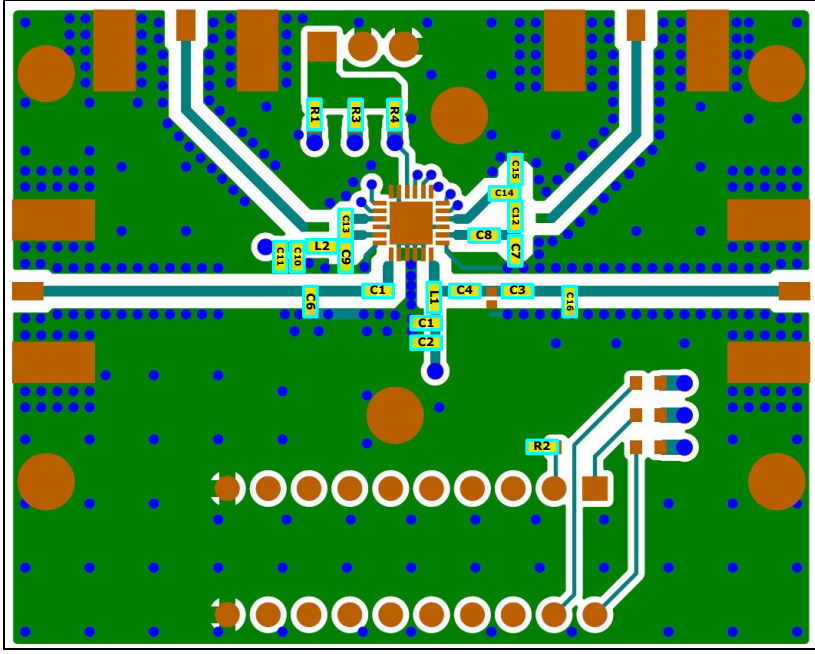
Table 13. Application Circuit : 900MHz

Schematic Diagram



BOM(900MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	22nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	5.6pF	
C14	0402	1.2nH	
C15	0402	NC	
C12	0402	5.6pF	
C7	0402	3.3pF	
C8	0402	2.2nH	
L1	0402	27nH	
C1	0402	100pF	
C2	0402	1uF	
C4	0402	1.5nH	
C3	0402	100pF	
C16	0402	2.4pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 900MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 13

Table 14. Typical RF Performance

parameter	Typical Values	Units
Frequency	**900**	**MHz**
Gain	40.3	dB
S11	-17.6	dB
S22	-13.0	dB
OIP3[1]	46.9	dBm
P1dB	27.3	dBm
Noise Figure	2.6	dB
LTE20MHz ACLR[2]	16.2	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 20. Gain vs. Frequency
over Temperature

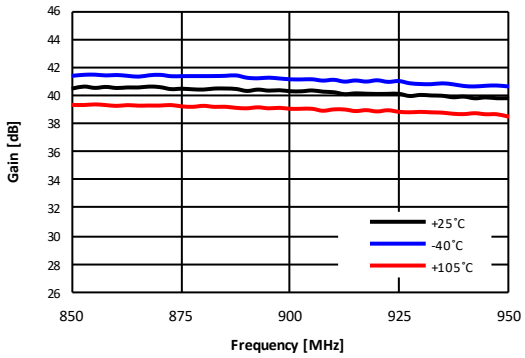


Figure 21. Input Return Loss vs. Frequency
over Major Attenuation States

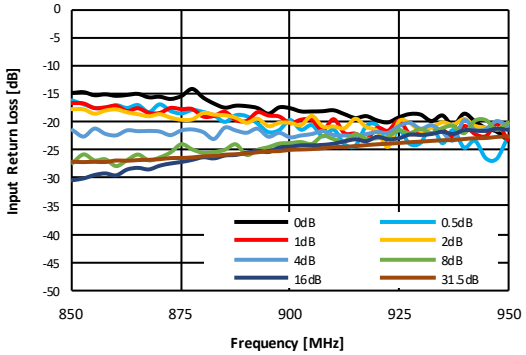


Figure 22. Input Return Loss vs. Frequency
over Temperature (Min,Max Gain State)

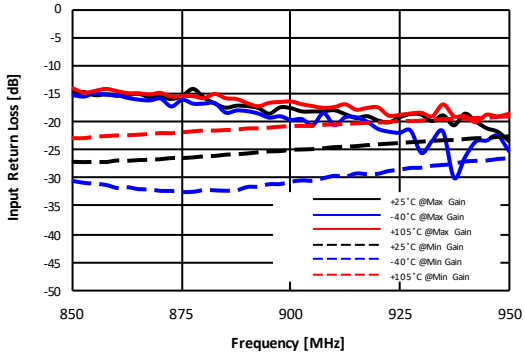


Figure 23. Output Return Loss vs. Frequency
over Major Attenuation States

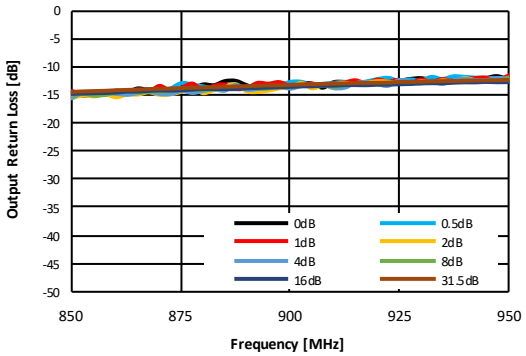
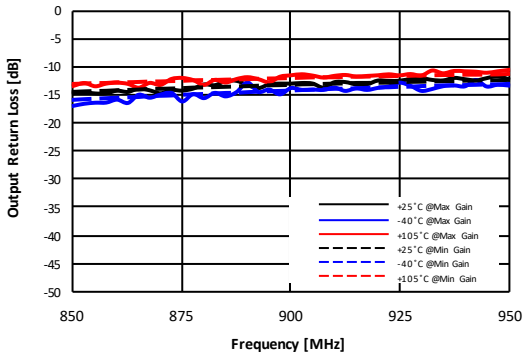


Figure 24. Output Return Loss vs. Frequency
over Temperature (Min,Max Gain State)



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 900MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 13

Figure 25. Gain vs. Frequency
over Major Attenuation States

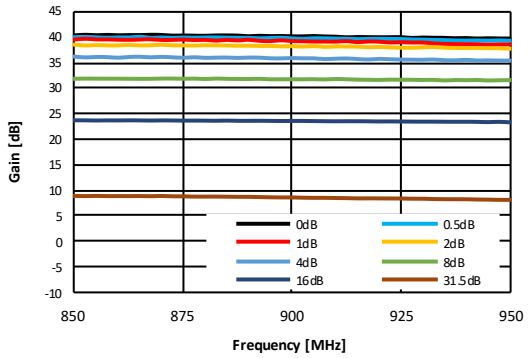


Figure 26. Attenuation Error vs Frequency
over Major Attenuation Steps

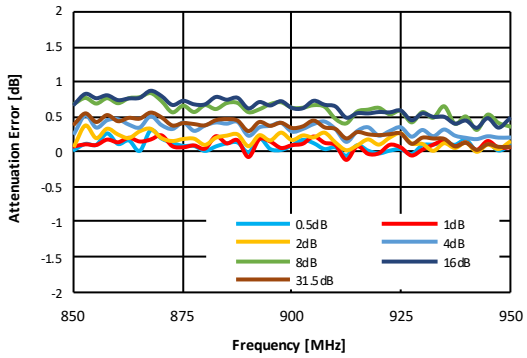


Figure 27. Attenuation Error vs Attenuation Setting
over Major Frequency(Max Gain State)

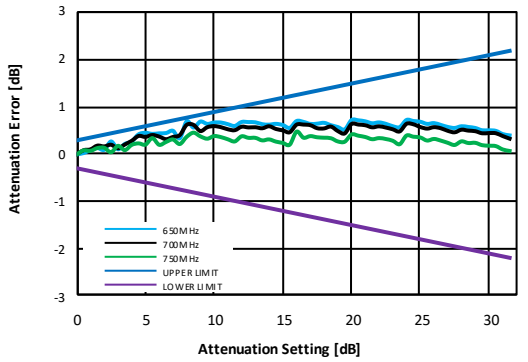


Figure 28. 0.5dB Step Attenuation vs Attenuation Setting
over Temperature @900MHz

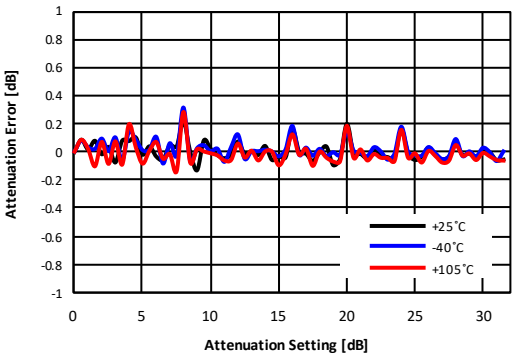


Figure 29. Attenuation Error vs Temperature @900MHz
over All Attenuation States

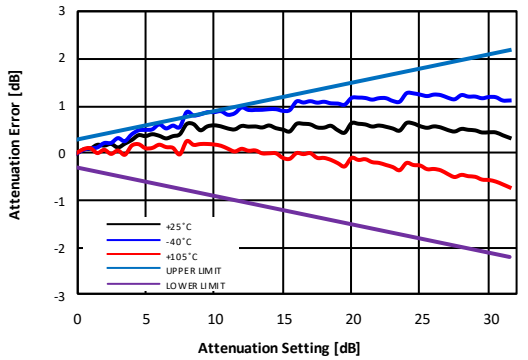
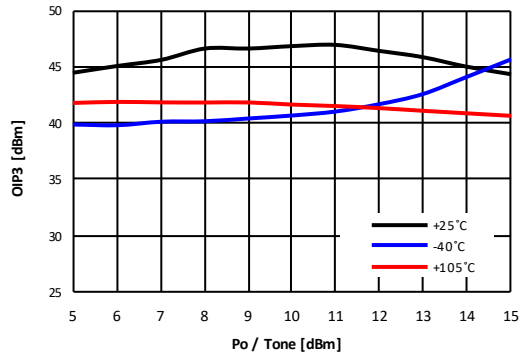


Figure 30. OIP3 vs Output Power @900MHz
over Temperature (Max Gain State)



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 900MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 13

Figure 31. Device Performance Pin-Pout-Gain @900MHz

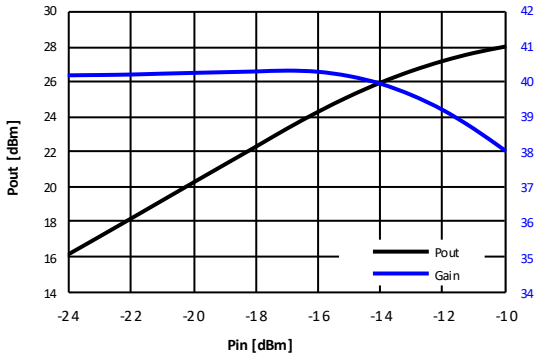


Figure 32. Noise Figure vs Frequency
over Temperature

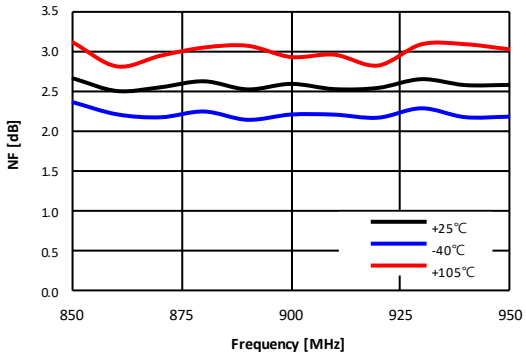


Figure 33. 3GPP LTE 20MHz ACLR vs Output Power
over Temperature @900MHz

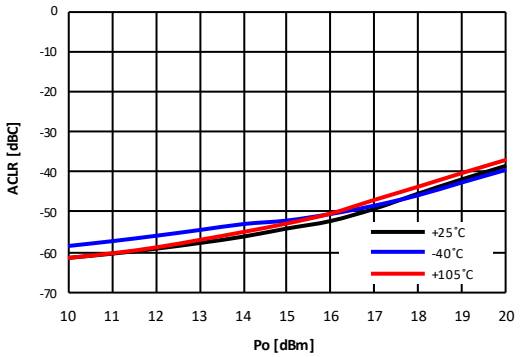
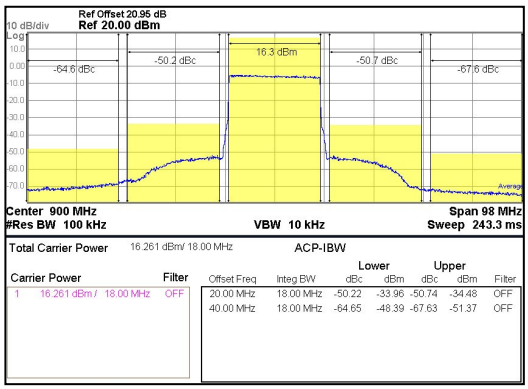


Figure 34. ACLR @700MHz, LTE20MHz[1], -50dBc



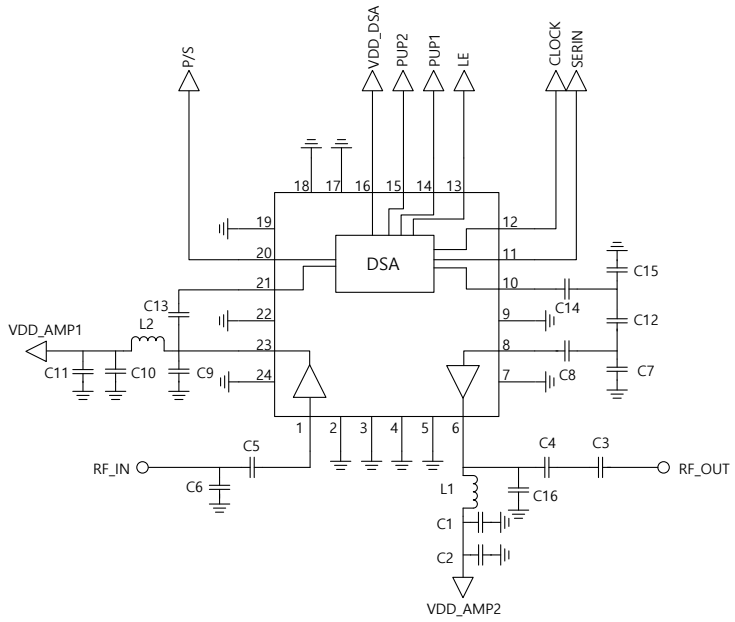
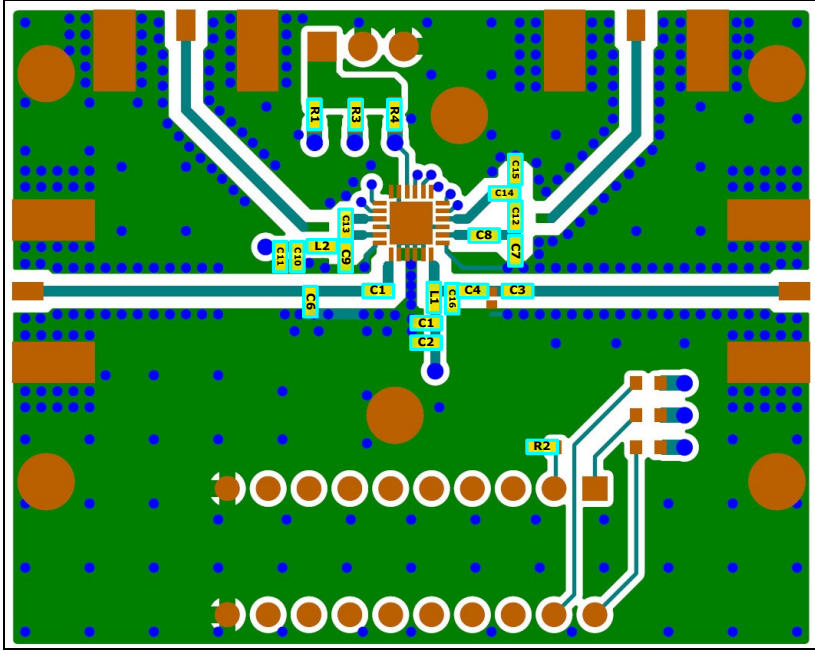
1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 1900MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 15

Table 15. Application Circuit : 1900MHz

Schematic Diagram	BOM(1900MHz)			Remark
	Ref	Size	Value	
	C6	0402	NC	
	C5	0402	22pF	
	C9	0402	NC	
	L2	0402	22nH	
	C10	0402	22pF	
	C11	0402	1nF	
	C13	0402	22pF	
	C14	0402	2nH	
	C15	0402	NC	
	C12	0402	1pF	
	C7	0402	1.2pF	
	C8	0402	0ohm	
	L1	0402	15nH	
	C1	0402	22pF	
	C2	0402	1uF	
	C4	0402	39pF	
	C3	0402	0ohm	
	C16	0402	1.3pF	
	NOTE: BOM's Information refer to table 23.			
	NOTE 1. R1, R2, R3, R4 is 0ohm(0805)			

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 1900MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 15

Table 16. Typical RF Performance

parameter	Typical Values	Units
Frequency	**1900**	**MHz**
Gain	31.1	dB
S11	-22.2	dB
S22	-13.4	dB
OIP3[1]	41.6	dBm
P1dB	26.8	dBm
Noise Figure	2.7	dB
LTE20MHz ACLR[2]	16.5	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 35. Gain vs. Frequency
over Temperature

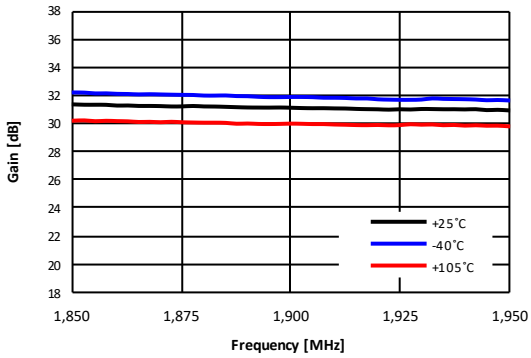


Figure 36. Input Return Loss vs. Frequency
over Major Attenuation States

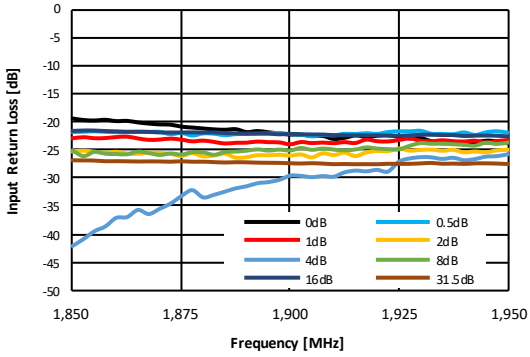


Figure 37. Input Return Loss vs. Frequency
over Temperature (Min,Max Gain State)

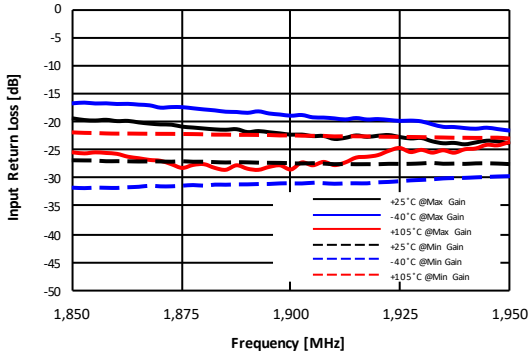


Figure 38. Output Return Loss vs. Frequency
over Major Attenuation States

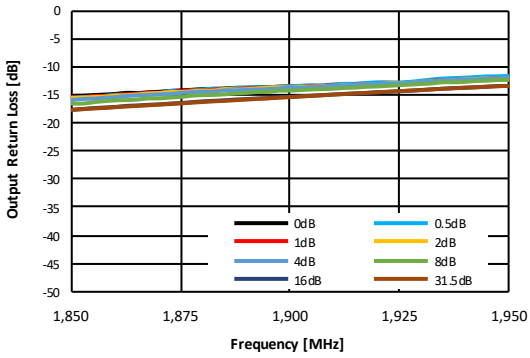
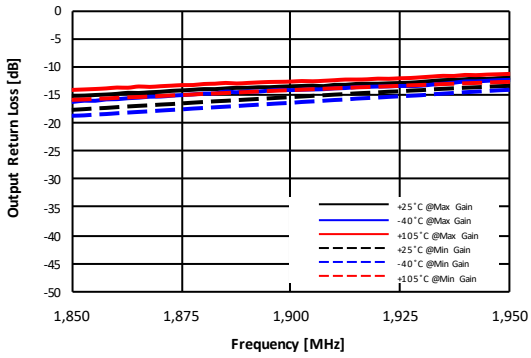


Figure 39. Output Return Loss vs. Frequency
over Temperature (Min,Max Gain State)



Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 1900MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 15

Figure 40. Gain vs. Frequency
over Major Attenuation States

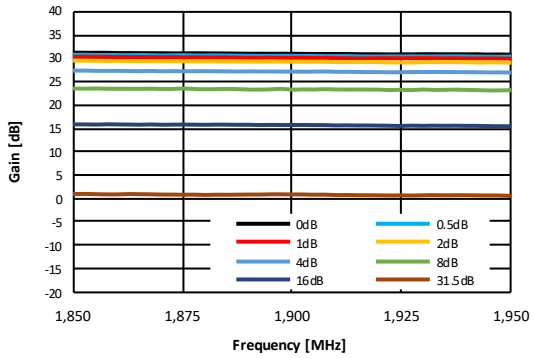


Figure 41. Attenuation Error vs Frequency
over Major Attenuation Steps

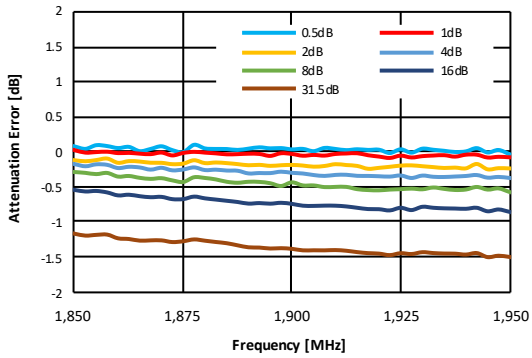


Figure 42. Attenuation Error vs Attenuation Setting
over Major Frequency(Max Gain State)

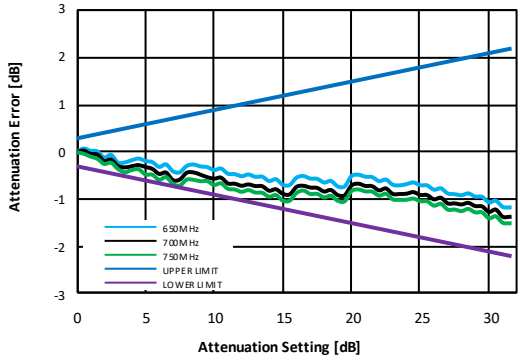


Figure 43. 0.5dB Step Attenuation vs Attenuation Setting
over Temperature @1.9GHz

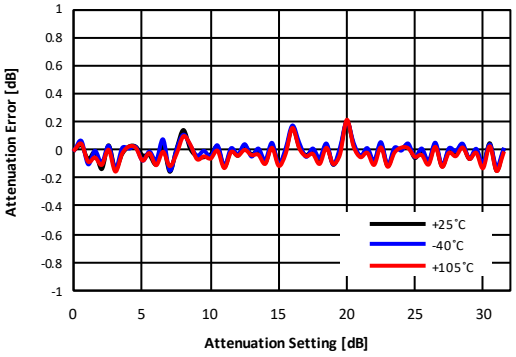


Figure 44. Attenuation Error vs Temperature @1.9GHz
over All Attenuation States

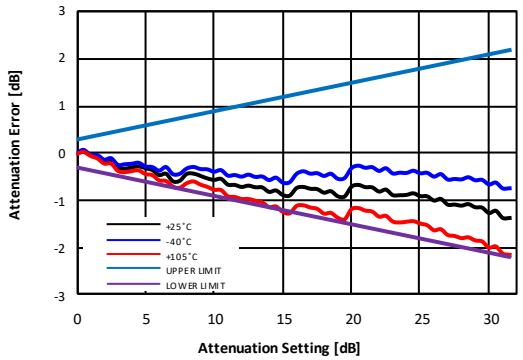
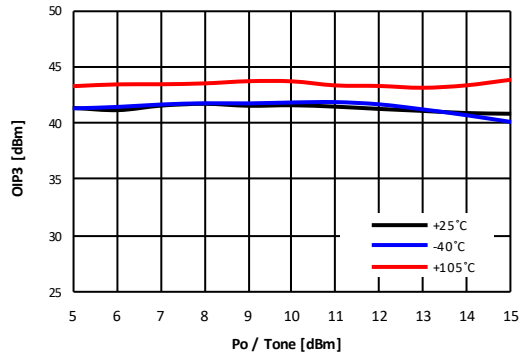


Figure 45. OIP3 vs Output Power @1.9GHz
over Temperature (Max Gain State)



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 1900MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 15

Figure 46. Device Performance Pin-Pout-Gain @1.9GHz

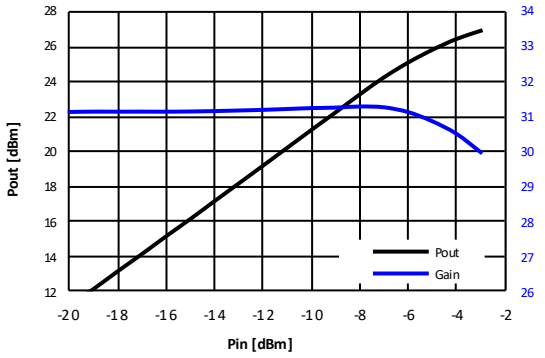


Figure 47. Noise Figure vs Frequency
over Temperature

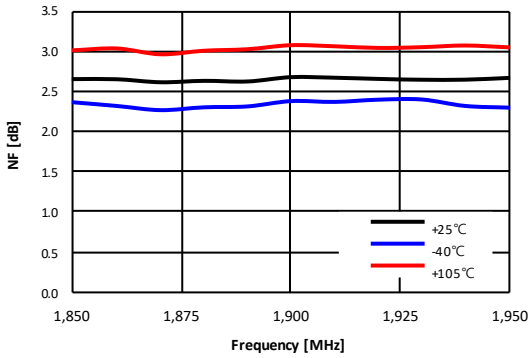


Figure 48. 3GPP LTE 20MHz ACLR vs Output Power
over Temperature @1.9GHz

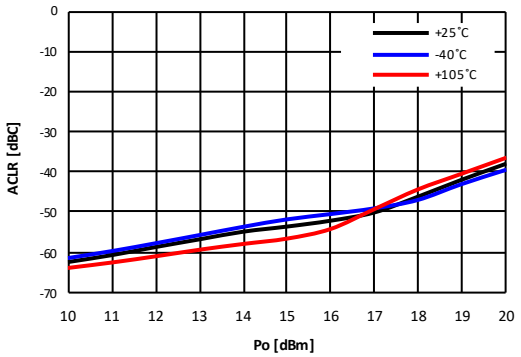
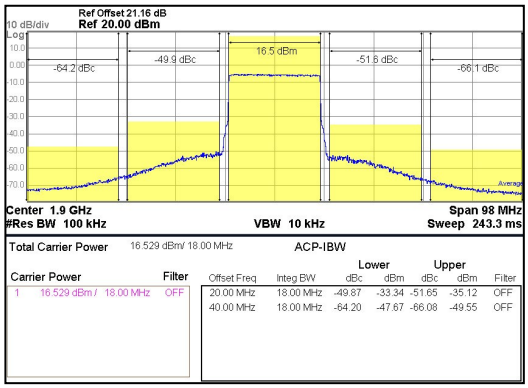


Figure 49. ACLR @1.9GHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

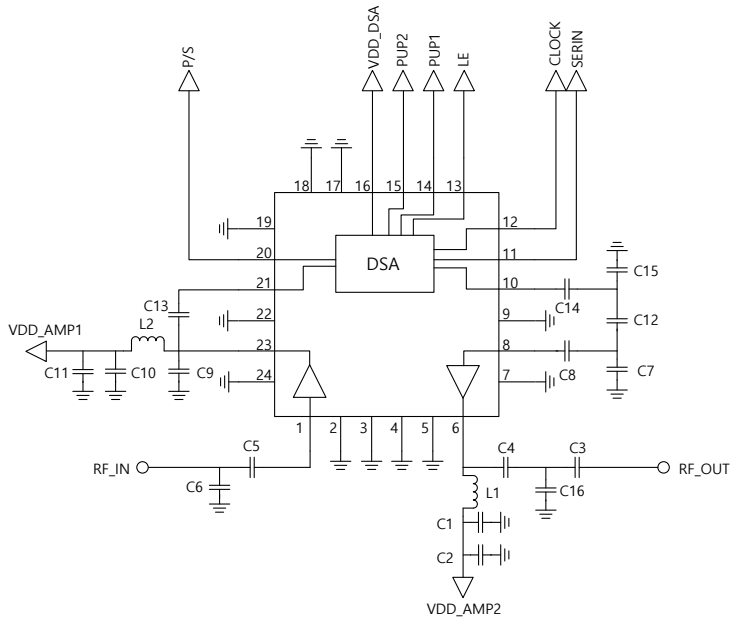
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 2140MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 17

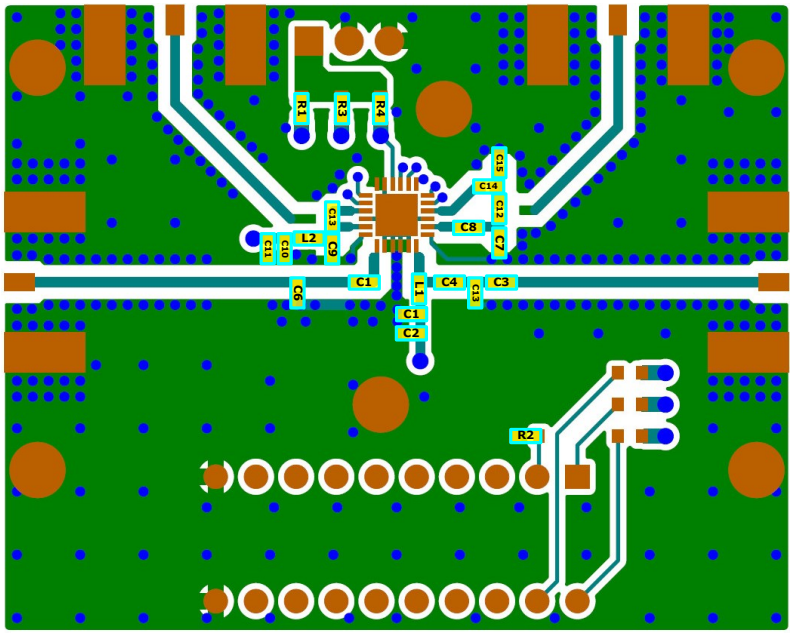
Table 17. Application Circuit : 2140MHz

Schematic Diagram



BOM(2140MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	15nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	22pF	
C14	0402	2nH	
C15	0402	0.5pF	
C12	0402	1pF	
C7	0402	1pF	
C8	0402	0ohm	
L1	0402	10nH	
C1	0402	100pF	
C2	0402	1uF	
C4	0402	1nH	
C3	0402	30pF	
C16	0402	1pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 2140MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 17

Table 18. Typical RF Performance

parameter	Typical Values	Units
Frequency	**2140**	**MHz**
Gain	30.4	dB
S11	-23.6	dB
S22	-12.2	dB
OIP3[1]	40.2	dBm
P1dB	25.6	dBm
Noise Figure	2.7	dB
LTE20MHz ACLR[2]	15.5	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 50. Gain vs. Frequency
over Temperature

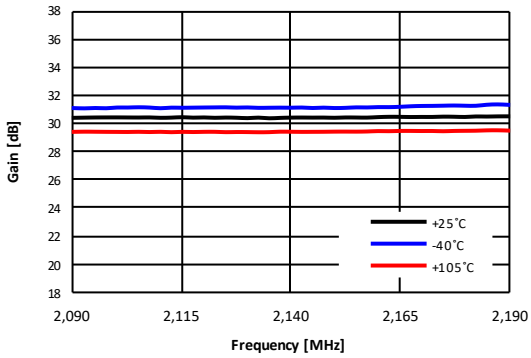


Figure 51. Input Return Loss vs. Frequency
over Major Attenuation States

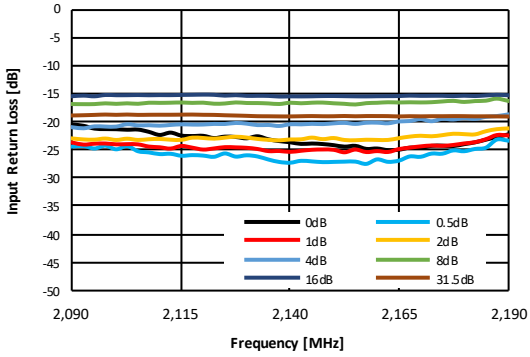


Figure 52. Input Return Loss vs. Frequency
over Temperature (Min,Max Gain State)

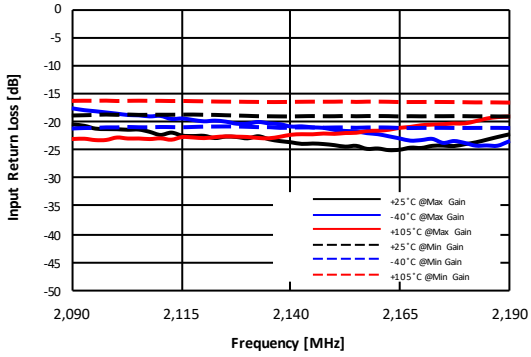


Figure 53. Output Return Loss vs. Frequency
over Major Attenuation States

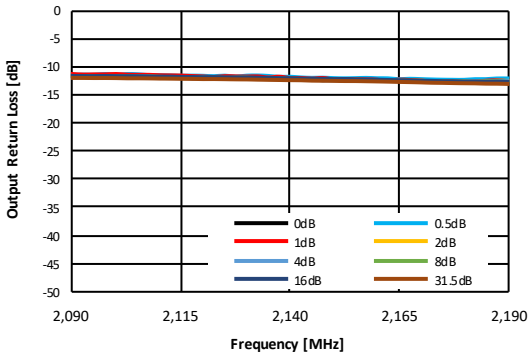
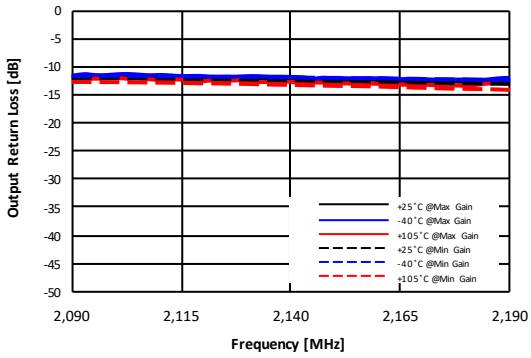


Figure 54. Output Return Loss vs. Frequency
over Temperature (Min,Max Gain State)



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 2140MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 17

Figure 55. Gain vs. Frequency
over Major Attenuation States

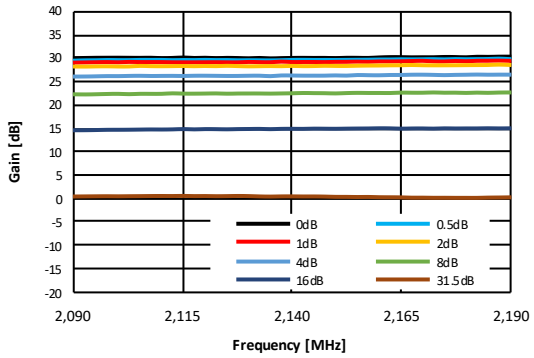


Figure 56. Attenuation Error vs Frequency
over Major Attenuation Steps

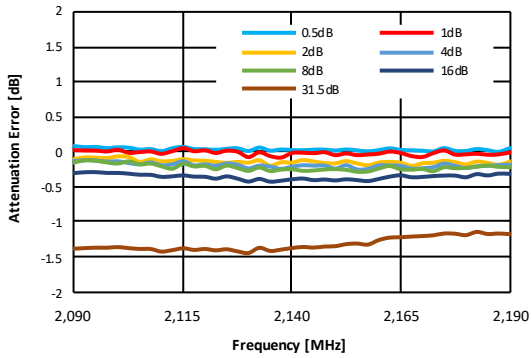


Figure 57. Attenuation Error vs Attenuation Setting
over Major Frequency(Max Gain State)

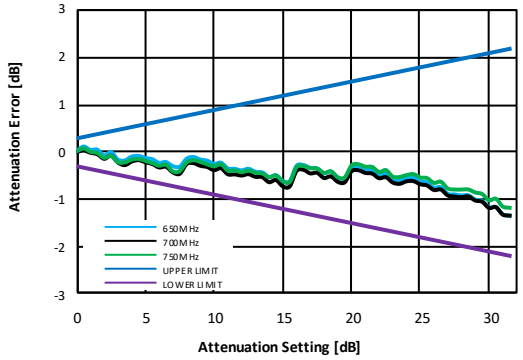


Figure 58. 0.5dB Step Attenuation vs Attenuation Setting
over Temperature @2.14GHz

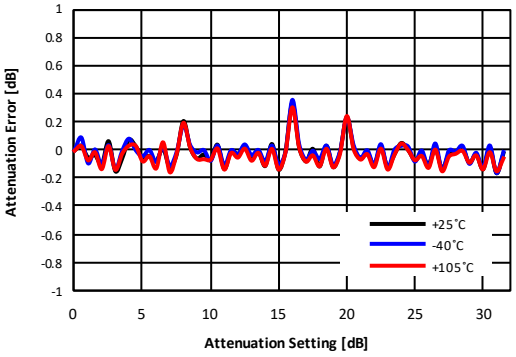


Figure 59. Attenuation Error vs Temperature @2.14GHz
over All Attenuation States

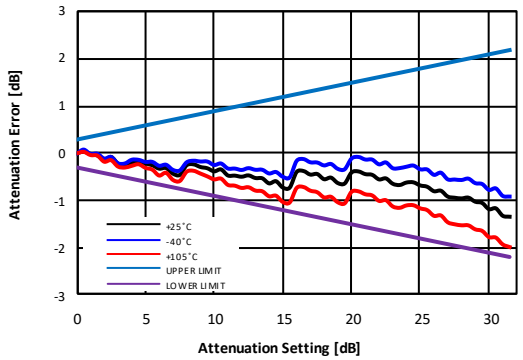
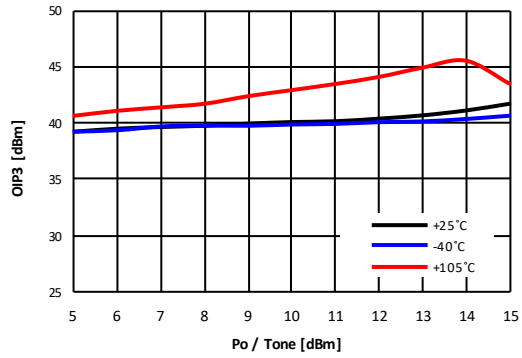


Figure 60. OIP3 vs Output Power @2.14GHz
over Temperature (Max Gain State)



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 2140MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 17

Figure 61. Device Performance Pin-Pout-Gain @2.14GHz

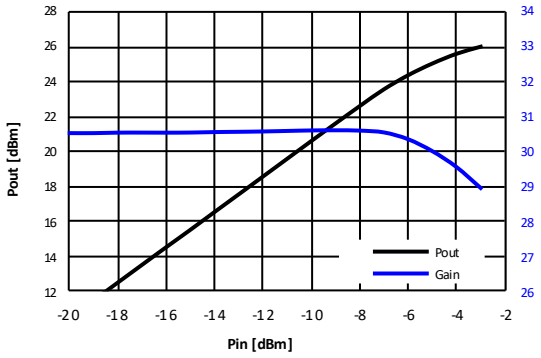


Figure 62. Noise Figure vs Frequency
over Temperature

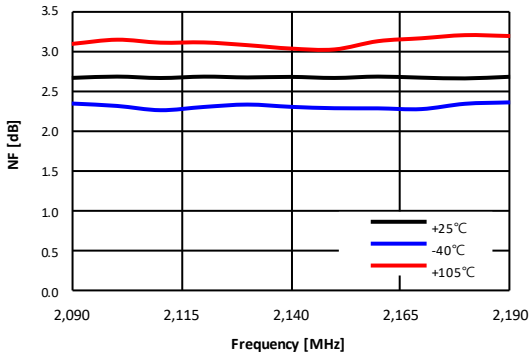


Figure 63. 3GPP LTE 20MHz ACLR vs Output Power
over Temperature @2.14GHz

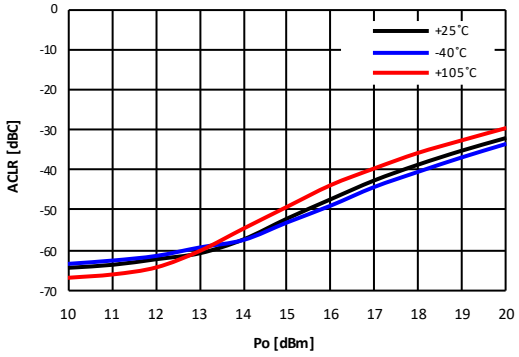
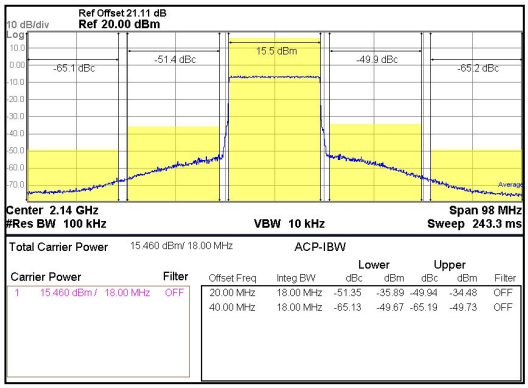


Figure 64. ACLR @2.14GHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

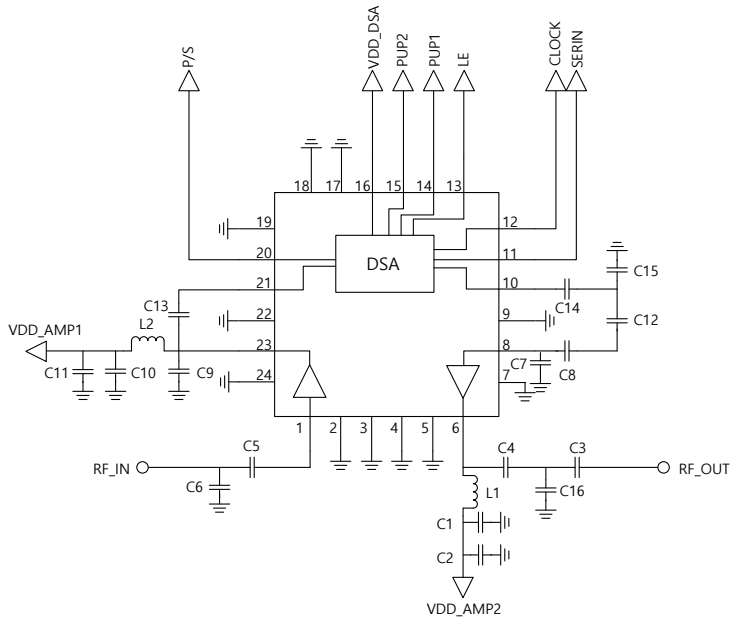
0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 2650MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 19

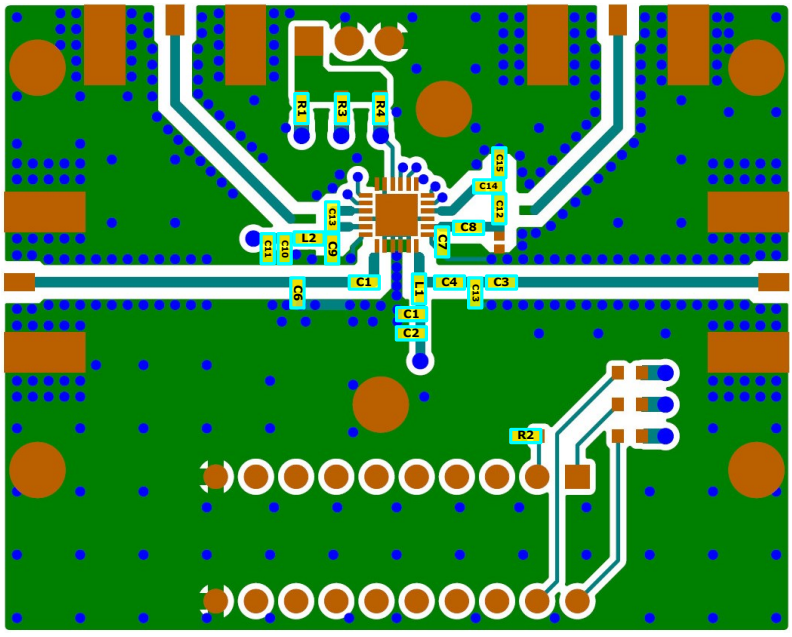
Table 19. Application Circuit : 2650MHz

Schematic Diagram



BOM(2650MHz)			Remark
Ref	Size	Value	
C6	0402	NC	
C5	0402	22pF	
C9	0402	NC	
L2	0402	15nH	
C10	0402	22pF	
C11	0402	1nF	
C13	0402	10pF	
C14	0402	3.3nH	
C15	0402	NC	
C12	0402	0ohm	
C7	0402	1.5pF	
C8	0402	2.2pF	
L1	0402	4.7nH	
C1	0402	22pF	
C2	0402	1uF	
C4	0402	0ohm	
C3	0402	22pF	
C16	0402	1pF	

NOTE: BOM's Information refer to table 23.



NOTE

1. R1, R2, R3, R4 is 0ohm(0805)

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 2650MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 19

Table 20. Typical RF Performance

parameter	Typical Values	Units
Frequency	**2650**	**MHz**
Gain	28.6	dB
S11	-19.5	dB
S22	-12.1	dB
OIP3[1]	38.3	dBm
P1dB	24.9	dBm
Noise Figure	2.9	dB
LTE20MHz ACLR[2]	15.3	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 65. Gain vs. Frequency
over Temperature

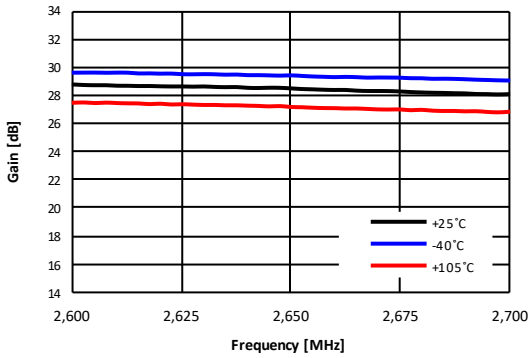


Figure 66. Input Return Loss vs. Frequency
over Major Attenuation States

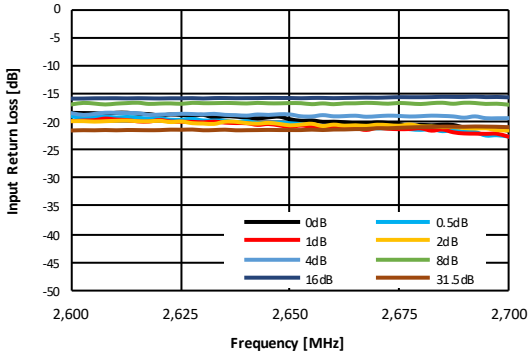


Figure 67. Input Return Loss vs. Frequency
over Temperature (Min,Max Gain State)

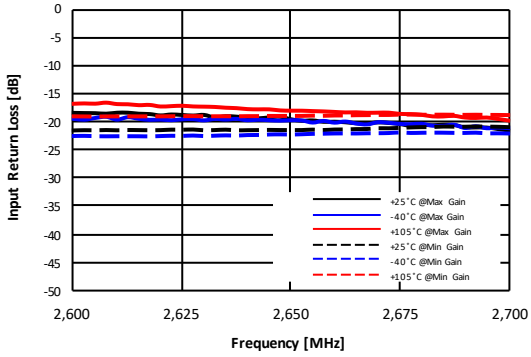


Figure 68. Output Return Loss vs. Frequency
over Major Attenuation States

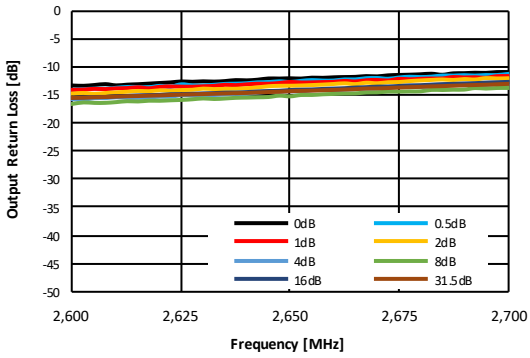
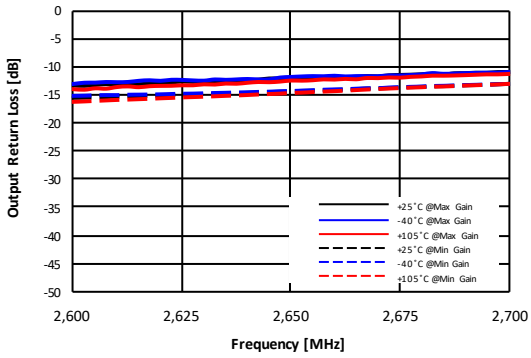


Figure 69. Output Return Loss vs. Frequency
over Temperature (Min,Max Gain State)



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 2650MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 19

Figure 70. Gain vs. Frequency
over Major Attenuation States

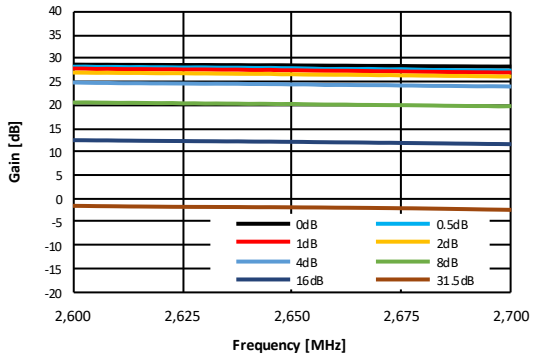


Figure 71. Attenuation Error vs Frequency
over Major Attenuation Steps

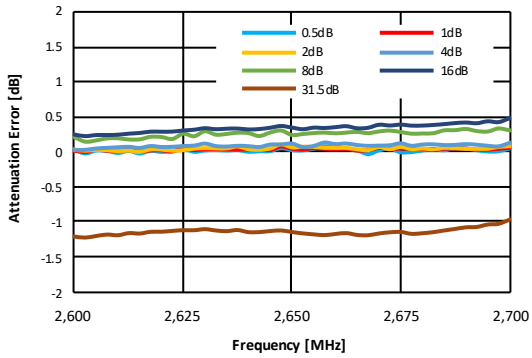


Figure 72. Attenuation Error vs Attenuation Setting
over Major Frequency(Max Gain State)

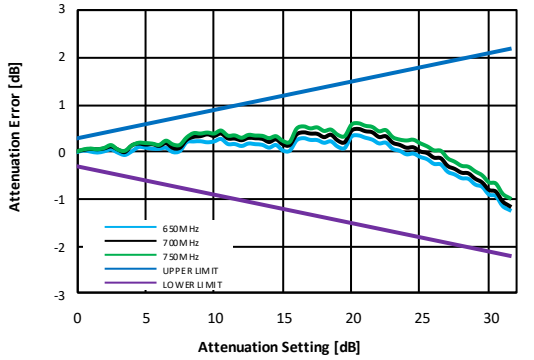


Figure 73. 0.5dB Step Attenuation vs Attenuation Setting
over Temperature @2.65GHz

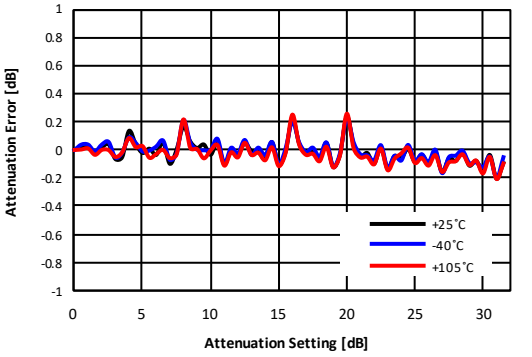


Figure 74. Attenuation Error vs Temperature @2.65GHz
over All Attenuation States

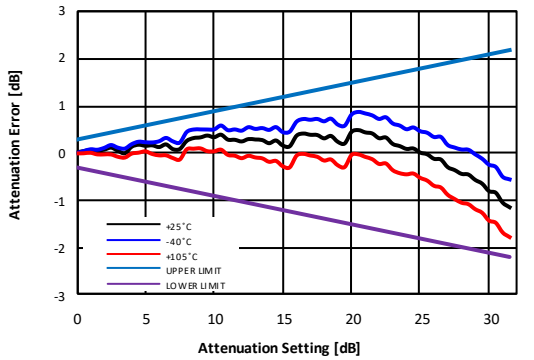
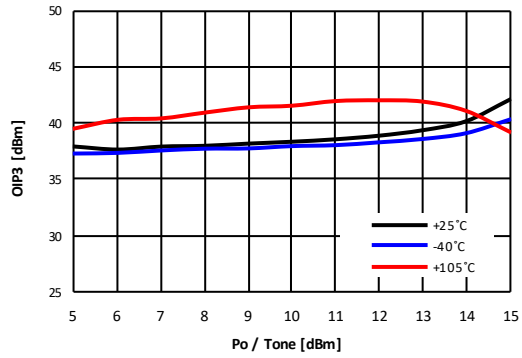


Figure 75. OIP3 vs Output Power @2.65GHz
over Temperature (Max Gain State)



Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 2650MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 19

Figure 76. Device Performance Pin-Pout-Gain @2.65GHz

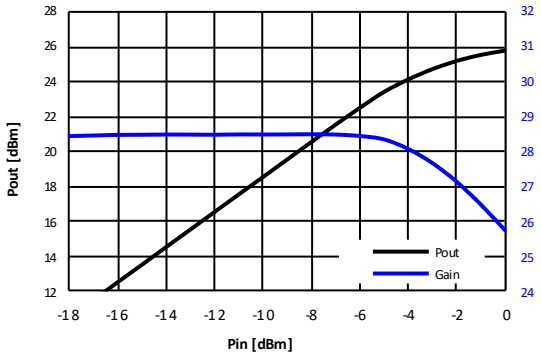


Figure 77. Noise Figure vs Frequency
over Temperature

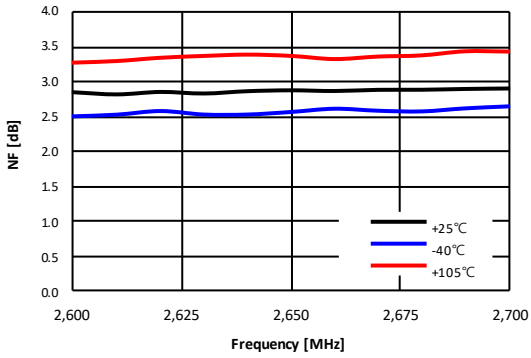


Figure 78. 3GPP LTE 20MHz ACLR vs Output Power
over Temperature @2.65GHz

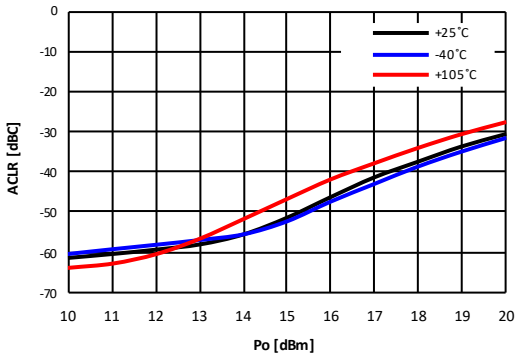
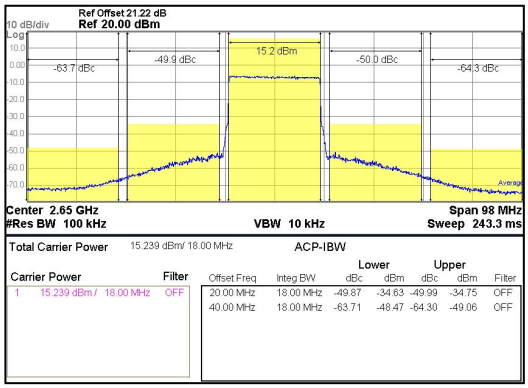


Figure 79. ACLR @2.65GHz, LTE20MHz[1], -50dBc



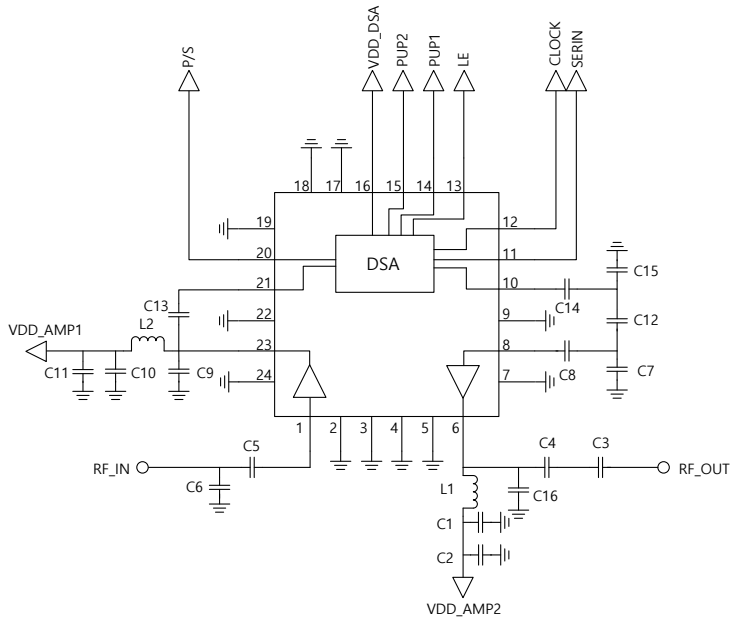
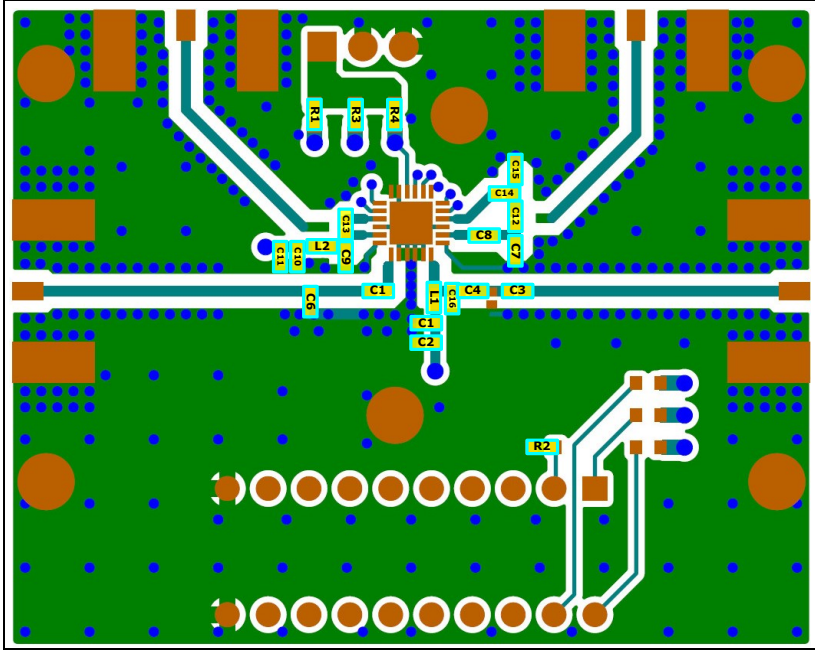
1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 3500MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 21

Table 21. Application Circuit : 3500MHz

Schematic Diagram	BOM(3500MHz)			Remark
	Ref	Size	Value	
	C6	0402	0.5pF	
	C5	0402	22pF	
	C9	0402	NC	
	L2	0402	10nH	
	C10	0402	22pF	
	C11	0402	1nF	
	C13	0402	10pF	
	C14	0402	2nH	
	C15	0402	NC	
	C12	0402	2.2pF	
	C7	0402	0.5pF	
	C8	0402	2.7pF	
	L1	0402	3nH	
	C1	0402	22pF	
	C2	0402	1uF	
	C4	0402	10pF	
	C3	0402	copper	
	C16	0402	1pF	
	NOTE: BOM's Information refer to table 23.			
	NOTE 1. R1, R2, R3, R4 is 0ohm(0805)			

0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 3500MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 21

Table 22. Typical RF Performance

parameter	Typical Values	Units
Frequency	**3500**	**MHz**
Gain	24.2	dB
S11	-21.1	dB
S22	-15.3	dB
OIP3[1]	36.8	dBm
P1dB	24.4	dBm
Noise Figure	3.4	dB
LTE20MHz ACLR[2]	14.9	dBm

1. OIP3 measured with two tones at an output of 10 dBm per tone separated by 1 MHz.
2. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 80. Gain vs. Frequency
over Temperature

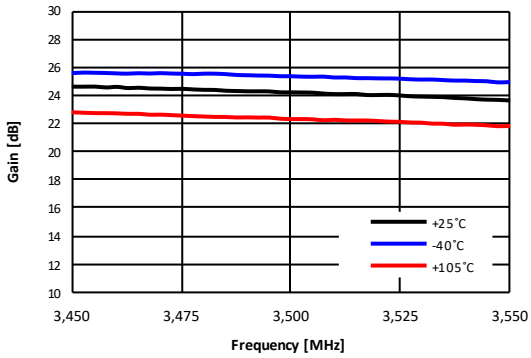


Figure 81. Input Return Loss vs. Frequency
over Major Attenuation States

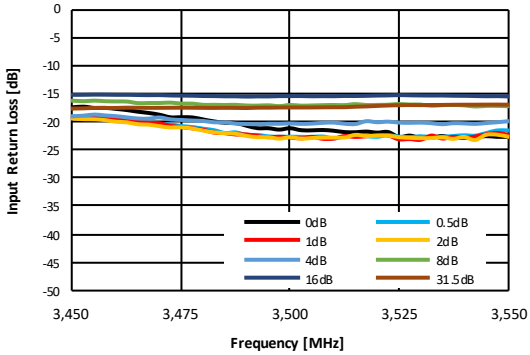


Figure 82. Input Return Loss vs. Frequency
over Temperature (Min,Max Gain State)

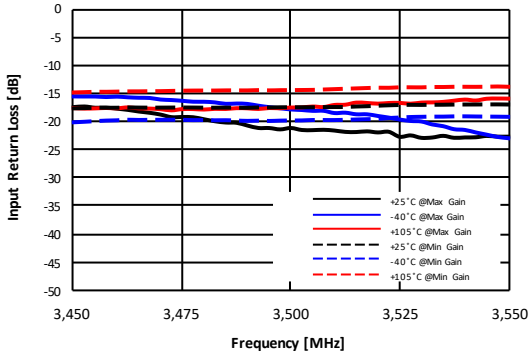


Figure 83. Output Return Loss vs. Frequency
over Major Attenuation States

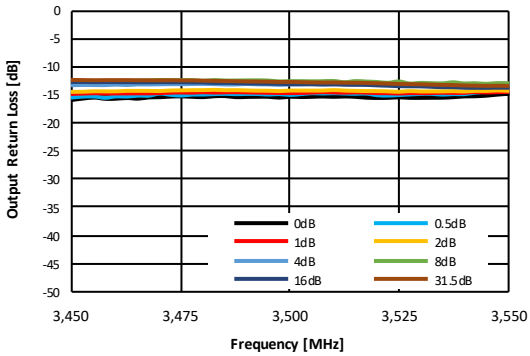
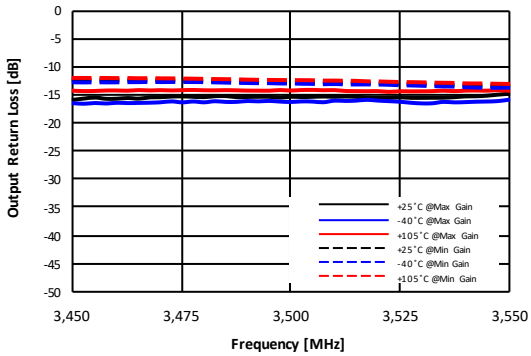


Figure 84. Output Return Loss vs. Frequency
over Temperature (Min,Max Gain State)



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 3500MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 21

Figure 85. Gain vs. Frequency
over Major Attenuation States

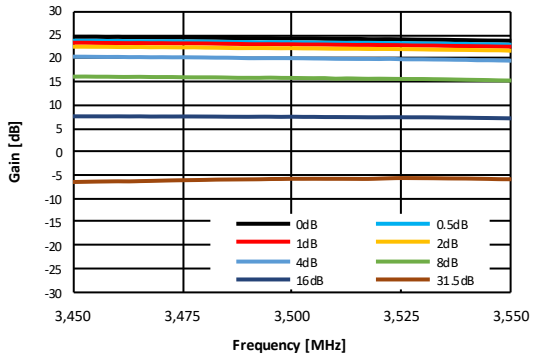


Figure 86. Attenuation Error vs Frequency
over Major Attenuation Steps

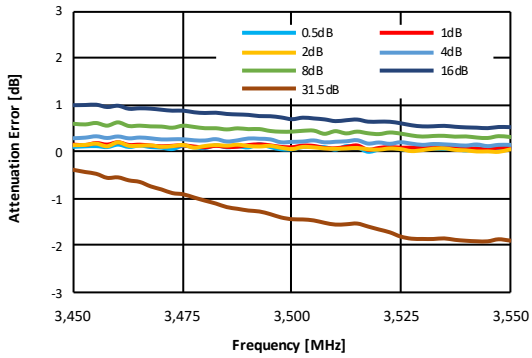


Figure 87. Attenuation Error vs Attenuation Setting
over Major Frequency(Max Gain State)

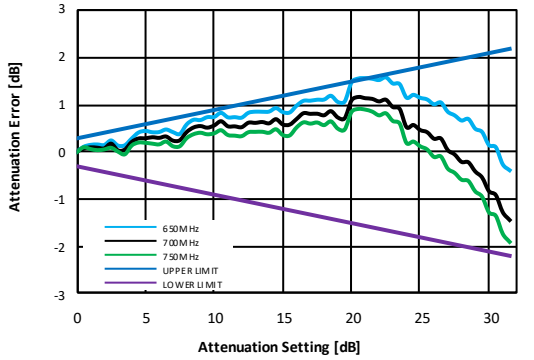


Figure 88. 0.5dB Step Attenuation vs Attenuation Setting
over Temperature @3.5GHz

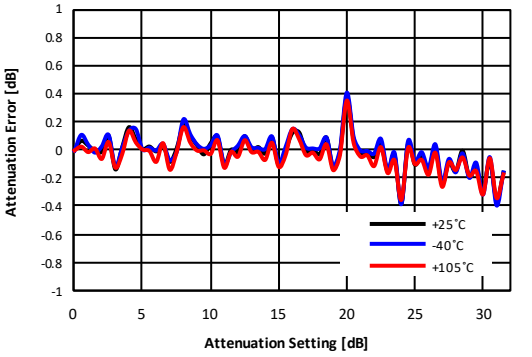


Figure 89. Attenuation Error vs Temperature @3.5GHz
over All Attenuation States

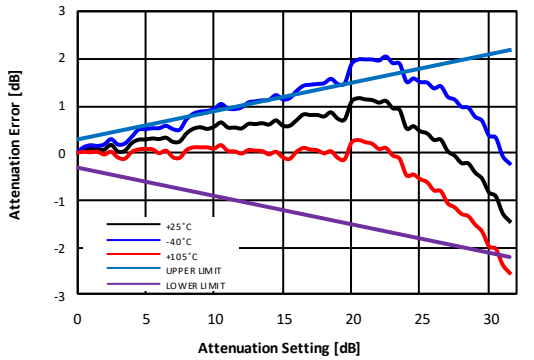
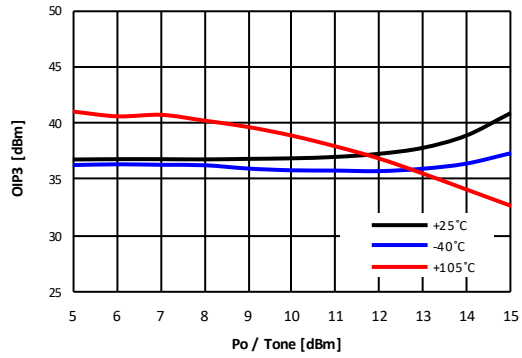


Figure 90. OIP3 vs Output Power @3.5GHz
over Temperature (Max Gain State)



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Typical RF Performance Plot - BVA2140B EVK - PCB (Application Circuit: 3500MHz)

Typical Performance Data @ 25°C and V_{DD} = 5V unless otherwise noted and Application Circuit refer to Table 21

Figure 91. Device Performance Pin-Pout-Gain @3.5GHz

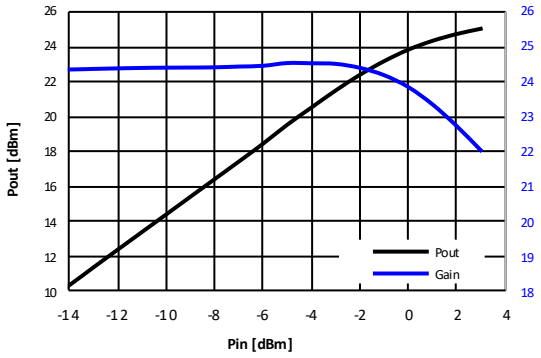


Figure 92. Noise Figure vs Frequency
over Temperature

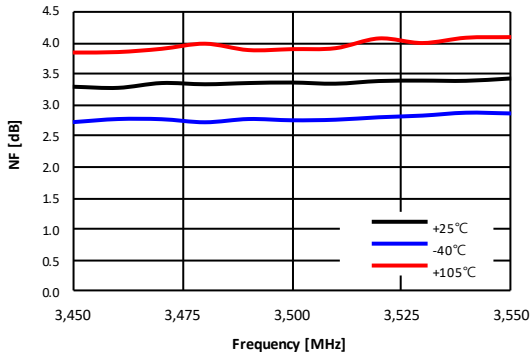


Figure 93. 3GPP LTE 20MHz ACLR vs Output Power @3.5GHz
over Temperature

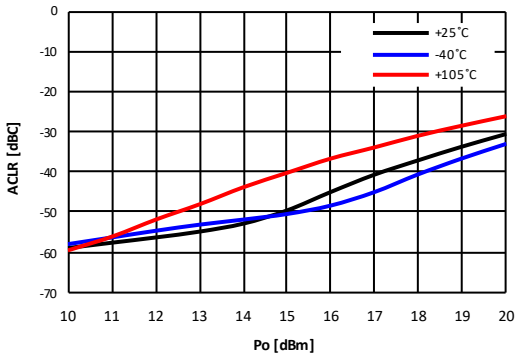
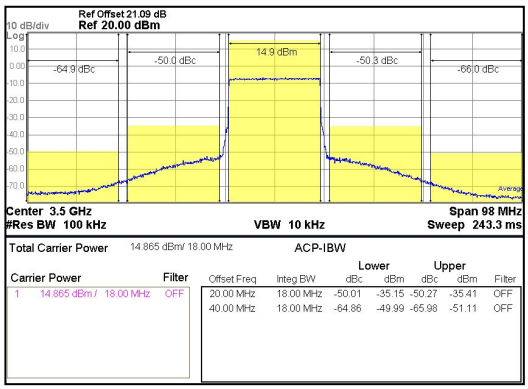


Figure 94. ACLR @3.5GHz, LTE20MHz[1], -50dBc



1. LTE set-up: 3GPP LTE, FDD E-TM1.1, 20MHz BW, ±20MHz offset, PAR 9.81 at 0.01% Prob. @ACLR –50dBc .

Figure 95. Evaluation Board PCB Layer Information

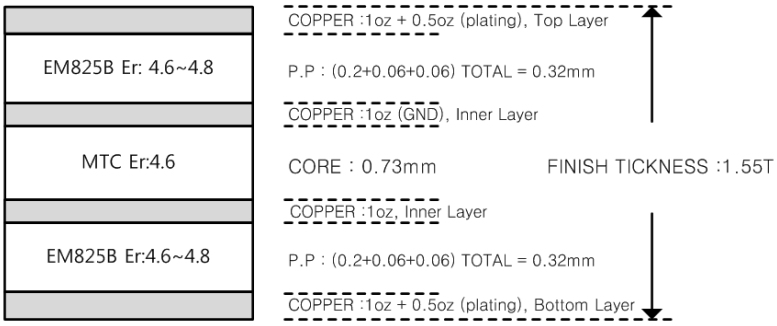
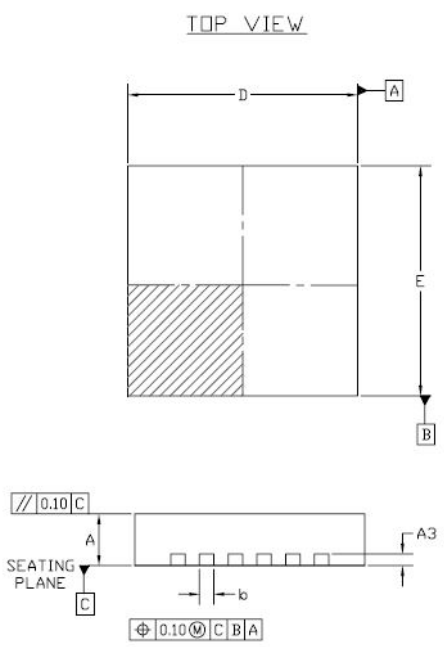


Table 23. Bill of material Information

No.	Value	Description	Manuf.	Part Number
1	1.0nF	IND, 0402, CHIP, 5%	murata	LQG15HS1N0S02D
2	1.2nH	IND, 0402, CHIP, 5%	murata	LQG15HS1N2S02D
3	1.5nH	IND, 0402, CHIP, 5%	murata	LQG15HS1N5S02D
4	2.0nH	IND, 0402, CHIP, 5%	murata	LQG15HS2N0S02D
5	3.0nH	IND, 0402, CHIP, 5%	murata	LQG15HS3N0S02D
6	4.3nH	IND, 0402, CHIP, 5%	murata	LQG15HS4N3S02D
7	4.7nH	IND, 0402, CHIP, 5%	murata	LQG15HS4N7S02D
8	5.1nH	IND, 0402, CHIP, 5%	murata	LQG15HS5N1S02D
9	10nH	IND, 0402, CHIP, 5%	murata	LQG15HS10NJ02D
10	15nH	IND, 0402, CHIP, 5%	murata	LQG15HS15NJ02D
11	22nH	IND, 0402, CHIP, 5%	murata	LQG15HS22NJ02D
12	27nH	IND, 0402, CHIP, 5%	murata	LQG15HS27NJ02D
13	33nH	IND, 0402, CHIP, ±5%	murata	LQG15HS33NJ02D
14	0.5pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C0R5CB5NNNC
15	0.75pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05CR75CB5NNNC
16	1.0pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R0CB5NNNC
17	1.2pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R2CB5NNNC
18	1.3pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R3CB5NNNC
19	1.5pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R5CB5NNNC
20	1.8pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C1R8CB5NNNC
21	2.0pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C020CB5NNNC
22	7.5pF	CAP, 0402, CHIP Ceramic, ±0.25%	WALSIN tech	0402N7RD500CT
23	9pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C090CB5NNNC
24	10pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C100CB5NNNC
25	20pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C200CB5NNNC
26	22pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C220CB5NNNC
27	62pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C620CB5NNNC
28	100pF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C101CB5NNNC
29	1nF	CAP, 0402, CHIP Ceramic, ±0.25%	samsung	CL05C102CB5NNNC
30	1uF	CAP, 0402, (105Z 10V)	WALSIN tech	0402F105Z100CT
31	0ohm	RES, 0402, CHIP, ±5%	samsung	RC1005J000CS

Figure 96. Packing outline Dimension



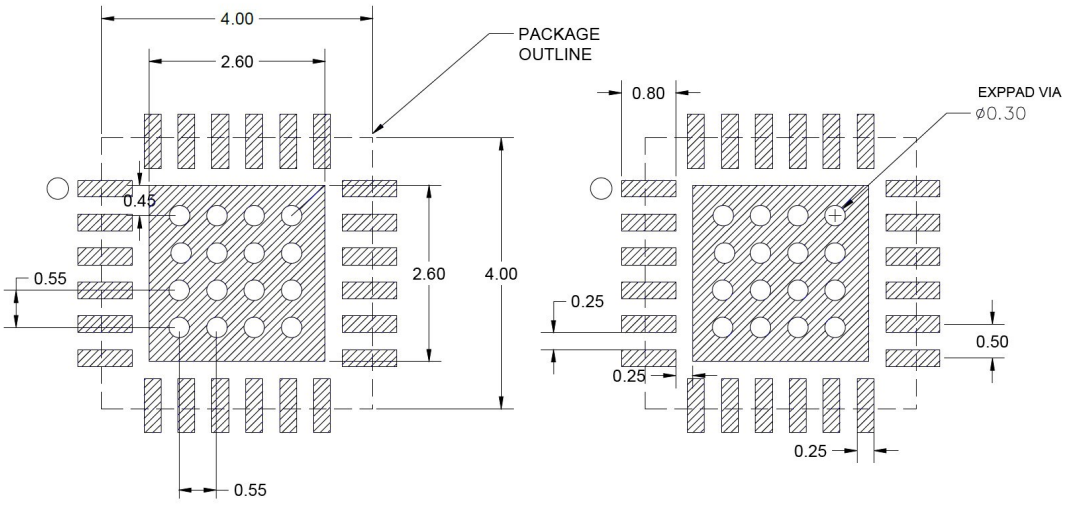
NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM. FROM TERMINAL TIP.

SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	SEE VARIATION "A"					
A3	0.203 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.925	4.00	4.075	0.154	0.157	0.160
D2	2.30	2.40	2.50	0.090	0.094	0.098
E	3.925	4.00	4.075	0.154	0.157	0.160
E2	2.30	2.40	2.50	0.090	0.094	0.098
e	0.500 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017

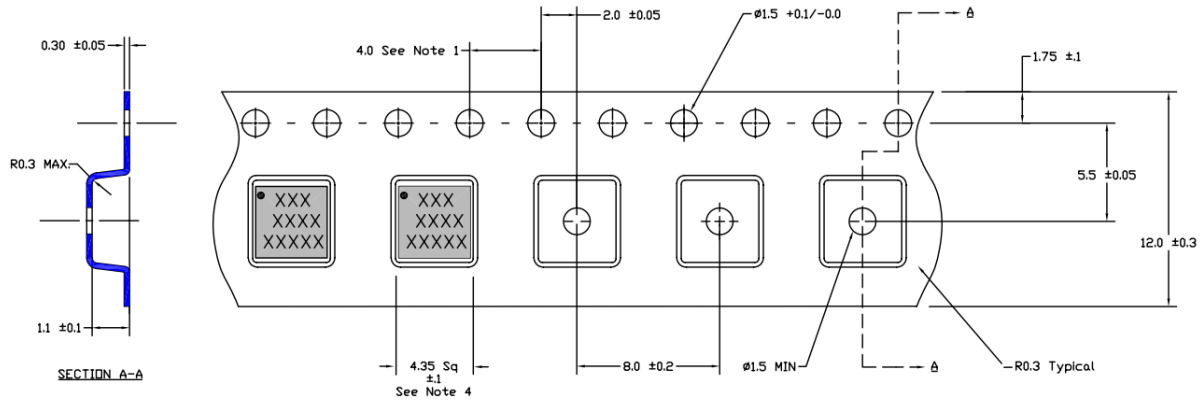
SYMBOL	VARIATION "A"					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
QFN	0.85	0.90	0.95	0.033	0.035	0.037
TQFN	0.70	0.75	0.80	0.027	0.029	0.031

Figure 97. Suggested PCB Land Pattern and PAD Layout



0.7- 4GHz 1/4W Medium Power DIGITAL VARIABLE GAIN AMPLIFIER

Figure 98. Tape & Reel



Packaging information:	
Tape Width	12mm
Reel Size	7”
Device Cavity Pitch	8mm
Devices Per Reel	1K

Figure 99. Package Marking

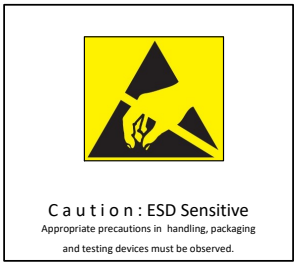
Marking information:	
BVA2140B	Device Name
YY	Year
WW	Work Week
XX	LOT Number

Lead plating finish

100% Tin Matte finish

MSL / ESD Rating

ESD Rating:	Class 1C
Value:	Passes ≤ 2000V
Test:	Human Body Model(HBM)
Standard:	JEDEC Standard JS-001-2017
MSL Rating:	**Level 1 at +265°C convection reflow**
Standard:	JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

NATO CAGE code:

2	N	9	6	F