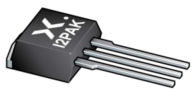


BUK7E2R3-40C

N-channel TrenchMOS standard level FET

Rev. 03 — 26 January 2009 Product data sheet

1. Product profile

1.1 General description

Standard level gate drive N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using advanced TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in high performance automotive applications.

1.2 Features and benefits

- AEC Q101 compliant
- Avalanche robust
- Suitable for standard level gate drive
- Suitable for thermally demanding environment up to 175°C rating

1.3 Applications

- 12V Motor, lamp and solenoid loads
- High performance automotive power systems
- High performance Pulse Width Modulation (PWM) applications

1.4 Quick reference data

Table 1. Quick reference

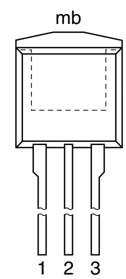
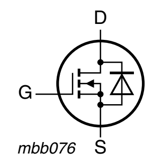
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	40	V
I_D	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 3;	[1] [2]	-	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	-	333	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 12; see Figure 13		-	1.96	2.3	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped		-	-	1.2	J

[1] Refer to document 9397 750 12572 for further information.

[2] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT226 (TO-220AB;I2PAK)

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7E2R3-40C	TO-220AB; I2PAK	plastic single-ended package (I2PAK); low-profile 3-lead TO-220AB	SOT226

4. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3;	[1][2]	-	100	A
		$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1; see Figure 3;	[1][3]	-	276	A
		$T_{mb} = 100$ °C; $V_{GS} = 10$ V; see Figure 1;	[1][2]	-	100	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 3		-	1104	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2		-	333	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25$ °C;	[1][3]	-	276	A
		$T_{mb} = 25$ °C;	[1][2]	-	100	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C		-	1104	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 100$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped		-	1.2	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 4;	[4][5][6][7]	-	-	J

[1] Refer to document 9397 750 12572 for further information.

[2] Continuous current is limited by package.

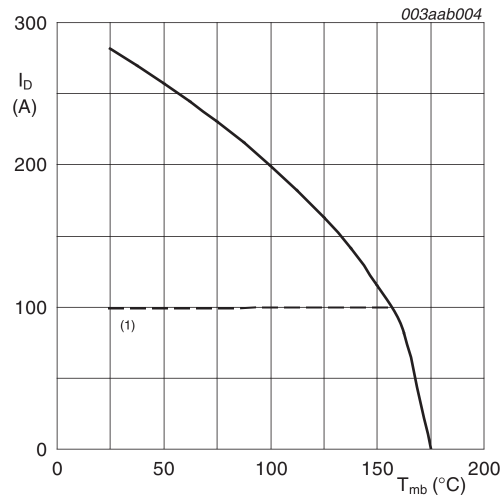
[3] Current is limited by power dissipation chip rating.

[4] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.

[5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[6] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

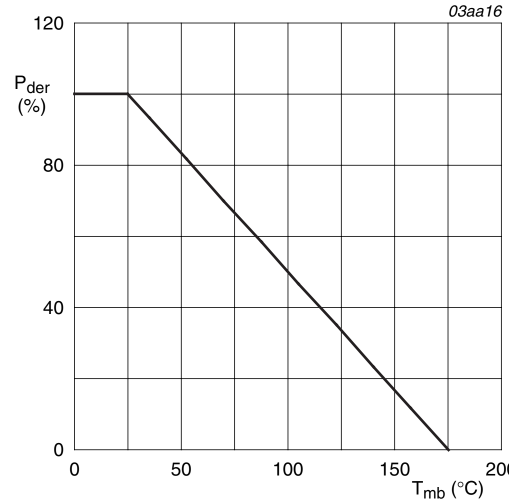
[7] Refer to application note AN10273 for further information.



$V_{GS} \geq 10\,V$

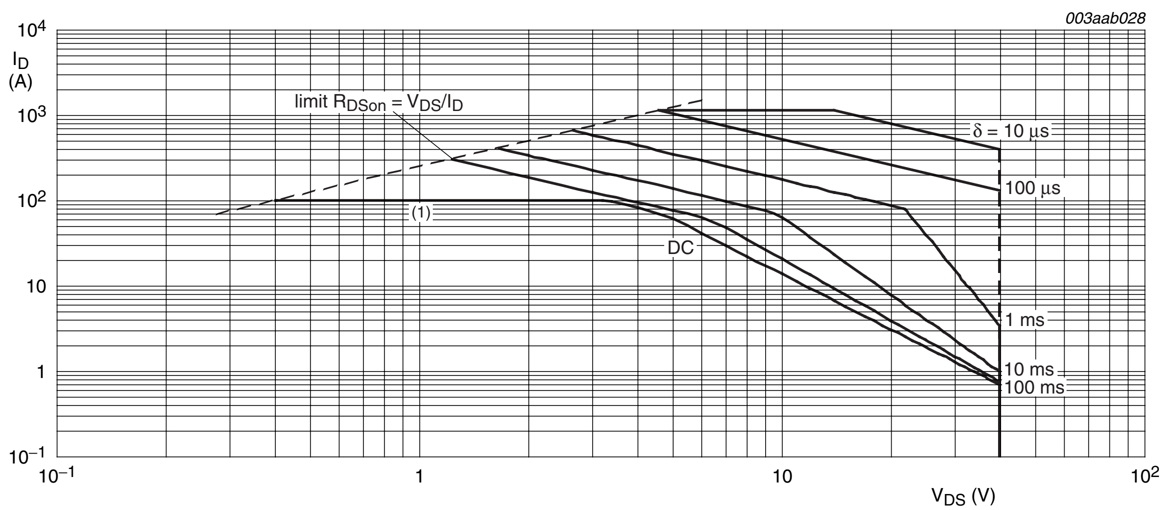
(1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



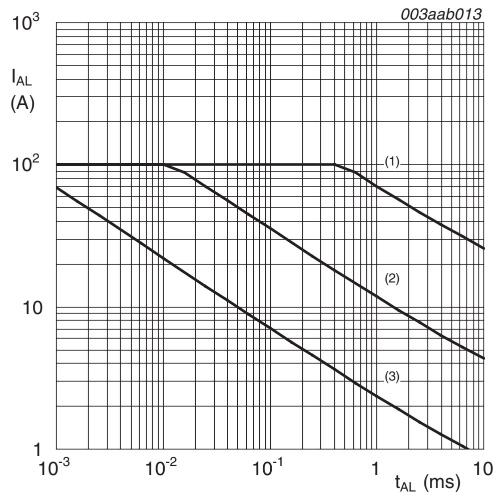
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25\,°C$; I_{DM} is single pulse. (1) Capped at 100 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) Single-pulse; $T_{mb} = 25\,°C$.
(2) Single-pulse; $T_{mb} = 150\,°C$.
(3) Repetitive.

Fig 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in free air	-	50	-	K/W

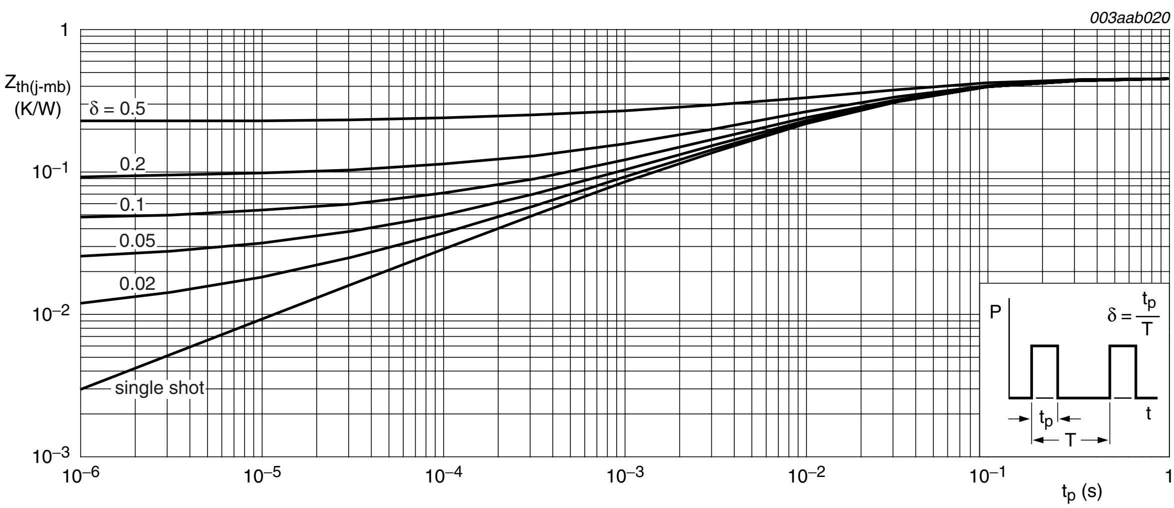
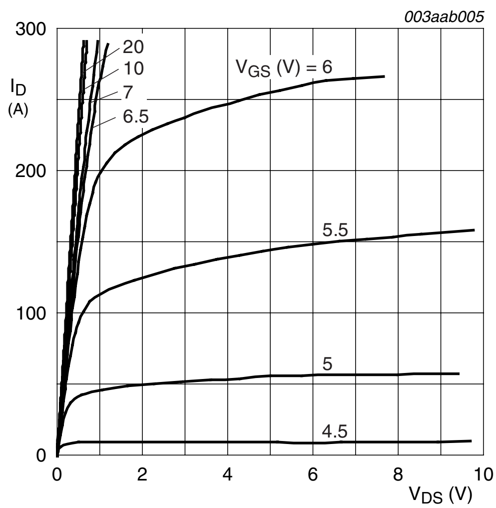


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

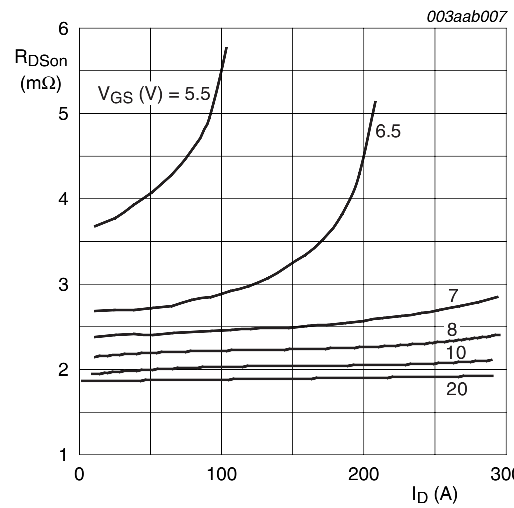
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10; see Figure 11	2	3	4	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 10; see Figure 11	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10; see Figure 11	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -20 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 12; see Figure 13	-	-	4.26	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 12; see Figure 13	-	1.96	2.3	mΩ
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; see Figure 15	-	175	-	nC
Q_{GS}	gate-source charge		-	49	-	nC
Q_{GD}	gate-drain charge		-	67	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 32 V; see Figure 15	-	5	-	V
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 16	-	8492	11323	pF
C_{oss}	output capacitance		-	1606	1927	pF
C_{rss}	reverse transfer capacitance		-	1101	1508	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω	-	65	-	ns
t_r	rise time		-	133	-	ns
$t_{d(off)}$	turn-off delay time		-	146	-	ns
t_f	fall time		-	119	-	ns
L_D	internal drain inductance	from drain lead 6 mm from package to centre of die	-	4.5	-	nH
		from upper edge of drain mounting base to centre of die	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 14	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V	-	75	-	ns
Q_r	recovered charge		-	57	-	nC



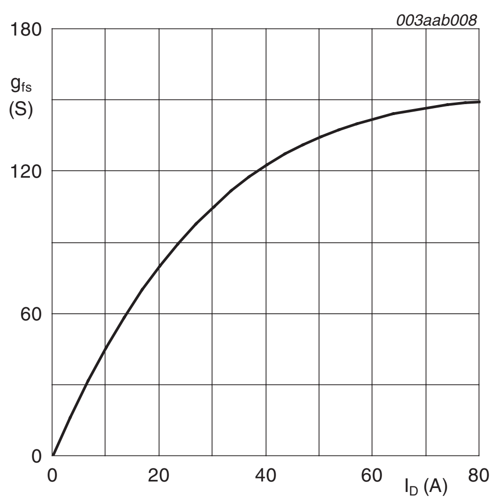
$T_j = 25\,°C$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



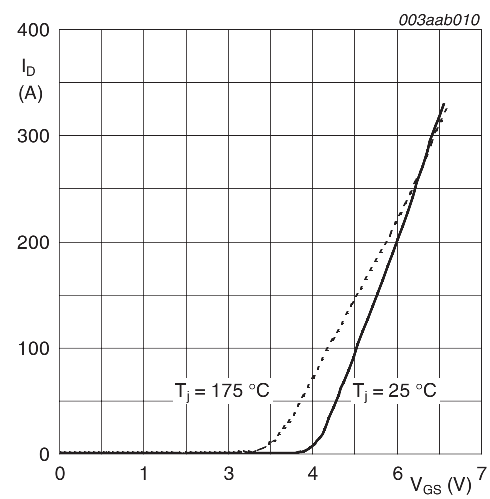
$T_j = 25\,°C$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



$T_j = 25\,°C; V_{DS} = 25\,V$

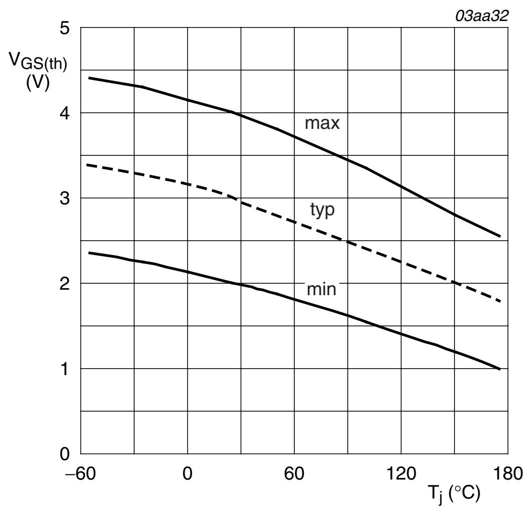
Fig 8. Forward transconductance as a function of drain current; typical values



$V_{DS} = 25\,V$

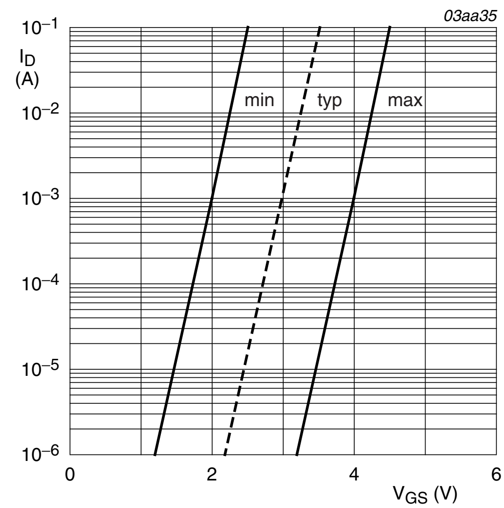
Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

BUK7E2R3-40C_3



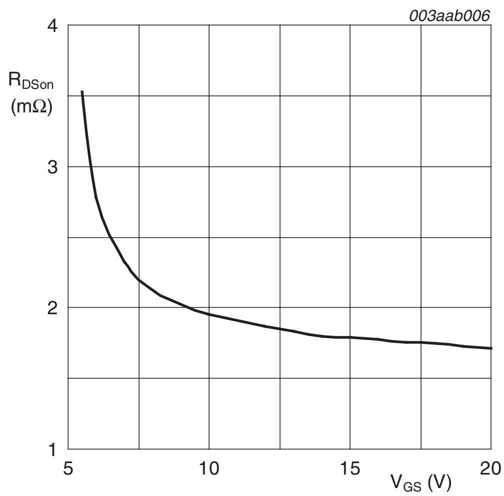
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



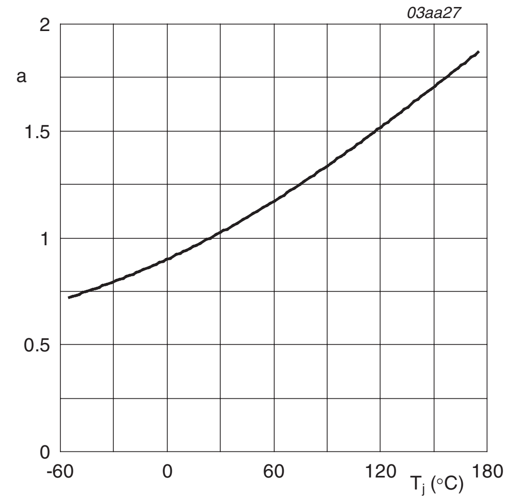
$T_j = 25\,°C; V_{DS} = 5V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



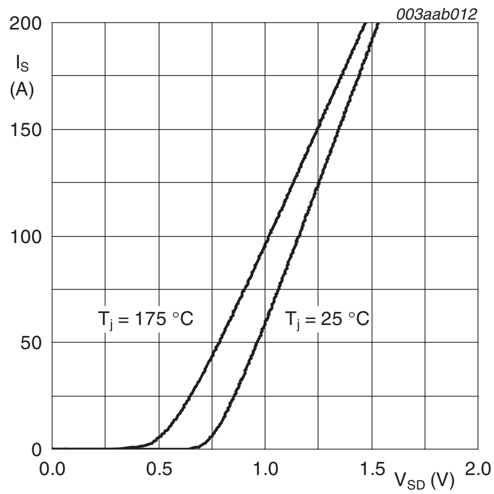
$T_j = 25\,°C; I_D = 25\,A$

Fig 12. Drain-source on-state resistance as a function of gate-source voltage; typical values



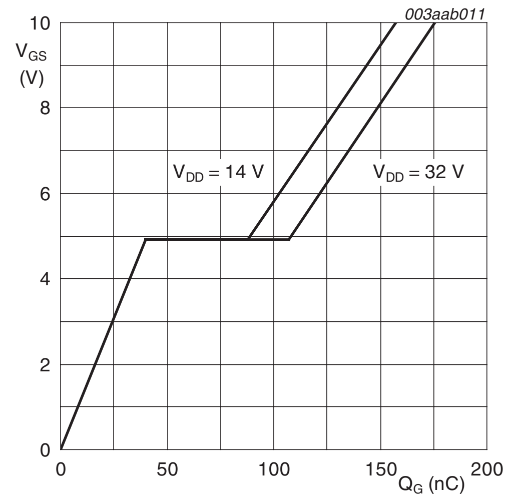
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



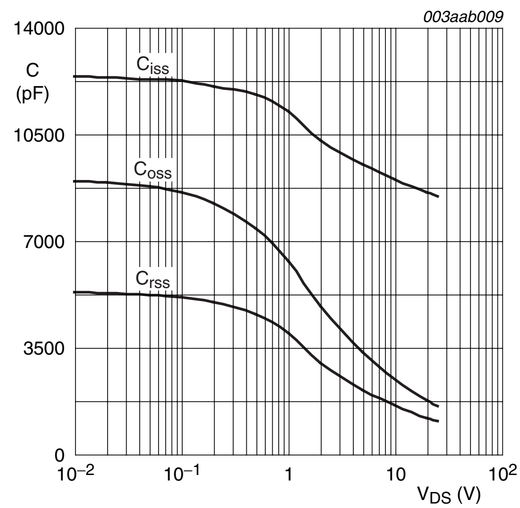
$V_{GS} = 0V$

Fig 14. Source current as a function of source-drain voltage; typical values



$T_j = 25\,°C; I_D = 25A$

Fig 15. Gate-source voltage as a function of gate charge; typical values

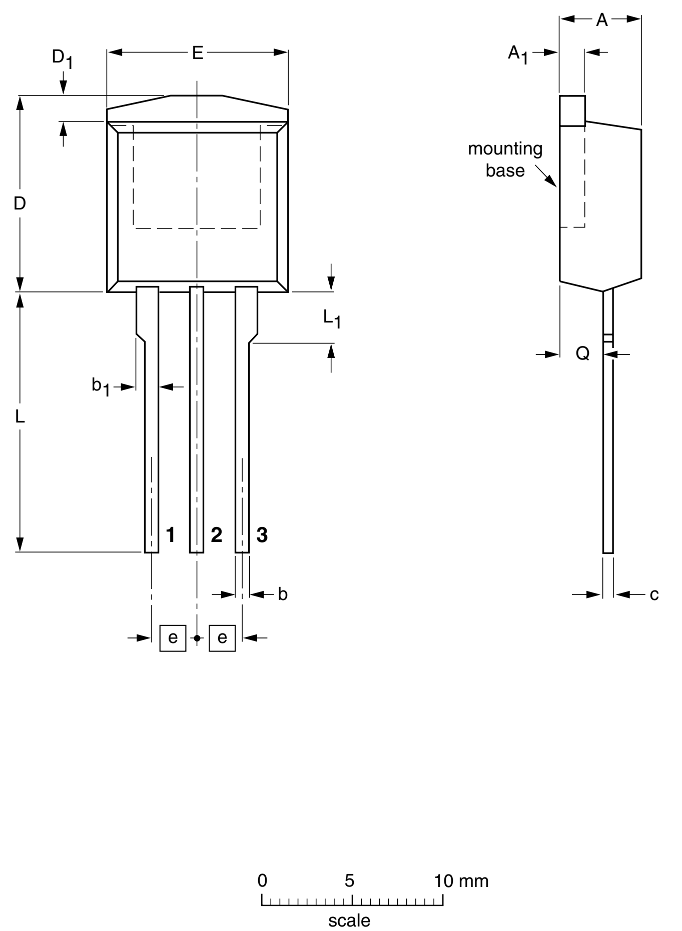


$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-220AB **SOT226**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D max	D_1	E	e	L	L_1	Q
mm	4.5 4.1	1.40 1.27	0.85 0.60	1.3 1.0	0.7 0.4	11	1.6 1.2	10.3 9.7	2.54	15.0 13.5	3.30 2.79	2.6 2.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT226		low-profile 3-lead TO-220AB				~~05-06-23~~ 06-02-14

Fig 17. Package outline SOT226 (I2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7E2R3-40C_3	20090126	Product data sheet	-	BUK75_7E2R3-40C_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number BUK7E2R3-40C separated from data sheet BUK75_7E2R3-40C_2.			
BUK75_7E2R3-40C_2	20060810	Product data sheet	-	BUK75_7E2R3-40C_1
BUK75_7E2R3-40C_1	20060503	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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11. Contents

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Date of release: 26 January 2009