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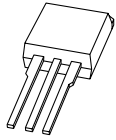
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Team Nexperia



BUK7E07-55B

N-channel TrenchMOS standard level FET

Rev. 01 — 29 January 2008

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in Automotive critical applications.

1.2 Features

- Very low on-state resistance
- 175 °C rated
- Q101 compliant
- Standard level compatible

1.3 Applications

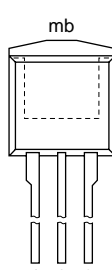
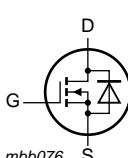
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V and 24 V loads

1.4 Quick reference data

- $E_{DS(AL)S} \leq 351$ mJ
- $I_D \leq 75$ A
- $R_{DS(on)} = 5.8$ m Ω (typ)
- $P_{tot} \leq 203$ W

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)		
2	drain (D)		
3	source (S)		
mb	mounting base; connected to drain (D)		

SOT226 (I2PAK)

3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
BUK7E07-55B	I2PAK	plastic single-ended package (I2PAK); low-profile 3-lead TO-220AB	SOT226

4. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

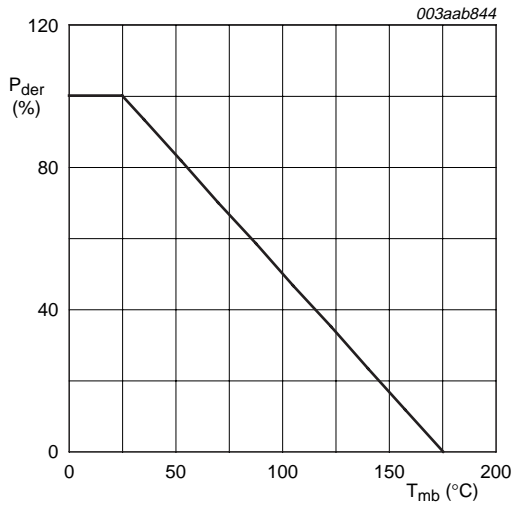
Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage		-	55	V	
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	-	55	V	
V_{GS}	gate-source voltage		-	± 20	V	
I_D	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; see Figure 2 and 3	[1]	-	119	A
			[2]	-	75	A
		$T_{mb} = 100\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; see Figure 2	[2]	-	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	478	A	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; see Figure 1	-	203	W	
T_{stg}	storage temperature		-55	+175	$^\circ\text{C}$	
T_j	junction temperature		-55	+175	$^\circ\text{C}$	
Source-drain diode						
I_{DR}	reverse drain current	$T_{mb} = 25\text{ }^\circ\text{C}$	[2]	-	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	478	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	Unclamped inductive load; $I_D = 75\text{ A}$; $V_{DS} \leq 55\text{ V}$; $V_{GS} = 10\text{ V}$; $R_{GS} = 50\text{ }\Omega$; starting at $T_j = 25\text{ }^\circ\text{C}$	-	351	mJ	
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	Repetitive rating defined in Figure 16	[3]	-	-	J

[1] Current is limited by chip power dissipation rating.

[2] Continuous current is limited by package.

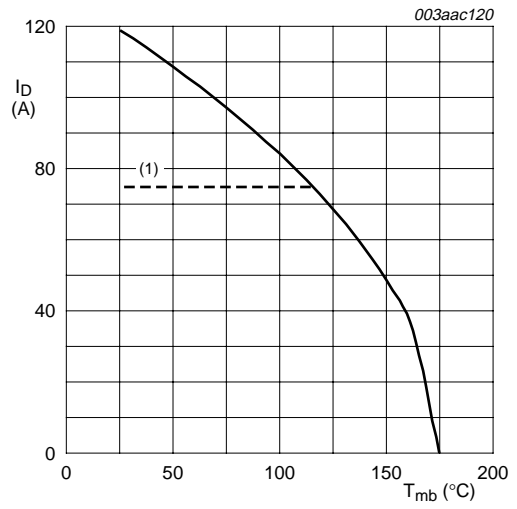
[3] Conditions:

- a) Maximum value not quoted.
- b) Single-pulse avalanche rating limited by $T_{j(max)}$ of 175 $^\circ\text{C}$.
- c) Repetitive avalanche rating limited by an average junction temperature of 170 $^\circ\text{C}$.
- d) Refer to application note *AN10273* for further information.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

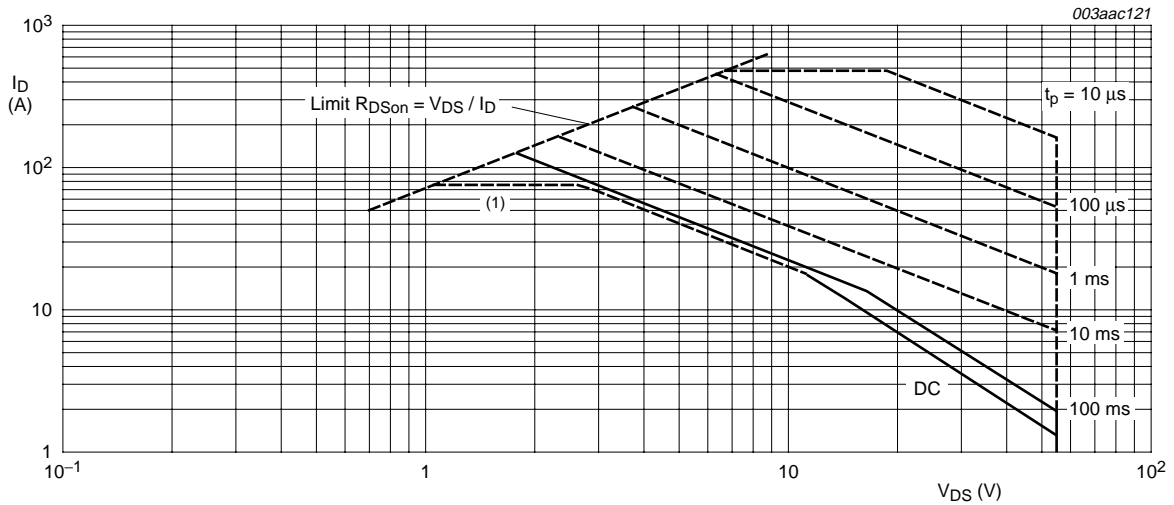
Fig 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10$ V

(1) Capped at 75 A due to package.

Fig 2. Continuous drain current as a function of mounting base temperature



$T_{mb} = 25$ °C; I_{DM} is single pulse.

(1) Capped at 75 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	-	-	-	0.74	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

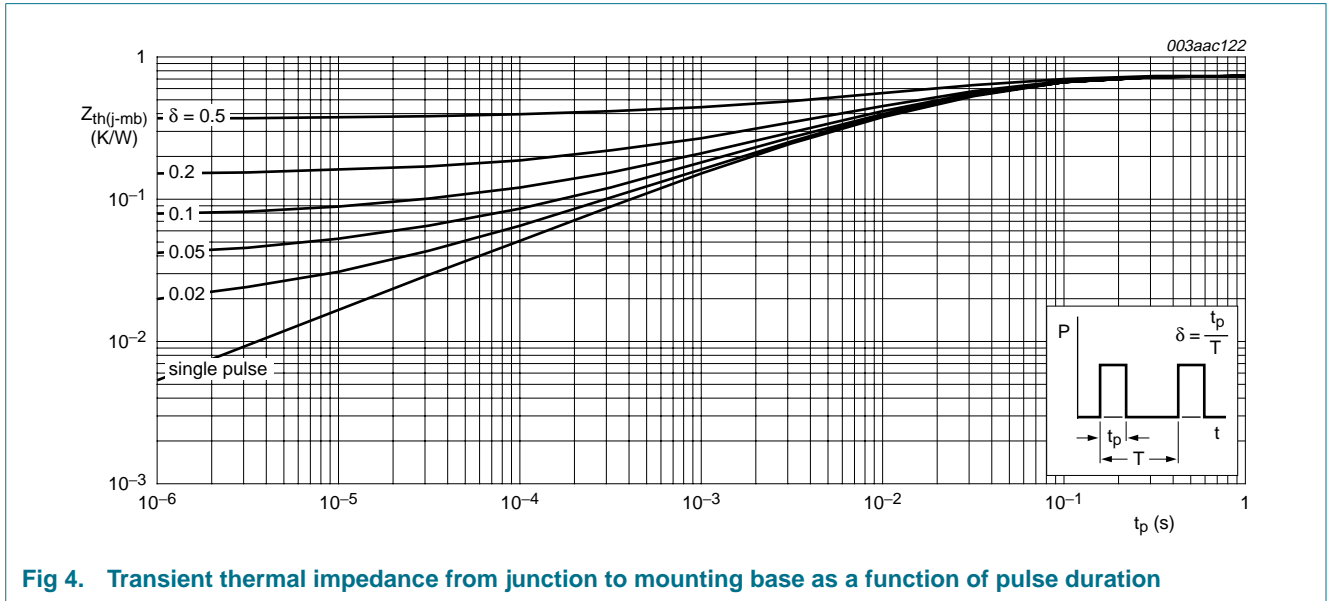
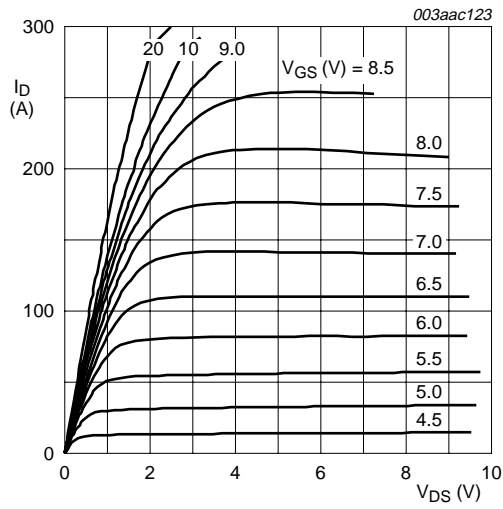


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

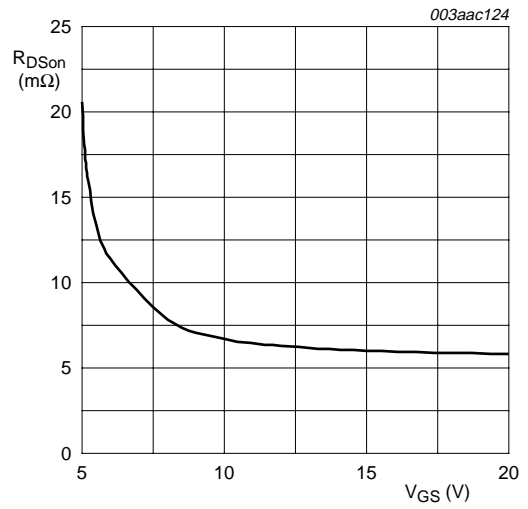
Table 5. Characteristics
 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	55	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ }^\circ\text{C}$	2	3	4	V
		$T_j = 175\text{ }^\circ\text{C}$	1	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	-	-	4.4	V
I_{DSS}	drain leakage current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	0.02	1	μA
		$T_j = 175\text{ }^\circ\text{C}$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$; see Figure 6 and 8				
		$T_j = 25\text{ }^\circ\text{C}$	-	5.8	7.1	m Ω
		$T_j = 175\text{ }^\circ\text{C}$	-	-	14.2	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}; V_{DS} = 44\text{ V}; V_{GS} = 10\text{ V}$; see Figure 14	-	53	-	nC
Q_{GS}	gate-source charge		-	12	-	nC
Q_{GD}	gate-drain charge		-	17	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$; see Figure 12	-	2820	3760	pF
C_{oss}	output capacitance		-	554	665	pF
C_{rss}	reverse transfer capacitance		-	200	274	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega$;	-	24	-	ns
t_r	rise time	$V_{GS} = 10\text{ V}; R_G = 10\text{ }\Omega$	-	52	-	ns
$t_{d(off)}$	turn-off delay time		-	77	-	ns
t_f	fall time		-	41	-	ns
L_D	internal drain inductance	measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_S	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}$; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}$;	-	62	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}; V_R = 30\text{ V}$	-	60	-	nC



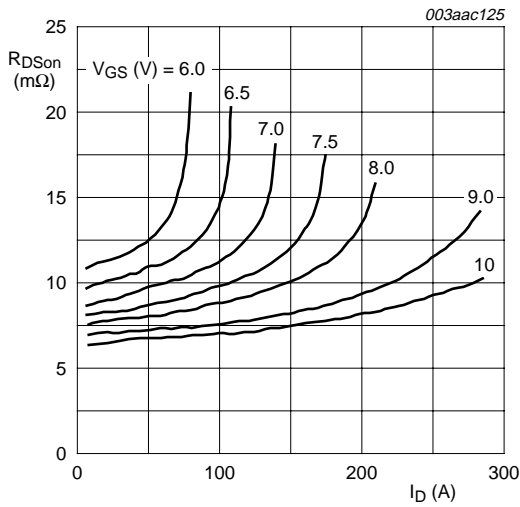
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



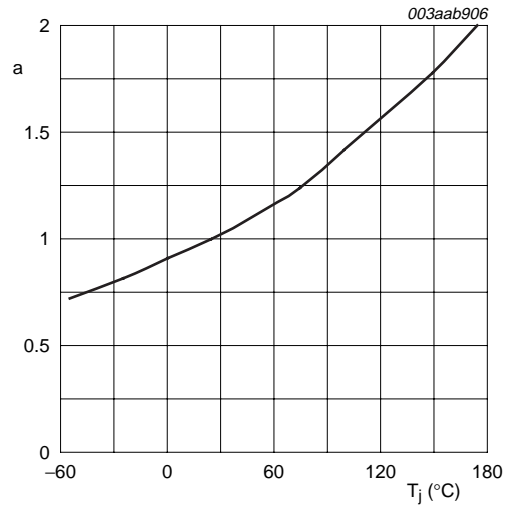
$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



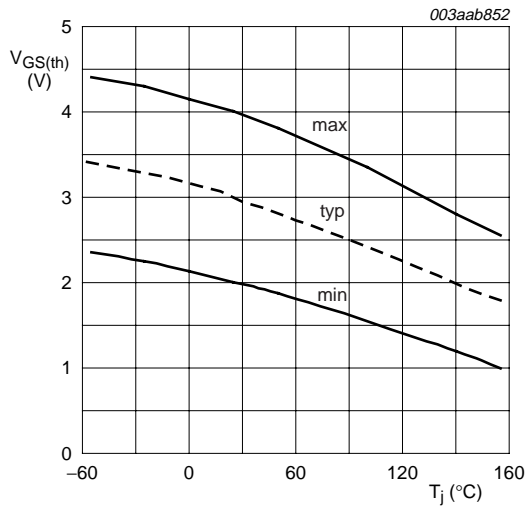
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



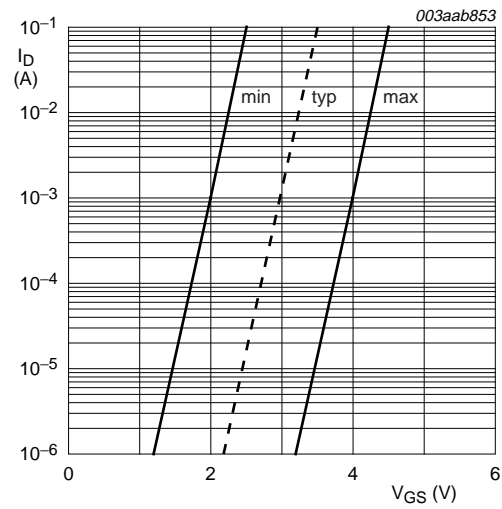
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



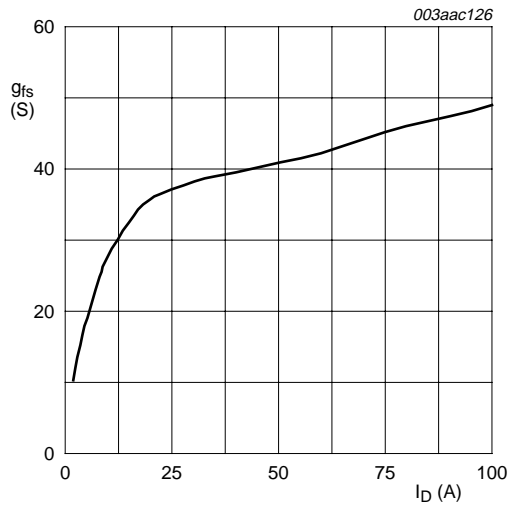
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



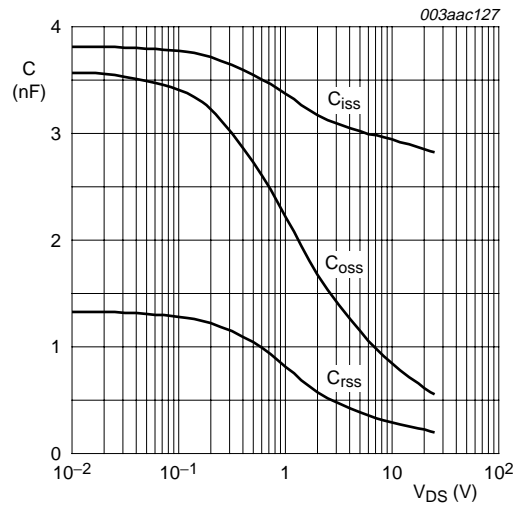
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



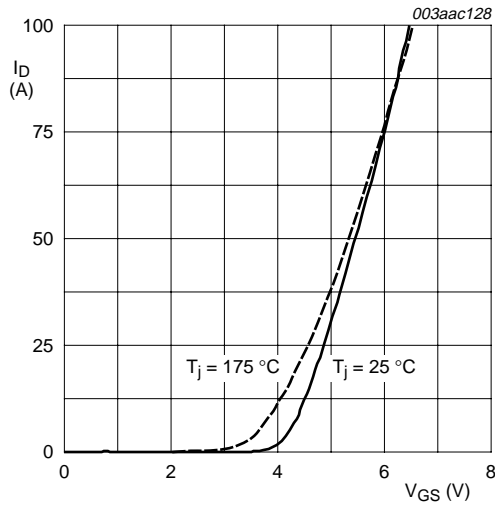
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values



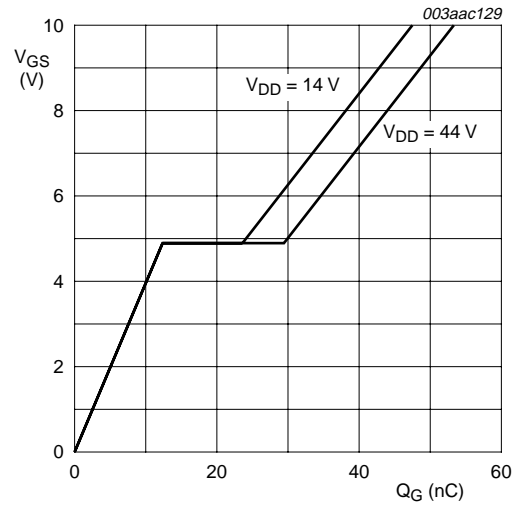
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



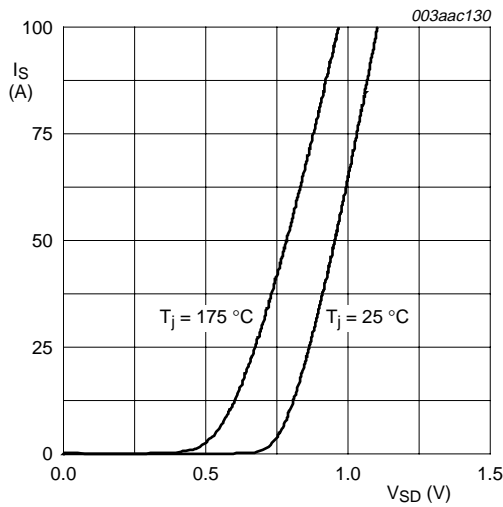
$V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



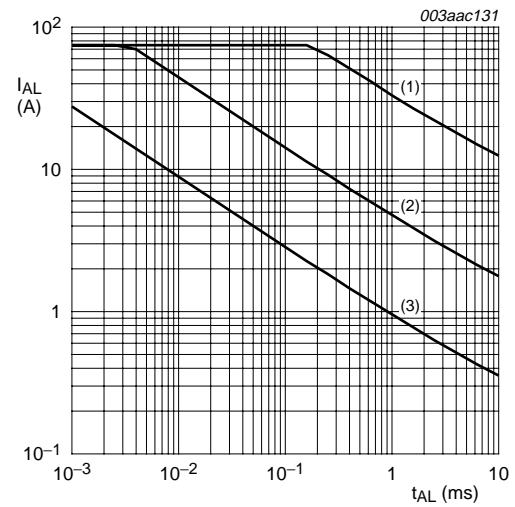
$T_j = 25 \text{ °C}; I_D = 25 \text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 \text{ V}$

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



See [Table note 3](#) of [Table 3](#) Limiting values.

- (1) Single-pulse; $T_j = 25 \text{ °C}$.
- (2) Single-pulse; $T_j = 150 \text{ °C}$.
- (3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic single-ended package (I2PAK); low-profile 3-lead TO-220AB

SOT226

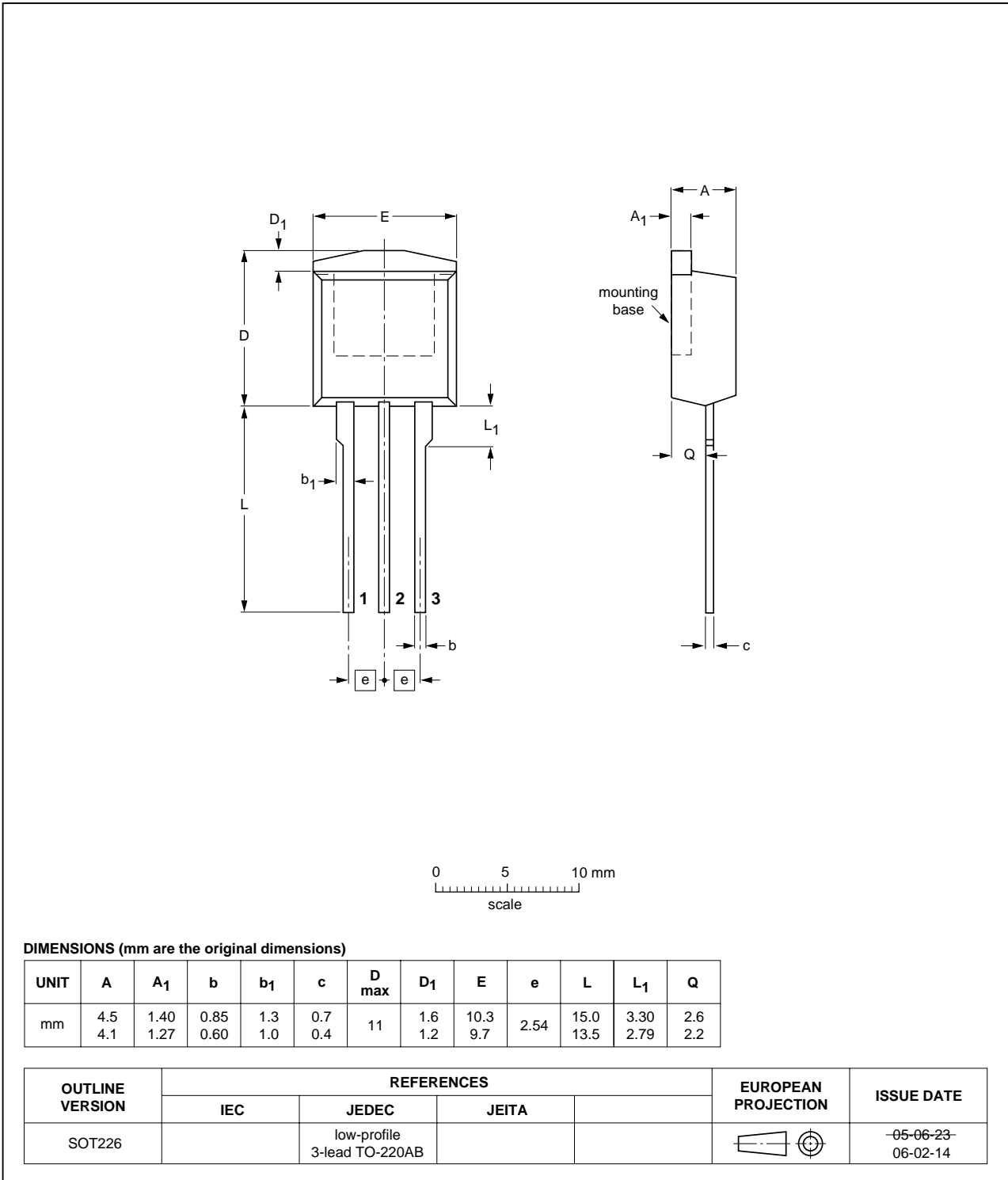


Fig 17. Package outline SOT226 (I2PAK)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7E07-55B_1	20080129	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 29 January 2008

Document identifier: BUK7E07-55B_1