For Home Electronics and Security Devices Camera Image Processor Series

Camera Image Processors Compatible with JPEG Image

BU6566GVW, BU6568GV

No.09061JET02

●Description

BU6566GVW/BU6568GV is a camera image processor compatible with standard JPEG.
Pin-to-Pin compatibility enable support for both standard and high-resolution cameras.

●Features

1)Built-in Camera Module Interface

VGA size (640×480)/BU6566GVW, SXGA size (1280×1024)/BU6568GV for input of image data up to 15 fps (zooming function is available).
Input data format for YUV=4:2:2, RGB=4:4:4.
Filter processing (image processing) to input images (2 gradations / gray scale / sepia / emboss / edge enhancement/ negative).
Multi-step size reduction down to 1/8 (BU6566GVW), 1/16 (BU6568GV) in X- and Y-direction possible.
Cutting out into an arbitrary size after resizing.
D range enlargement processing of Y (brightness) available in YUV color space to cut images.
Cut images to be stored into an arbitrary position in frame memory in YUV=4:2:2 format.
2-line serial interface built in for camera module control.

2)Built-in frame memory / JPEG code memory

Image frame memory built in (80KB for storing 1 frame of 176x232 @16 bits/pixel).
Display area settable to an arbitrary LCD size.
Data to be stored into image frame memory in YUV=4:2:2 format.
Mask data to be stored into mask frame memory in 1bit/2pixels in YUV=4:2:2 format.
An arbitrary position of frame memory to be updated to camera image according to mask memory.
Image frame memory accessible from HOST CPU (access available both in RGB and YUV).
Rectangular writing function and rectangular reading function for transparent color to image frame memory.
Frame memory usable as JPEG code memory (80KB) to store JPEG compressed images.
Frame memory usable as a ring buffer for JPEG code of 80KB or more.

3)Built-in LCD controller interface

Built-in input/output interface to LCD controller
For display colors of 262144 colors / 65536 colors / 4096 colors.
Up to 2 LCD module controllers controllable.
Arbitrary rectangular selection in frame memory to be transferred to LCD controller.

4)Built-in JPEG CODEC

ISO/IEC10918 conforming base line method.

・Compression

For YUV=4:2:2 only.
Quantization table selectable from 20 built-in tables.

・Decompression

For YUV=4:4:4, 4:2:2(horizontal sub-sampling:BU6566GVW),
4:2:0, 4:1:1(horizontal sub-sampling:BU6566GVW), and gray scale.

5) Built-in HOST CPU interface

For 8-bit/16-bit bus interface in parallel interface.

Read/ write access to frame memory.

Read/ write access to internal registers (Indirect access with a index register as the address).

Read/ write access to the LCD controller: Parallel/Serial (Direct access available via the LCD interface).

6) Extended overlay function

Supporting overlay of icon-data/font-data of up to two points during LCD data transfer.

Both icon-data and font-data corresponding to 65536 display colors. Possible to setting transparent colors.

7) LED interface, GIO function

Built-in PWM output of 4 systems for 3 color LED controls and white LED control.

7 GIO's in total available for the GIO function.

8) Clock generation, power management function

Oscillation circuit configuration by XIN and XOUT terminals, or clock input from XIN terminal available.

Built-in PLL in BU6568GV.

Clock control of IC inside in unit of block (suspend mode available).

9) Key interfaces built in

3 systems of key interfaces built in. Interruption to be generated at key input.

Useable for removing software chattering.

∗ Data is prepared separately about each register setup. Please refer to the Development Scheme on page 14.

System 1 (VDDIO1)	System 2 (VDDIO2)
P3-P4(D15-14),P6-P11(D13-8), P14-P18(D7-0),P23(A2), P28-P31(A1,CSB,WRB,RDB), P97-P98(XOUT,XIN),P33(INT*1)	P34-P44(CAMVS, CAMHS, CAMD0-3, GIO2, CAMD4-7), P46(CAMCKI), P48(CAMCKO), P53-P65(SDA, SDC, LEDCNT, PWM1-3, VD, LCDCS1B, LCDCS2B, KEY0, LCDWRB, LCDRDB, LCDA0) P67-P69(LCDD0-2), P71-P72(LCDD3-4) P78-P87(LCDD5-7, TEST, X16_8, LCDD8-12), P89-P94(KEY1, LCDD13-15, RESETB, PWM0)

*1 ; P33 (INT) terminal is the power source system of VDDIO2 in BU6568GV.

●Application

Security camera, Intercom with camera, Drive recorder, and Web camera etc.

●Lineup

Parameter	Power source voltage IO1:HOSTI/F IO2:Camera, LCD	Camera interface	Host CPU interface	LCD interface	Codec [Image]	Multimedia interface	Package
BU6566GVW	1.45-1.55V(V_{DD}Core) 1.70-3.15V(V_{DD}IO1) 2.70-3.15V(V_{DD}IO2)	Supported up to 0.3M pixels. (640×480)	8bit/16bit bus 80 systems CPU Interface	Supported up to QCIF+(232×176)	0.3M pixels JPEG Codec Motion-JPEG	-	SBGA099W070
BU6568GV		Supported up to 1.3M pixels. (1280×1024)			1.3M pixels JPEG Codec Motion-JPEG		SBGA099T070

∗ Although QCIF+ is 220x176 pixels, it is supported to 232x176 pixels by effective use of memory in ROHM products.

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Applied power source voltage 1	VDDIO1	-0.3～+4.2	V
Applied power source voltage 2	VDDIO2	-0.3～+4.2	V
Applied power source voltage 3	VDD	-0.3～+2.1	V
Other terminals	-	-0.3～VDDIO+0.3	V
Storage temperature range	Tstg	-40～+150	℃
Power dissipation	PD	410	mW

＊ In the case exceeding 25ºC, 4.1mW should be reduced at the rating 1ºC.

●Recommended operating range

Parameter	Symbol	Rating	Unit
Applied power source voltage 1	VDDIO1	1.70～3.15(Typ:1.80V)	V
Applied power source voltage 2	VDDIO2	2.70～3.15(Typ:2.85V)	V
Applied power source voltage 3	VDD	1.45～1.55(Typ:1.50V)	V
Input voltage range	VIN	0～VDDIO	V
Operating temperature range	Topr	-30～+85	℃

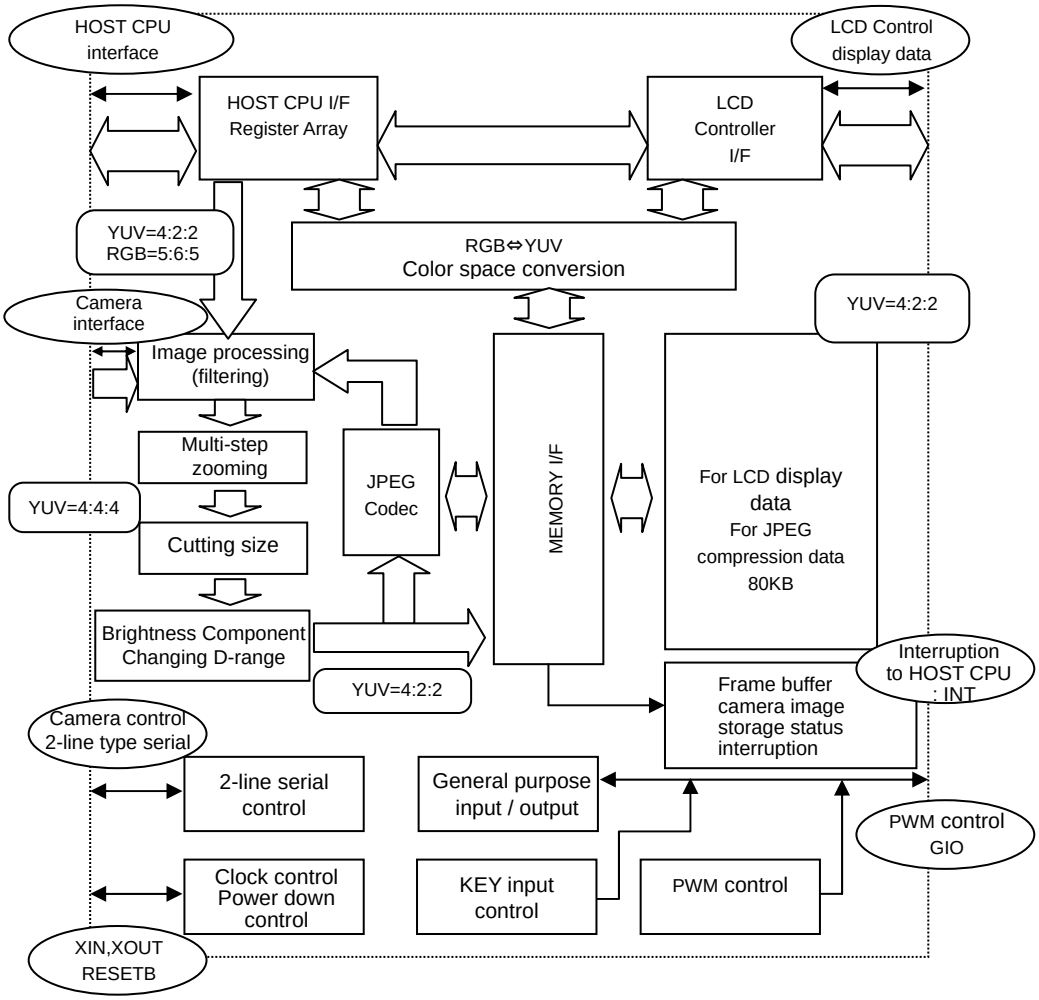
＊ Please supply power source in order of VDD→VDDIO1→VDDIO2.

●Electric characteristics

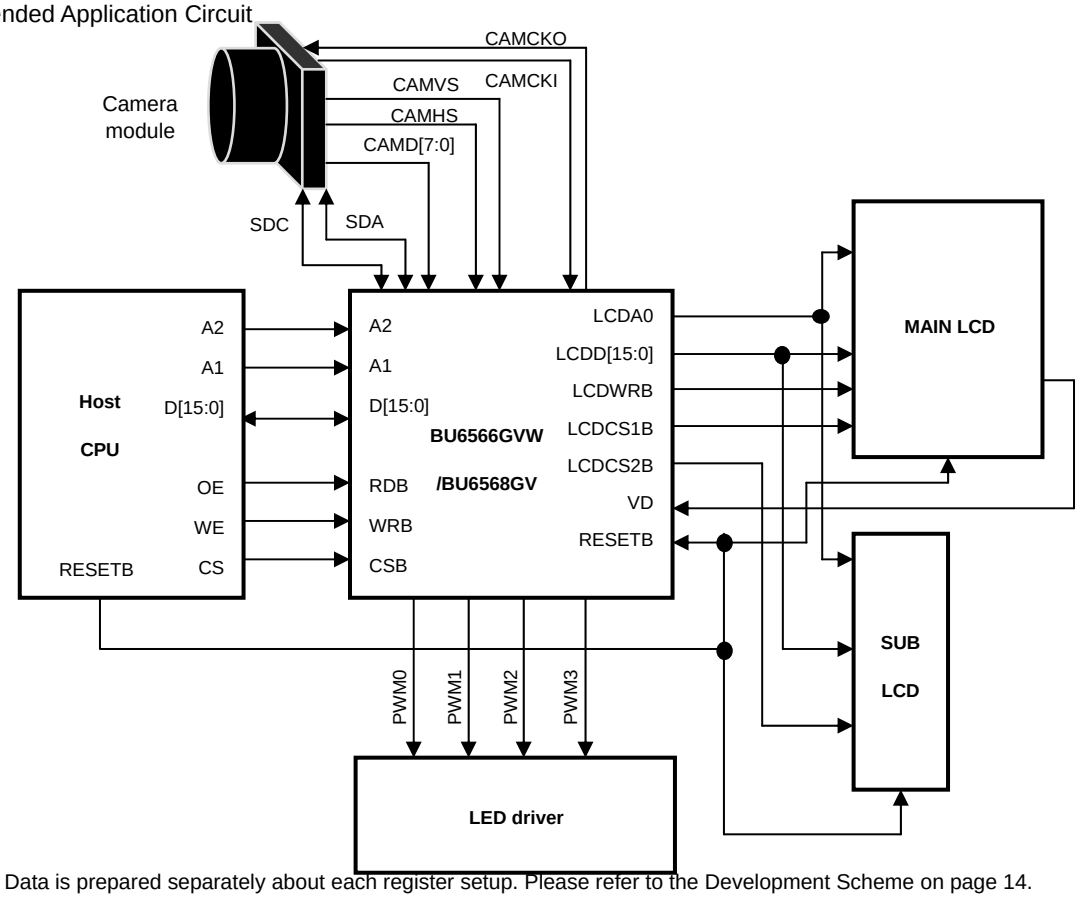
(Unless otherwise specified, Ta=25℃,VDD=1.50V,VDDIO=2.85V, fin=30.0MHz,fSYS=30.0MHz/BU6566GVW
fin=13.0MHz ,fSYS=52.0MHz (using PLL)/BU6568GV)

Parameter	Symbol	Limits			Unit	Condition	
		MIN.	TYP.	MAX.			
Input frequency	f IN	-	-	30.0 /30.0	MHz	BU6566GVW BU6568GV	XIN XIN (Duty 50±5%), at PLL OFF
Internal operating frequency	f SYS	-	-	30.0 /52.0	MHz	BU6566GVW BU6568GV	Internal SCLK frequency
Operating consumption current	IDD	-	6.4 /15	-	mA	BU6566GVW BU6568GV	At camera ON, LCD display ON At viewer operating
Static consumption current	IDDst	-	-	50 /100	μA	BU6566GVW BU6568GV	At suspend mode setting
Input "H" current 1	IIH1	-10	-	10	μA		VIH=VDDIO
Input "H" current 2	IIH2	25	50	100	μA		Pull-Down terminal, VIH=VDDIO
Input "H" current 3	IIH3	-10	-	10	μA		Pull-Up terminal, VIH=VDDIO
Input "L" current 1	IIL1	-10	-	10	μA		VIL=GND
Input "L" current 2	IIL2	-10	-	10	μA		Pull-Down terminal, VIL=GND
Input "L" current 3	IIL3	-160	-80	-25	μA		Pull-Up terminal, VIL=GND
Input "H" voltage1	VIH1	VDDIO ×0.8	-	VDDIO +0.3	V		Normal input (including input mode of I/O terminal)
Input "L" voltage 1	VIL1	-0.3	-	VDDIO ×0.2	V		Normal input (including input mode of I/O terminal)
Input "H" voltage 2	VIH2	VDDIO ×0.85	-	VDDIO +0.3	V		Hysteresis input
Input "L" voltage 2	VIL2	-0.3	-	VDDIO ×0.15	V		Hysteresis input
Hysteresis voltage width	Vhys	-	0.9 /0.6	-	V	BU6566GVW BU6568GV	Hysteresis input
Output "H" voltage 1	VOH1	VDDIO -0.4	-	VDDIO	V		IOH1=-1.0mA(DC) (Including output mode of I/O terminal)
Output "L" voltage 1	VOL1	0.0	-	0.4	V		IOL1=1.0mA(DC) (Including output mode of I/O terminal)

●Block Diagram



●Recommended Application Circuit



∗ Data is prepared separately about each register setup. Please refer to the Development Scheme on page 14.

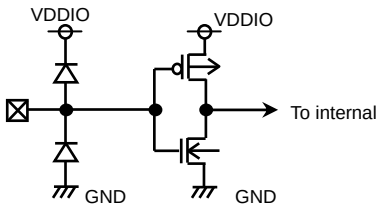
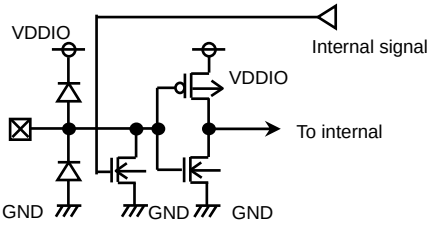
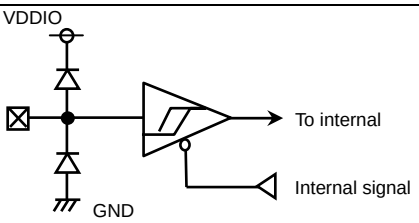
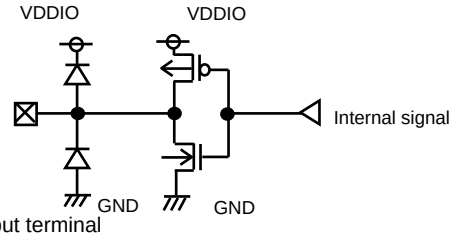
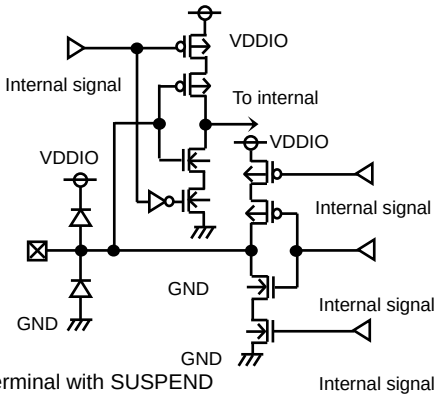
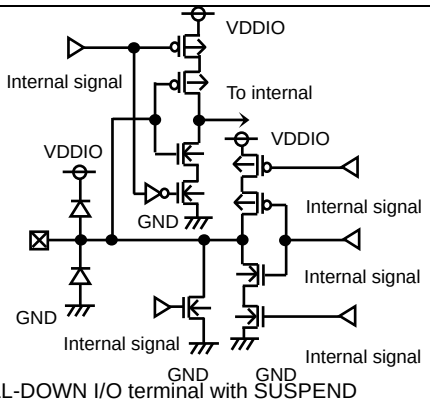
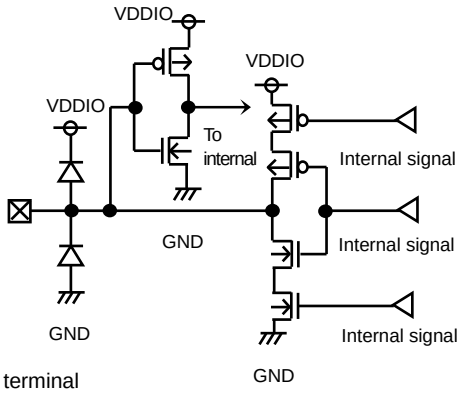
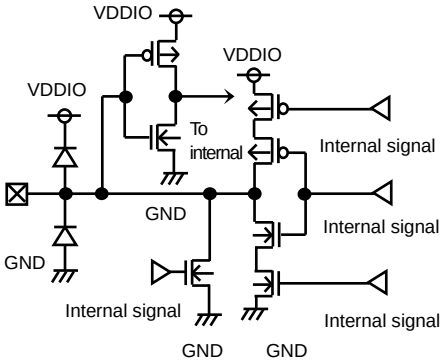
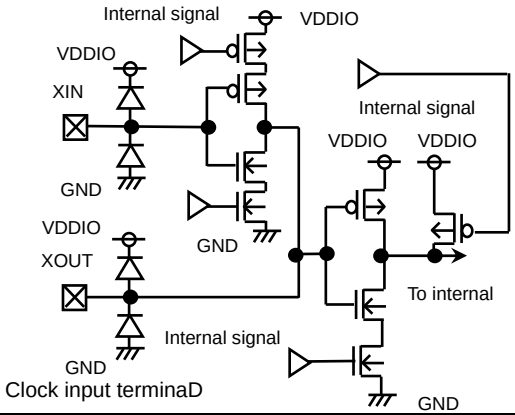
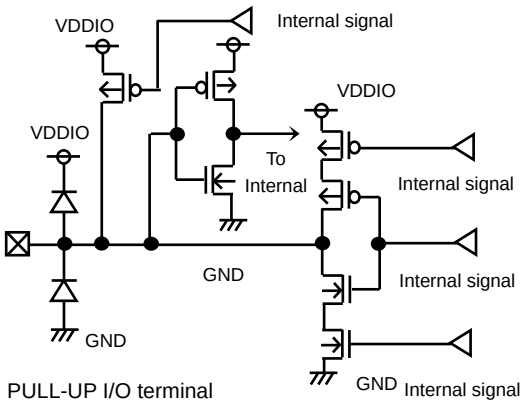
●Terminal functions

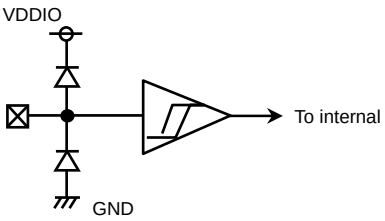
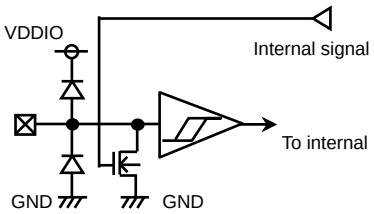
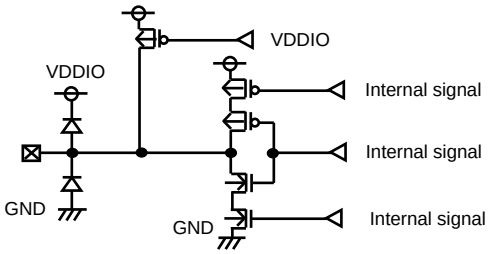
PIN No.	Land No.	PIN Name	In /Out	Active Level	Init	Function explanation	Function division	I/O type BU6566GVW	I/O type BU6568GV
1	A1	N.C.	-	-	-	-	-	-	-
2	B2	VDDIO1	-	PWR	-	Digital I/O power source (system 1)	-	-	-
3	B1	D15/HOST_MODE	In/Out	DATA	IN *1	Switch parallel / Serial of HOST I/F (BU6566GVW	HOST IF	F*3	-
		D15/EXGIO7	In/Out	DATA	IN *1	Host data bus bit 15		-	H
4	C2	D14/EXGIO6	In/Out	DATA	IN *1	Host data bus bit 14	HOST IF	F	H
5	C1	N.C.	-	-	-	-	-	-	-
6	D3	D13/EXGIO5	In/Out	DATA	IN *1	Host data bus bit 13	HOST IF	F	H
7	D2	D12/EXGIO4	In/Out	DATA	IN *1	Host data bus bit 12	HOST IF	F	H
8	D1	D11/EXGIO3	In/Out	DATA	IN *1	Host data bus bit 11	HOST IF	F	H
9	E1	D10/EXGIO2	In/Out	DATA	IN *1	Host data bus bit 10	HOST IF	F	H
10	E2	D9/EXGIO1	In/Out	DATA	IN *1	Host data bus bit 9	HOST IF	F	H
11	E3	D8/EXGIO0	In/Out	DATA	IN *1	Host data bus bit 8	HOST IF	F	H
12	E4	GND	-	GND	-	Common ground	-	-	-
13	F5	VDD	-	PWR	-	Digital core power source	-	-	-
14	F4	D7	In/Out	DATA	IN *1	Host data bus bit 7	HOST IF	E	G
15	F3	D6	In/Out	DATA	IN *1	Host data bus bit 6	HOST IF	E	G
16	F2	D5	In/Out	DATA	IN *1	Host data bus bit 5	HOST IF	E	G
17	F1	D4	In/Out	DATA	IN *1	Host data bus bit 4	HOST IF	E	G
18	G1	D3	In/Out	DATA	IN *1	Host data bus bit 3	HOST IF	E	G
19	G2	D2	In/Out	DATA	IN *1	Host data bus bit 2	HOST IF	E	G
20	G3	D1/SIF_RD	In/Out	DATA	IN *1	Host data bus bit 1 Serial data from BU6566GVW to HOST	HOST IF	E	-
		D1	In/Out	DATA	IN *1	Host data bus bit 1		-	G
21	H1	D0/SIF/WD	In/Out	DATA	IN *1	Host data bus bit 0 Serial data from HOST to BU6566GVW	HOST IF	E	-
		D0	In/Out	DATA	IN *1	Host data bus bit 0		-	G
22	H2	N.C.	-	-	-	-	-	-	-
23	J1	A2	In	DATA	- *2	Host data bus bit 2	HOST IF	A	A
24	G4	GND	-	GND	-	Common ground			
25	H3	N.C.	-	-	-	-	-	-	-
26	K1	N.C.	-	-	-	-	-	-	-
27	J2	VDDIO1	-	PWR	-	Digital I/O power source (system 1)	-	-	-
28	K2	A1/SIF_CD	In	DATA	-	Host address bus bit 1 signal Command / data identification in HOST serial I/F(BU6566GVW	HOST IF	A	-
		A1	In	DATA	-	Host address bus bit 1		-	A
29	J3	CSB/SIF_CS1	In	Low		Chip select signal Chip select signal in HOST serial I/F(BU6566GVW only)	HOST IF	A	-
		CSB	In	Low		Chip select signal		-	K
30	K3	WRB/SIF_SCK	In	Low		Write enable signal Serial clock in HOST serial I/F(BU6566GVW only)	HOST IF	C	-
		WRB	In	Low		Write enable signal		-	K
31	H4	RDB	In	Low	-*2	Read enable signal	HOST IF	C	K
32	J4	N.C.	-	-	-	-	-	-	-
33	K4	INT	Out	*	Low	Interruption signal	HOST IF	D	D
34	K5	CAMVS	In	*	-	Camera vertical timing signal (pull down at CAMOFF)	CAMERA	B	B
35	J5	CAMHS	In	*	-	Camera horizontal timing signal (pull down at CAMOFF)	CAMERA	B	B
36	H5	CAMD0	In	DATA	-	Camera data input bit0 (pull down at CAMOFF)	CAMERA	B	B
37	G5	CAMD1	In	DATA	-	Camera data input bit1 (pull down at CAMOFF)	CAMERA	B	B
38	F6	CAMD2	In	DATA	-	Camera data input bit2 (pull down at CAMOFF)	CAMERA	B	B
39	G6	CAMD3	In	DATA	-	Camera data input bit3 (pull down at CAMOFF)	CAMERA	B	B
40	H6	GIO2 / KEY2	In/Out	DATA	Out/Low	General purpose I/O2 / Key input2 (pull down for register control)	SYSTEM	H	H
41	J6	CAMD4	In	DATA	-	Camera data input bit4 (pull down at CAMOFF)	CAMERA	B	B
42	K6	CAMD5	In	DATA	-	Camera data input bit5 (pull down at CAMOFF)	CAMERA	B	B
43	K7	CAMD6	In	DATA	-	Camera data input bit6 (pull down at CAMOFF)	CAMERA	B	B
44	J7	CAMD7	In	DATA	-	Camera data input bit7 (pull down at CAMOFF)	CAMERA	B	B
45	H7	VDDIO2	-	PWR	-	Digital I/O power source (system 2)	-	-	-
46	K8	CAMCKI	In	CLK	-	Camera clock input (pull down at CAMOFF)	CAMERA	B	B
47	J8	N.C.	-	-	-	-	-	-	-
48	K9	CAMCKO	Out	CLK	Low	Camera clock output	CAMERA	D	D

PIN No.	Land No.	PIN Name	In /Out	Active Level	Init	Function explanation	Function division	I/O type BU6566GV	I/O BU6568G
49	G7	GND	-	GND	-	Common ground	-	-	-
50		N.C.	-	-	-	-	-	-	-
51	K10	N.C.	-	-	-	-	-	-	-
52	J9	VDD	-	PWR	-	Digital core power source	-	-	-
53	J10	SDA	In/Out	DATA	Out/Lo	Serial control input / output	CAMERA	J	J
54	H9	SDC	In/Out	CLK	Out/Lo	Serial clock output	CAMERA	J	J
55	H10	LEDCNT/GIO1	In/Out	*	In *5	LED PWM control signal / General purpose input1	SYSTEM	H	H
56	G8	PWM1/GIO3	In/Out	-	In *5	LED PWM control signal1/ General purpose input3	SYSTEM	H	H
57	G9	PWM2/GIO4	In/Out	-	In *5	LED PWM control signal2/ General purpose input4	SYSTEM	H	H
58	G10	PWM3/GIO5	In/Out	-	In *5	LED PWM control signal3/ General purpose input5	SYSTEM	H	H
59	F10	VD/GIO6	In/Out	*	In *5	LCD controller vertical synchronization signal/ general purpose	LCD IF	H	H
60	F9	LCDCS1B	Out	Low	-	LCD controller chip select 1	LCD IF	D	D
61	F8	LCDCS2B	Out	Low	High	LCD controller chip select 2	LCD IF	D	D
62	F7	KEY0	In	*	-	KEY input	SYSTEM	H*6	H*6
63	E6	LCDWRB	Out	Low	-	LCD controller write enable signal	LCD IF	G*4	G*4
64	E7	LCDRDB	Out	Low	-	LCD controller read enable signal	LCD IF	G*4	G*4
65	E8	LCDA0	Out	*	-	LCD controller command parameter identification signal	LCD IF	G*4	G*4
66	E9	VDDIO2	-	PWR	-	Digital IO power source (system 2)	-	-	-
67	E10	LCDD0	In/Out	DATA	Out/Lo	LCD controller data bus bit 0	LCD IF	H	H
68	D10	LCDD1	In/Out	DATA	Out/Lo	LCD controller data bus bit 1	LCD IF	H	H
69	D9	LCDD2	In/Out	DATA	Out/Lo	LCD controller data bus bit 2	LCD IF	H	H
70	D8	N.C.	-	-	-	-	-	-	-
71	C10	LCDD3	In/Out	DATA	Out/Lo	LCD controller data bus bit 3	LCD IF	H	H
72	C9	LCDD4	In/Out	DATA	Out/Lo	LCD controller data bus bit 4	LCD IF	H	H
73	B10	N.C.	-	-	-	-	-	-	-
74	D7	GND	-	GND	-	Common ground	-	-	-
75	C8	N.C.	-	-	-	-	-	-	-
76	A10	N.C.	-	-	-	-	-	-	-
77	B9	VDD	-	PWR	-	Digital core power source	-	-	-
78	A9	LCDD5	In/Out	DATA	Out/Lo	LCD controller data bus bit 5	LCD IF	H	H
79	B8	LCDD6	In/Out	DATA	Out/Lo	LCD controller data bus bit 6	LCD IF	H	H
		/ SCL	In/Out	DATA	Out/Lo	LCD clock of serial transmission (BU6566GVW		H	H
80	A8	LCDD7	In/Out	DATA	Out/Lo	LCD controller data bus bit 7	LCD IF	H	H
		/ SI	In/Out	DATA	Out/Lo	LCD data of serial transmission (BU6566GVW only)		H	H
81	C7	TEST	In	Low	-	Test mode terminal (Connect with GND)	SYSTEM	B	B
82	B7	X16_8	In	-	-	Host data bus 16-bit / 8-bit selection	SYSTEM	A	A
83	A7	LCDD8	In/Out	DATA	Out/Lo	LCD controller data bus bit 8	LCD IF	H	H
84	A6	LCDD9	In/Out	DATA	Out/Lo	LCD controller data bus bit 9	LCD IF	H	H
85	B6	LCDD10	In/Out	DATA	Out/Lo	LCD controller data bus bit 10	LCD IF	H	H
86	C6	LCDD11	In/Out	DATA	Out/Lo	LCD controller data bus bit 11	LCD IF	H	H
87	D6	LCDD12	In/Out	DATA	Out/Lo	LCD controller data bus bit 12	LCD IF	H	H
88	E5	N.C.	-	-	-	-	-	-	-
89	D5	KEY1	In	-	-	Key input	SYSTEM	H*6	H*6
90	C5	LCDD13	In/Out	DATA	Out/Lo	LCD controller data bus bit 13	LCD IF	H	H
91	B5	LCDD14	In/Out	DATA	Out/Lo	LCD controller data bus bit 14	LCD IF	H	H
92	A5	LCDD15	In/Out	DATA	Out/Lo	LCD controller data bus bit 15	LCD IF	H	H
93	A4	RESETB	In	Low	-	System reset signal	SYSTEM	C	K
94	B4	PWM0/GIO0	In/Out	DATA	In *5	LED PWM control signal0/ General purpose input /	SYSTEM	H	H
95	C4	VDDIO1	-	PWR	-	Digital IO power source (system 1)	-	-	-
96	A3	N.C.	-	-	-	-	-	-	-
97	B3	XOUT	Out	CLK	High	Clock output (always HIGH output at setting of external input)	SYSTEM	I	I
98	A2	XIN	In	CLK	-	Clock input *7	SYSTEM	C,I	K,I
99	D4	GND	-	GND	-	Common ground	-	-	-
100	C3	N.C.	-	-	-	-	-	-	-

＊"＊" in Active Level column means active level can be changed by setting of register. Moreover, Init is a pin state at the time of reset release.
*1: Under the condition of RESETB="L" or CSB= "H".
*2: Please connect A2 and RDB to GND when to use Host serial I/F.
*3: Pull down only except for a test mode.
*4: Input only except for a test mode.
*5: Pull down while RESETB='L'(initial state).
*6: Output only except for a test mode.
*7: The crystal oscillation circuit does not include a return resistance, so it is needed to examine an external circuit including return resistance.

●Equivalent Circuit Structures of input / output pins.

Type	Equivalent circuit structure	Type	Equivalent circuit structure
A	 Input terminal	**B**	 PULL-DOWN Input terminal
C	 Hysteresis input terminal with SUSPEND	**D**	 Output terminal
E	 I/O terminal with SUSPEND	**F**	 PULL-DOWN I/O terminal with SUSPEND
G	 I/O terminal	**H**	 PULL-DOWN I/O terminal
I	 Clock input terminaD	**J**	 PULL-UP I/O terminal

Type	Equivalent circuit structure	Type	Equivalent circuit structure
K	 Hysterisisinput terminal (only for BU6568GV)	**L**	 PULL-DOWN Hysterisisinput terminal (only for BU6568GV)
M	 Pull-up 3-state output terminal (only for BU6568GV)		

●Terminal Layout

	1	2	3	4	5	6	7	8	9	10
K	26 NC	28 A1	30 WRB	33 INT	34 CAMVS	42 CAMD5	43 CAMD6	46 CAMCKI	48 CAMCKO	51 NC
J	23 A2	27 VDDIO1	29 CSB	32 NC	35 CAMHS	41 CAMD4	44 CAMD7	47 NC	52 VDD	53 SDA
H	21 D0	22 NC	25 NC	31 RDB	36 CAMD0	40 GIO2	45 VDDIO2	50 NC	54 SDC	55 LEDCNT
G	18 D3	19 D2	20 D1	24 GND	37 CAMD1	39 CAMD3	49 GND	56 PWM1	57 PWM2	58 PWM3
F	17 D4	16 D5	15 D6	14 D7	13 VDD	38 CAMD2	62 KEY0	61 LCDCS2B	60 LCDCS1B	59 VD
E	9 D10	10 D9	11 D8	12 GND	88 NC	63 LCDWRB	64 LCDRDB	65 LCDA0	66 VDDIO2	67 LCDD0
D	8 D11	7 D12	6 D13	99 GND	89 KEY1	87 LCDD12	74 GND	70 NC	69 LCDD2	68 LCDD1
C		4 D14	100 NC	95 VDDIO1	90 LCDD13	86 LCDD11	81 TEST	75 NC	72 LCDD4	71 LCDD3
B	3 D15	2 VDDIO1	97 XOUT	94 PWM0	91 LCDD14	85 LCDD10	82 X16_8	79 LCDD6	77 VDD	73 NC
A	1 NC	98 XIN	96 NC	93 RESETB	92 LCDD15	84 LCDD9	83 LCDD8	80 LCDD7	78 LCDD5	76 NC

1pin marker (Top View) corner.

（Bottom View）

●Timing Chart

1. HOST interface timing

1.1 System timing

Table 1.1-1 BU6566GVW timing conditions (system)

Symbol	Details	MIN.	TYP.	MAX.	Unit	Conditions
tXIN	Clock input cycle	33.0	-	-	ns	
DutyXIN	Clock duty	45.0	50.0	55.0	%	"H" width / cycle
tSCLK	System clock cycle	33.0	-	-	ns	
DutySCLK	System clock duty	33.3	50.0	66.7	%	"H" width / cycle
tCAMCKO	Camera clock output cycle	33.0	-	-	ns	
DutyCAMCKO	Camera clock output duty	33.3	50.0	66.7	%	""H" width / cycle
tCAMCKI	Camera clock input cycle	66.0	-	-	ns	
DutyCAMCKI	Camera clock input duty	40.0	50.0	60.0	%	"H" width / cycle
tRESETB	RESETB "L" pulse width	1.0	-	-	us	

∗ Regulation all at threshold of VDDIO×1/2

Table 1.1-2 BU6568GV timing conditions (system)

Symbol	Details	MIN.	TYP.	MAX.	Unit	Conditions
tXIN	Clock input cycle	33.0	-	-	ns	
DutyXIN	Clock duty	45.0	50.0	55.0	%	"H" width / cycle
tSCLK	System clock cycle	19.2	-	-	ns	
DutySCLK	System clock duty	33.3	50.0	66.7	%	"H" width / cycle
tCAMCKO	Camera clock output cycle	19.2	-	-	ns	
DutyCAMCKO	Camera clock output duty	45.0	50.0	55.0	%	"H" width / cycle
tCAMCKI	Camera clock input cycle	19.2	-	-	ns	
DutyCAMCKI	Camera clock input duty	45.0	50.0	55.0	%	"H" width / cycle
tRESETB	RESETB "L" pulse width	1.0	-	-	us	

∗ Regulation all at threshold of VDDIO×1/2

1.2 Register (including RAM via register) write timing.

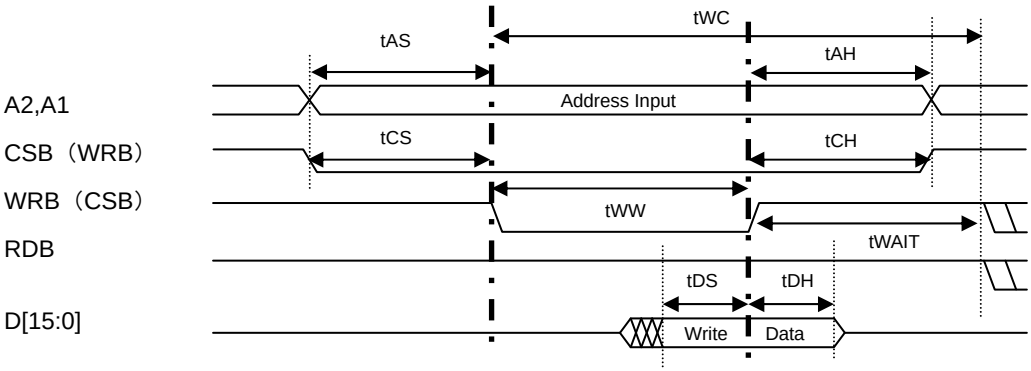


Table 1.2-1 BU6566GVW timing conditions（RAM, register write cycle）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tWC	Write cycle time	70	-	-	ns
tAS	Address setup time before WRB(CSB) falling	-5	-	-	ns
tAH	Address hold time after WRB(CSB) rising	-1	-	-	ns
tCS	CSB(WRB) input setup time before WRB(CSB) falling	0	-	-	ns
tCH	CSB(WRB) input hold time after WRB(CSB) rising	0	-	-	ns
tWW	WRB(CSB) active time width	40	-	-	ns
tWAIT	Wait time from WRB(CSB) rising to the next WRB(CSB) or to RDB falling	30	-	-	ns
tDS	Data setup time before WRB(CSB) rising	35	-	-	ns
tDH	Data hold time after WRB(CSB) rising	-1	-	-	ns

∗ Regulation all at threshold of VDDIO1×1/2 (VDD=1.50V,VDDIO=2.85V,GND=0.0V,Ta=25ºC)

∗ It is possible to use it with either CSB or WRB active. However, either of them must do LOW pulse operation.

Table 1.2-2 BU6568GV timing conditions（RAM, register write cycle）

Symbol	Details	MIN.	TYP.	MAX	Unit
tWC	Write cycle time	55	-	-	ns
tAS	Address setup time before WRB(CSB) falling	-4	-	-	ns
tAH	Address hold time after WRB(CSB) rising	0	-	-	ns
tCS	CSB(WRB) input setup time before WRB(CSB) falling	0	-	-	ns
tCH	CSB(WRB) input hold time after WRB(CSB) rising	0	-	-	ns
tWW	WRB(CSB) active time width	40	-	-	ns
tWAIT	Wait time from WRB(CSB) rising to the next WRB(CSB) or to RDB falling	15	-	-	ns
tDS	Data setup time before WRB(CSB) rising	30	-	-	ns
tDH	Data hold time after WRB(CSB) rising	0	-	-	ns

∗ Regulation all at threshold of VDDIO1×1/2 (VDD=1.50V,VDDIO=2.85V,GND=0.0V,Ta=25ºC)
∗ It is possible to use it with either CSB or WRB active. However, either of them must do LOW pulse operation.

1.3 Register (including RAM via register) read timing.

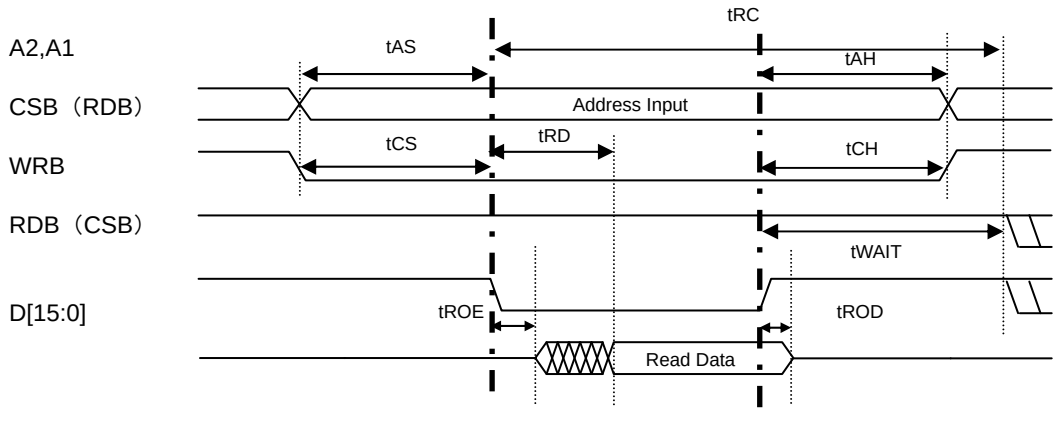


Table 1.3-1 BU6566GVW timing conditions (RAM, register read cycle)

Symbol	Details	MIN.	TYP.	MAX.	Unit
tRC	Read cycle time	100	-	-	ns
tAS	Address setup time before RDB(CSB) falling	-5	-	-	ns
tAH	Address hold time after RDB(CSB) rising	-1	-	-	ns
tCS	CSB(RDB) input setup time before RDB(CSB) falling	0	-	-	ns
tCH	CSB(RDB) input hold time after RDB(CSB) rising	0	-	-	ns
tRD	Access time after RDB(CSB) falling	-	-	70	ns
tWAIT	Wait time from RDB(CSB) rising to the next RDB(CSB) falling or to WRB falling	30	-	-	ns
tROE,tROD	Data output enable time after RDB(CSB) falling, Data output disable time after RDB(CSB) rising	-	-	15	ns

∗ Regulation all at threshold of VDDIO1×1/2 (VDD=1.50V,VDDIO=2.85V,GND=0.0V,Ta=25ºC)
∗ It is possible to use it with either CSB or RDB active. However, either of them must do LOW pulse operation.

Table 1.3-2 BU6568GV timing conditions (RAM, register read cycle)

Symbol	Details	MIN.	TYP.	MAX.	Unit
tRC	Read cycle time	74.5	-	-	ns
tAS	Address setup time before RDB(CSB) falling	-4	-	-	ns
tAH	Address hold time after RDB(CSB) rising	0	-	-	ns
tCS	CSB(RDB) input setup time before RDB(CSB) falling	0	-	-	ns
tCH	CSB(RDB) input hold time after RDB(CSB) rising	0	-	-	ns
tRD	Access time after RDB(CSB) falling	-	-	70	ns
tWAIT	Wait time from RDB(CSB) rising to the next RDB(CSB) falling or to WRB falling	30	-	-	ns
tROE,tROD	Data output enable time after RDB(CSB) falling, Data output disable time after RDB(CSB) rising	8	-	-	ns

∗ Regulation all at threshold of VDDIO1×1/2 (VDD=1.50V,VDDIO=2.85V,GND=0.0V,Ta=25ºC)
∗ It is possible to use it with either CSB or RDB active. However, either of them must do LOW pulse operation.

2. Camera Module Interface Timing

2.1. System clock and camera clock

External input clock (XIN) may be divided set and supplied as CAMCKO clock to camera module.
The relation of data synchronization clock CAMCKI clock from camera and system clock SCLK must be set so as to meet the following formula.

$$fSCLK \geq 2 \times fCAMCKI \quad \text{……(2.1-1)}$$

fSCLK System clock frequency
fCAMCKI Camera clock frequency input to CAMCKI terminal

Moreover, [Camera timing 1] or [Camera timing 2] shown below must be satisfied.

[Camera timing 1] (In the case when CAMCKI signal is as asynchronous as CAMCKO)

$$tCAMCKIH > tSCLK + 1ns \quad \text{and} \quad tCAMCKIL > tSCLK + 1ns \quad \text{……(2.1-2)}$$

tCAMCKIH CAMCKI High interval
tCAMCKIL CAMCKI Low interval

[Camera timing 2] (In the case when CAMCKI signal is as synchronous as CAMCKO)

$$\text{total delay} + \text{margin} (\ 10ns) < tSCLK \quad \text{……(2.1-3)}$$

total delay delay from CAMCKO change point to CAMCKI change point

The clock relation in fSCLK = fCAMCKO = 2 × fCAMCKI is shown in Figure.2.1-1.

[fSCLK=fCAMCKO=2 × fCAMCKI]

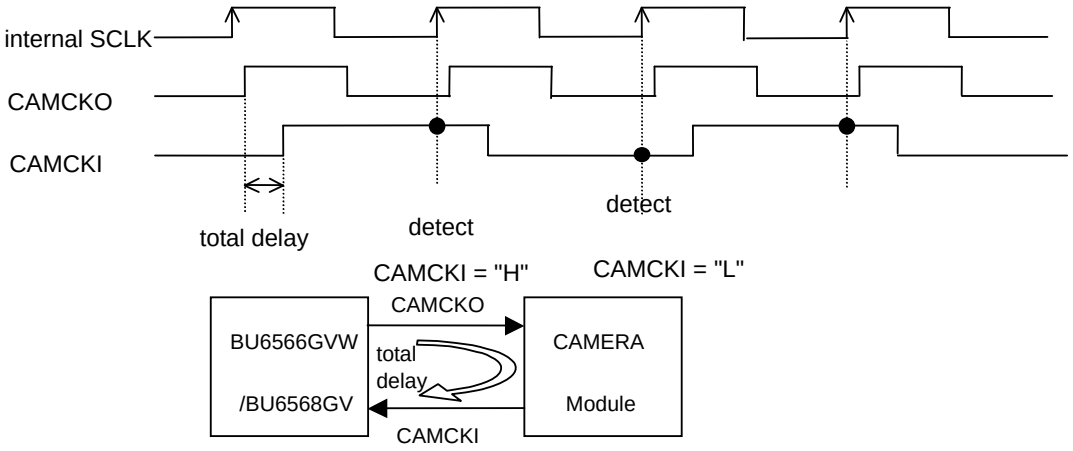


Figure .2.1-1 Relation between system clock and camera clock

2.2. Camera module interface timing

The timing of the camera image signal in camera I/F is shown in Table 2.2-1.

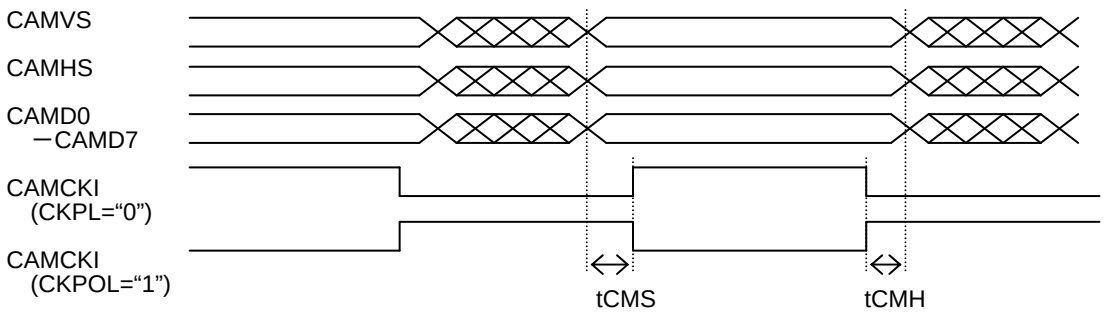


Table 2.2-1 BU6566GVW/BU6568GV timing (camera data)

Symbol	Details	MIN.	TYP.	MAX.	Unit	Remarks
tCMS	CAMCKI rising/falling camera set up time	1/5	-	-	ns	BU6566GVW/BU6568GV
tCMH	CAMCKI rising/falling camera hold time	1/5	-	-	ns	BU6566GVW/BU6568GV

3. LCD direct access

When to set up with A2="L", direct access to LCD module is set up, and HOST CPU signal penetrated to LCD signal.

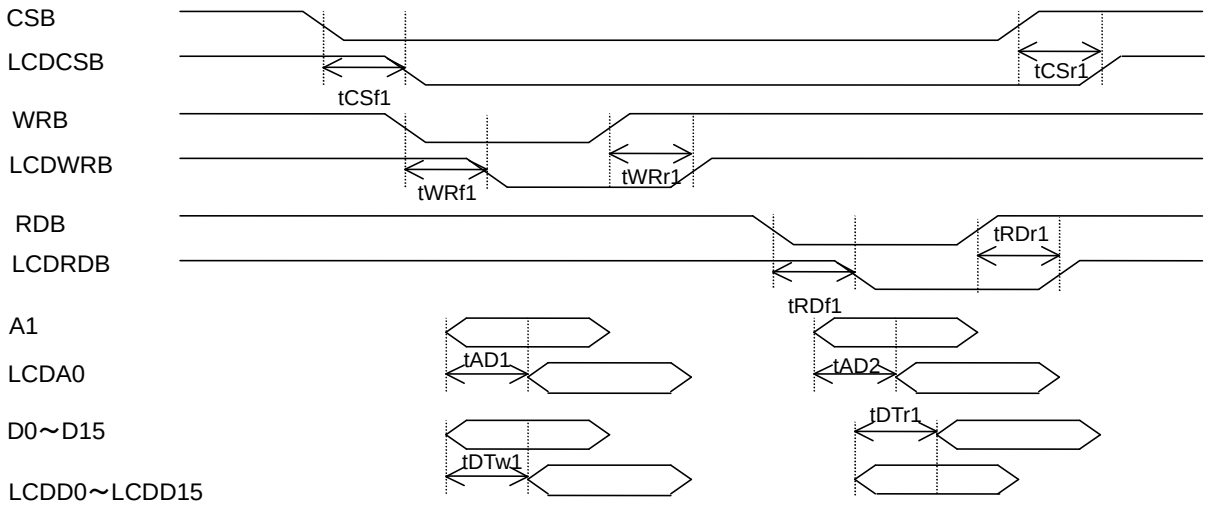


Table 3-1 BU6566GVW timing conditions（LCD direct access）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tCSf1	Delay from CSB to LCDCSB falling	3.5	-	12.0	ns
tCSr1	Delay from CSB to LCDCSB rising	2.1	-	9.3	ns
tWRf1	Delay from WRB to LCDWRB falling	3.0	-	11.2	ns
tWRr1	Delay from WRB to LCDWRB rising	2.0	-	9.2	ns
tRDf1	Delay from RDB to LCDRDB falling	3.0	-	11.8	ns
tRDr1	Delay from RDB to LCDRDB rising	2.0	-	9.1	ns
tAD1	Delay from A1 to LCDA0	1.8	-	9.6	ns
tDTw1	Delay from D0～D15 to LCDD0～LCDD15	7.4	-	22.3	ns
tDTr1	Delay from LCDD0～LCDD15 to D0～D15	3.0	-	13.35	ns

Table 3-2 BU6568GV timing conditions（LCD direct access）

Symbol	Details	MIN.	TYP.	MAX.	Unit
tCSf1	Delay from CSB to LCDCSB falling	3.0	-	12.0	ns
tCSr1	Delay from CSB to LCDCSB rising	2.5	-	10.0	ns
tWRf1	Delay from WRB to LCDWRB falling	3.0	-	12.0	ns
tWRr1	Delay from WRB to LCDWRB rising	2.5	-	10.0	ns
tRDf1	Delay from RDB to LCDRDB falling	3.0	-	12.0	ns
tRDr1	Delay from RDB to LCDRDB rising	2.5	-	10.0	ns
tAD1	Delay from A1 to LCDA0	2.5	-	10.0	ns
tAD2	Delay from A1 to LCDA0	6.0		24.0	ns
tDTw1	Delay from D0～D15 to LCDD0～LCDD15	4.0	-	16.0	ns
tDTr1	Delay from LCDD0～LCDD15 to D0～D15	4.0	-	16.0	ns

4. LCD transfer timing

Transfer timing to LCD is shown below.

RESO	Nwrb	Npix	Tseq	Th_rest
0	2	1	(WL+WH+2)×2	0
1	2	1	(WL+WH+2)×2	0
2	3	2	(WL+WH+max(WL,WH)+3)×2	abs(WL-WH)
3	1	1	(WL+WH+2)	0
4	2	1	(WL+WH+2)×2	0
5	3	1	(WL+WH+2)×3	0
6	3	1	(WL+WH+2)×3	0
7	2	1	(WL+WH+2)×2	0

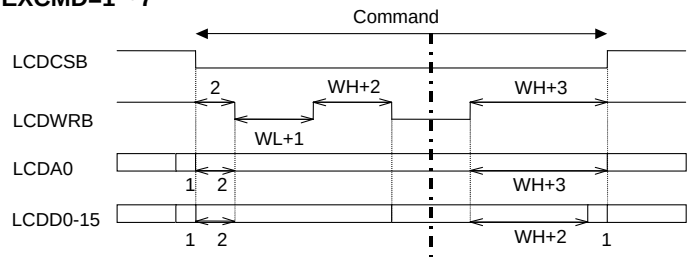
∗ RESO(IDX:42h bit [2:0]) shows a color resolution setting of LCD.
∗ Nwrb, Npix, Tseq, and Th_rest are the parameters determined by RESO.
∗ WL, WH are the value of LCDWL, LCDWH of Register MLCDWAV (IDX:49h), respectively.
∗ max (WL, WH) shows the maximum of WL and WH.
∗ abs(WL-WH) shows the absolute value of (WL-WH).

TRN_CMD=1

Waveform at command transfer (T_{SCLK} for all unit)

EXCMD=0

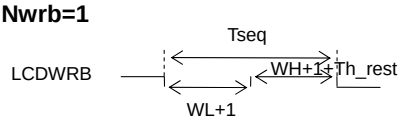
EXCMD=1～7



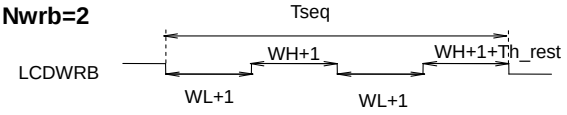
TRN_CMD=0

Waveform at data transfer (T_{SCLK} for all unit)

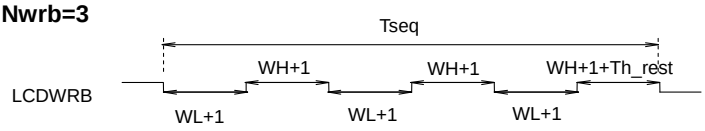
Nwrb=1



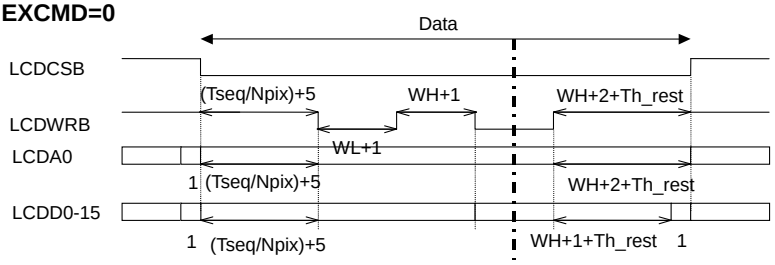
Nwrb=2



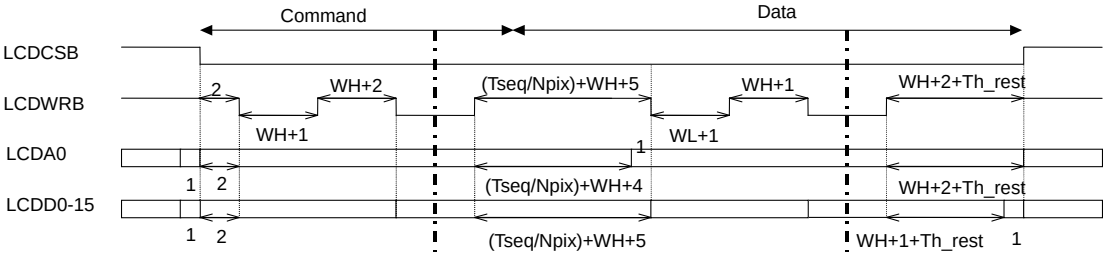
Nwrb=3



EXCMD=0



EXCMD=1-7



（Note1）In LCD_DELAY[1:0](IDX:49h bit [9:8]) ="00", LCDA0 and LCDD change in LCDWRB falling, and are held to the next LCDWRB falling.
（Note2）Change of LCDWRB is late for LCDA0 and LCDD 15-0 according to a setup of LCD_DELAY [1:0] (at the time of output no-load).
Typ. delays 10ns in LCD_DELAY[1:0] ="01." 1tSCLK in LCD_DELAY[1:0] ="10". 1tSCLK＋Typ.10ns in LCD_DELAY[1:0] ="11".

Figure 4-1 MAIN LCD data transfer waveform（Unit：tSCLK）

● Development Scheme

This technical note is aimed at trying the connectivity in the hardware between customer's system and our camera image processor series.

We prepare various data and tools for every development STEP as follows other than this technical note, please contact the sales staff in your duty also including the support system.

(1) Demonstration STEP

(You can try the standard image processing functions by the standard Demonstration kit at once.)

You can confirm the standard functions such as camera image preview, memory data display to LCD, camera image composition JPEG compression/ expansion, frame composition, divided display, and LED lighting, and so forth on the Demonstration board.

・Standard Demonstration board kit

◎Demonstration board

（LCD module provided by ROHM, Camera module provided by ROHM, Check board equipped with the camera image processor, ARM-equipped controller board）

◎Demonstration board operation manual

◎Demonstration software

If the software for the trial board is installed in your Windows PC(Windows 2000/XP/ME/98), more detailed setting is possible.

(Execution tools for the macro command, sample macro command file)

◎USB cable

(2) Confirmation STEP

(We will respond to customer's camera module, LCD module, HOST CPU.)

・Specifications

We will provide specifications for camera image processor according to customer's requirements.

・Function explanation

We will deliver you the function explanation describing detailed functions, register settings, external interfaces, timing, and so forth of camera image processor according to your requests.

・Application note

We will deliver you the detailed explanation data on application development of camera image processor according to your requests.

(3) System check STEP

(You can check the application operation as a system by the kit of system check tools and your module(camera/LCD).)

ROHM creates the system check board using your camera/LCD module.

You can check the interface with your module and the application operation on the system check board using the tools for user's only.

・System check tools kit

・System check software (For Windows PC)

◎Reference C source code summarizing ARM –compatible application program interface(API)

◎The application software (API) as a reference C source code

◎The execution tools for the macro command (BU65XX_USB) for the check by your PC.

◎The macro command file for the check by your PC.

・System check document

◎System check board manual

◎BU65XX Demo_Board Application using API

◎Board circuit diagram

*You can check the detailed functions of the application operation by your PC using the macro command file.

(4) Integrated check STEP with user's system

(You can check the application operation as a system on your system check board using the integrated check software.)

You can check the application operation on the sample LSI-equipped system check board by your camera / LCD module using the integrated check software.

・On line Support；We will answer your questions about the software development.

How to use the macro command file, API file, and APL file.

Setting flow of the camera function (camera JPEG, preview, etc.)

Interface setting of the camera module, LCD module and the camera image processor.

Header analysis method oh JPEG decode, etc.

・On site Support；We will help you clarify the questions about the software development on site together on spot.

Check of the operation of each function and the basic operation at each register setting, etc. based on the specification.

Explanation about the specific usage of the macro command file, API file and APL file and relative questions.

How to develop the overlay or special functions, etc.

●Cautions on use

(1)Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2)Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3)Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4)Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5)GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6)Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7)Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8)Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10)Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11)External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Order Model Name Selection

ROHM model name

Product number

Package type

GVW:SBGA099W070

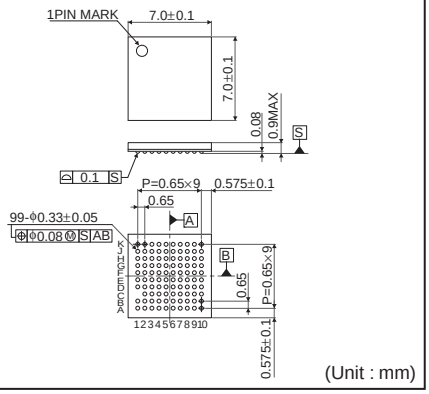
GV:SBGA099T070

Taping model name

E2: Embossed reel tape

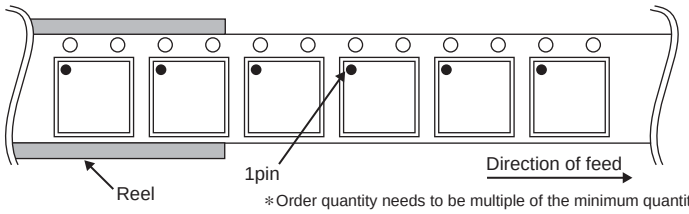
● Tape and Reel information

SBGA099W070



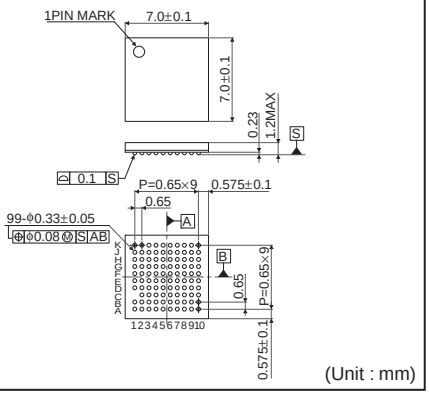
<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



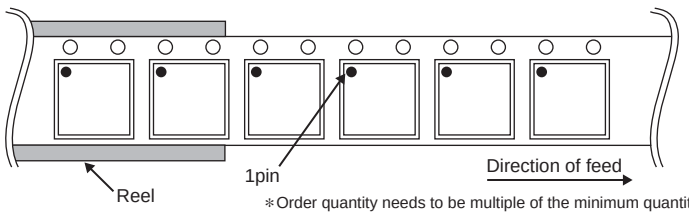
∗Order quantity needs to be multiple of the minimum quantity.

SBGA099T070



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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