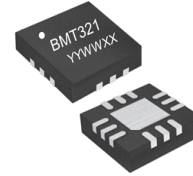


Device Features

- +5V/355mA at operating bias condition
- Gain = 27.0 dB @ 1900 MHz
- P1dB = 32.5 dBm @ 1900MHz
- LTE 20M ACLR = 22dBm Output Power at -50dBc @ 1900MHz
- Intergrated interstage matching
- Green/RoHS2-compliant QFN3x3 SMT package



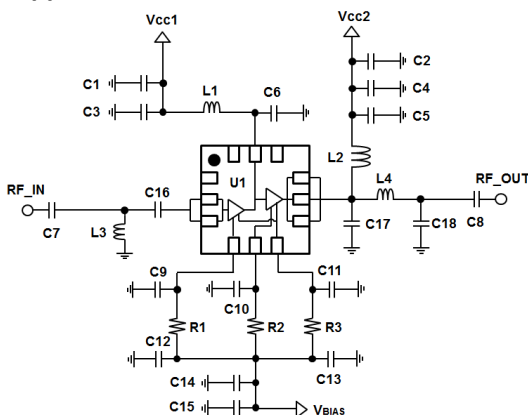
Product Description

The BMT321 is a high dynamic range two-stage power amplifier, housed in a green/RoHS2 compliant 3x3mm QFN package. The BMT321 uses a high reliability InGaP/GaAs HBT process technology. The BMT321 is designed for use where high linearity and gain are required. The BMT321 is able to deliver over 22 dBm output power from 700 to 2800MHz while maintaining superior ACLR performance with a few external matching components. All devices are 100% RF/DC screened.

Applications

- Base station /Repeaters Infrastructure/Small Cell
- Commercial/Industrial/Military wireless system
- LTE / WCDMA /CDMA Wireless Infrastructure
- MMD & wireless LAN

Application Circuits



*External matching circuit: refer to the page 5 to 17.

Electrical Specifications

Device performance _ measured on a BeRex evaluation board at 25°C, Vc=5V, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Unit
Operational Frequency Range		700		2800	MHz
Test Frequency			1900		MHz
Gain		25.5	27.0		dB
Input Return Loss			-18.0		dB
Output Return Loss			-10.0		dB
Output IP3 ¹	17 dBm/tone, Δf=1 MHz	47.0	50.0		dBm
Output P1dB		31.5	32.5		dBm
LTE 20M ACLR*		21.0	22.0		dBm
WCDMA ACLR*		22.2	23.2		dBm
Noise Figure			5.0		dB

¹OIP3_tuned for max OIP3

*ACLR Channel Power measured at -50dBc.

- LTE set-up: 3GPP LTE, FDD E-TM3.1, 20MHz BW, ±5MHz offset, PAR 9.75 @0.01% Prob.

- WCDMA set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz offset, PAR 9.78 at 0.01% Prob.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Bandwidth	700		2800	MHz
I _{bias} @ (I _{REF1&2} + I _{B1&2})	21	26	31	mA
I _{cq} @ (I _{cq1} + I _{cq2})	290	355	420	mA
V _{CC} /V _{bias}	4.75	5.0	5.25	V
R _{TH}		12.9		°C/W
Operating Case Temperature	-40		+85	°C

Electrical specifications are measured at specified test conditions.

Specifications are not guaranteed over all recommended operating conditions.

Absolute Maximum Ratings

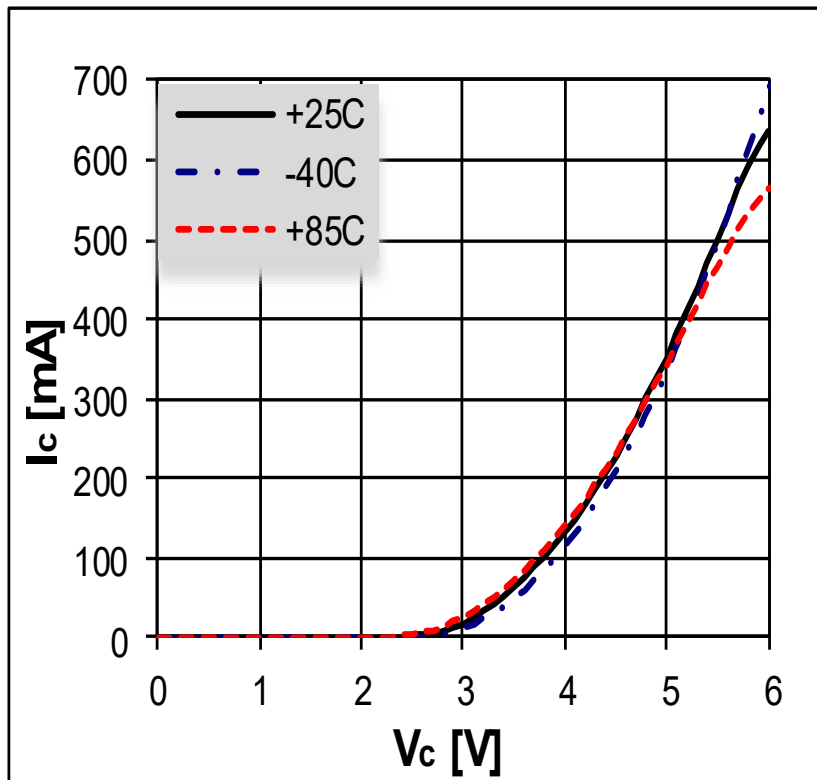
Parameter	Rating	Unit
Storage Temperature	-55 to +155	°C
Junction Temperature	+175	°C
Supply Voltage	+6.0	V
Supply Current	1.5	A
Input RF Power	26	dBm

*Operation of this device above any of these parameters may result in permanent damage.

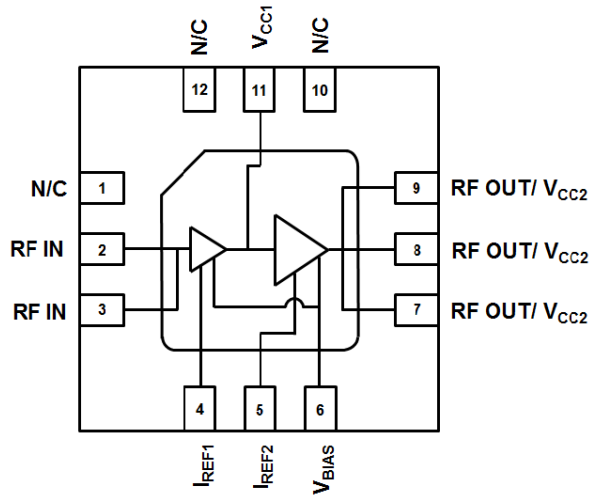
Typical Performance (V_{cc} & $V_{Bias} = +5V$, $I_{cq}=355mA$, $T_a=25^\circ C$)

Parameter	Frequency					Unit
	900	1800	1900	2140	2650	MHz
Gain	29.8	27.4	27.0	25.3	22.3	dB
S11	-20.0	-18.0	-18.0	-20.0	-20.0	dB
S22	-6.0	-8.0	-10.0	-12.0	-6.5	dB
OIP3	50.0	50.0	50.0	50.0	50.0	dBm
P1dB	30.2	32.4	32.5	32.4	31.4	dBm
LTE 20M ACLR	20.0	22.3	22.0	22.0	22.2	dBm
LTE 10M ACLR	21.0	23.5	23.1	22.8	22.9	dBm
WCDMA ACLR	21.1	23.5	23.2	23.1	23.0	dBm
Noise Figure	11.5	5.3	5.0	5.2	5.0	dB

V-I Characteristics



Pin Configuration



Pin No.	Label
1,10,12	N/C
2,3	RF IN
4	I _{REF1}
5	I _{REF2}
6	V _{Bias}
7,8,9	RF OUT/V _{CC2}
11	V _{CC1}
Backside Paddle	GND

BeRex Evaluation Board

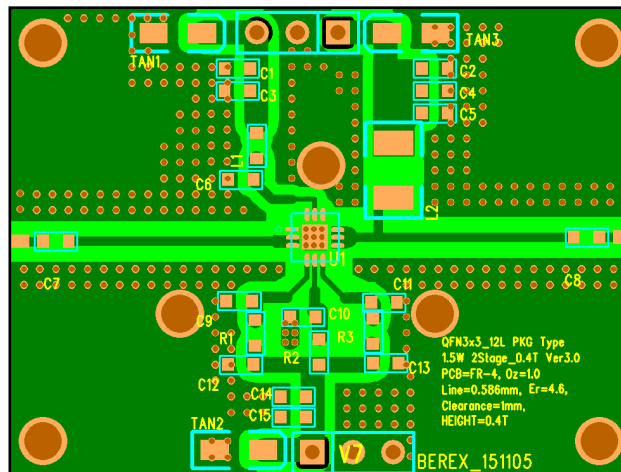
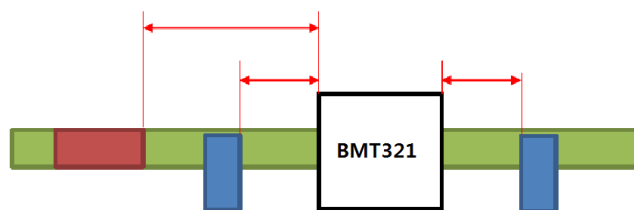
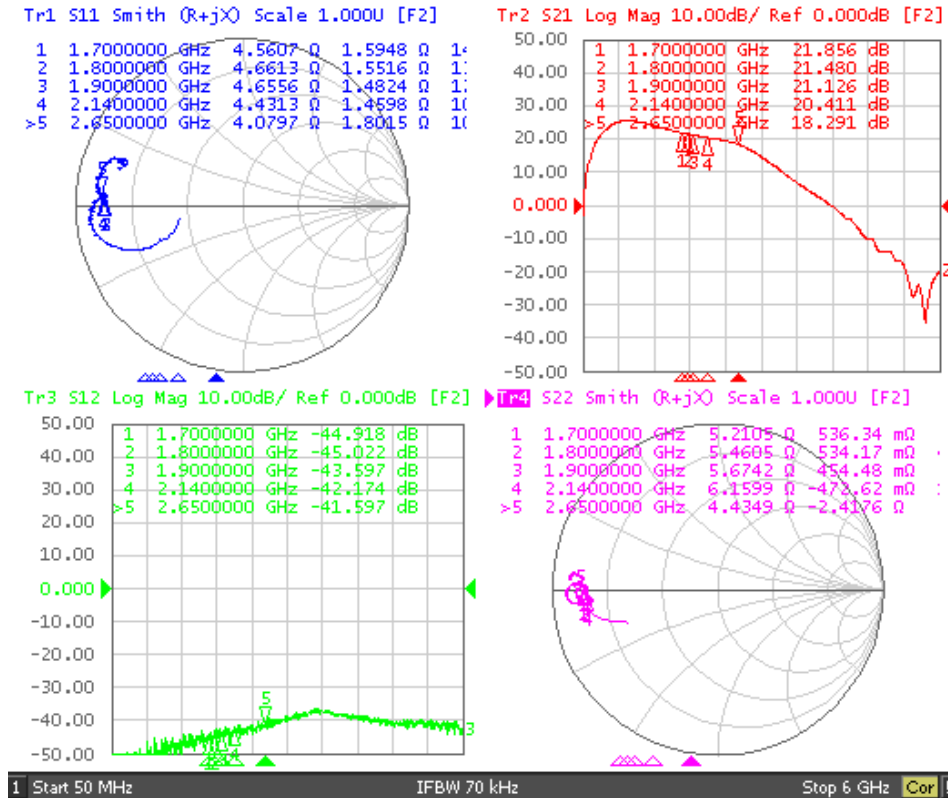


Figure about the reference position of components



Typical Device Data

S-parameters (V_{cc} & V_{Bias} = +5V, I_{cq} =355mA, T_a =25°C)



S-Parameter

(V_{cc} & V_{Bias} = +5V, I_{cq} = 355mA, T_a = 25 °C, calibrated to device leads)

Freq [MHz]	S11		S21		S12		S22	
	[Mag]	[Ang]	[Mag]	[Ang]	[Mag]	[Ang]	[Mag]	[Ang]
1700	0.83	176.59	12.33	-174.19	0.0062	85.84	0.81	178.90
1800	0.83	176.42	11.86	175.32	0.0059	83.54	0.80	178.72
1900	0.83	176.37	11.39	164.65	0.0063	90.40	0.80	179.14
2000	0.84	176.10	11.01	153.58	0.0058	89.55	0.79	179.63
2100	0.83	176.04	10.59	142.51	0.0062	85.21	0.79	-179.59
2200	0.84	176.37	10.26	131.64	0.0065	76.33	0.79	-178.42
2300	0.83	176.32	9.91	119.62	0.0073	83.92	0.79	-177.55
2400	0.84	175.60	9.53	106.79	0.0060	86.10	0.80	-176.54
2500	0.85	176.32	9.05	93.61	0.0082	82.26	0.81	-175.34
2600	0.85	176.01	8.56	80.02	0.0080	81.87	0.83	-174.71
2700	0.85	175.47	7.85	65.85	0.0079	77.26	0.85	-174.46

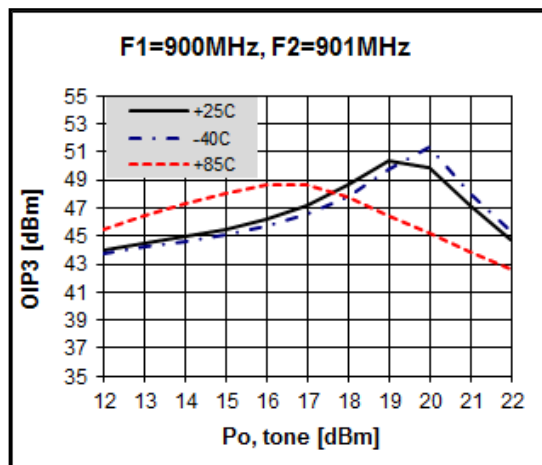
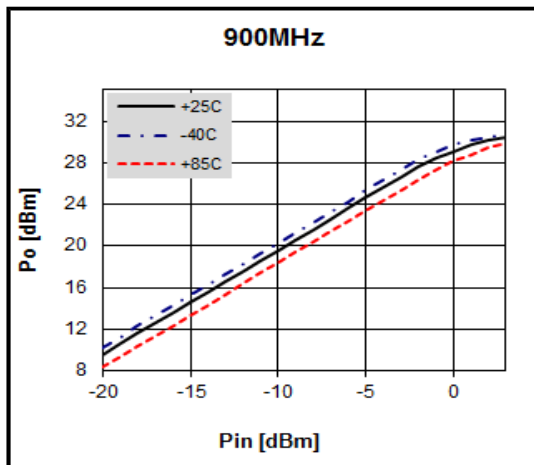
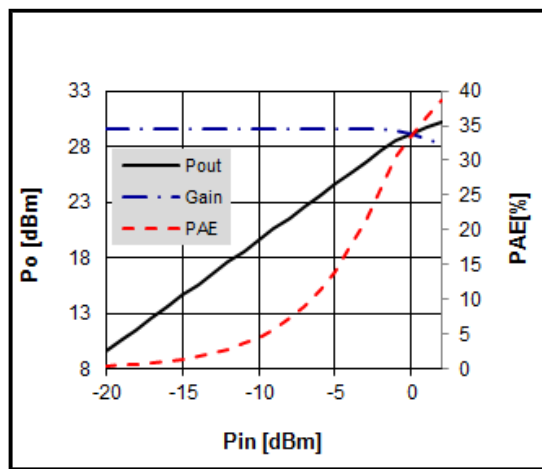
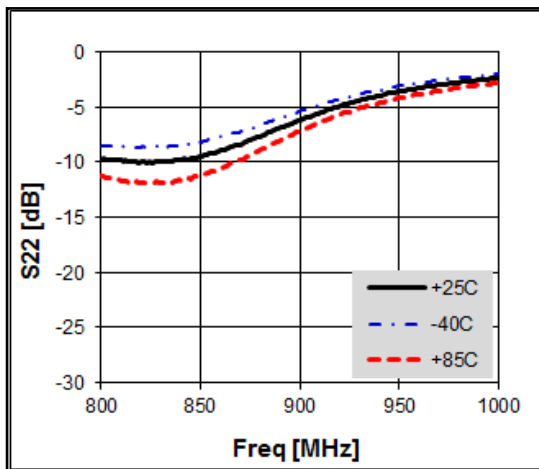
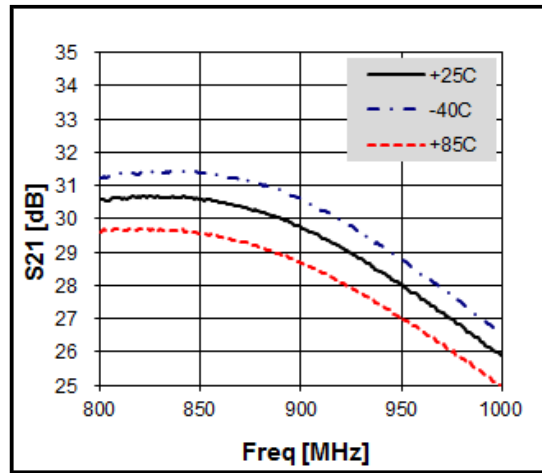
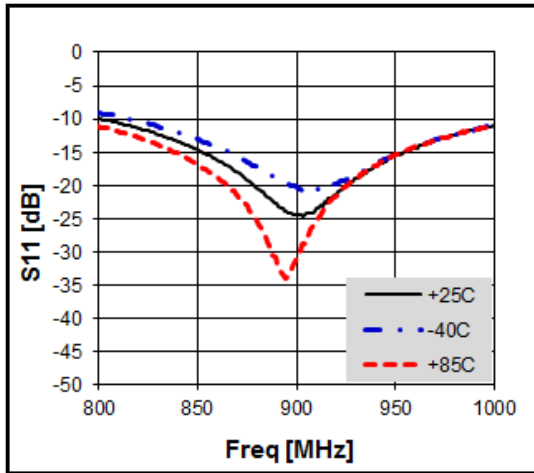
Application Circuit: 900 MHz

Schematic Diagram	BOM	Marks		
	C1	0603	1uF	Samsung
	C2	0603	1uF	Samsung
	C3	0603	100pF	Samsung
	C4	0603	100pF	Samsung
	C5	0603	N/A	-
	C6	0603	N/A	-
	C7	0603	100pF	Samsung
	C8	0603	100pF	Samsung
	C9	0603	N/A	-
	C10	0603	N/A	-
	C11	0603	N/A	-
	C12	0603	N/A	-
	C13	0603	N/A	-
	C14	0603	1uF	Samsung
	C15	0603	100pF	Samsung
	C16	0603	6.8 Ω	Samsung
	C17	0603	3.9pF	Samsung
	C18	0603	8pF	Samsung
L1	0603	39nH	Taiyo Yuden	
L2	1008	22nH	Coilcraft-HQ	
L3	0603	7pF	Samsung	
L4	0603	2.7nH	Taiyo Yuden	
R1	0603	300 Ω	Samsung	
R2	0603	430 Ω	Samsung	
R3	0603	82 Ω	Samsung	

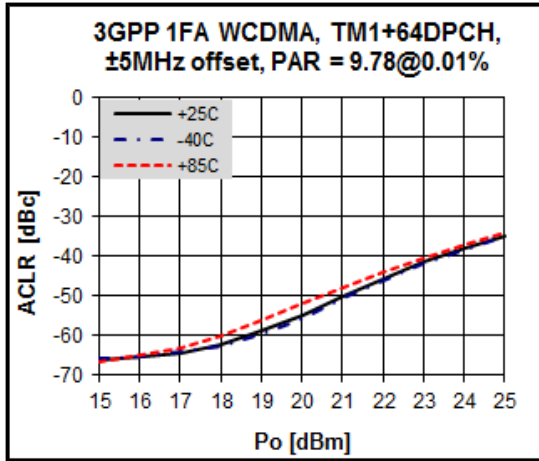
PCB Diagram	Notice																		
	Below information is subject to change as conditions of the substrate.																		
	<table border="1"> <thead> <tr> <th>Reference</th> <th>Object</th> <th>Distance</th> </tr> </thead> <tbody> <tr> <td>Input pin</td> <td>L3</td> <td>5.7mm</td> </tr> <tr> <td>Input pin</td> <td>C16</td> <td>3.5mm</td> </tr> <tr> <td>Output pin</td> <td>C17</td> <td>2.3mm</td> </tr> <tr> <td>Output pin</td> <td>L4</td> <td>3.6mm</td> </tr> <tr> <td>Output pin</td> <td>C18</td> <td>5.8mm</td> </tr> </tbody> </table>	Reference	Object	Distance	Input pin	L3	5.7mm	Input pin	C16	3.5mm	Output pin	C17	2.3mm	Output pin	L4	3.6mm	Output pin	C18	5.8mm
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	Input pin	C16	3.5mm																
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Output pin	L4	3.6mm																	
Output pin	C18	5.8mm																	

Typical Performance

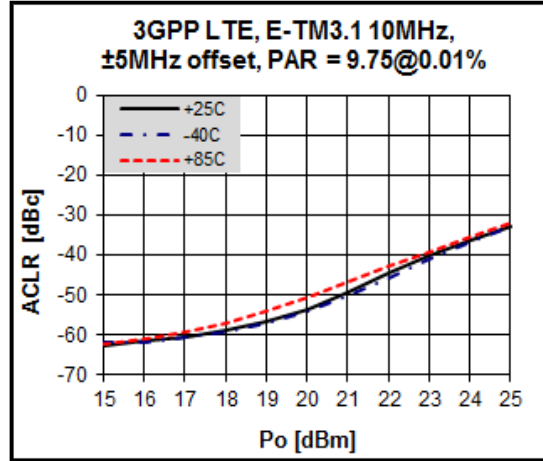
V_{CC} & $V_{Bias} = +5V$, $I_{CQ} = 355mA$, $T_a = 25^\circ C$



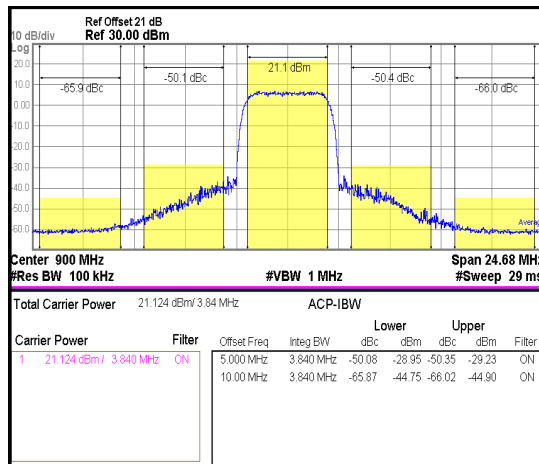
700-2800 MHz 1.5W High Linearity 5V 2-Stage Power Amplifier



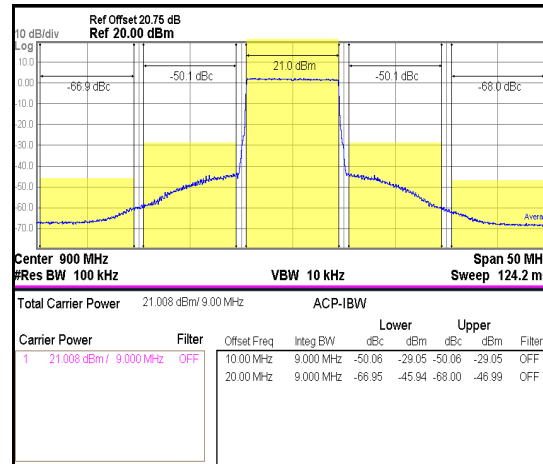
3GPP WCDMA TM1 +64DPCH 1FA



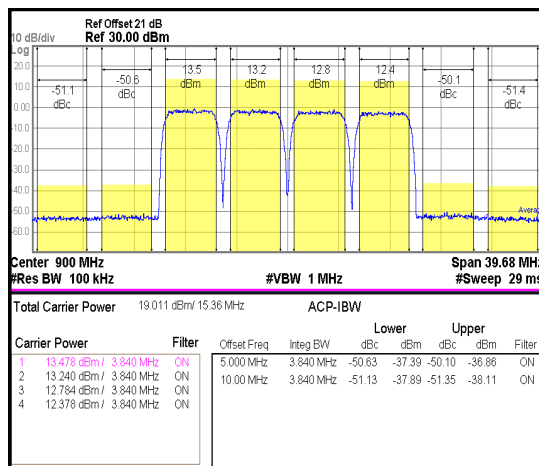
3GPP LTE E-TM3.1 10MHz



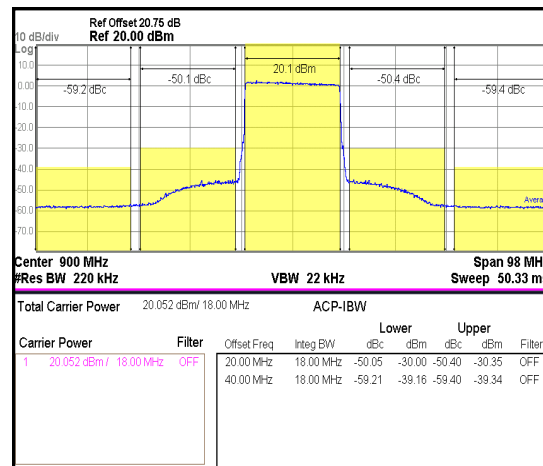
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3GPP LTE E-TM3.1 20MHz



3GPP WCDMA TM1 +64DPCH 4FA



3GPP LTE E-TM3.1 20MHz

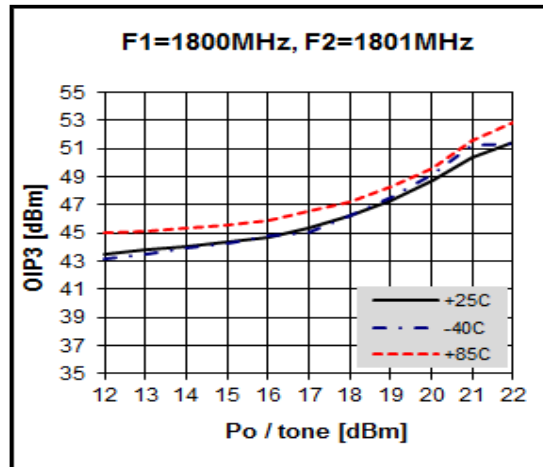
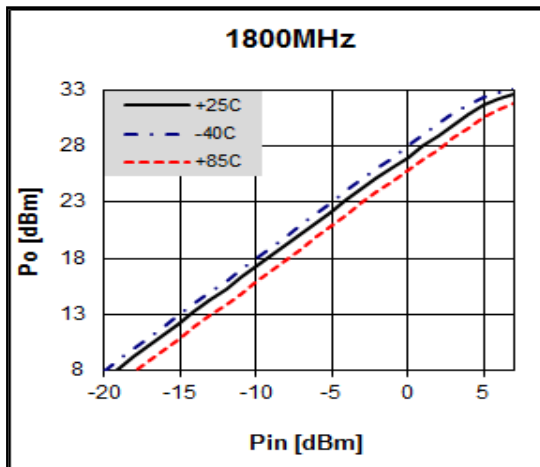
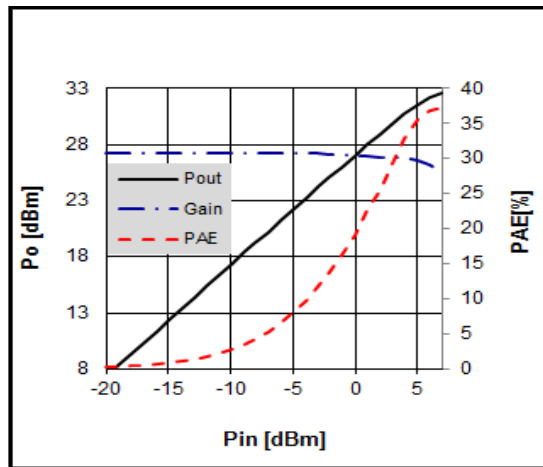
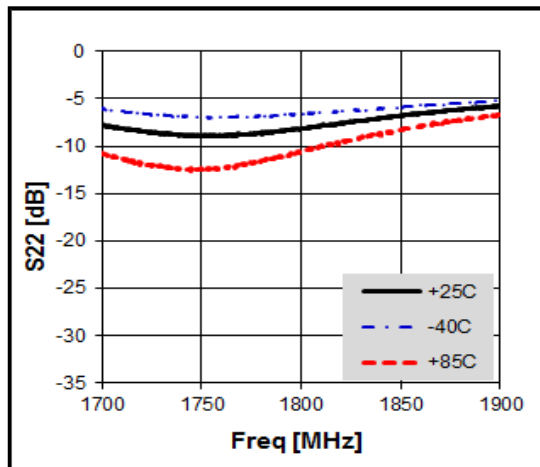
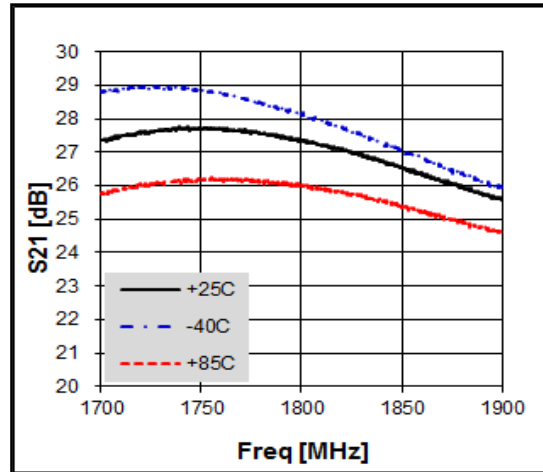
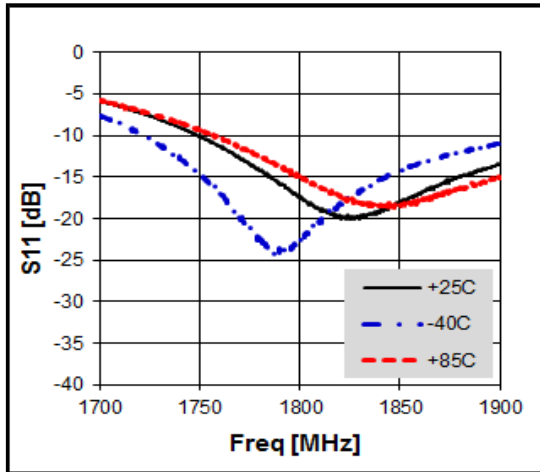
Application Circuit: 1800 MHz

Schematic Diagram	BOM	Marks		
	C1	0603	1uF	Samsung
	C2	0603	1uF	Samsung
	C3	0603	22pF	Samsung
	C4	0603	22pF	Samsung
	C5	0603	N/A	-
	C6	0603	N/A	-
	C7	0603	5pF	Samsung
	C8	0603	22pF	Samsung
	C9	0603	N/A	-
	C10	0603	2pF	Samsung
	C11	0603	N/A	-
	C12	0603	N/A	-
	C13	0603	N/A	-
	C14	0603	1uF	Samsung
C15	0603	22pF	Samsung	
C16	0603	1.5pF	Samsung	
C17	0603	3pF	Samsung	
L1	0603	18nH	Taiyo Yuden	
L2	1008	22nH	Coilcraft-HQ	
L3	0603	2.2nH	Taiyo Yuden	
R1	0603	300 Ω	Samsung	
R2	0603	430 Ω	Samsung	
R3	0603	82 Ω	Samsung	

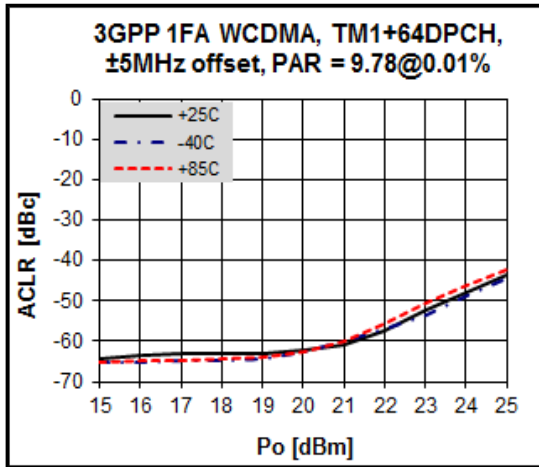
PCB Diagram	Notice															
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Input pin	C16	3.5mm														
Output pin	C17	4.1mm														
Pin 5	C10	3.1mm														
<p>1. We recommend to adjust capacitance of C10, when balance for multicarrier response of LTE20MHz is broken .</p>																

Typical Performance

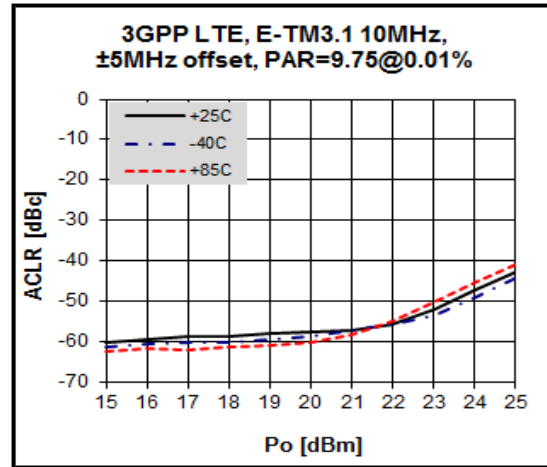
V_{cc} & V_{Bias} = +5V, I_{cq} =355mA, T_a =25°C



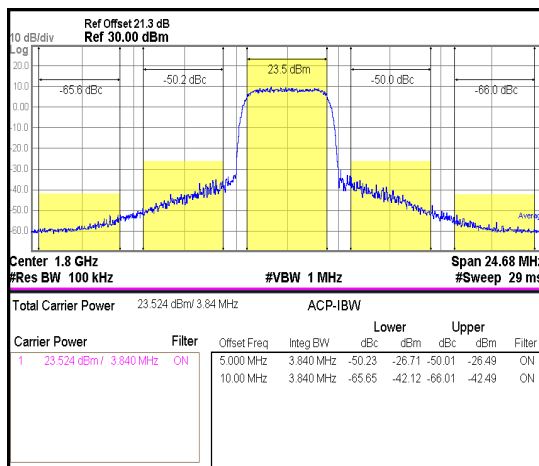
700-2800 MHz 1.5W High Linearity 5V 2-Stage Power Amplifier



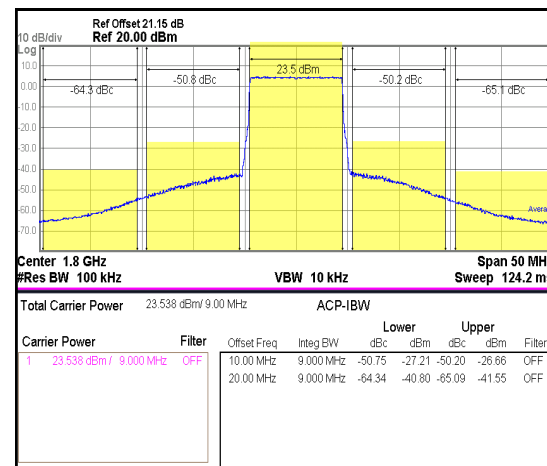
3GPP WCDMA TM1 +64DPCH 1FA



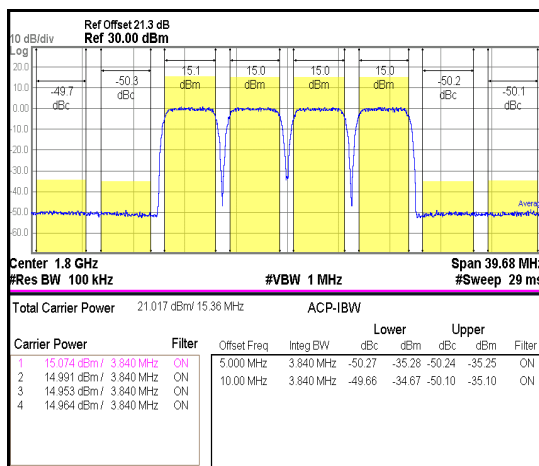
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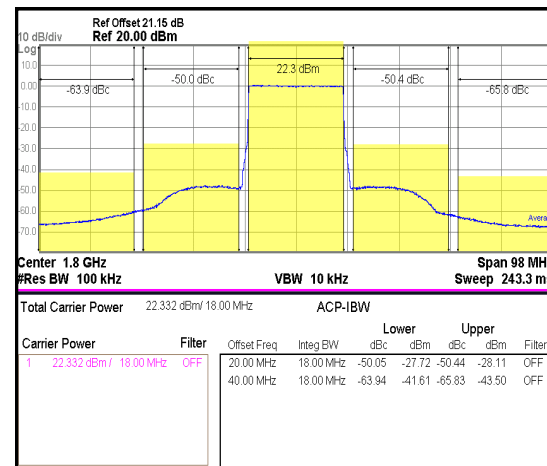
3GPP WCDMA TM1 +64DPCH 4FA



3GPP LTE E-TM3.1 20MHz

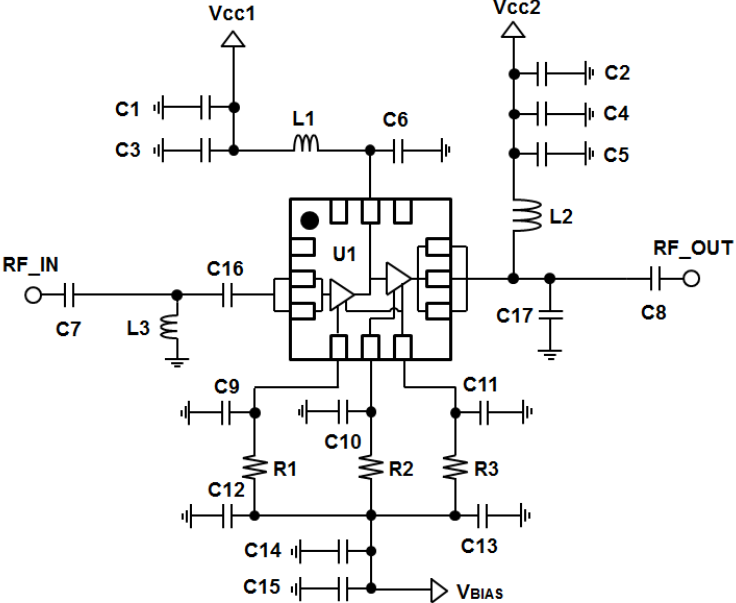
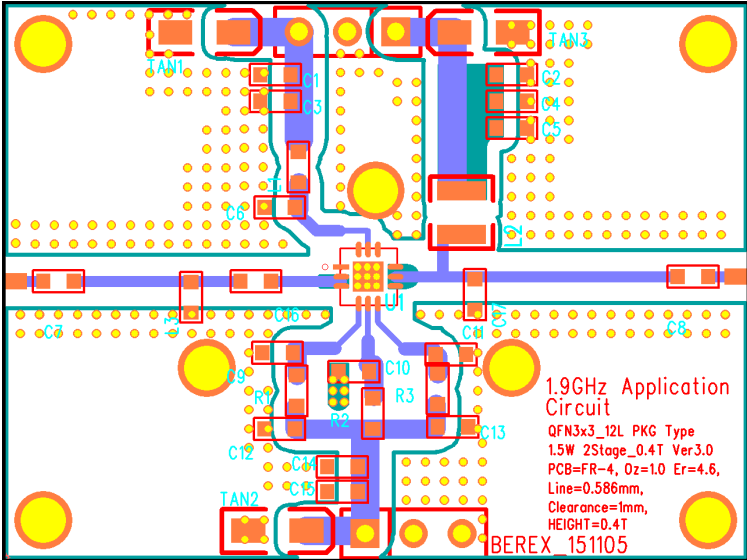


3GPP WCDMA TM1 +64DPCH 4FA



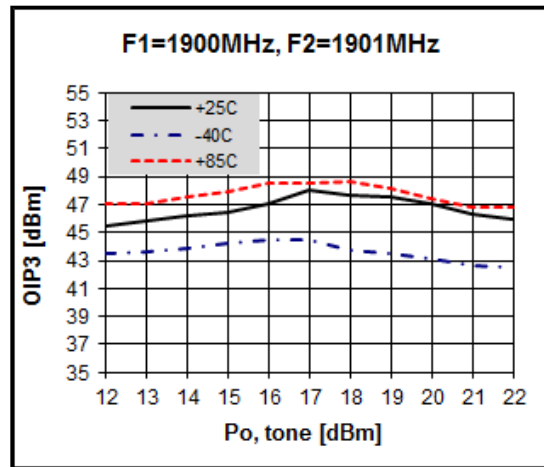
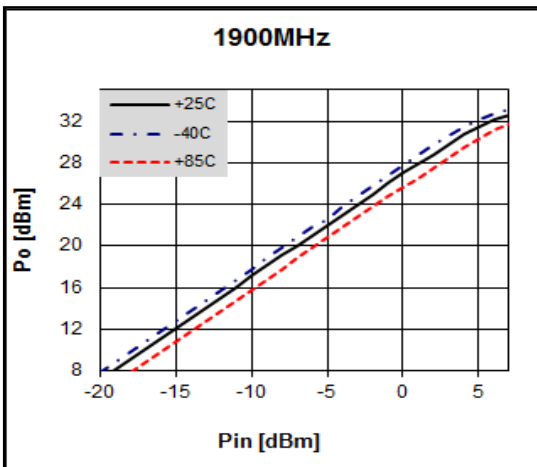
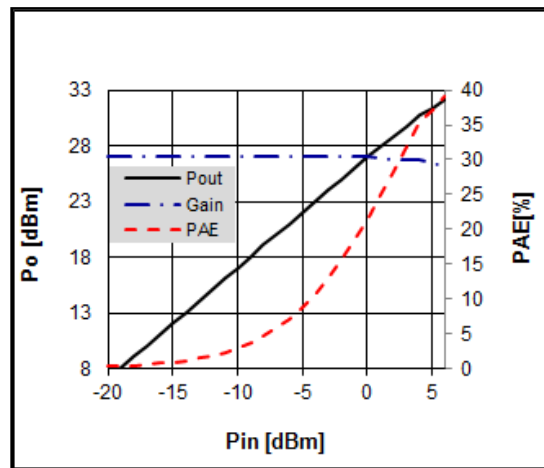
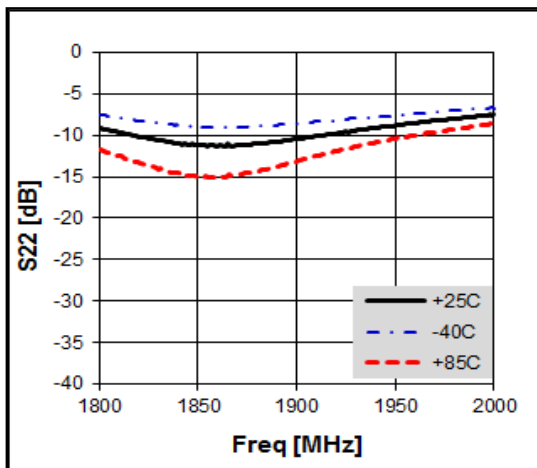
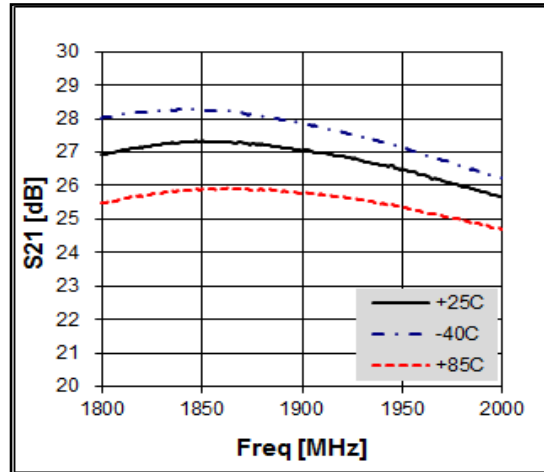
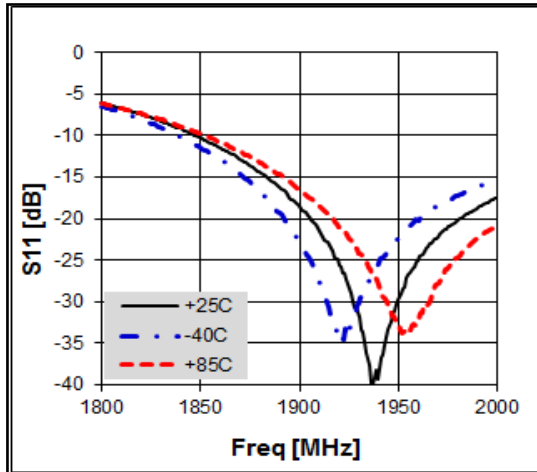
3GPP LTE E-TM3.1 20MHz

Application Circuit: 1900 MHz

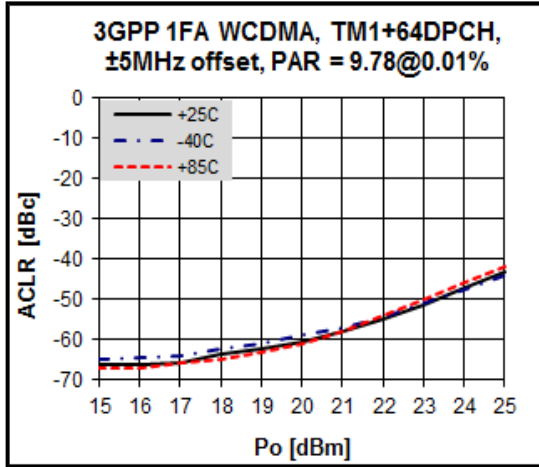
Schematic Diagram	BOM	Marks		
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	C4	0603	22pF	Samsung
	C5	0603	N/A	-
	C6	0603	N/A	-
	C7	0603	5pF	Samsung
	C8	0603	22pF	Samsung
	C9	0603	N/A	-
	C10	0603	1.8pF	Samsung
	C11	0603	N/A	-
	C12	0603	N/A	-
	C13	0603	N/A	-
	C14	0603	1uF	Samsung
	C15	0603	22pF	Samsung
	C16	0603	1.5pF	Samsung
	C17	0603	2.7pF	Samsung
L1	0603	15nH	Taiyo Yuden	
L2	1008	22nH	Coilcraft-HQ	
L3	0603	2.2nH	Taiyo Yuden	
R1	0603	300 Ω	Samsung	
R2	0603	430 Ω	Samsung	
R3	0603	82 Ω	Samsung	
PCB Diagram	Notice			
 <p data-bbox="755 1669 950 1858"> 1.9GHz Application Circuit QFN3x3_12L PKG Type 1.5W 2Stage_0.4T Ver3.0 PCB=FR-4, Dz=1.0 Er=4.6, Line=0.586mm, Clearance=1mm, HEIGHT=0.4T BEREX_151105 </p>	Below information is subject to change as conditions of the substrate.			
	Reference	Object	Distance	
	Input pin	L3	7.3mm	
	Input pin	C16	3.5mm	
Output pin	C17	3.7mm		
Pin 5	C10	3.1mm		
1. We recommend to adjust capacitance of C10, when balance for multicarrier response of LTE20MHz is broken .				

Typical Performance

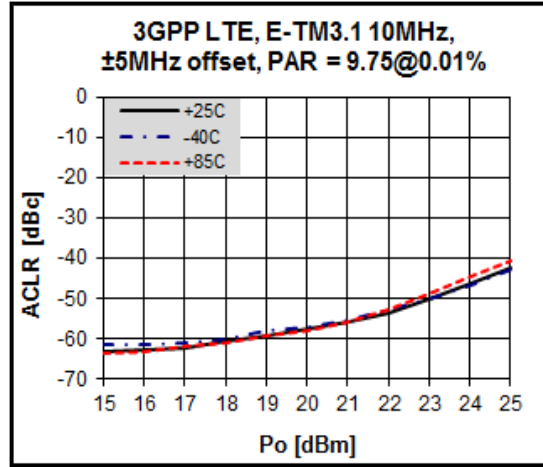
V_{CC} & $V_{Bias} = +5V$, $I_{CQ} = 355mA$, $T_a = 25^\circ C$



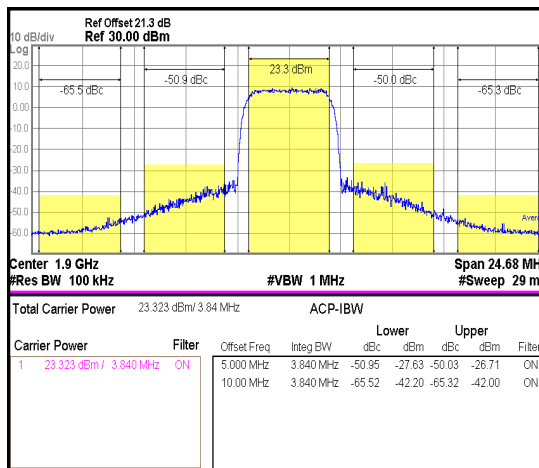
700-2800 MHz 1.5W High Linearity 5V 2-Stage Power Amplifier



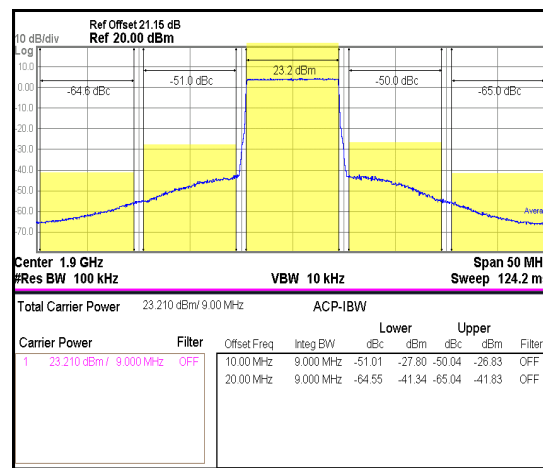
3GPP WCDMA TM1 +64DPCH 1FA



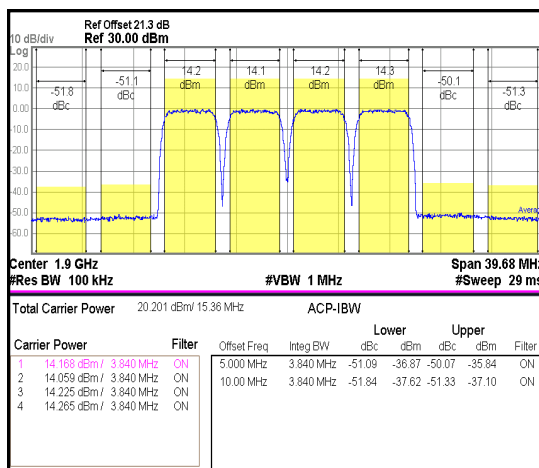
3GPP LTE E-TM3.1 10MHz



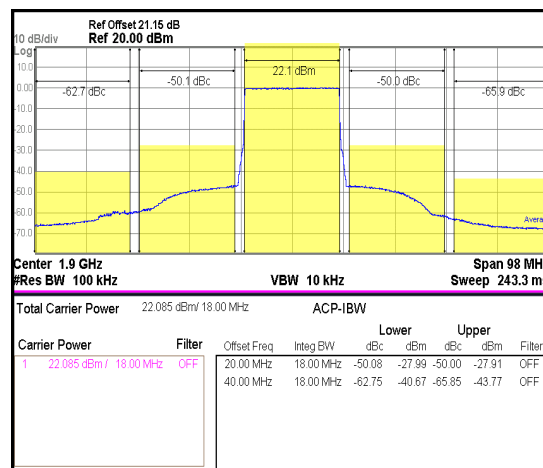
3GPP WCDMA TM1 +64DPCH 4FA



3GPP LTE E-TM3.1 20MHz



3GPP WCDMA TM1 +64DPCH 4FA



3GPP LTE E-TM3.1 20MHz

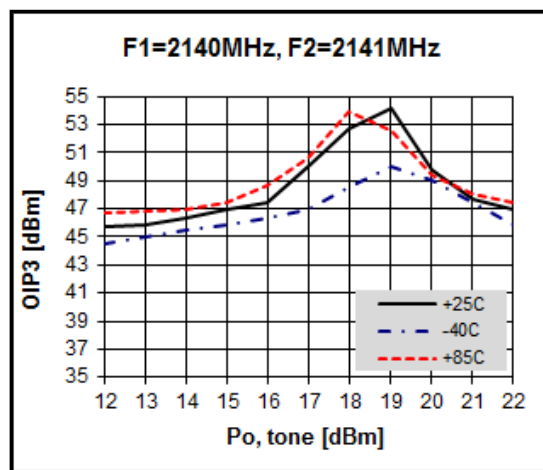
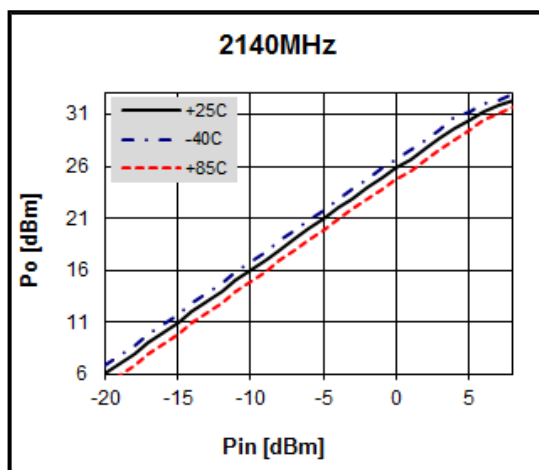
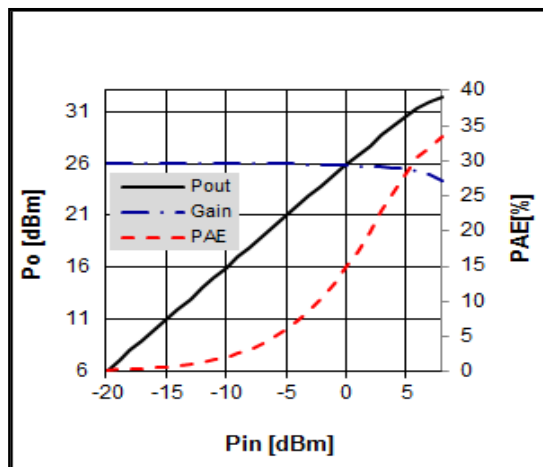
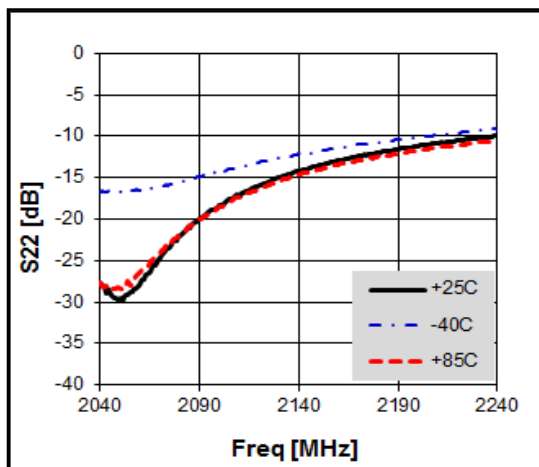
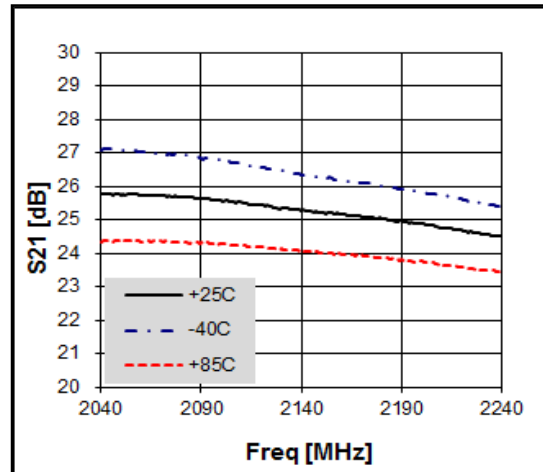
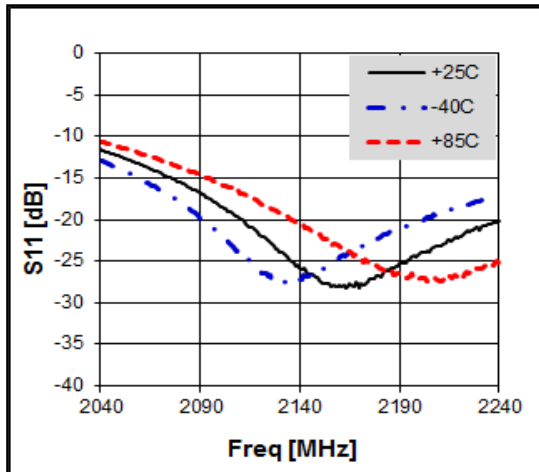
Application Circuit: 2140 MHz

Schematic Diagram	BOM	Marks		
	C1	0603	1uF	Samsung
	C2	0603	1uF	Samsung
	C3	0603	N/A	
	C4	0603	22pF	Samsung
	C5	0603	N/A	-
	C6	0603	N/A	-
	C7	0603	5pF	Samsung
	C8	0603	22pF	Samsung
	C9	0603	N/A	-
	C10	0603	1.2pF	Samsung
	C11	0603	N/A	-
	C12	0603	N/A	-
	C13	0603	N/A	-
	C14	0603	1uF	Samsung
	C15	0603	22pF	Samsung
	C16	0603	1.2pF	Samsung
C17	0603	2.2pF	Samsung	
L1	0603	33nH	Taiyo Yuden	
L2	1008	18nH	Coilcraft-HQ	
L3	0603	2.2nH	Taiyo Yuden	
R1	0603	300 Ω	Samsung	
R2	0603	430 Ω	Samsung	
R3	0603	82 Ω	Samsung	

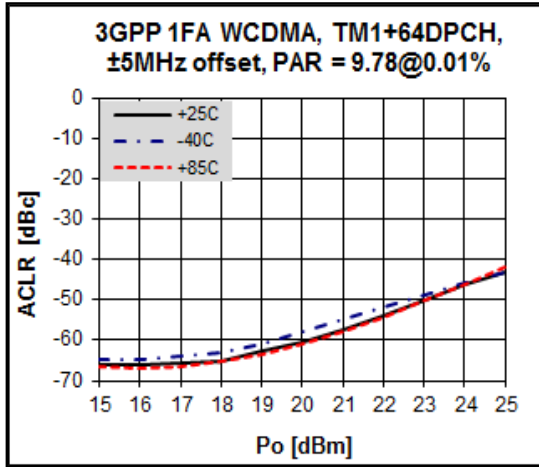
PCB Diagram	Notice														
	<p>Below information is subject to change as conditions of the substrate.</p>														
	<table border="1"> <thead> <tr> <th>Reference</th> <th>Object</th> <th>Distance</th> </tr> </thead> <tbody> <tr> <td>Input pin</td> <td>L3</td> <td>5.3mm</td> </tr> <tr> <td>Input pin</td> <td>C16</td> <td>3.5mm</td> </tr> <tr> <td>Output pin</td> <td>C17</td> <td>3.5mm</td> </tr> <tr> <td>Pin 5</td> <td>C10</td> <td>3.1mm</td> </tr> </tbody> </table> <p>1. We recommend to adjust capacitance of C10, when balance for multicarrier response of LTE20MHz is broken .</p>	Reference	Object	Distance	Input pin	L3	5.3mm	Input pin	C16	3.5mm	Output pin	C17	3.5mm	Pin 5	C10
Reference	Object	Distance													
Input pin	L3	5.3mm													
Input pin	C16	3.5mm													
Output pin	C17	3.5mm													
Pin 5	C10	3.1mm													

Typical Performance

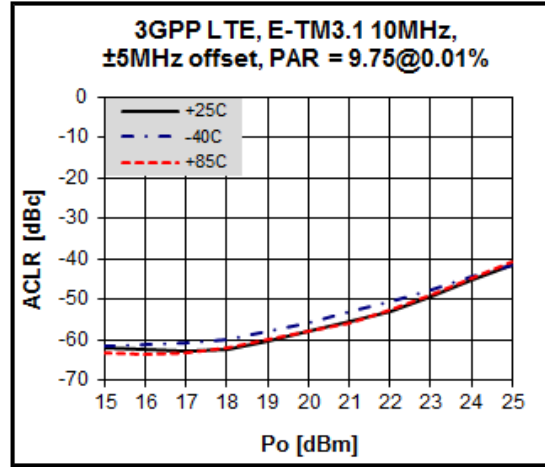
V_{CC} & $V_{Bias} = +5V$, $I_{CQ}=355mA$, $T_a=25^{\circ}C$



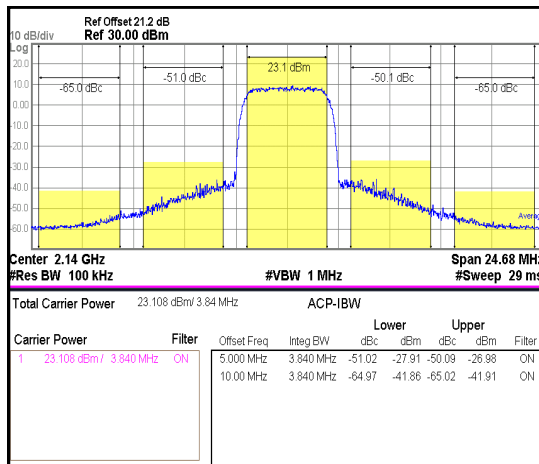
700-2800 MHz 1.5W High Linearity 5V 2-Stage Power Amplifier



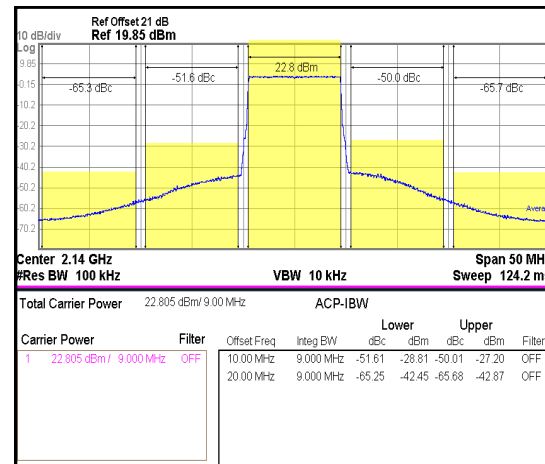
3GPP WCDMA TM1 +64DPCH 1FA



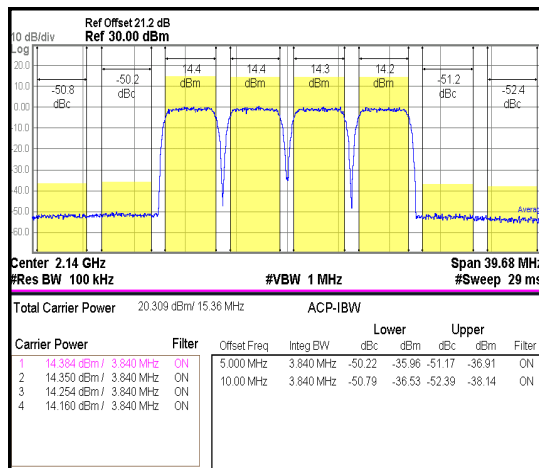
3GPP LTE E-TM3.1 10MHz



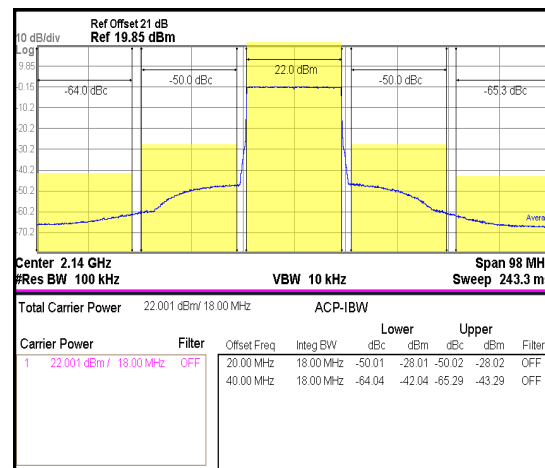
3GPP WCDMA TM1 +64DPCH 4FA



3GPP LTE E-TM3.1 20MHz

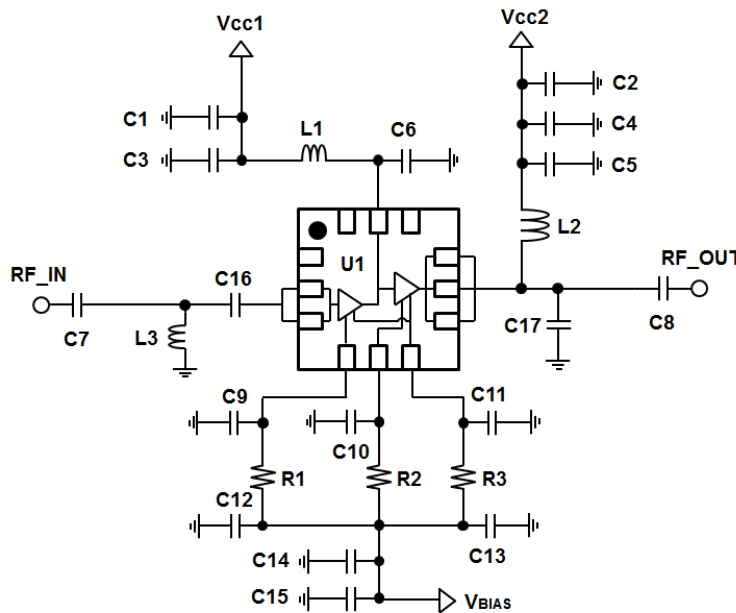


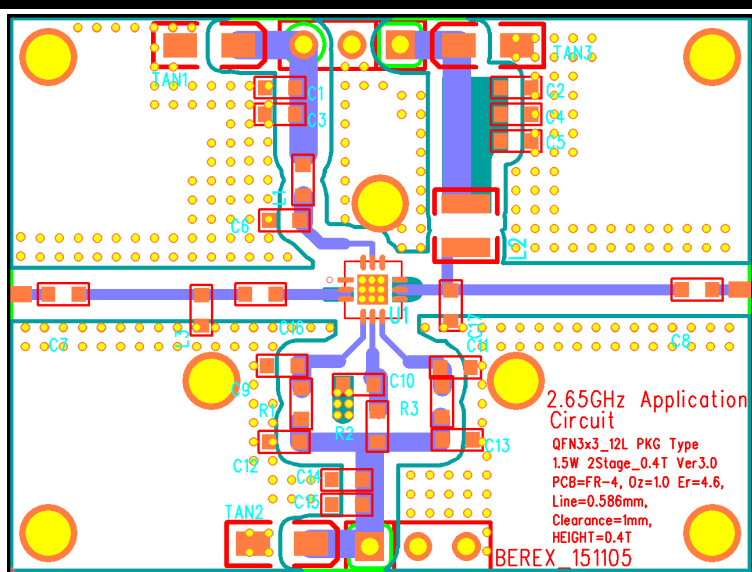
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3GPP LTE E-TM3.1 20MHz

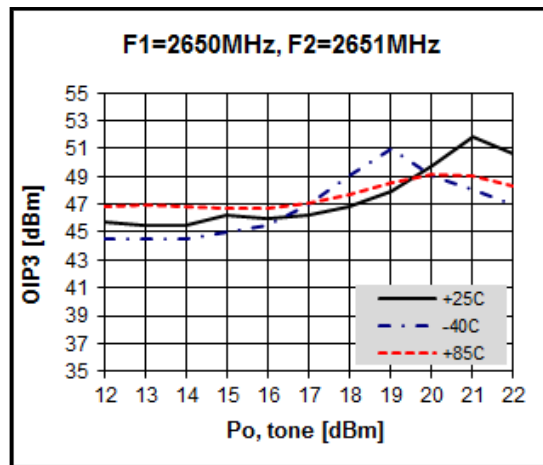
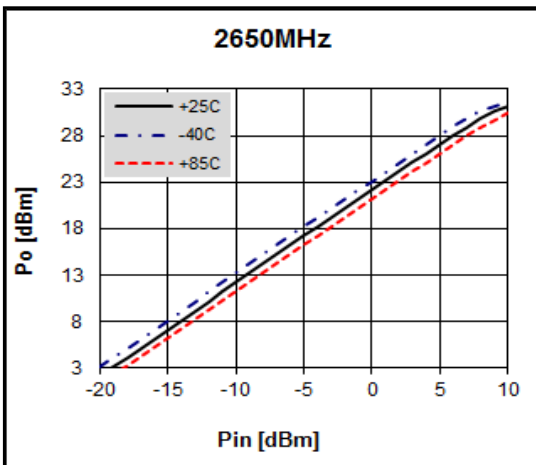
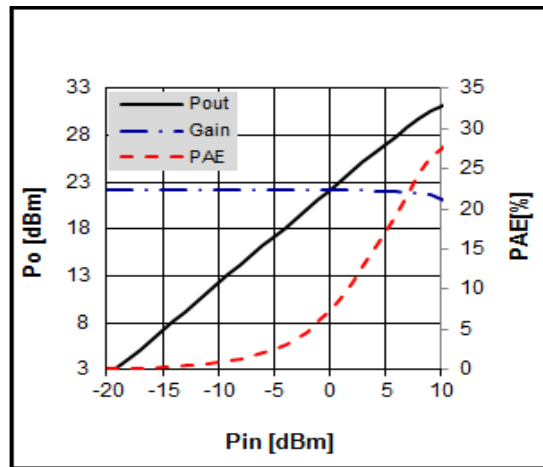
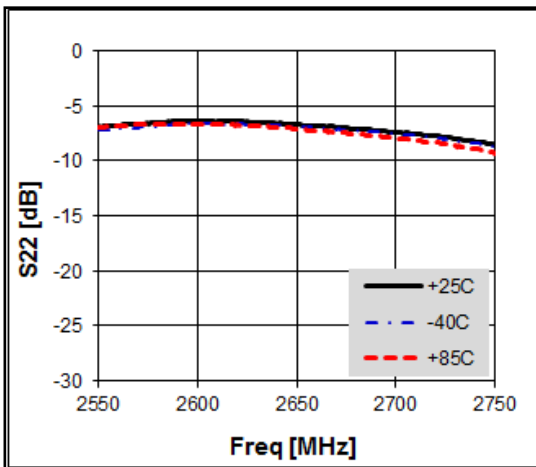
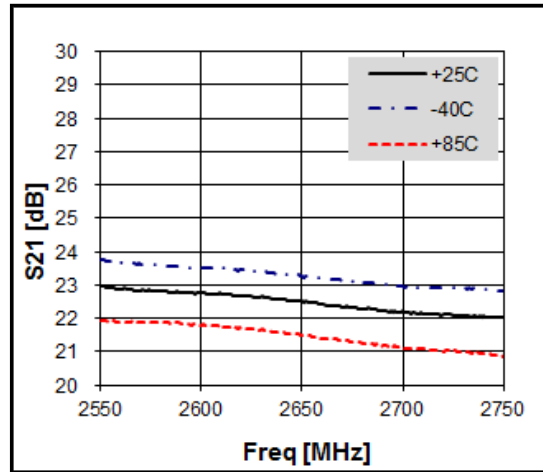
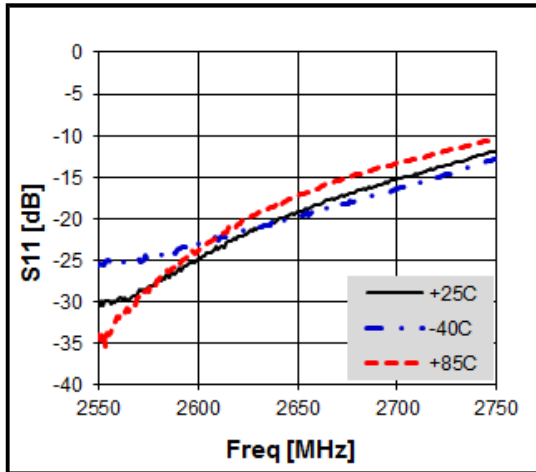
Application Circuit: 2650 MHz

Schematic Diagram		BOM		Marks	
		C1	0603	1uF	Samsung
		C2	0603	1uF	Samsung
		C3	0603	N/A	-
		C4	0603	22pF	Samsung
		C5	0603	N/A	-
		C6	0603	N/A	-
		C7	0603	5pF	Samsung
		C8	0603	22pF	Samsung
		C9	0603	N/A	-
		C10	0603	2.2pF	Samsung
		C11	0603	N/A	-
		C12	0603	N/A	-
		C13	0603	N/A	-
		C14	0603	1uF	Samsung
		C15	0603	22pF	Samsung
		C16	0603	0.75pF	Samsung
C17	0603	1.5pF	Samsung		
L1	0603	27nH	Taiyo Yuden		
L2	1008	18nH	Coilcraft-HQ		
L3	0603	1.8nH	Taiyo Yuden		
R1	0603	300 Ω	Samsung		
R2	0603	430 Ω	Samsung		
R3	0603	82 Ω	Samsung		

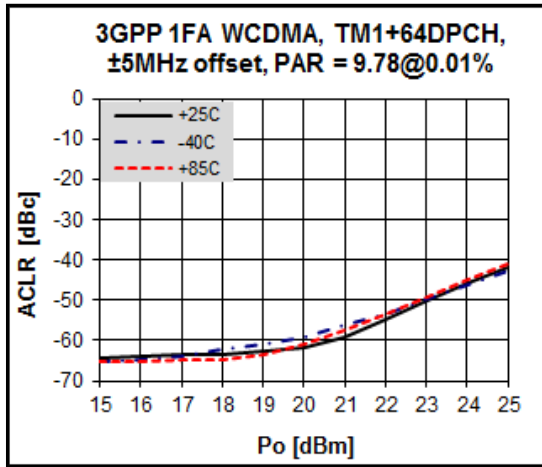
PCB Diagram		Notice		
 <p>2.65GHz Application Circuit QFN3x3_12L PKG Type 1.5W 2Stage_0.4T Ver3.0 PCB=FR-4, Oz=1.0 Er=4.6, Line=0.588mm, Clearance=1mm, HEIGHT=0.4T BEREX_151105</p>		Below information is subject to change as conditions of the substrate.		
		Reference	Object	Distance
		Input pin	L3	7.0mm
		Input pin	C16	3.5mm
		Output pin	C17	2.6mm
Pin 5	C10	3.1mm		

Typical Performance

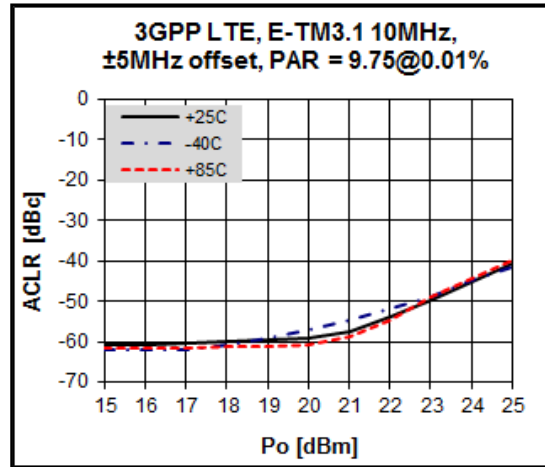
V_{CC} & $V_{Bias} = +5V$, $I_{CQ} = 355mA$, $T_a = 25^\circ C$



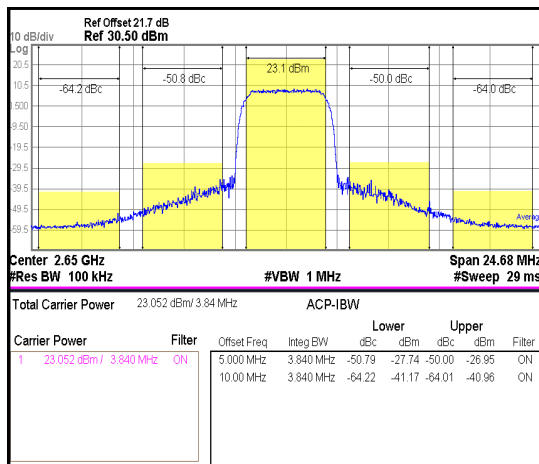
700-2800 MHz 1.5W High Linearity 5V 2-Stage Power Amplifier



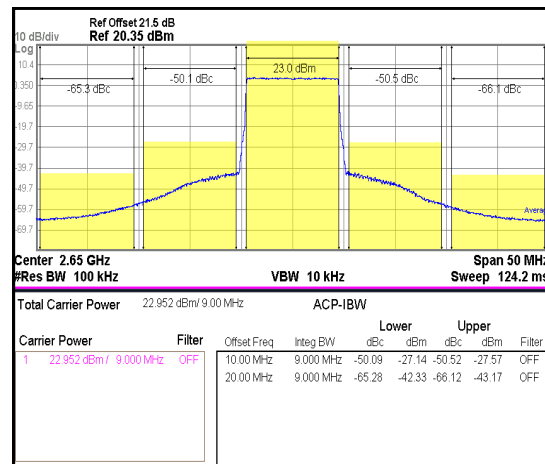
3GPP WCDMA TM1 +64DPCH 1FA



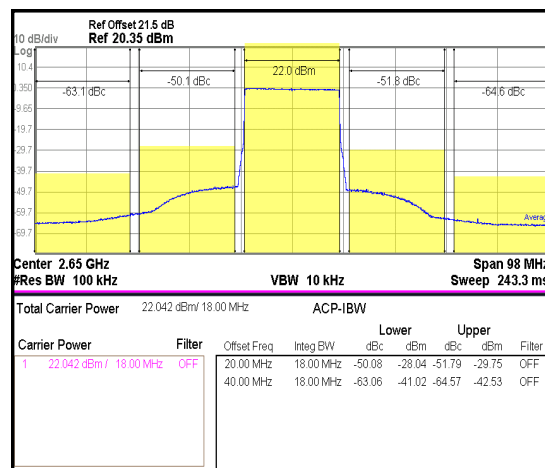
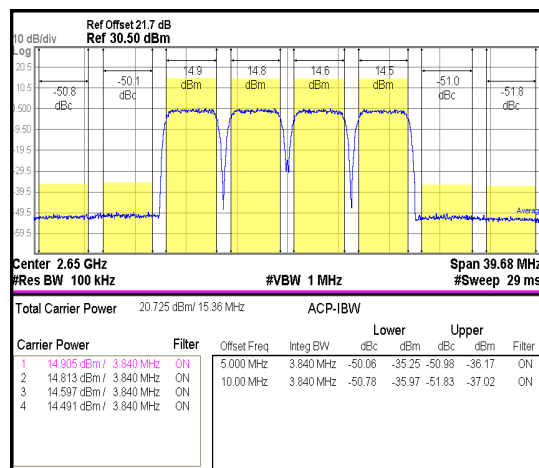
3GPP LTE E-TM3.1 10MHz



3GPP WCDMA TM1 +64DPCH 4FA

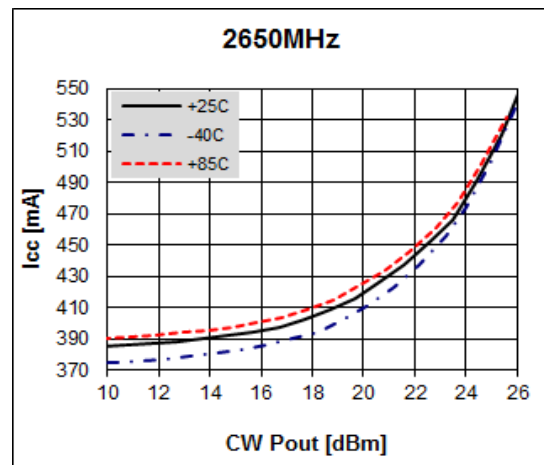
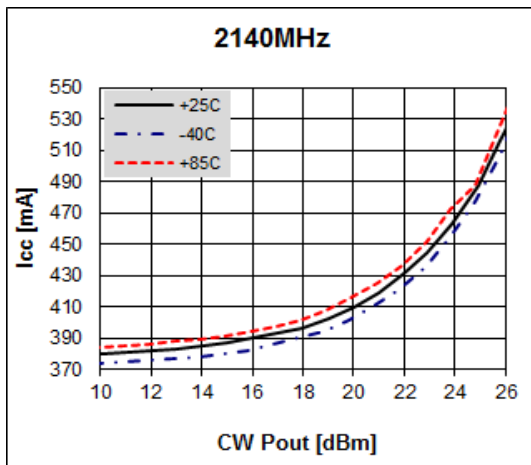
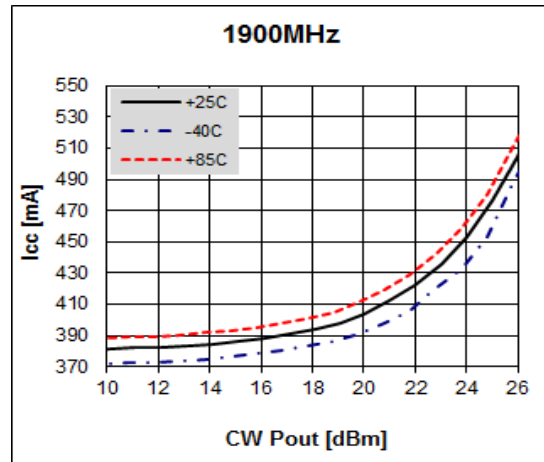
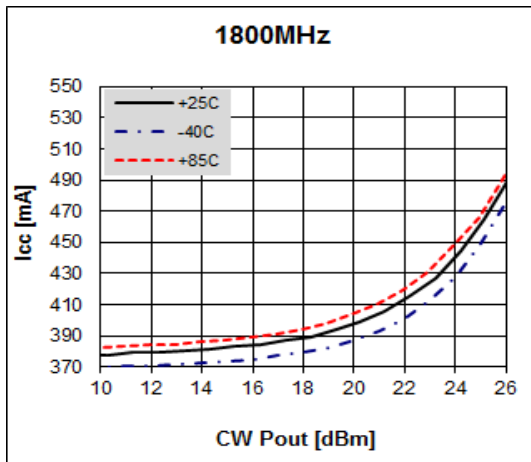
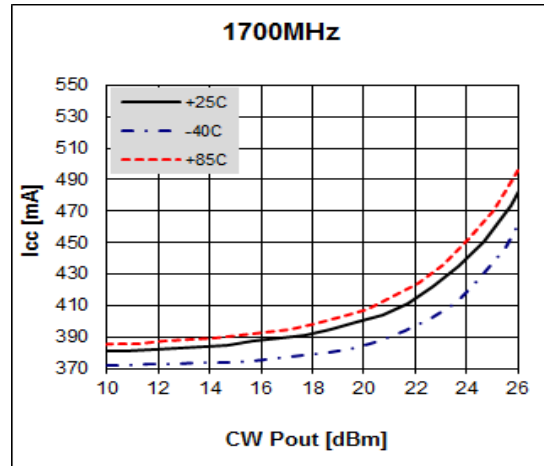
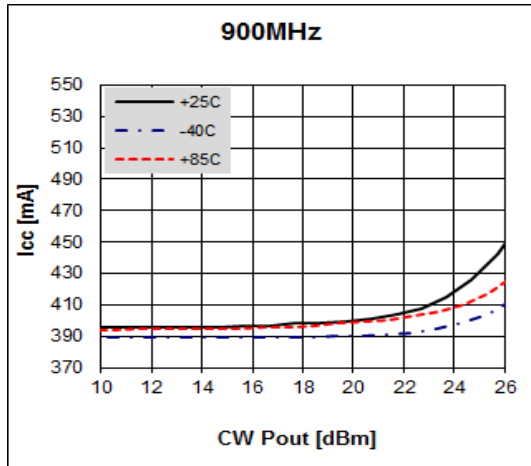


3GPP LTE E-TM3.1 20MHz

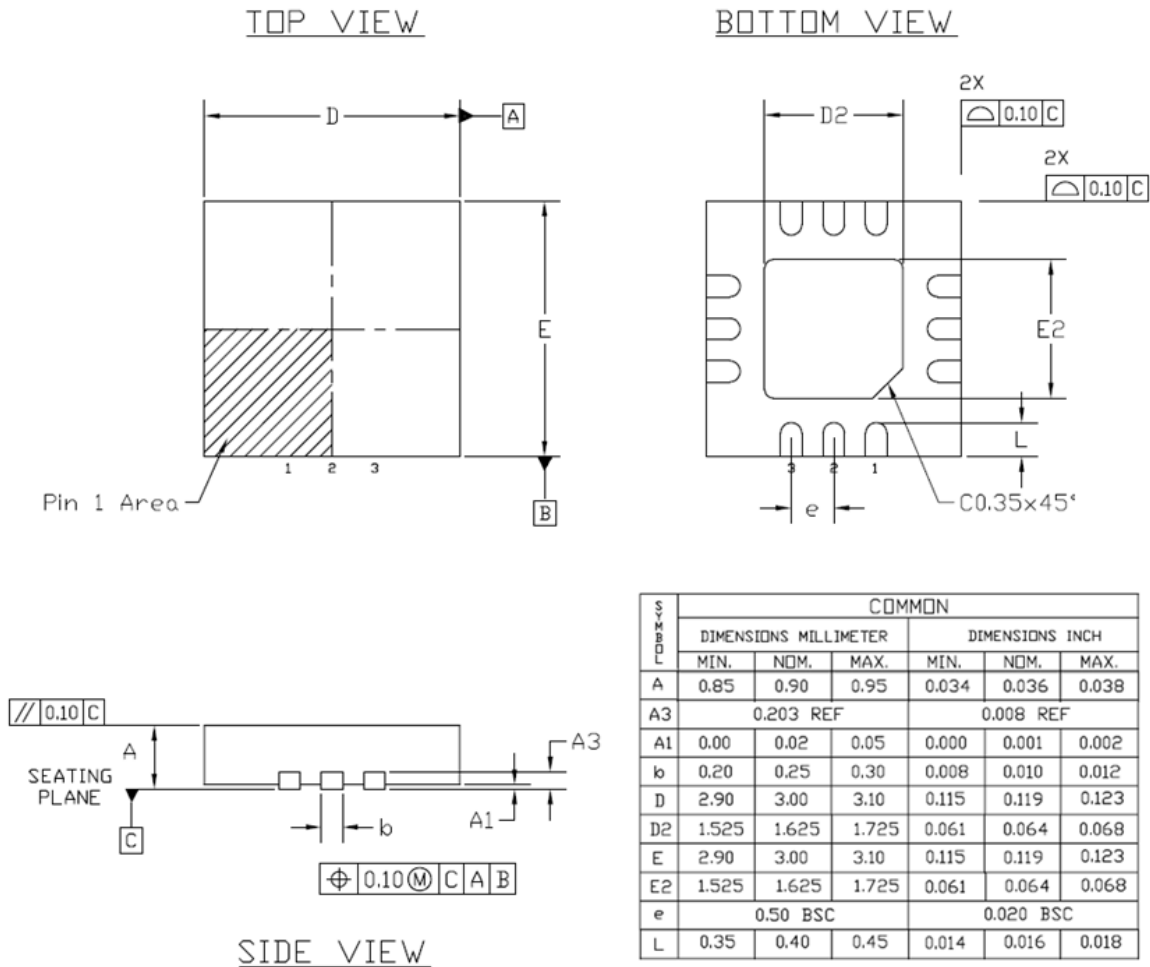


Typical Performance(Pout vs. Icc)

V_{cc} & $V_{Bias} = +5V$, $I_{cq}=355mA$, $T_a=25^{\circ}C$



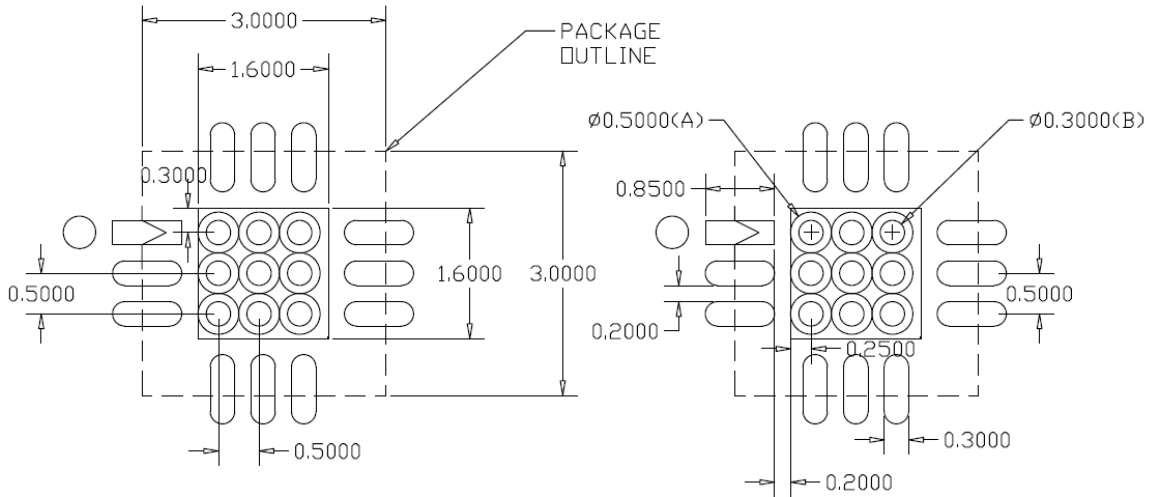
Package Outline Dimension



NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM. FROM TERMINAL TIP.
4. INSULATION THICKNESS, CLEARANCE OF OVERLAP ARE USER DEFINED.
5. INSULATION NOT COMPLETELY SHOWN FOR REASONS OF CLARITY.

Suggested PCB Land Pattern and PAD Layout



Unit : mm

• Notes

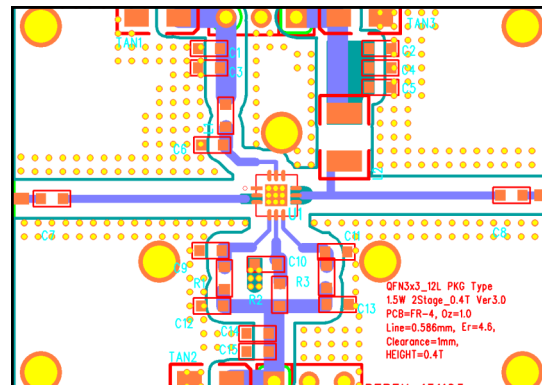
1. Use 1 oz. copper minimum for top and bottom layer metal.
2. A heatsink underneath the area of the PCB for the mounted device is required for proper thermal operation.
3. Ground / thermal vias are critical for the proper performance of this device.

Package Marking



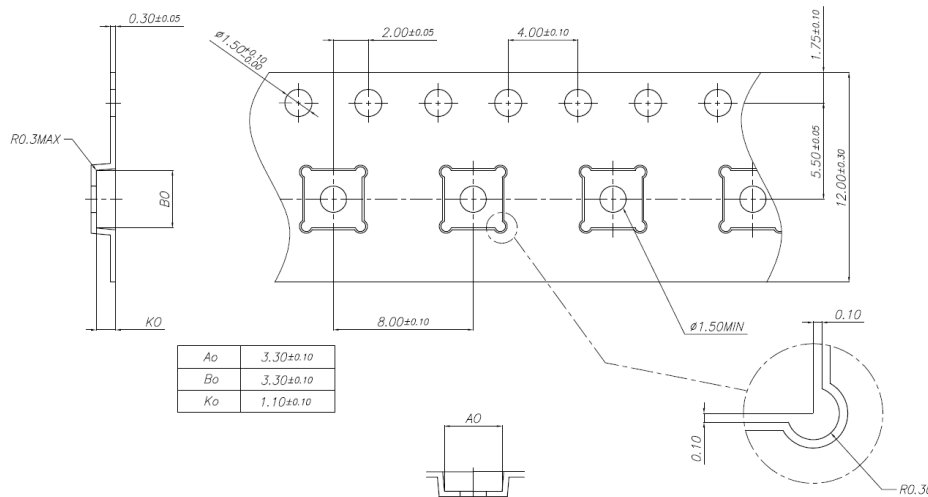
YY = Year, WW = Working Week,
XX = Wafer No.

PCB Mounting



Tape & Reel

QFN 3x3



Packaging information :

Tape width(mm) : 12

Reel Size (inches) : 7

Device Cavity Pitch(mm) : 8

Devices Per Reel : 1000

Lead plating finish

100% Tin Matte finish

(All BeRex products undergoes a 1 hour, 150 degree C, Anneal bake to eliminate thin whisker growth concerns.)

MSL / ESD Rating

ESD Rating: Class 1C
Value: Passes $\geq 1000V$ to $< 2000 V$
Test: Human Body Model (HBM)
Standard: JEDEC Standard JS-001-2012

ESD Rating: Class C3
Value: Passes $>1000V$
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101F

MSL Rating: Level 1 at $+260^{\circ}C$ convection reflow
Standard: JEDEC Standard J-STD-020



Proper ESD procedures should be followed when handling this device.

RoHS Compliance

This part is compliant with Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive 2011/65/EU as amended by Directive 2015/863/EU.

This product also is compliant with a concentration of the Substances of Very High Concern (SVHC) candidate list which are contained in a quantity of less than 0.1%(w/w) in each components of a product and/or its packaging placed on the European Community market by the BeRex and Suppliers.

NATO CAGE code:

2	N	9	6	F
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