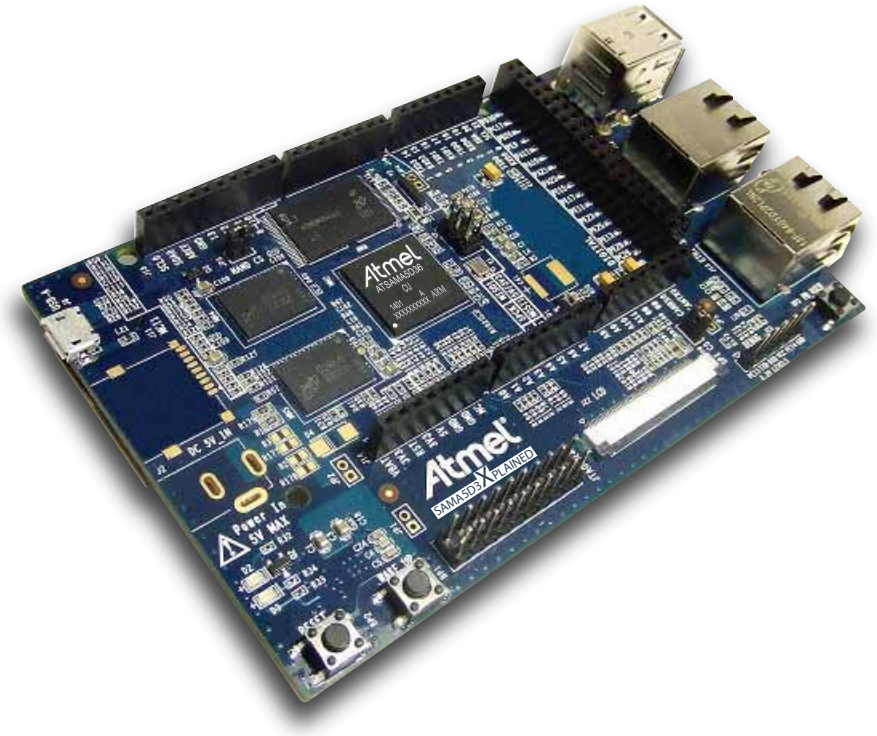
Atmel | SMART SAMA5D3 Series

SAMA5D3 Xplained

USER GUIDE



Introduction

This user guide introduces the Atmel® SAMA5D3 Xplained evaluation kit and describes the development and debugging capabilities for applications running on a SAMA5D36 ARM®-based embedded microprocessor unit (eMPU).

Scope

This guide provides details on the SAMA5D3 Xplained evaluation kit. It is made up of four main sections:

- Section 1. describes the evaluation kit content and its main features.
- Section 2. provides instructions to power up the SAMA5D3 Xplained board.
- Section 3. provides an overview of the SAMA5D3 Xplained board.
- Section 4. describes the SAMA5D3 Xplained board components.

Contents

- Boards
  - One SAMA5D3 Xplained board
- Cables
  - One micro-AB type USB cable
- A welcome letter

Related Items

- Atmel SAMA5D3 Series Datasheet
- SAMA5D3 Xplained Getting Started

Table of Contents

1. Evaluation Kit Specifications

Table 1-1. Evaluation Kit Specifications

Characteristic		Specifications
Temperature	Operating	0°C to +70°C
	Storage	-40°C to +85°C
Relative Humidity		0 to 90% (non-condensing)
RoHS status		Compliant
Ordering code		ATSAMA5D3-XPLD

1.1 Electrostatic Warning

ESD-Sensitive Electronic Equipment!

The evaluation kit is shipped in a protective anti-static package. The board system must not be subject to high electrostatic potentials.

We strongly recommend using a grounding strap or similar ESD protective device when handling the board in hostile ESD environments (offices with synthetic carpet, for example). Avoid touching the component pins or any other metallic element on the board.

1.2 Power Supply Warning

Hardware Power Supply Limitation

Using a power adapter greater than 5Vcc (e.g. the 12Vcc power adapters from other kits such as Arduino kits) may damage the board.

Hardware Power Budget

Using the USB as the main power source (max. 500 mA) is acceptable only with the use of the on-board peripherals and low-power LCD extension.

When external peripheral or add-on boards need to be powered, we recommend the use of an external power adapter connected to a J2 DC Jack (can provide up to 1.2A on the 3.3V node).

2. Power Up

Several power source options are available to power up the SAMA5D3 Xplained board.

The board can be:

- USB-powered through the USB Micro-AB connector (J6 connector - default configuration)
- Powered through an external AC-to-DC adapter connected via a 2.1 mm center-positive plug into the optional power jack of the board. The recommended output voltage range of the power adapter is 5V at 2A.
- Powered through the Arduino shield.

WARNING **Unlike Arduino Uno boards, the SAMA5D3 Xplained board runs at 3.3V. The maximum voltage that the I/O pins can tolerate is 3.3V. Providing higher voltages (e.g. 5V) to an I/O pin could damage the board.**

2.1 Power up the Board

Unpack the board, taking care to avoid electrostatic discharge. Simply connect the USB Micro-AB cable to the connector (J6).Then, connect the other end of the cable to a free USB port of your PC.

Table 2-1. Electrical Characteristics

Electrical Parameter	Values
Input voltage	5 VCC
Maximum input voltage	6 VCC
Max DC 3.3V current available	1.2A
I/O Voltage	3.3V only

2.2 Sample Code and Technical Support

After booting up the board, you can run sample code or your own application on the board. You can download sample code and get technical support from the Atmel website.

Linux software and demos can be found on the website Linux4SAM.

3. Hardware Introduction

3.1 Introduction

The Atmel SAMA5D3 Xplained board is a fully-featured evaluation platform for Atmel SAMA5D3 series microcontrollers. It allows users to extensively evaluate, prototype and create application-specific designs.

3.2 Equipment List

The SAMA5D3 Xplained board is built around the integration of a Cortex®-A5-based microcontroller (BGA 324 package) with external memory, dual Ethernet physical layer transceiver, two SD/MMC interfaces, two host USB ports and one device USB port, one 24-bit RGB LCD interface and one debug interface.

Seven headers, compatible with Arduino R3, are available for various shield connections.

3.3 Board features

Table 3-1. Board Specifications

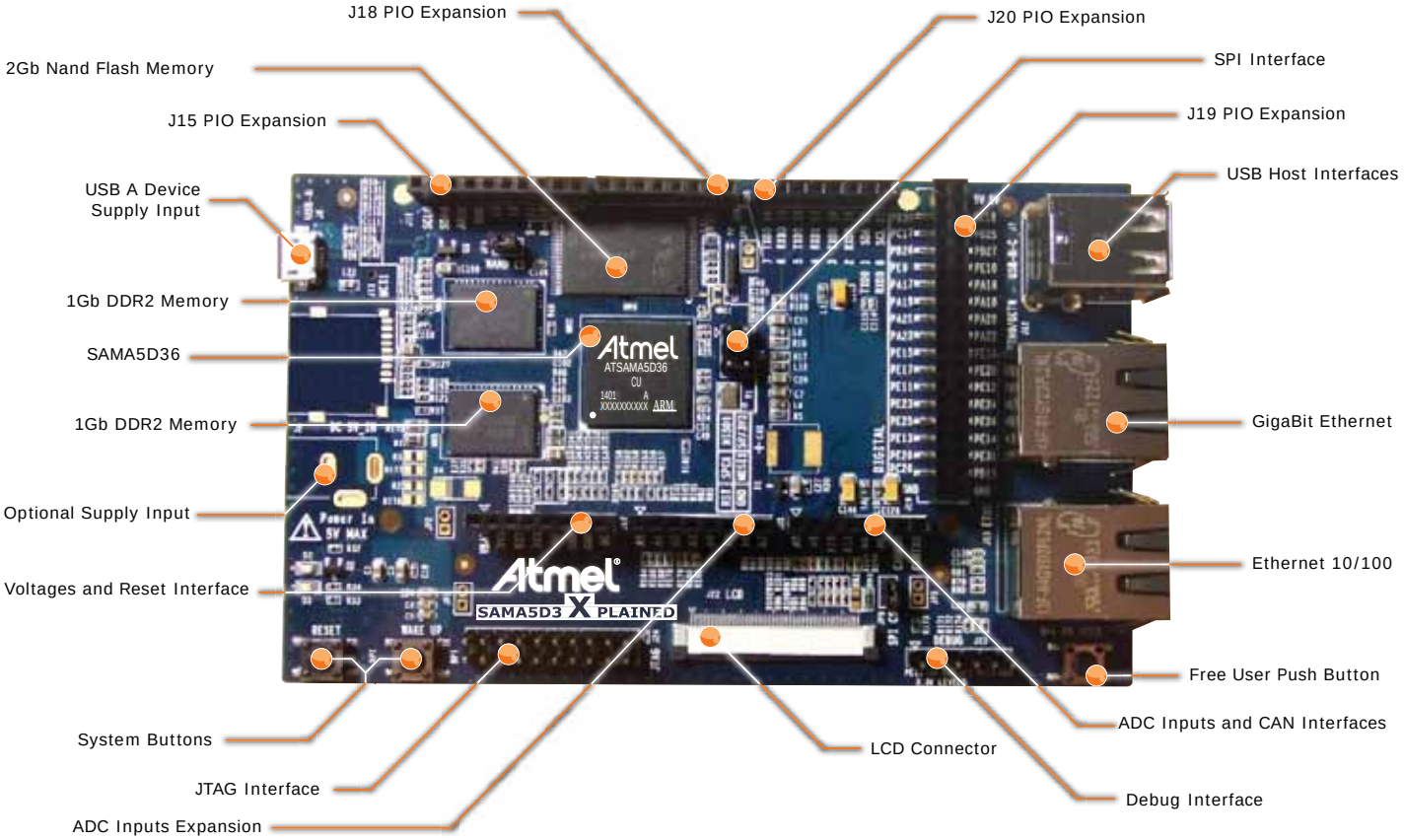
Characteristics	Specifications
PCB characteristics	125 x 75 x 20mm (10-layers)
Processor	SAMA5D36 (324-ball BGA package) ARM Cortex-A5 Processor with ARM v7-A Thumb2® instruction set, core frequency up to 536 MHz.
Processor clock sources	12-MHz crystal oscillator 32.768-kHz crystal oscillator
Memory	2 x 1Gb DDR2 (16M x 16 bits x 8 banks) 1 x 2Gb SLC NAND Flash (256M x 8 bits)
Optional on-board memory	One Serial EEPROM SPI One 1-Wire EEPROM
SD/MMC	One 8-bit SD card connector One optional 4-bit Micro-SD card connector
USB	Two USB Hosts with power switch One Micro-AB USB device
Display interface	One LCD interface connector, LCD TFT Controller with overlay, alpha-blending, rotation, scaling and color space conversion
Ethernet	One Gigabit Ethernet PHY (GRMII 10/100/1000) One Ethernet PHY (RMII 10/100)
Debug port	One JTAG interface connector One serial DBGU interface (3.3V level)
Expansion connectors	Arduino R3 compatible set of headers The SAMA5D36 GPIO,TWI, SPI, USART, UART, Audio and ISI interfaces are accessible through these headers.
Board supply voltage	5V from USB or power jack or Arduino shield On-board power regulation is performed by a Power Management Unit (PMU)
Battery	On-board optional power Cap for CMOS backup
User interface	Reset, wakeup and free user pushbutton One red user/power LED and one blue user LED

4. Board Components

4.1 Board Overview

The full-featured SAMA5D3 Xplained board integrates several peripherals and interface connectors, as shown in Figure 4-1.

Figure 4-1. SAMA5D3 Xplained Board Overview



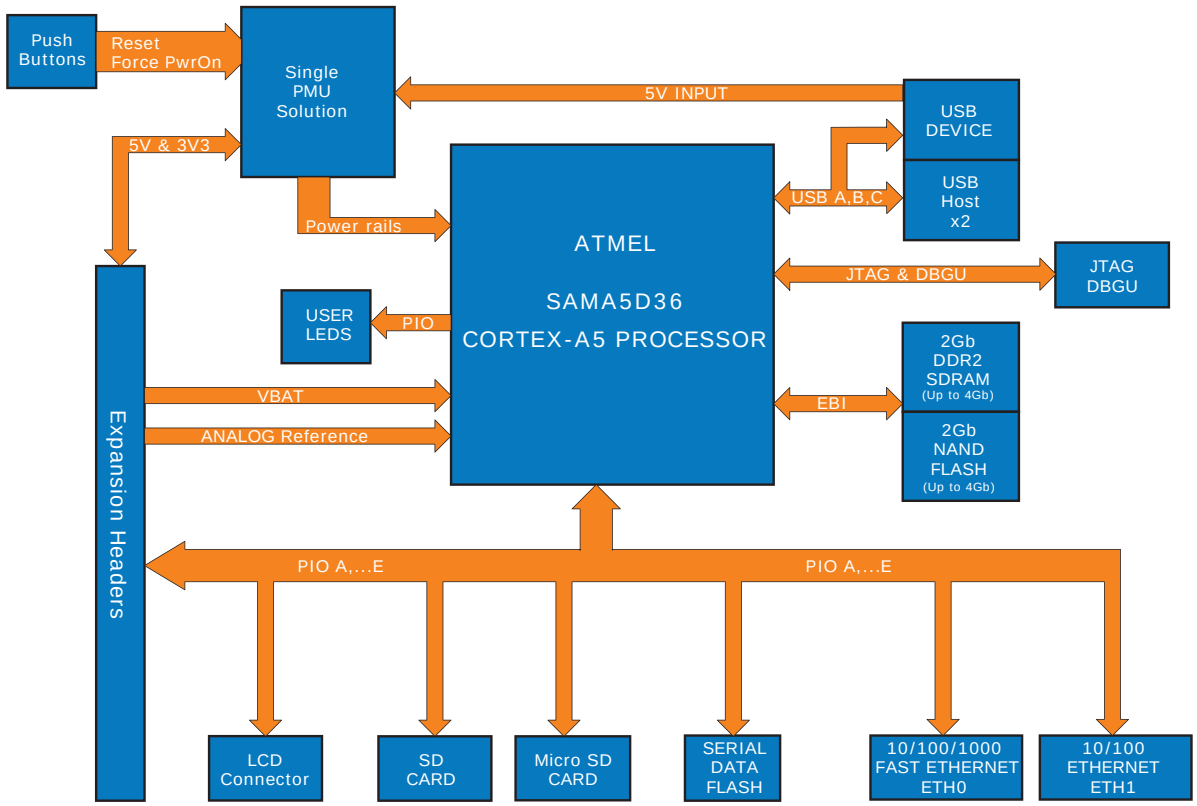
The SAMA5D3 Xplained board is equipped with the interface connectors described in Table 4-1.

Table 4-1. SAMA5D3 Xplained Board Interface Connectors

Header	Interfaces to
J2	Main power supply
J6	USB A device. Supports USB device using a Micro-AB connector
J7 (upper)	USB B Host. Supports USB host using a type A connector
J7 (lower)	USB C Host. Supports USB host using a type A connector
J23	Serial DBGU 3.3V level
J24	JTAG, 20-pin IDC connector
J10	SD/MMC connector
J11	Micro-SD connector
J12	Gigabit Ethernet ETH0
J13	Ethernet ETH1
J22	Expansion connector with all LCD controller signals for display module connection (QTouch®, TFT LCD display with Touch Screen and backlight
C41	Optional SuperCap
J14–J21	Expansion connectors with Arduino R3 compatible PIO signals
–	Various test points located on the board

4.2 Function Blocks

Figure 4-2. Evaluation Kit Architecture



4.2.1 Processor

The SAMA5D3 Xplained board is built around the SAMA5D36, a Cortex-A5 application processor which combines high-performance computing device with low-power consumption and a wide range of communication peripherals. It features a combination of user interface functionalities and high data rate IOs, including LCD controller, touchscreen, camera interface, Gigabit and 10/100 Ethernet ports, high-speed USB and SDIO.

The ARM Cortex-A5 supports the latest generation of DDR2 and NAND Flash memory interfaces for program and data storage. An internal 166-MHz multi-layer bus architecture associated with 24 DMA channels and two 64-Kbyte SRAM blocks, sustains the high bandwidth required by the processor and the high-speed peripherals.

4.2.2 Clock Circuitry

The SAMA5D3 Xplained evaluation board features four clock sources:

- Two clocks are alternatives for the SAMA5D3 series processor main clock
- Two crystal oscillators are used for the GETH and Ethernet MII/RMII chip

Table 4-2. Main Components Associated with the Clock Systems

Quantity	Description	Component Assignment
1	Crystal for internal clock, 12 MHz	Y1
1	Crystal for RTC clock, 32.768 kHz	Y2
1	Oscillator for ethernet clock RGMII, 25 MHz	Y3
1	Oscillator for ethernet clock RMII, 25 MHz	Y4

4.2.3 Power Supplies

The on-board power supply generation is based on the Active-Semi® Power Management Unit (PMU) featuring a 3-channel (3.3V / 1.8V /1.2V or 1.0V) topology. For maximum efficiency, these supply channels are generated by three integrated step-down converters.

In addition to these 3 DCDC channels, 4 LDO channels with low noise and high PSRR performance are available for the application. These channels are disabled at startup by default and can be turned on and adjusted under software control through an I²C link. They are also used to supply the 2.5V VDDFUSE and the 3.3V VDDANA power inputs of the processor.

The power supply sequencing of the three primary channels is controlled by the PMU itself in full compliance with the SAMAD3 requirements. The turn-on sequence is: 3.3V first, then 1.8V and finally 1.2V.

There is a known error on the ACT8865 I²C implementation. The port must be shut off after configuration or problems may occur with devices using the same I²C channel, e.g., TM43xx LCD display.

Refer to the ACT8865 datasheet at http://www.active-semi.com/ for more details.

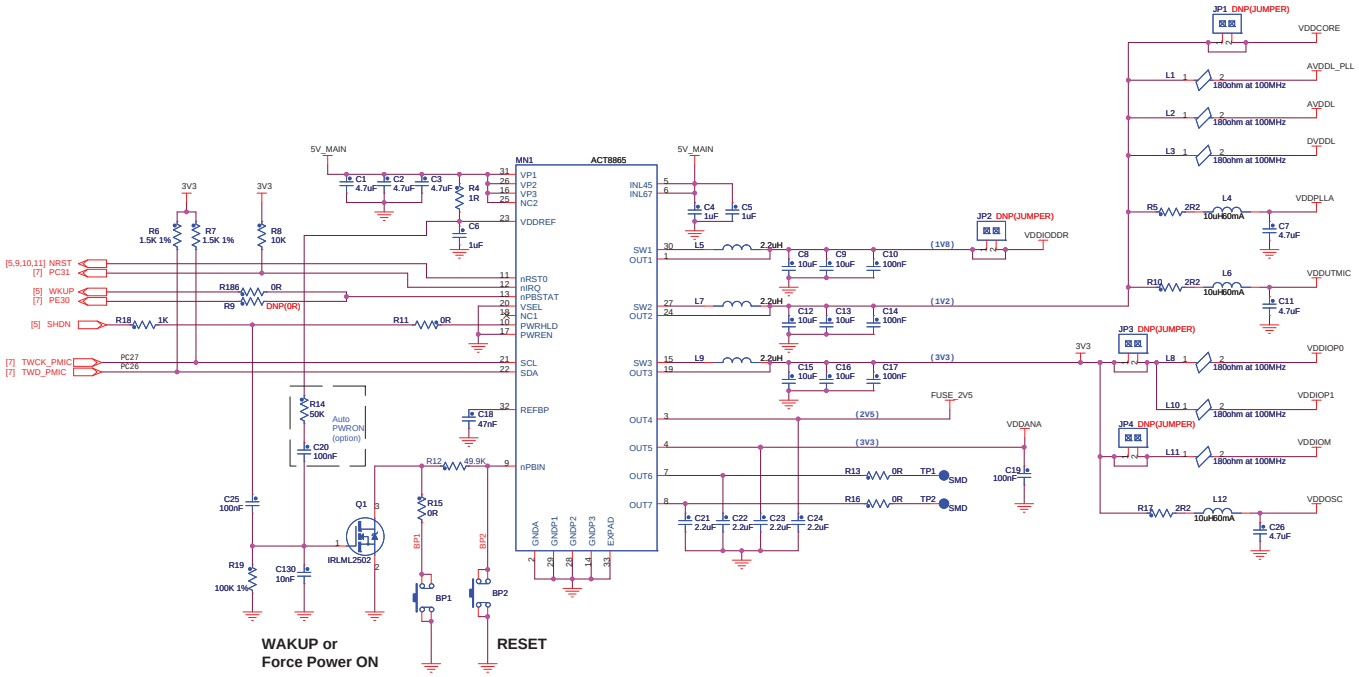
Table 4-3 summarizes the power specifications.

Table 4-3. Supply Group Configuration

Nominal	Name	Power domains	Power source
3.0V	VDDBU	The slow clock oscillator, the internal 32K RC, the internal 12M RC and a part of the system controller	Optional on-board battery
3.3V	VDDIOP0	A part of peripheral I/O lines	PMU
3.3V	VDDIOP1	A part of peripheral I/O lines	
3.3V	VDDUTMII	The three USB interfaces	
3.3V	VDDOSC	The main oscillator cells	
3.3V	VDDANA	The analog-to-digital converter	
1.2V	VDDCORE	The core, including the processor, the embedded memories and the peripherals	
1.2V	VDDUTMIC	The USB UTMI + core	PMU
1.2V	VDDPLLA	The PLLA cell	
1.8V	VDDIODDR	DDR2 interface I/O lines	
1.8V	VDDIOM	NAND, NOR Flash and SMC interface I/O lines	
3.0V to 3.3V	ADVREF	ADC reference voltage	J15 header
2.5V	VDDFUSE	Fuse box for programming	PMU

Note: Jumper footprints are available on board to measure power consumption on main power lines. By default, the jumpers are not implemented. They are short-circuited by a thin PCB wire. To use this functionality, open the short circuit and mount a 2-pin jumper.

Figure 4-3. Board Power Management Schematic



4.2.3.1 Power Options

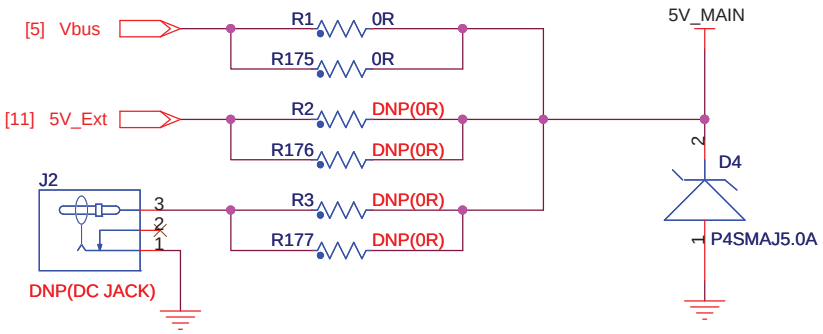
Several power options are available to configure the SAMA5D3 Xplained board powering scheme.

The power sources are selected by a set of 0R resistors.

The USB-powered operation is the default configuration. The power source is the USB device port (J6) connected to a PC or a mini-AB 5V DC supply. The USB supply is sufficient to power the board in most applications if USB host ports are not used. If USB host ports are used, it is recommended to use a DC supply source.

Schematic diagrams of various power options are illustrated in Figure 4-4.

Figure 4-4. Input Powering Scheme Option Schematic



Note: USB-powered operation is a good “single cable” solution because it combines powering and board control through a unique cable. Consequently, it eliminates the need for other wires and batteries. This power option is suitable for most projects that only require 5 volts at up to 500 mA.

4.2.3.2 Mains Power Adapter

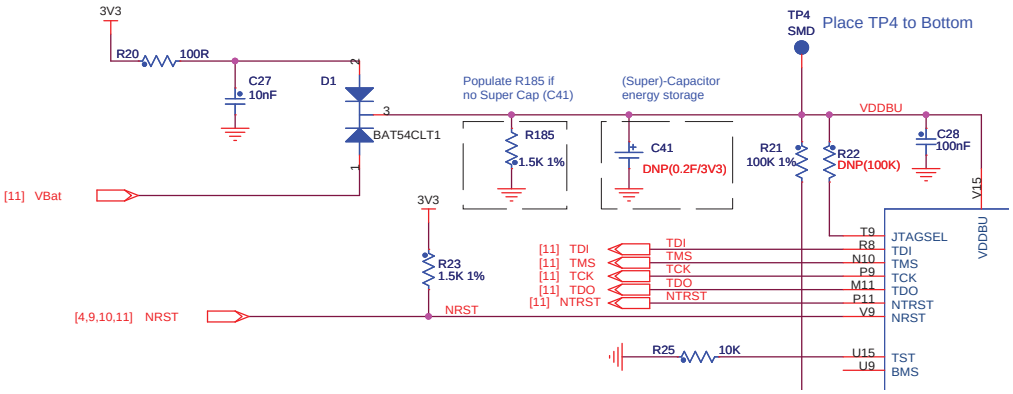
A mains power supply adapter can be used to provide power to the board. A regulated 5V DC supply of typically 2A is required but a current range of 3A is recommended if the USB ports and expansion headers are likely to be used. It needs a 2.1 mm plug with a center-hot configuration.

If you are using the USB host ports or expansion board Arduino shields, a higher current is required. To supply the full 500 mA per port, a mains power adapter must be used.

4.2.3.3 VBAT

By default, VDDBU is delivered through the 3.3V node. An optional SuperCap (C41), used for real-time clock backup, is provided. The board does not come equipped with the SuperCap. When the SuperCap is not installed, an R185 must be installed. You must make sure that the R185 is removed prior to installing the SuperCap.

Figure 4-5. VBAT Powering Scheme Option Schematic



4.2.4 Reset Circuitry

The reset sources for the SAMA5D3 Xplained board are:

- Power-on reset from the Power Management Unit (PMU),
- Reset Pushbutton BP2,
- JTAG reset from an in-circuit emulator (through JTAG interface)

4.2.5 Memory Organization

The SAMA5D3x-series processor features a DDR2/SDRAM memory interface and an External Bus Interface (EBI) to interface with a wide range of external memories and to almost any kind of parallel peripherals.

The memory devices that equip the SAMA5D3 Xplained evaluation kit are as follows:

- Two DDR2/SDRAM (MT47H64M16HR) used as main system memory (256 MByte). The board includes 2 Gbits of on-board soldered DDR2 (double data rate) SDRAM. The footprints can also host two DDR2 (MT47H128M16RT) from Micron® for a total of 512 MBytes of DDR2 memory. The memory bus is 32 bits wide and operates with a frequency of up to 166 MHz (See Figure 4-6).
- One NAND Flash (MT29F2G08ABAEAWP) connected to the processor. The default size is 256 MBytes. The footprint can also host a 4-Gbit Micron chip for a total of 512 MBytes of NAND Flash memory (See Figure 4-7).

Figure 4-6. DDR2 Schematic

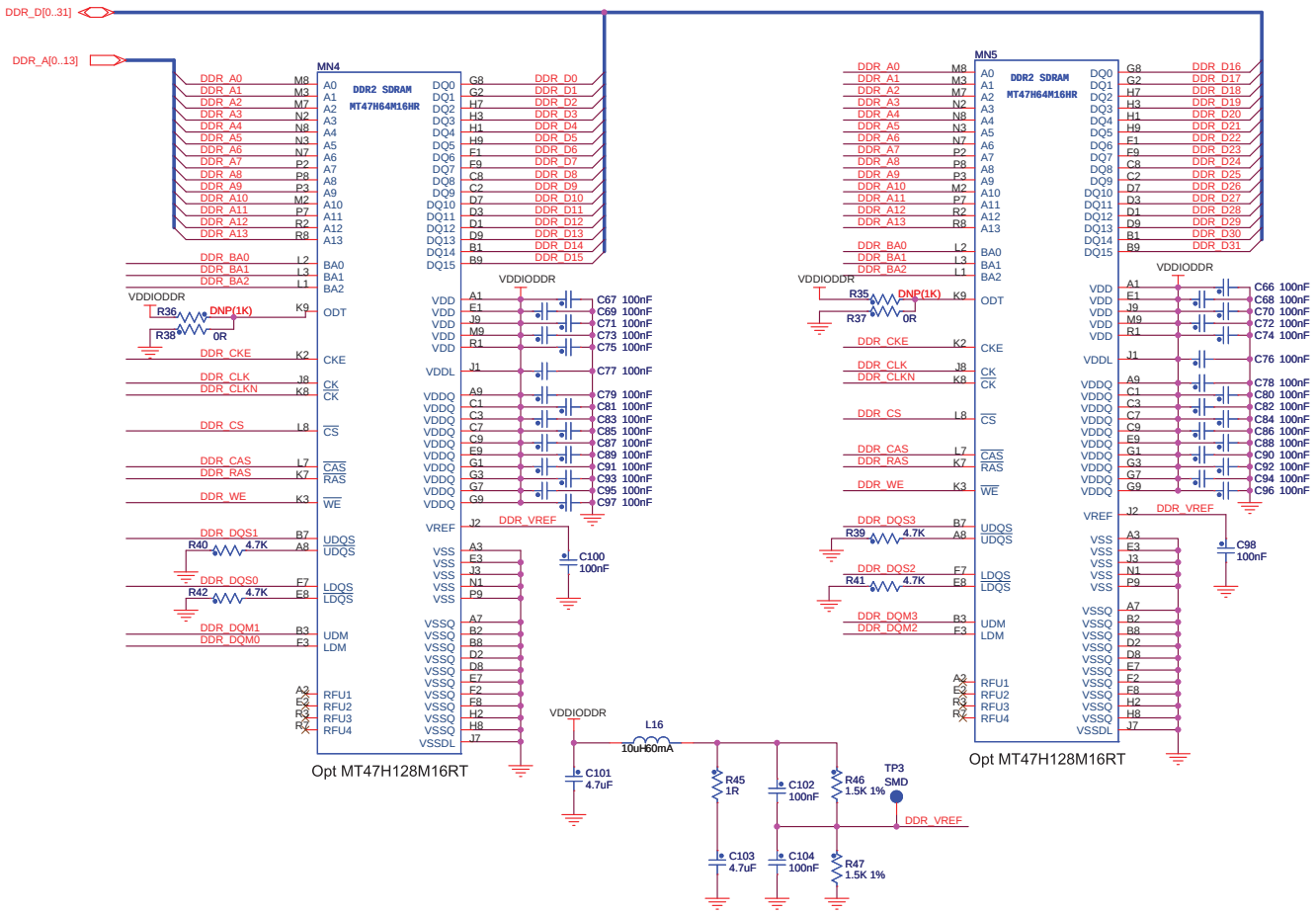
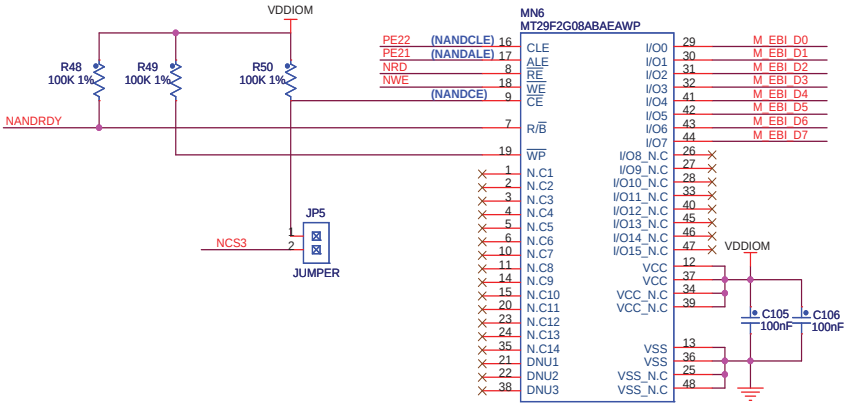


Figure 4-7. NAND Flash Schematic



The following memory part numbers are recommended:

Table 4-4. Recommended Memories

Part Number	Supplier	Size	Type
MT47H128M16	Micron	2 Gb (16 M x 16 x 8 banks)	DDR2 - BGA
MT47H128M32	Micron	4 Gb (32 M x 16 x 8 banks)	DDR2 - BGA
MT29F2G08	Micron	2 Gb	NAND Flash - TSOP
MT29F4G08	Micron	4 Gb	NAND Flash - TSOP

4.2.6 SD/MMC Interface

The SAMA5D3 Xplained board features two high-speed Multimedia Card Interfaces (MCI).

- The first interface is used as an 8-bit interface (MCI0), connected to a SD/MMC card slot (J10) located on the bottom side of the PCB.
- The second interface is used as a 4-bit interface (MCI1), connected to an optional Micro-SD card connector (J11) located on the top side of the PCB.

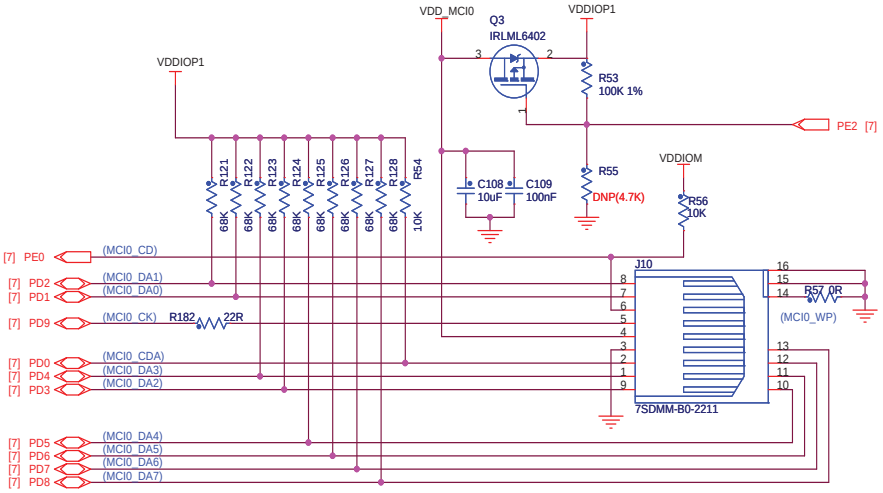
The MCI0 SD card power line is enabled by default. It is PIO-controlled through a MOSFET transistor.

Note: The power source is VCC (3.3 volts).

4.2.6.1 J10 SD Card Slot

When a card is inserted into the SD/MMC connector, the Card Detect pin (PE0) is tied to ground.

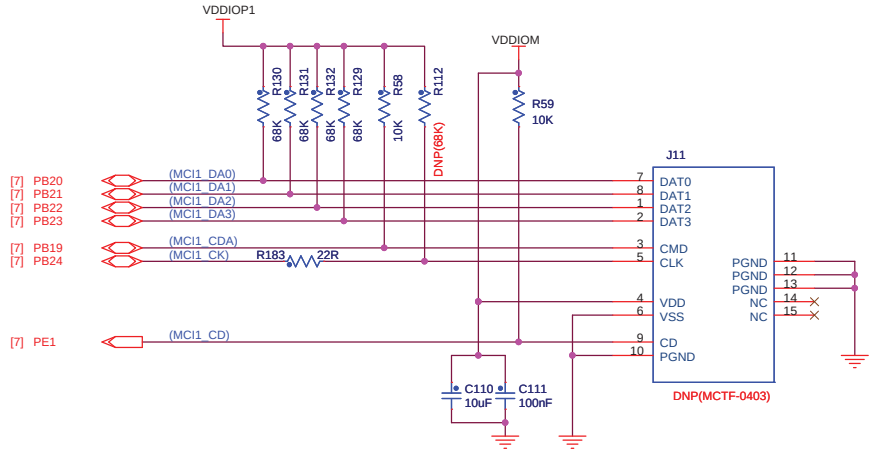
Figure 4-8. J10 SD Card Schematic



4.2.6.2 J11 SD Card Slot (optional)

When a card is inserted into the Micro SD connector, the Card Detect pin is tied to ground. This is detected on pin PE1 of the main processor.

Figure 4-9. J11 Micro SD Card Schematic



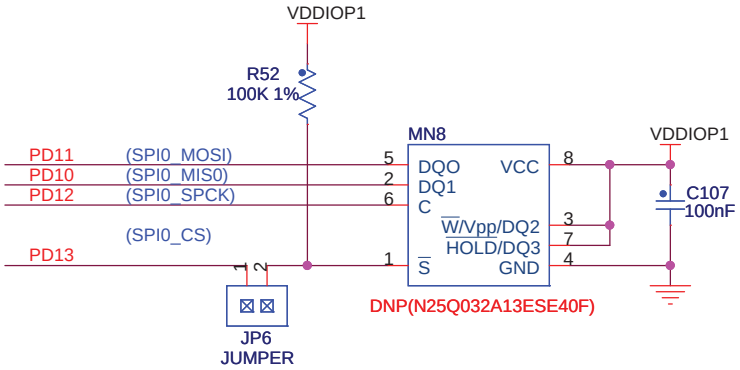
Micro SD CARD INTERFACE - MCI1

4.2.7 Serial Peripheral Interface (SPI)

The SAMA5D3X-series processor features two high-speed Serial Peripheral Interfaces. One port is used to interface with the optional on-board serial DataFlash®.

There are four main signals used in the SPI interface; Clock, Data In, Data Out, and Chip Select.

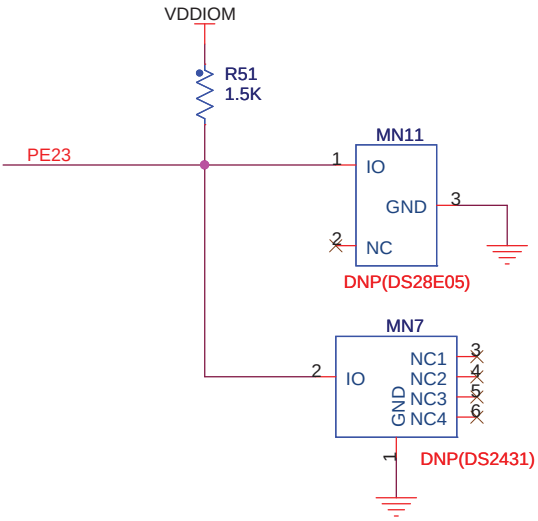
Figure 4-10. Optional Serial DataFlash Schematic



4.2.8 Optional 1-Wire EEPROM

The SAMA5D3 Xplained board can use a 1-Wire device as “soft label” to store data such as chip type, manufacturer’s name, production date, etc.

Figure 4-11. Optional One-Wire EEPROM Schematic



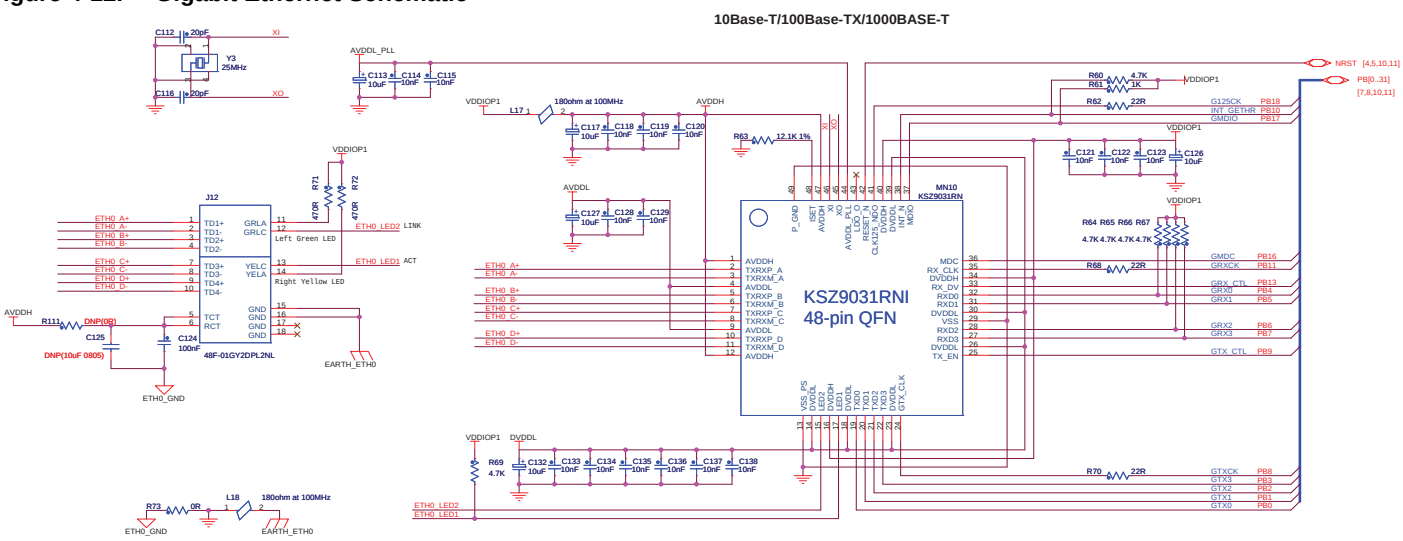
4.2.9 10/100/100 Ethernet Port

The SAMA5D3 Xplained board features a MICREL PHY device (KSZ9031RN) operating at 10/100/1000 Mb/s. The board supports the RGMII interface mode. The Ethernet interface consists of four pairs of low-voltage differential pair signals designated from GRX± and GTX± plus control signals for link activity indicators. These signals are routed to the 10/100/1000 BaseT RJ45 connector (J12).

For monitoring and control purposes, LEDs are integrated in the RJ45 connectors to indicate activity, link, and speed status information for the corresponding ports.

For more information about the Ethernet controller device, refer to the MICREL KSZ9031RN datasheet.

Figure 4-12. Gigabit Ethernet Schematic



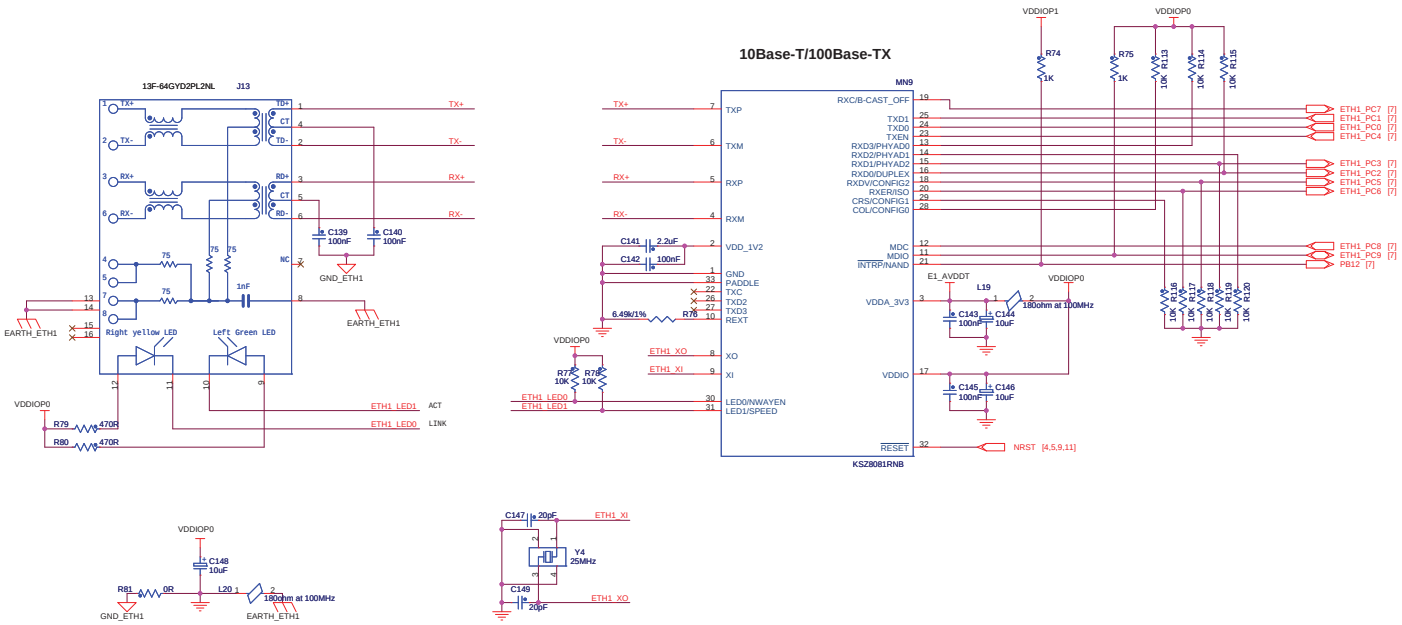
4.2.10 Ethernet 10/100 Port

The SAMA5D3 Xplained board features a MICREL PHY device (KSZ8081RNB) operating at 10/100 Mb/s. The board supports RMII interface modes. The Ethernet interface consists of two pairs of low-voltage differential pair signals designated from GRX± and GTX± plus control signals for link activity indicators. These signals are routed to the 10/100 BaseT RJ45 connector (J13).

For monitoring and control purposes, a LED functionality is added on the RJ45 connectors to indicate activity, link, and speed status information for the corresponding ports.

For more information about the Ethernet controller device, refer to the MICREL KSZ8081RNB controller manufacturer's datasheet.

Figure 4-13. RMII Ethernet Schematic

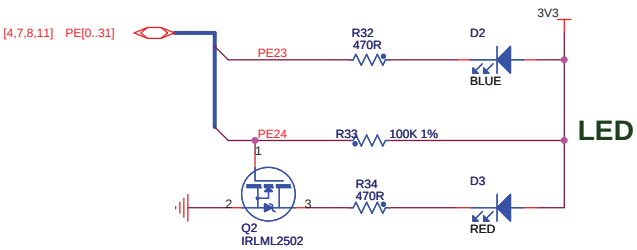


4.2.11 Indicators

Two LEDs are available on the SAMA5D3 Xplained board. Both can be software-controlled by the user.

- The red LED indicates that power is applied to the board (by default). It can be controlled via software.
- The blue LED is mainly controlled by one GPIO line.

Figure 4-14. LED Indicators Schematic



4.2.12 USB

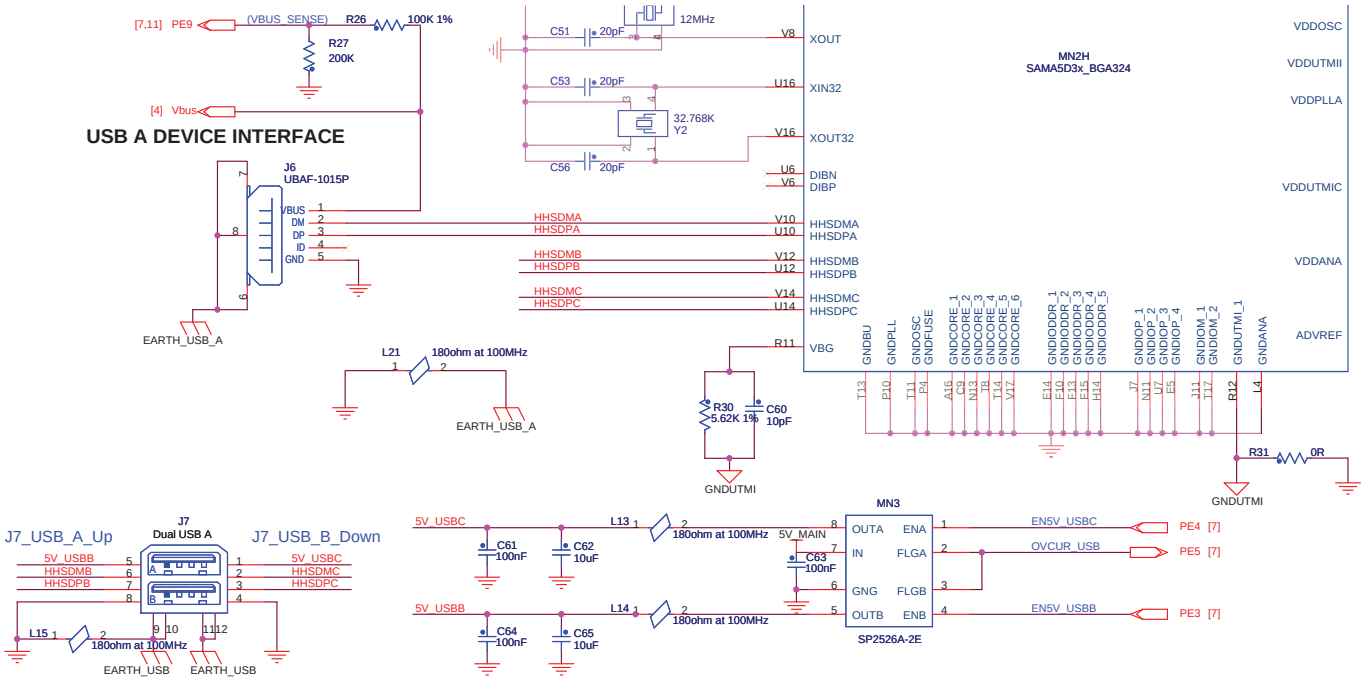
The SAMA5D3 Xplained board features three USB communication ports:

- Port A: High-speed (EHCI) and full-speed (OHCI) host multiplexed with high-speed USB device Micro-AB connector (J6)
- Port B: High-speed (EHCI) and full-speed (OHCI) host, standard type A connector (J7 upper port)
- Port C: Full-speed OHCI host, standard type A connector (J7 lower port)

The two USB host ports are equipped with 500-mA high-side power switch for self-powered and bus-powered applications.

The USB device port A (J6) features a VBUS insert detection function through the ladder-type resistors R26 and R27.

Figure 4-15. USB Interface Schematic

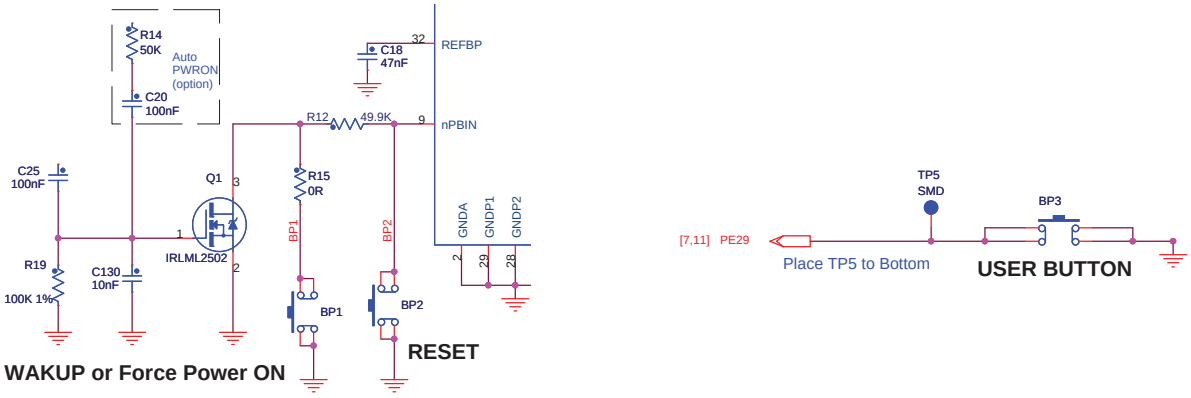


4.2.13 Pushbutton Switches

The following pushbuttons switches are available:

- One board reset button (BP2). When pressed and released, this pushbutton causes a power-on reset of the whole board.
- One wakeup pushbutton that brings the processor out of Low-power mode (BP1)
- One user pushbutton (BP3)

Figure 4-16. Pushbutton Schematic



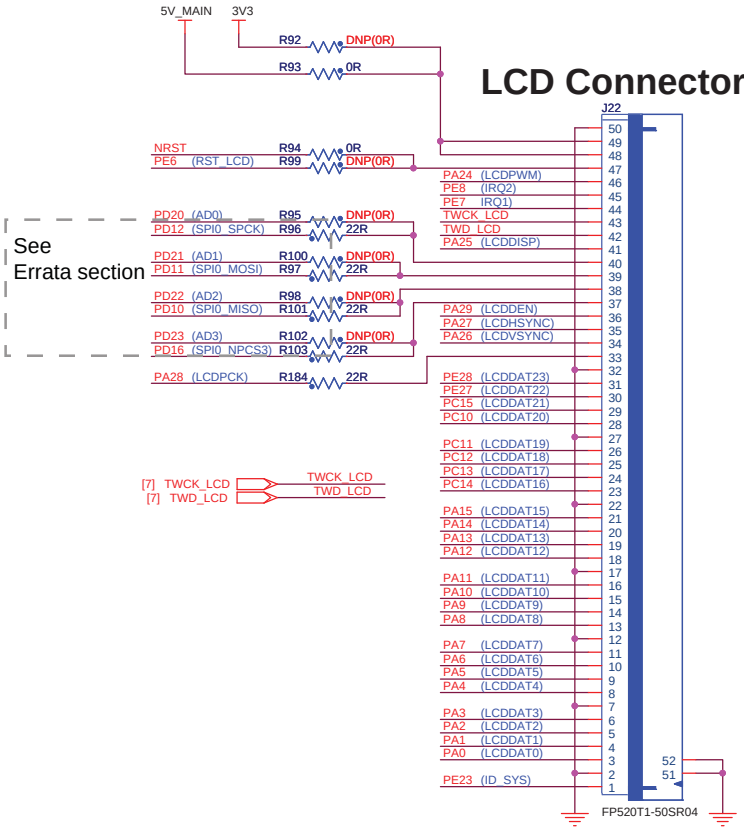
4.2.14 LCD

The SAMA5D36 processor drives 24 bits of data and control signals to the LCD interface. Other signals are used to control the LCD and are also routed to the J22 connector: TWI, SPI, 2 GPIOs for interrupt, ID for 1-Wire EEPROM (ID_SYS) and power supply lines.

4.2.14.1 LCD Connector

One 1.27 mm pitch 50-pin header is provided to gain access to the LCD signals.

Figure 4-17. LCD Expansion Header Interface Schematic



4.2.14.2 LCD Power

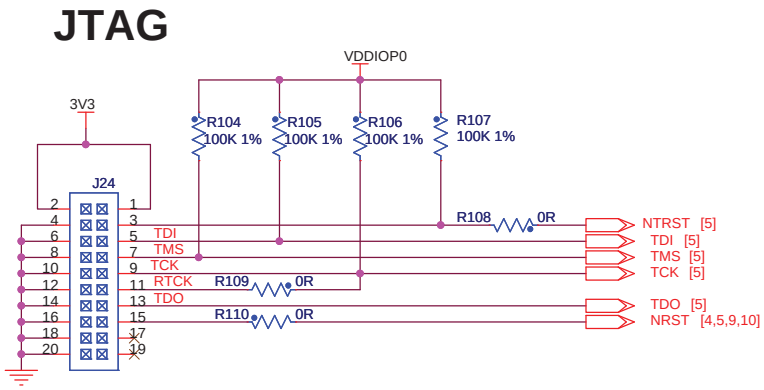
To operate correctly with various LCD modules, regardless of the processor, two voltage lines are available: 3V3 by default and 5V_MAIN, both selected by 0R resistors R92 and R93.

4.2.15 Debug JTAG/ICE and DBGU

4.2.15.1 Debug JTAG/ICE

A 2x10-pin JTAG header is implemented on the SAMA5D3 Xplained board to enable the software development and debugging of the board by using various JTAG emulators. The interface signals have a voltage level of 3.3V.

Figure 4-18. JTAG/ICE Interface Schematic



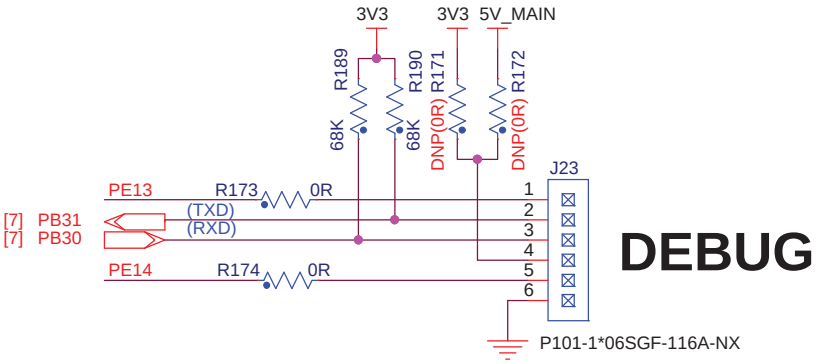
4.2.15.2 DBGU

The SAMA5D3 Xplained board has a dedicated serial port for debugging, which is accessible through the 6-pin male header J23. Various interfaces can be used as USB/Serial DBGU port bridge, such as FTDI TTL-232R-3V3 USB to TTL serial cable or basic breakout board for the 232/USB converter.

These interfaces are available on the following websites:

- Adafruit: http://www.adafruit.com/products/284
- Sparkfun: https://www.sparkfun.com/products/9873

Figure 4-19. DBGU Interface Schematic



R171 and R172 are optional (not implemented) resistors that can be used for power selection. Power can be delivered either by the SAMA5D3 Xplained board or by the debug interface tool. To avoid a contention between your debug interface (e.g. FTDI) and the on-board power system, be careful during the installation of one of this resistor.

4.2.16 Expansion Ports

Five 8-pin, one 10-pin, one 6-pin and one 2x18-pin headers (J14 to J21) are implemented on the board to enable the PIO connection of various expansion cards that could be developed by users or by other sources. Due to

multiplexing, different signals can be provided on each pin. These connectors are mechanically- and footprint-compatible with the Arduino R3 shields. As the SAMA5D3 signals have a voltage level of 3.3V, 5-V level shields must not be used on the SAMA5D3 Xplained.

In addition to its standard IO functionality, the SAMA5D3 processor can provide alternate functions to external IO lines available on the J14 to J21 headers.

These alternate functions are:

- UARTs: UART0, UART1
- USARTs: USART0, USART1, USART2, USART3
- SPI: SPI1
- I²C: TWI0, TWI1
- Timer capture and compare: TIOA, TIOB
- Clock out: PCK0, PCK1, PCK2
- PWMs: PWML0, PWMH0, PWML1, PWMH1
- DIGITAL AUDIO: TD0, TK0, TF0, RD0, RK0, RF0
- ISI: ISI[D0:D11], ISI_HSYNC, ISI_VSYNC, ISI_PCK
- CAN: CAN-RX0, CANTX0, CANRX1, CAN_TX1
- Analog: AD[0:11], ADTRG, ADREF
- GPIO: MISC
- RESET
- VBAT

Refer to the SAMA5D3 series datasheet for further details on the PIO multiplexing and alternate function selection.

4.2.16.1 Functions Available Through the Arduino Headers

The following tables illustrate the functionalities provided by the SAMA5D3 Xplained board. They show the pins used to implement each functionality.

Note: Some pins are multiplexed for different functionalities, which means that only one at a time can be active for each pin.

Table 4-5. Function by PIO (Part 1)

PIO NAME	PCK	ISI	SSC	CAN	SPI
PC16	--	--	TK0	--	--
PC17	--	--	TF0	--	--
PC18	--	--	TD0	--	--
PC20/PD28	--	--	RF0	--	--
PC21/PD29	--	--	RD0	--	--
PC19/PD30	PCK0	--	RK0	--	--
PD30/PC15	PCK0/PCK2	--	--	--	--
PD31	PCK1	--	--	--	--
PB14	--	--	--	CANRX1	--
PD14	--	--	--	CANRX0	--
PB15	--	--	--	CANTX1	--
PD15	--	--	--	CANTX0	--
PC22/PC1	--	--	--	--	SPI1_MISO
PC24/PC0	--	--	--	--	SPI1_SPCK
PC23/PC2	--	--	--	--	SPI1_MOSI
PC25	--	--	--	--	SPI1_NPCS0
PC26/PA30	--	ISI_D11/VSYNC	--	--	SPI1_NPCS1
PC27/PA31	--	ISI_D10/HSYNC	--	--	SPI1_NPCS2
PC28	--	ISI_D9	--	--	SPI1_NPCS3
PC29	--	ISI_D8	--	--	--
PA23	--	ISI_D7	--	--	--
PA22	--	ISI_D6	--	--	--
PA21	--	ISI_D5	--	--	--
PA20	--	ISI_D4	--	--	--
PA19	--	ISI_D3	--	--	--
PA18	--	ISI_D2	--	--	--
PA17	--	ISI_D1	--	--	--
PA16	--	ISI_D0	--	--	--
PC30	--	ISI_PCK	--	--	--
PA30	--	ISI_VSYNC	--	--	--
PA31	--	ISI_HSYNC	--	--	--

Table 4-6. Function by PIO (Part 2)

PIO NAME	TWI	UART/USART	ANALOG	MISC
3V3/5V	--	--	--	3V3/5V
nRTS	--	--	--	nRTS
GND	--	--	--	GND
AREF	--	--	AREF	--
5V	--	--	--	5V
PC18	--	--	AD0	--
PD21	--	--	AD1	--
PD22	--	--	AD2	--
PD23	--	--	AD3	--
PD24	--	--	AD4	--
PD25	--	--	AD5	--
PD26	--	--	AD6	--
PD27	--	--	AD7	--
PC20/PD28	--	--	AD8	--
PC21/PD29	--	--	AD9	--
PC19/PD30	--	--	AD10	--
PD31	--	--	AD11	--
PD19/PB15	--	--	ADTRG	--
PA19	TWCK2	--	--	--
PA18	TWD2	--	--	--
PC26	TWD1	--	--	--
PA30	TWD0	URXD1	--	--
PA31	TWCK0	UTXD1	--	--
PC26/PA30	TWD0/TWD1	URXD1	--	--
PC27/PA31	TWCK0/TWCK1	URTD1	--	--
PC30	--	UTXD0	--	--
PC29	--	URXD0	--	PWMFI2
PD14	--	SCK0	--	--
PD15	--	CTS0	--	--
PD18	--	TXD0	--	--
PD17	--	RXD0	--	--
PB25	--	SCK1	--	--
PB26	--	CTS1	--	--
PB29	--	TXD1	--	--
PB28	--	RXD1	--	--
PB27	--	RTS1	--	PWMH1

Table 4-6. Function by PIO (Part 2) (Continued)

PIO NAME	TWI	UART/USART	ANALOG	MISC
PE20	--	SCK2	--	--
PE23	--	CTS2	--	--
PE26	--	TXD2	--	--
PE25	--	RXD2	--	--
PE24	--	RTS2	--	--
PE15	--	SCK3	--	--
PE16	--	CTS3	--	--
PE19	--	TXD3	--	--
PE18	--	RXD3	--	--
PE17	--	RTS3	--	--
PC22/PC1	--	--	--	GPIO
PC23/PC2	--	--	--	GPIO
PC24/PC0	--	--	--	GPIO
PC9	--	--	--	GPIO
PE9	--	--	--	GPIO
PE10	--	--	--	GPIO
PE11	--	--	--	GPIO
PE12	--	--	--	GPIO
PE16	--	--	--	GPIO
PE31	--	--	--	IRQ/PWML1
PC28	--	--	--	PWMFI0
PA20	--	--	--	PWMH0
PA22	--	--	--	PWMH1
PA21	--	--	--	PWML0
PA23	--	--	--	PWML1
PE29	--	--	--	TCLK2
PC5	--	--	--	TCLK4
PC8	--	--	--	TCLK5
PC3	--	--	--	TIOA4
PC6	--	--	--	TIOA5
PC4	--	--	--	TIOB4
PC7	--	--	--	TIOB5

4.2.16.2 J15 Header

Figure 4-20. J15 Header

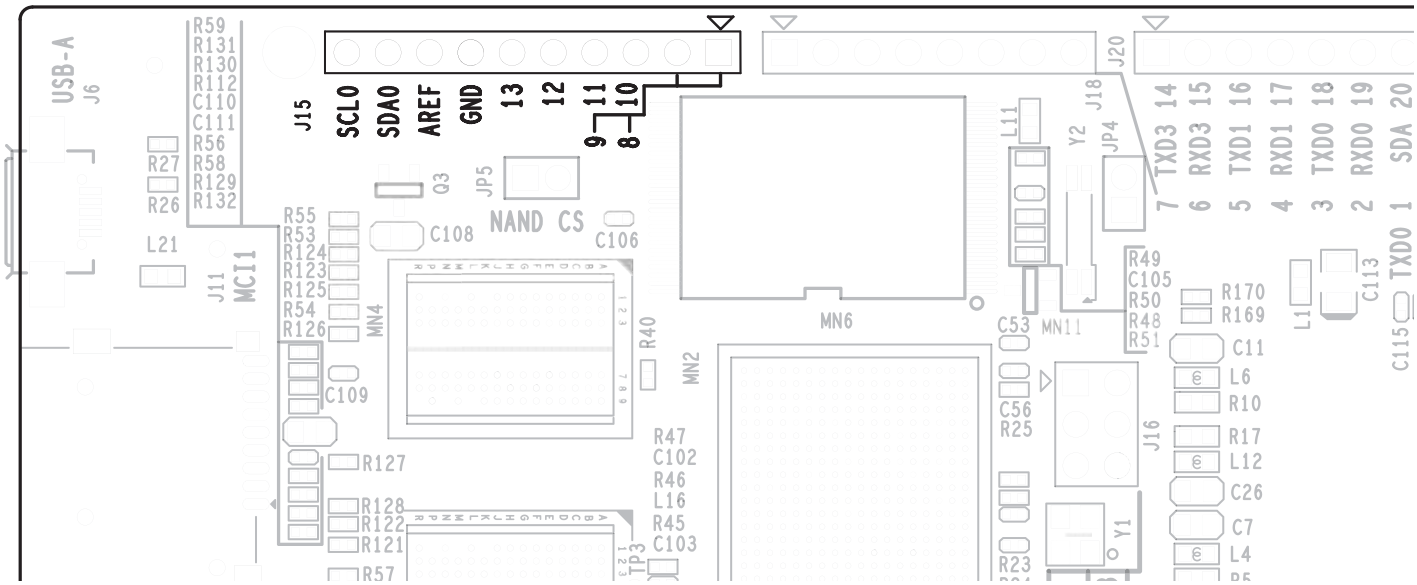


Table 4-7. J15 Header IOs

Silkscreen	PIO	Function 1	Function 2	Function 3	PIO	Function 4	Function 5
SCL0	PA31	TWCK0	UTXD1	ISI_HSYNC	--	--	--
SDA0	PA30	TWD0	URXD1	ISI_VSYNC	--	--	--
ARFE	--	--	--	--	--	--	--
GND	--	--	--	--	--	--	--
13	PC24	SPI1_SPCK	--	--	PC0	ETX0	TIOA3
12	PC22	SPI1_MISO	--	--	PC1	ETX1	TIOB3
11	PC23	SPI1_MOSI	--	--	PC2	ERX0	TCLK3
10	PC25	SPI1_NPCS0	--	--	--	--	--
9	PC3	ERX1	TIOA4	--	--	--	--
8	PC4	ETXEN	TIOB4	--	--	--	--

4.2.16.3 J18 Header

Figure 4-21. J18 Header

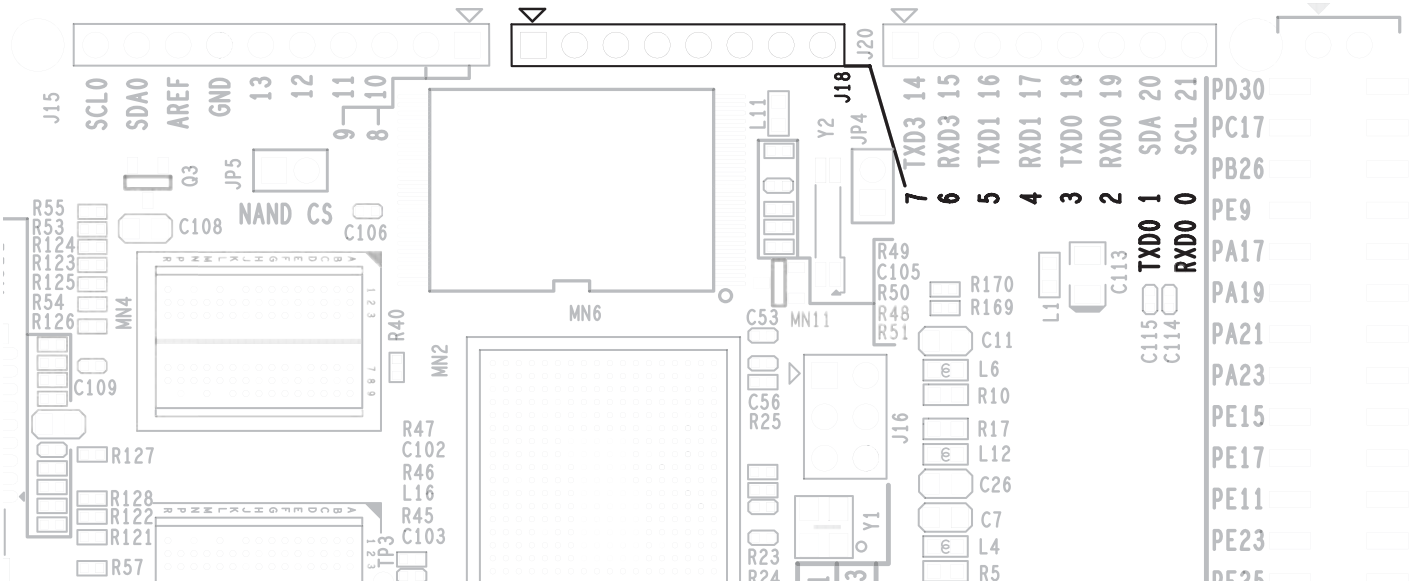


Table 4-8. J18 Header IOs

Silkscreen	PIO	Function 1	Function 2	Function 3
7	PC5	ECRSDV	TCLK4	--
6	PC6	ERXER	TIOA5	--
5	PC7	EREFCK	TIOB5	--
4	PC28	SPI1_NPCS3	PWMFI0	ISI_D9
3	PC8	EMDC	TCLK5	--
2	PC9	EMDIO	--	--
1	PC30	UTXD0	ISI_PCK	--
0	PC29	URXD0	PWMFI2	ISI_D8

4.2.16.4 J20 Header

Figure 4-22. J20 Header

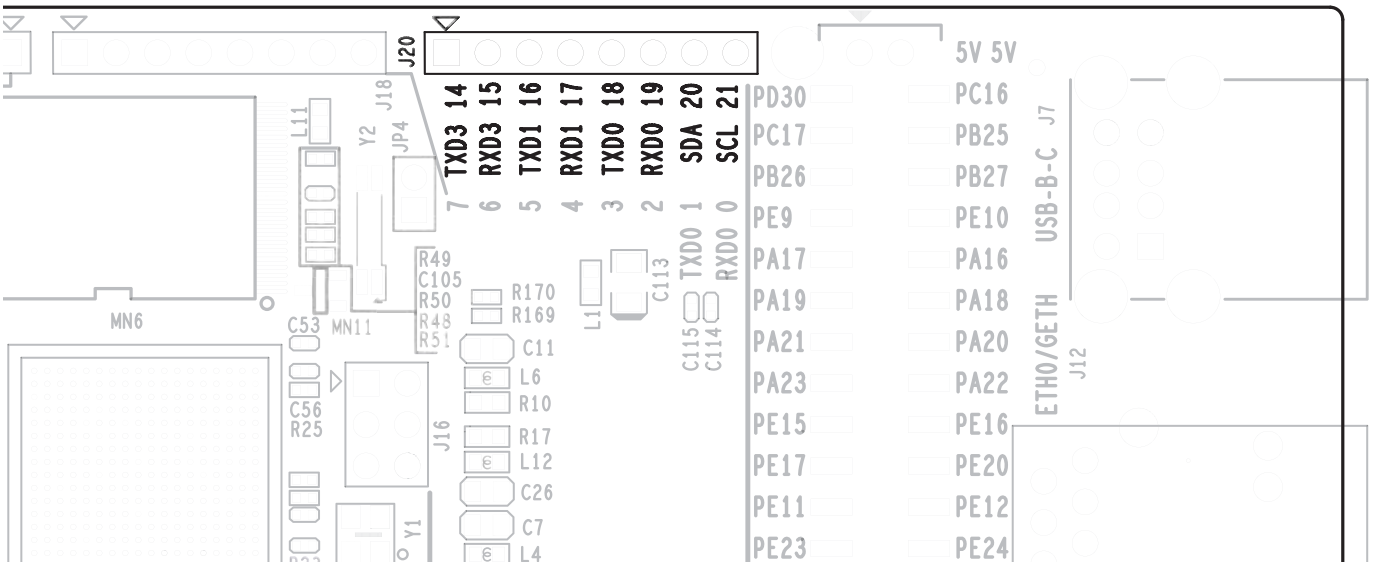


Table 4-9. J20 Header IOs

Silkscreen	PIO	Function 1	Function 2	Function 3	PIO	Function 4	Function 5	Function 6
TXD3 14	PE19	A19	TXD3	--	--	--	--	--
RXD3 15	PE18	A18	RXD3	--	--	--	--	--
TXD1 16	PB29	TXD1	--	--	--	--	--	--
RXD1 17	PB28	RXD1	--	--	--	--	--	--
TXD0 18	PD18	TXD0	--	--	--	--	--	--
RXD0 19	PD17	RXD0	--	--	--	--	--	--
SDA 20	PC26	SPI1_NPCS1	TXWD1	ISI_D11	PA30	TWD0	URXD1	ISI_VSYNC
SCL 21	PC27	SPI1_NPCS2	TWCK1	ISI_D10	PA31	TWCK0	UTXD1	ISI_HSYNC

4.2.16.5 J19 Header

Figure 4-23. J19 Header

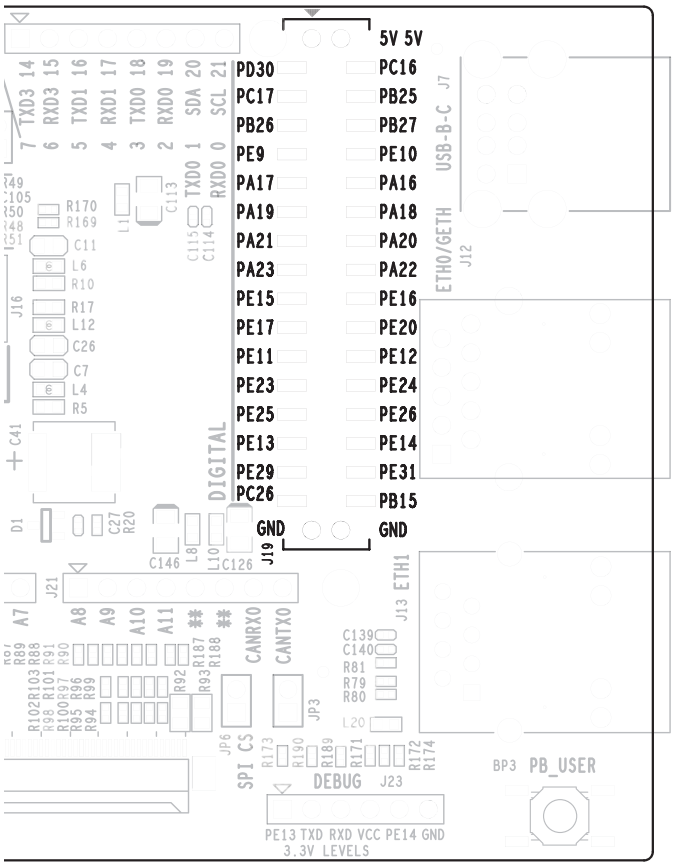


Table 4-10. J19 Header IOs

Silkscreen	PIO	Function 1	Function 2	Function 3	PIO	Function 4	Function 5
PD30	PD30	AD10	PCK0	--	PC15	PCI2_CK	PCK2
PC17	PC17	TF0	--	--	--	--	--
PB26	PB26	CTS1	GRX7	--	--	--	--
PE9	PE9	A9	--	--	--	--	--
PA17	PA17	LCDDAT17	ISI_D1	--	--	--	--
PA19	PA19	LCDDAT19	TWCk2	ISI_D3	--	--	--
PA21	PA21	LCDDAT21	PWML0	ISI_D5	--	--	--
PA23	PA23	LCDDAT23	PWML1	ISI_D7	--	--	--
PE15	PE15	A15	SCK3	--	--	--	--
PE17	PE17	A17	RTS3	--	--	--	--
PE11	PE11	A11	--	--	--	--	--
PE23	PE23	A23	CTS2	--	--	--	--
PE25	PE25	A25	RXD2	--	--	--	--
PE13	PE13	A13	--	--	--	--	--

Table 4-10. J19 Header IOs (Continued)

Silkscreen	PIO	Function 1	Function 2	Function 3	PIO	Function 4	Function 5
PE29	PE29	NWR1/NBS1	TCLK2	--	--	--	--
PC26	PC26	SPI1_NPCS1	TXWD1	ISI_D11	--	--	--
PC16	PC16	TK0	--	--	--	--	--
PB25	PB25	SCK1	GRX6	--	--	--	--
PB27	PB27	RTS1	PWMH1	--	--	--	--
PE10	PE10	A10	--	--	--	--	--
PA16	PA16	LCDDAT16	ISI_D0	--	--	--	--
PA18	PA18	LCDDAT18	TWD2	ISI_D2	--	--	--
PA20	PA20	LCDDAT20	PWMH0	ISI_D4	--	--	--
PA22	PA22	LCDDAT22	PWMH1	ISI_D6	--	--	--
PE16	PE16	A16	CTS3	--	--	--	--
PE20	PE20	A20	SCK2	--	--	--	--
PE12	PE12	A12	--	--	--	--	--
PE24	PE24	A24	RTS2	--	--	--	--
PE26	PE26	NCS0	TXD2	--	--	--	--
PE14	PE14	A14	--	--	--	--	--
PE31	PE31	IRQ	PWML1	--	--	--	--
PB15	PB15	GCOL	CANTX1	--	--	--	--

4.2.16.6 J16 Header

Figure 4-24. J16 Header

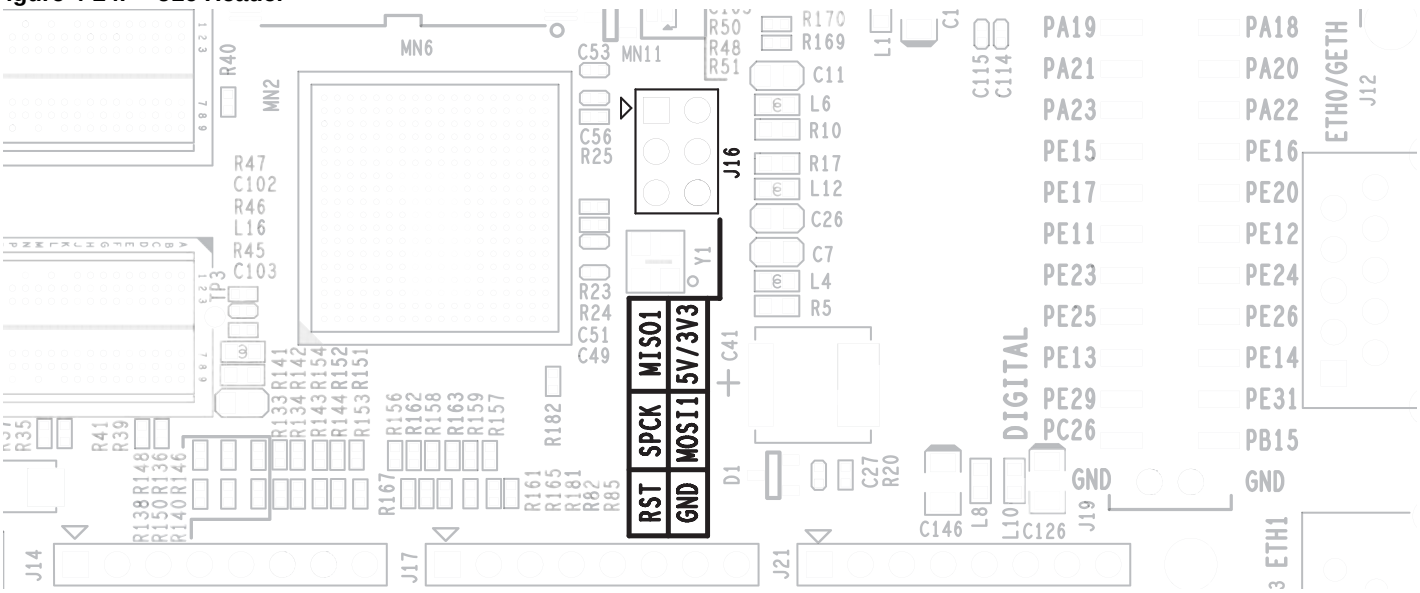


Table 4-11. J16 Header IOs

Silkscreen	PIO	Function 1
MISO1	PC22	SPI1_MISO
5V/3V3	--	Power supply
SPCK	PC24	SPI1_SPCK
MOSI1	PC23	SPI1_MOSI
RST	NRST	System reset
GND	--	Power ground

4.2.16.7 J14 Header

Figure 4-25. J14 Header Position

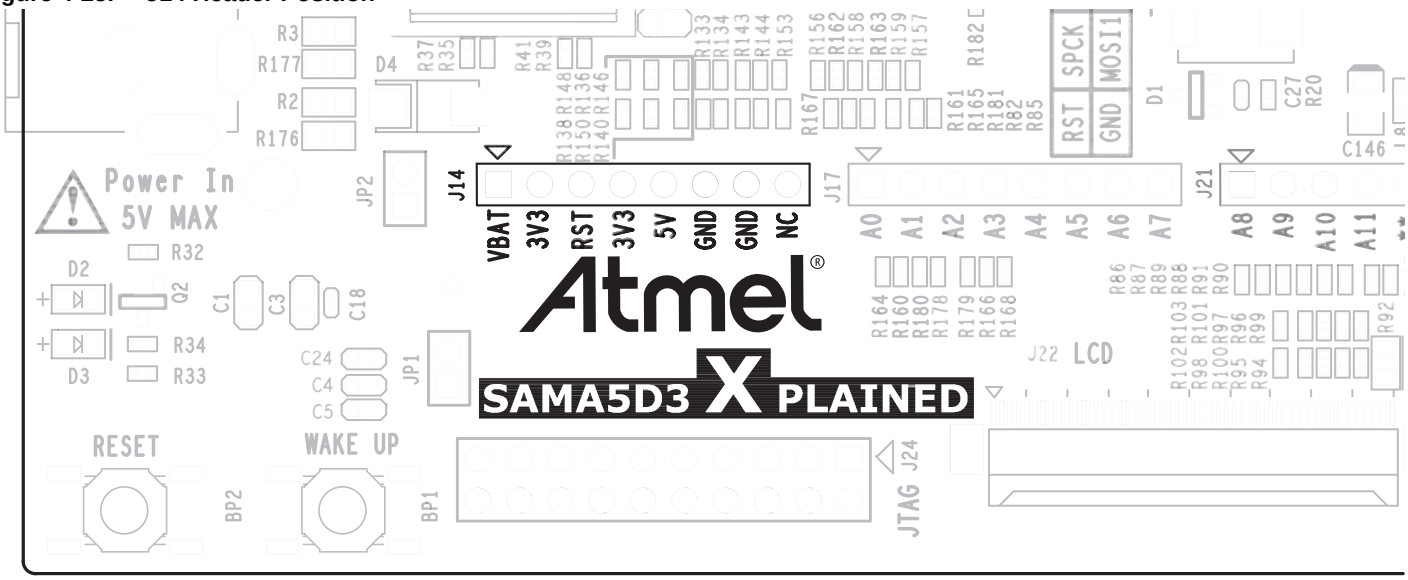


Table 4-12. J14 Header IOs

Silkscreen	Function
VBAT	VBAT supply
3V3	AREF. Reference voltage for the analog inputs of the SAMA5D36 processor.
RST	System reset
3V3	Main 3.3V supply - generated by the on-board regulator. Maximum sourced current is 1.2A. This regulator also provides the power supply to the SAMA5D36 microcontroller and components.
5V	Main 5.0V supply
GND	System ground
GND	System ground
NC	Not connected

4.2.16.8 J17 Header

Figure 4-26. J17 Header

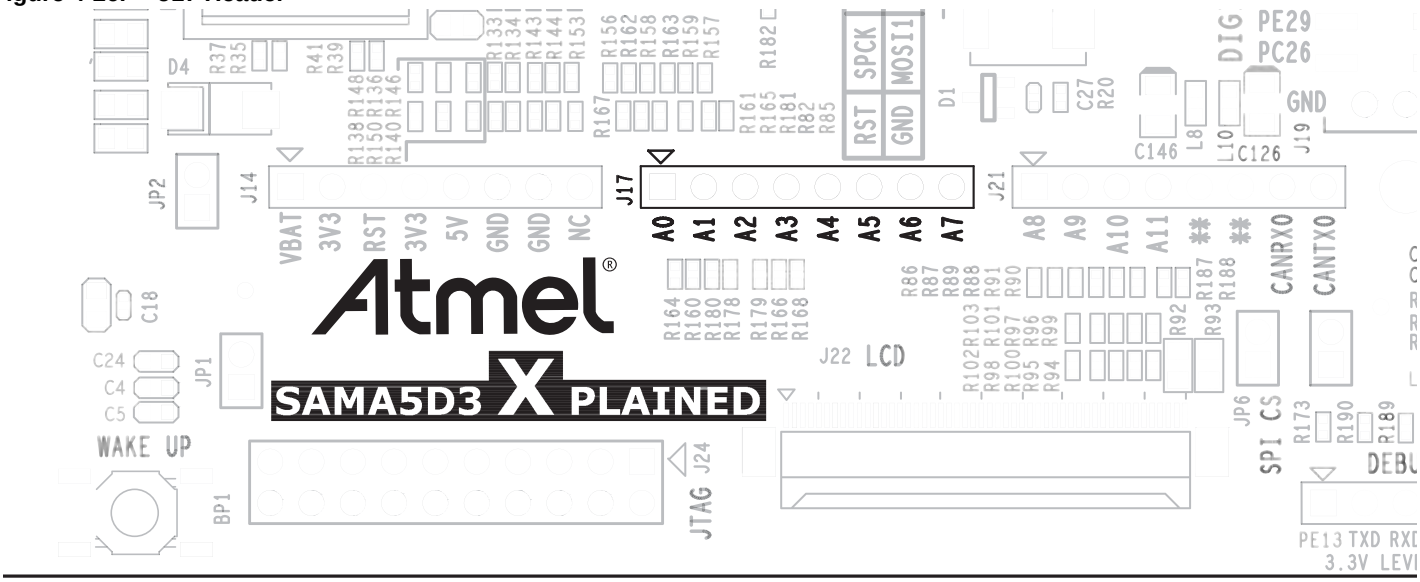


Table 4-13. J17 Header IOs

Silkscreen	PIO	Function 1	Function 2	Function 3	PIO	Function 4	Function 5
A0	PC18	TD0	--	--	PD20	AD0	--
A1	PD21	AD1	--	--	--	--	--
A2	PD22	AD2	--	--	--	--	--
A3	PD23	AD3	--	--	--	--	--
A4	PD24	AD4	--	--	--	--	--
A5	PD25	AD5	--	--	--	--	--
A6	PD26	AD6	--	--	--	--	--
A7	PD27	AD7	--	--	--	--	--

4.2.16.9 J21 Header

Figure 4-27. J21 Header

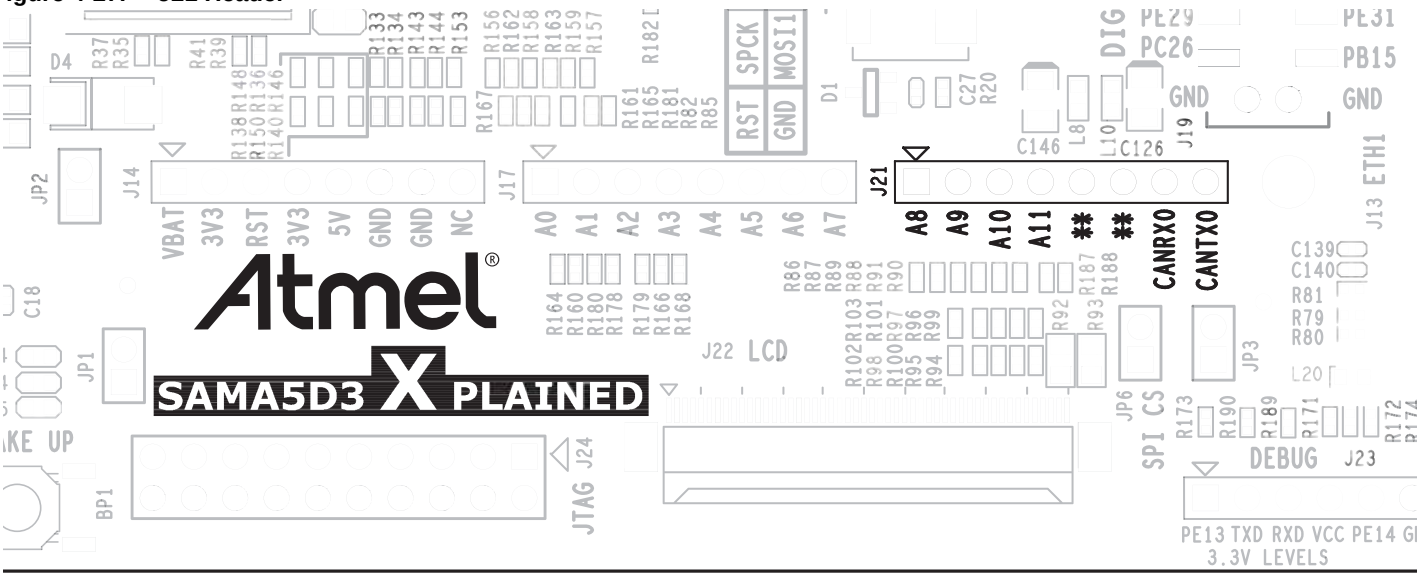


Table 4-14. J21 Header IO

Silkscreen	PIO	Function 1	Function 2	Function 3	PIO	Function 4	Function 5
A8	PC20	RF0	--	--	PD28	AD8	--
A9	PC21	RD0	--	--	PD29	AD9	--
A10	PC19	RK0	--	--	PD30	AD10	PCK0
A11	PD31	PCK1	--	--	--	--	--
**	PB14	GCRS	CANRX1	--	--	--	--
**	PD19	ADTRG	--	--	PB15	GCOL	CANTX1
CANRX0	PD14	SCK0	SPO_NPCS1	CANRX0	--	--	--
CANTX0	PD15	CTS0	SPI0_NPCS2	CANTX0	--	--	--

4.3 Other Connector Details and PIO Usage Summary

4.3.1 Power Supply

Figure 4-28. Power Supply Connector J2 (Optional)

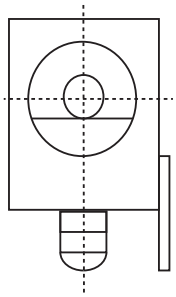


Table 4-15. Power Supply Connector J2 Signal Description

Pin	Mnemonic	Signal Description
1	Center	+5V
2	--	GND
3	--	Floating

4.3.2 JTAG/ICE Connector

Figure 4-29. JTAG port J24

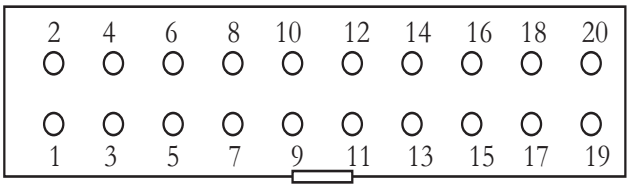


Table 4-16. JTAG/ICE Connector J24 Signal Descriptions

Pin	Mnemonic	Signal Description
1	VTref 3.3V power	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators, and to control the output logic levels to the target. It is normally fed from VDD on the target board and must not have a series resistor.
2	Vsupply 3.3V power	This pin is not connected in SAM-ICE™. It is reserved for compatibility with other equipment. Connect to VDD or leave open in target system.
3	nTRST Target Reset - Active-low output signal that resets the target.	JTAG Reset. Output from SAM-ICE to the reset signal on the target JTAG port. Typically connected to nTRST on the target CPU. This pin is normally pulled High on the target to avoid unintentional resets when there is no connection.
4	GND	Common ground.

Table 4-16. JTAG/ICE Connector J24 Signal Descriptions (Continued)

Pin	Mnemonic	Signal Description
5	TDI Test Data Input - Serial data output line, sampled on the rising edge of the TCK signal.	JTAG data input of target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TDI on target CPU.
6	GND	Common ground.
7	TMS Test Mode Select.	JTAG mode set input of target CPU. This pin should be pulled up on the target. Typically connected to TMS on target CPU. Output signal that sequences the target's JTAG state machine, sampled on the rising edge of the TCK signal.
8	GND	Common ground.
9	TCK Test Clock - Output timing signal, for synchronizing test logic and control register access.	JTAG clock signal to target CPU. It is recommended that this pin is pulled to a defined state on the target board. Typically connected to TCK on target CPU.
10	GND	Common ground.
11	RTCK - Input Return Test Clock signal from the target.	Some targets must synchronize the JTAG inputs to internal clocks. To fulfill this requirement, a returned and resynchronized TCK can be used to dynamically control the TCK rate. SAM-ICE supports adaptive clocking which waits for TCK changes to be echoed correctly before making further changes. Connect to RTCK if available, otherwise to GND.
12	GND	Common ground.
13	TDO JTAG Test Data Output - Serial data input from the target.	JTAG data output from target CPU. Typically connected to TDO on target CPU.
14	GND	Common ground
15	nSRST RESET	Active-low reset signal. Target CPU reset signal.
16	GND	Common ground
17	RFU	This pin is not connected.
18	GND	Common ground
19	RFU	This pin is not connected.
20	GND	Common ground

4.3.3 USB Type A Dual Port

Figure 4-30. USB Type A Dual Port J19

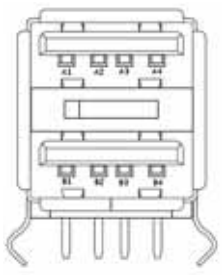


Table 4-17. USB Type A Dual Port J19 Signal Descriptions

Pin	Mnemonic	Signal Description
A1	Vbus - USB_A	5V power
A2	DM - USB_A	Data minus
A3	DP - USB_A	Data plus
A4	GND	Common ground
B1	Vbus - USB_A	5V power
B2	DM - USB_A	Data minus
B3	DP - USB_A	Data plus
B4	GND	Common ground
Mechanical pins	--	Shield

4.3.4 USB Micro-AB

Figure 4-31. USB Host/Device Micro-AB Connector J6

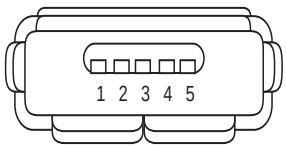


Table 4-18. USB Device Micro-AB Connector J6 Signal Descriptions

Pin	Mnemonic	Signal Description
1	Vbus	5V power
2	DM	Data minus
3	DP	Data plus
4	ID	On-the-go identification
5	GND	Common ground

4.3.5 DEBUG Connector

Figure 4-32. DEBUG Connector J23

Table 4-19. DEBUG Connector J23 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	--	PE13	--
2	TXD (transmitted data)	PB31	RS232 serial data input signal
3	RXD (transmitted data)	PB30	RS232 serial data output signal
4	--	--	Power line (5V/3V3)
5	--	PE14	--
6	GND	--	Common ground

4.3.6 SD/MMC Plus MCI0

Figure 4-33. SD/MMC Socket J10

Table 4-20. SD/MMC Socket J10 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	DAT3	PD4	Data bit
2	CMD	PD0	Command line
3	VSS	--	Command line
4	VCC	--	Supply voltage 3.3V
5	CLK	PD9	Clock / command line
6	CD	PE0	Card detect
7	DAT0	PD1	Data bit
8	DAT1	PD2	Data bit
9	DAT2	PD3	Data bit
10	DAT4	PD5	Data bit
11	DAT5	PD6	Data bit
12	DAT6	PD7	Data bit
13	DAT7	PD8	Data bit

Table 4-20. SD/MMC Socket J10 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
14	WP	R57	Protect
15	VSS	--	Common ground
16	VSS	--	Common ground

4.3.7 MicroSD MCI1

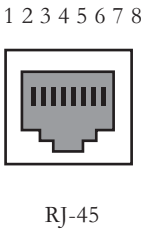
Figure 4-34. MicroSD Socket J11

Table 4-21. MicroSD Socket J11 Signal Descriptions

Pin	Mnemonic	PIO	Signal Description
1	DAT2	PB22	Data bit 2
2	CD/DAT3	PB23	Card detect / data bit 3
3	CMD	PB19	Command line
4	VCC	--	Supply voltage 3.3V
5	CLK	PB24	Clock / command line
6	VSS	--	Common ground
7	DAT0	PB20	Data bit 0
8	DAT1	PB21	Data bit 1
9	SW1	--	Not used, grounded
10	CARD DETECT	PE1	Card detect

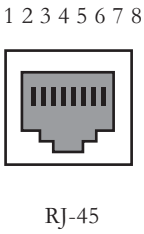
4.3.8 Gigabit Ethernet ETH0 RJ45 Socket J12

Figure 4-35. Gigabit Ethernet RJ45 Socket J12



4.3.9 Ethernet ETH1 RJ45 Socket J13

Figure 4-36. Ethernet RJ45 Socket J13



4.3.10 LCD Socket J22

Figure 4-37. LCD Socket J22

Table 4-22. LCD Socket J22 Signal Descriptions

PIN	Signal	Display Module Interface Function	MCU Interface Function
1	ID_SYS	Extension module identification (connected to 1-wire EEPROM available on LCD display module)	Extension module identification
2	GND	GND	GND
3	D0	Data line	Data line
4	D1	Data line	Data line
5	D2	Data line	Data line
6	D3	Data line	Data line
7	GND	GND	GND
8	D4	Data line	Data line
9	D5	Data line	Data line
10	D6	Data line	Data line
11	D7	Data line	Data line
12	GND	GND	GND
13	D8	Data line	Data line
14	D9	Data line	Data line
15	D10	Data line	Data line
16	D11	Data line	Data line
17	GND	GND	GND
18	D12	Data line	Data line

Table 4-22. LCD Socket J22 Signal Descriptions (Continued)

PIN	Signal	Display Module Interface Function	MCU Interface Function
19	D13	Data line	Data line
20	D14	Data line	Data line
21	D15	Data line	Data line
22	GND	GND	GND
23	D16	Data line	Data line
24	D17	Data line	Data line
25	D18	Data line	Data line
26	D19	Data line	Data line
27	GND	GND	GND
28	D20	Data line	Data line
29	D21	Data line	Data line
30	D22	Data line	Data line
31	D23	Data line	Data line
32	GND	GND	GND
33	PCLK	Pixel clock	--
34	VSYNC/CS	Vertical sync	Chip select
35	HSYNC/WE	Horizontal sync	Write enable
36	DATA_ENABLE/ RE	Data enable	Read enable
37 (1)	SPI_SCK (1)	--	SPI_SCK (1)
38 (1)	SPI_MOSI (1)	--	SPI_MOSI (1)
39 (1)	SPI_MISO (1)	--	SPI_MISO (1)
40 (1)	SPI_CS (1)	--	SPI_CS (1)
41	ENABLE	Display enable signal	Display enable signal
42	TWI_SDA	I2C data line (maXTouch®)	I2C data line (maXTouch)
43	TWI_SCL	I2C clock line (maXTouch)	I2C clock line (maXTouch)
44	IRQ1	maXTouch interrupt line	maXTouch interrupt line
45	IRQ2	Interrupt line for other I2C devices	Interrupt line for other I2C devices
46	PWM	Backlight control	Backlight control
47	RESET	Reset for both display and maXTouch	Reset for both display and maXTouch
48	VCC	3.3V or 5V supply (0R)	3.3V supply
49	VCC	3.3V or 5V supply (0R)	3.3V supply
50	GND	GND	GND

Note: 1. See Section 5. “Errata”.

4.3.11 PIO Usage

Most signals can also be configured as simple inputs or outputs from the processor.

Table 4-23. PIO A Pin Assignment and Signal Description

Power Rail	PIO	Signal	Signal	Signal	Main Board Function	Extended Function
VDDIOP0	PA0	LCDDAT0	–	–	–	LCDDAT0
VDDIOP0	PA1	LCDDAT1	–	–	–	LCDDAT1
VDDIOP0	PA2	LCDDAT2	–	–	–	LCDDAT2
VDDIOP0	PA3	LCDDAT3	–	–	–	LCDDAT3
VDDIOP0	PA4	LCDDAT4	–	–	–	LCDDAT4
VDDIOP0	PA5	LCDDAT5	–	–	–	LCDDAT5
VDDIOP0	PA6	LCDDAT6	–	–	–	LCDDAT6
VDDIOP0	PA7	LCDDAT7	–	–	–	LCDDAT7
VDDIOP0	PA8	LCDDAT8	–	–	–	LCDDAT8
VDDIOP0	PA9	LCDDAT9	–	–	–	LCDDAT9
VDDIOP0	PA10	LCDDAT10	–	–	–	LCDDAT10
VDDIOP0	PA11	LCDDAT11	–	–	–	LCDDAT11
VDDIOP0	PA12	LCDDAT12	–	–	–	LCDDAT12
VDDIOP0	PA13	LCDDAT13	–	–	–	LCDDAT13
VDDIOP0	PA14	LCDDAT14	–	–	–	LCDDAT14
VDDIOP0	PA15	LCDDAT15	–	–	–	LCDDAT15
VDDIOP0	PA16	LCDDAT16	ISI_D0	–	–	ISI_D0
VDDIOP0	PA17	LCDDAT17	ISI_D1	–	–	ISI_D1
VDDIOP0	PA18	LCDDAT18	TWD2	ISI_D2	–	TWD2/ISI_D2
VDDIOP0	PA19	LCDDAT19	TWCK2	ISI_D3	–	TWCK2/ISI_D3
VDDIOP0	PA20	LCDDAT20	PWMH0	ISI_D4	–	ISI_D4
VDDIOP0	PA21	LCDDAT21	PWML0	ISI_D5	–	ISI_D5
VDDIOP0	PA22	LCDDAT22	PWMH1	ISI_D6	–	ISI_D6
VDDIOP0	PA23	LCDDAT23	PWML1	ISI_D7	–	ISI_D7
VDDIOP0	PA24	LCDPWM	–	–	–	LCDPWM
VDDIOP0	PA25	LCDDISP	–	–	–	LCDDISP
VDDIOP0	PA26	LCDVSYNC	–	–	–	LCDVSYNC
VDDIOP0	PA27	LCDHSYNC	–	–	–	LCDHSYNC
VDDIOP0	PA28	LCDPCK	–	–	–	LCDPCK
VDDIOP0	PA29	LCDDEN	–	–	–	LCDDEN
VDDIOP0	PA30	TWD0	URXD1	ISI_VSYNC	TWD0	URXD1/ISI_VSYNC
VDDIOP0	PA31	TWCK0	UTXD1	ISI_HSYNC	TWCK0	UTXD1/ISI_HSYNC

Table 4-24. PIO B Pin Assignment and Signal Description

Power Rail	PIO	Signal	Signal	Signal	Main Board Function	Extended Function
VDDIOP1	PB0	GTX0	PWMH0	–	GTX0	–
VDDIOP1	PB1	GTX1	PWML0	–	GTX1	–
VDDIOP1	PB2	GTX2	TK1	–	GTX2	–
VDDIOP1	PB3	GTX3	TF1	–	GTX3	–
VDDIOP1	PB4	GRX0	PWMH1	–	GRX0	–
VDDIOP1	PB5	GRX1	PWML1	–	GRX1	–
VDDIOP1	PB6	GRX2	TD1	–	GRX2	–
VDDIOP1	PB7	GRX3	RK1	–	GRX3	–
VDDIOP1	PB8	GTXCK	PWMH2	–	GTXCK	–
VDDIOP1	PB9	GTXEN	PWML2	–	GTXEN	–
VDDIOP1	PB10	GTXER	RF1	–	INT_GETH	--
VDDIOP1	PB11	GRXCK	RD1	–	GRXCK	--
VDDIOP1	PB12	GRXDV	PWMH3	–	INT_ETH	–
VDDIOP1	PB13	GRXER	PWML3	–	GRXER	–
VDDIOP1	PB14	GCRS	CANRX1	–	–	CANRX1
VDDIOP1	PB15	GCOL	CANTX1	–	–	CANTX1
VDDIOP1	PB16	GMDC	–	–	GMDC	--
VDDIOP1	PB17	GMDIO	–	–	GMDIO	–
VDDIOP1	PB18	G125CK	–	–	G125CK	–
VDDIOP1	PB19	MCI1_CDA	GTX4	–	MCI1_CDA	--
VDDIOP1	PB20	MCI1_DA0	GTX5	–	MCI1_DA0	–
VDDIOP1	PB21	MCI1_DA1	GTX6	–	MCI1_DA1	--
VDDIOP1	PB22	MCI1_DA2	GTX7	–	MCI1_DA2	--
VDDIOP1	PB23	MCI1_DA3	GRX4	–	MCI1_DA3	–
VDDIOP1	PB24	MCI1_CK	GRX5	–	MCI1_CK	–
VDDIOP1	PB25	SCK1	GRX6	–	–	SCK1
VDDIOP1	PB26	CTS1	GRX7	–	–	CTS1
VDDIOP1	PB27	RTS1	PWMH1	–	–	RTS1
VDDIOP1	PB28	RXD1	–	–	–	RXD1
VDDIOP1	PB29	TXD1	–	–	–	TXD1
VDDIOP0	PB30	DRXD	–	–	DRXD (DBGU)	--
VDDIOP0	PB31	DTXD	–	–	DTXD (DBGU)	--

Table 4-25. PIO C Pin Assignment and Signal Description

Power Rail	PIO	Signal	Signal	Signal	Main Board Function	Extended Function
VDDIOP0	PC0	ETX0	TIOA3	–	ETX0	ETX0/TIOA3
VDDIOP0	PC1	ETX1	TIOB3	–	ETX1	ETX1/TIOB3
VDDIOP0	PC2	ERX0	TCLK3	–	ERX0	ERX0/TCLK3
VDDIOP0	PC3	ERX1	TIOA4	–	ERX1	ERX1/TIOA4
VDDIOP0	PC4	ETXEN	TIOB4	–	ETXEN	ETXEN/TIOB4
VDDIOP0	PC5	ECRSDV	TCLK4	–	ECRSDV	ECRSDV/TCLK4
VDDIOP0	PC6	ERXER	TIOA5	–	ERXER	ERXER/TIOA5
VDDIOP0	PC7	EREFCK	TIOB5	–	EREFCK	EREFCK/TIOB5
VDDIOP0	PC8	EMDC	TCLK5	–	EMDC	EMDC/TCLK5
VDDIOP0	PC9	EMDIO	--	–	EMDIO	EMDIO
VDDIOP0	PC10	MCI2_CDA	LCDDAT20	–	–	LCDDAT20
VDDIOP0	PC11	MCI2_DA0	LCDDAT19	–	–	LCDDAT19
VDDIOP0	PC12	MCI2_DA1	TIOA1	LCDDAT18	–	LCDDAT18
VDDIOP0	PC13	MCI2_DA2	TIOB1	LCDDAT17	–	LCDDAT17
VDDIOP0	PC14	MCI2_DA3	TCLK1	LCDDAT16	–	LCDDAT16
VDDIOP0	PC15	MCI2_CK	PCK2	LCDDAT21	–	LCDDAT21/PCK2
VDDIOP0	PC16	TK0	–	–	–	TK0 Audio
VDDIOP0	PC17	TF0	–	–	–	TF0 Audio
VDDIOP0	PC18	TD0	–	–	–	TD0 Audio
VDDIOP0	PC19	RK0	–	–	–	RK0 Audio
VDDIOP0	PC20	RF0	–	–	–	RF0 Audio
VDDIOP0	PC21	RD0	–	–	–	RD0 Audio
VDDIOP0	PC22	SPI1_MISO	–	–	–	SPI1_MISO
VDDIOP0	PC23	SPI1_MOSI	–	–	–	SPI1_MOSI
VDDIOP0	PC24	SPI1_SPCK	–	–	–	SPI1_SPCK
VDDIOP0	PC25	SPI1_NPCS0	–	–	–	SPI1_NPCS0
VDDIOP0	PC26	SPI1_NPCS1	TWD1	ISI_D11	–	SPI1_NPCS1/TWD1
VDDIOP0	PC27	SPI1_NPCS2	TWCK1	ISI_D10	–	SPI1_NPCS2/TWCK1
VDDIOP0	PC28	SPI1_NPCS3	PWMFI0	ISI_D9	–	SPI1_NPCS3/ISI_D9
VDDIOP0	PC29	URXD0	PWMFI2	ISI_D8	–	URXD0/ISI_D8
VDDIOP0	PC30	UTXD0	ISI_PCK	–	–	UTXD0/ISI_PCK
VDDIOP0	PC31	FIQ	PWMFI1	–	IRQ_PMIC	–

Table 4-26. PIO D Pin Assignment and Signal Description

Power Rail	PIO	Signal	Signal	Signal	Main Board Function	Extended Function
VDDIOP1	PD0	MCI0_CDA	–	–	MCI0_CDA	–
VDDIOP1	PD1	MCI0_DA0	–	–	MCI0_DA0	–
VDDIOP1	PD2	MCI0_DA1	–	–	MCI0_DA1	–
VDDIOP1	PD3	MCI0_DA2	–	–	MCI0_DA2	–
VDDIOP1	PD4	MCI0_DA3	–	–	MCI0_DA3	–
VDDIOP1	PD5	MCI0_DA4	TIOA0	PWMH2	MCI0_DA4	–
VDDIOP1	PD6	MCI0_DA5	TIOB0	PWML2	MCI0_DA5	–
VDDIOP1	PD7	MCI0_DA6	TCLK0	PWMH3	MCI0_DA6	–
VDDIOP1	PD8	MCI0_DA7	PWML3	–	MCI0_DA7	–
VDDIOP1	PD9	MCI0_CK	–	–	MCI0_CK	–
VDDIOP1	PD10	SPI0_MISO	–	–	SPI0_MISO	SPI0_MISO
VDDIOP1	PD11	SPI0_MOSI	–	–	SPI0_MOSI	SPI0_MOSI
VDDIOP1	PD12	SPI0_SPCK	–	–	SPI0_SPCK	SPI0_SPCK
VDDIOP1	PD13	SPI0_NPCS0	–	–	SPI0_NPCS0	–
VDDIOP1	PD14	SCK0	SPI0_NPCS1	CANRX0	–	SCK0/SPI0_NPCS 0/CANRX0
VDDIOP1	PD15	CTS0	SPI0_NPCS2	CANTX0	–	CST0/SPI0_NPCS 2/CANTX0
VDDIOP1	PD16	RTS0	SPI0_NPCS3	PWMFI3	–	SPI0_NPCS3
VDDIOP1	PD17	RXD0	–	–	–	RXD0
VDDIOP1	PD18	TXD0	–	–	–	TXD0
VDDIOP1	PD19	ADTRG	–	–	–	ADTRG (HSYNC)
VDDANA	PD20	AD0	–	–	–	AD0/LCD TSC
VDDANA	PD21	AD1	–	–	–	AD1/LCD TSC
VDDANA	PD22	AD2	–	–	–	AD2/LCD TSC
VDDANA	PD23	AD3	–	–	–	AD3/LCD TSC
VDDANA	PD24	AD4	–	–	–	AD4
VDDANA	PD25	AD5	–	–	–	AD5
VDDANA	PD26	AD6	–	–	–	AD6
VDDANA	PD27	AD7	–	–	–	AD7
VDDANA	PD28	AD8	–	–	–	AD8
VDDANA	PD29	AD9	–	–	–	AD9
VDDANA	PD30	AD10	PCK0	–	--	AD10/PCK0
VDDANA	PD31	AD11	PCK1	–	–	AD11/PCK1

Table 4-27. PIO E Pin Assignment and Signal Description

Power Rail	PIO	Signal	Signal	Signal	Main Board Function	Extended Function
VDDIOM	PE0	A0/NBS0	–	–	MCI0_CD	–
VDDIOM	PE1	A1	–	–	MCI1_CD	–
VDDIOM	PE2	A2	–	–	PWR_MCI0	–
VDDIOM	PE3	A3	–	–	EN5V_USBB	–
VDDIOM	PE4	A4	–	–	EN5V_USBC	–
VDDIOM	PE5	A5	–	–	OVCUR_USB	–
VDDIOM	PE6	A6	–	–	–	RST_LCD
VDDIOM	PE7	A7	–	–	–	IRQ1 / ChgMXT
VDDIOM	PE8	A8	–	–	–	IRQ2/ChgQT
VDDIOM	PE9	A9	–	–	VBUS_SENSE	A9
VDDIOM	PE10	A10	–	–	–	A10
VDDIOM	PE11	A11	–	–	–	A11
VDDIOM	PE12	A12	–	–	–	A12
VDDIOM	PE13	A13	–	–	–	A13
VDDIOM	PE14	A14	–	–	–	A14
VDDIOM	PE15	A15	SCK3	–	–	A15/SCK3
VDDIOM	PE16	A16	CTS3	–	–	A16/CTS3
VDDIOM	PE17	A17	RTS3	–	–	A17/RTS3
VDDIOM	PE18	A18	RXD3	–	–	A18/RXD3
VDDIOM	PE19	A19	TXD3	–	–	A19/TXD3
VDDIOM	PE20	A20	SCK2	–	–	A20/SCK2
VDDIOM	PE21	A21/NANDALE	–	–	A21/NANDALE	–
VDDIOM	PE22	A22/NANDCLE	–	–	A22/NANDCLE	–
VDDIOM	PE23	A23	CTS2	–	1-Wire / User LED	A23/1-Wire/CTS2
VDDIOM	PE24	A24	RTS2	–	Power LED	A24/RTS2
VDDIOM	PE25	A25	RXD2	–	–	A25/RXD2
VDDIOM	PE26	NCS0	TXD2	–	–	NCS0/TXD2
VDDIOM	PE27	NCS1	TIOA2	LCDDAT22	–	LCDDAT22
VDDIOM	PE28	NCS2	TIOB2	LCDDAT23		LCDDAT23
VDDIOM	PE29	NWR1/NBS1	TCLK2	–	USER_PB	NWR1/NBS1/TCLK2
VDDIOM	PE30	NWAIT	–	–	nPBSTA_PMIC	–
VDDIOM	PE31	IRQ	PWML1	–	–	IRQ/PWML1

4.4 SAMA5D3 Xplained Board Schematics

This section contains the following schematics:

- General information
- Block Diagram
- PIO Multiplexing Table
- Power Supplies
- SAMA5D3 Device and USB Interfaces
- DDR2 Memory
- NAND Flash and Optional Memories
- SD and Micro-SD Interfaces
- Gigabit Ethernet
- Ethernet 10/100
- LCD, JTAG, DEBUG and Extended Connectors

Figure 4-38. General information

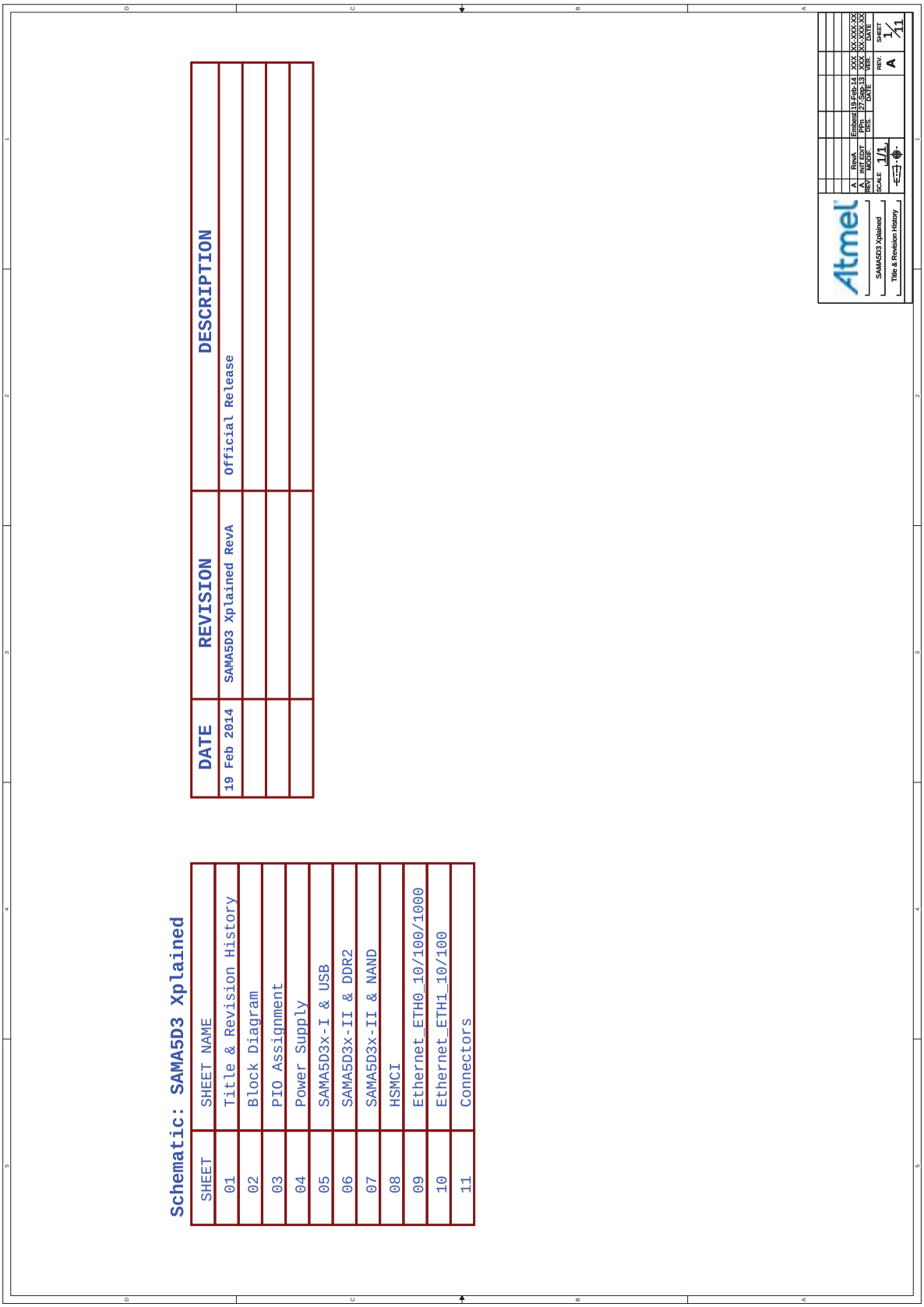


Figure 4-39. Block diagram

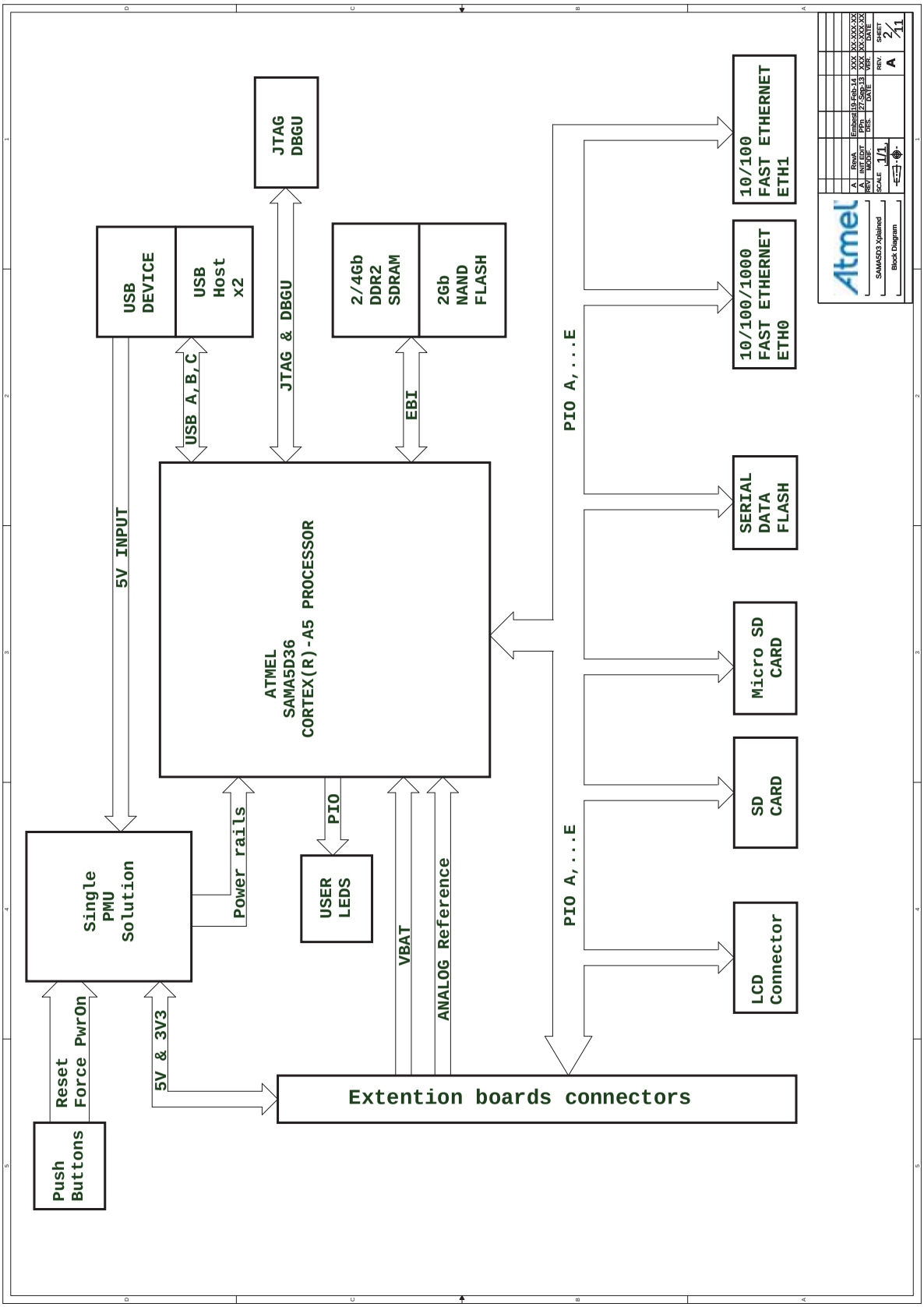
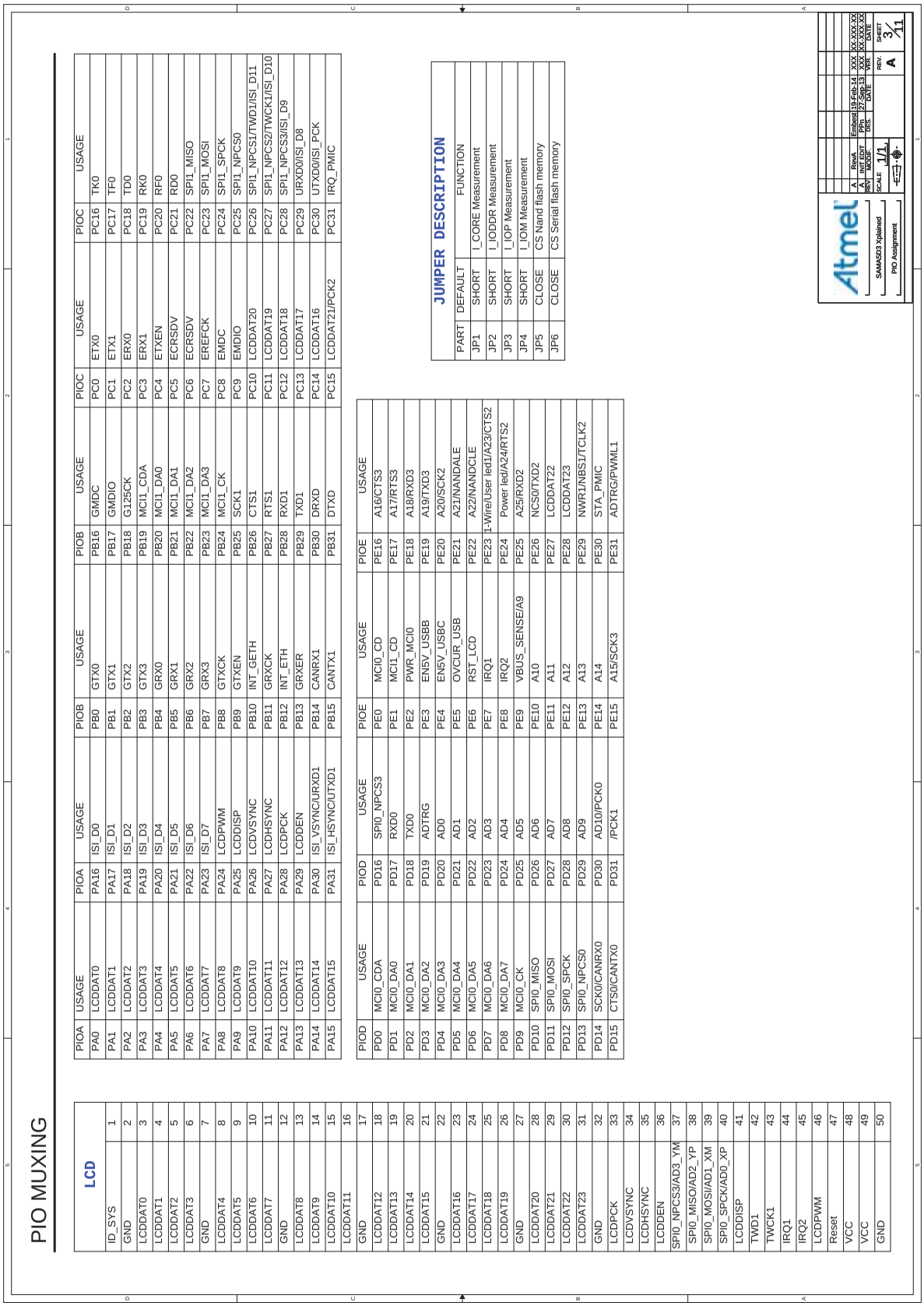


Figure 4-40. PIO Multiplexing Table



PIO MUXING

LCD		
ID_SYS	1	
GND	2	
LCDDAT0	3	
LCDDAT1	4	
LCDDAT2	5	
LCDDAT3	6	
GND	7	
LCDDAT4	8	
LCDDAT5	9	
LCDDAT6	10	
LCDDAT7	11	
GND	12	
LCDDAT8	13	
GND	14	
LCDDAT10	15	
LCDDAT11	16	
GND	17	
LCDDAT12	18	
LCDDAT13	19	
LCDDAT14	20	
LCDDAT15	21	
GND	22	
LCDDAT16	23	
LCDDAT17	24	
LCDDAT18	25	
LCDDAT19	26	
GND	27	
LCDDAT20	28	
LCDDAT21	29	
LCDDAT22	30	
LCDDAT23	31	
GND	32	
LCDPCK	33	
LCDVSYNC	34	
LCDHSYNC	35	
LCDDEN	36	
SPI0_NPCS3/AD3_YM	37	
SPI0_MISO/AD2_YP	38	
SPI0_MOSI/AD1_XM	39	
SPI0_SPCK/AD0_XP	40	
LCDDISP	41	
TWD1	42	
TWCK1	43	
IRQ1	44	
IRQ2	45	
LCDPWM	46	
Reset	47	
VCC	48	
VCC	49	
GND	50	

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE
PA0	LCDDAT0	PA16	ISI_D0	PB0	GTX0	PB16	GMDC	PC0	ETX0	PC16	TK0
PA1	LCDDAT1	PA17	ISI_D1	PB1	GTX1	PB17	GMDIO	PC1	ETX1	PC17	TF0
PA2	LCDDAT2	PA18	ISI_D2	PB2	GTX2	PB18	G125CK	PC2	ERX0	PC18	TD0
PA3	LCDDAT3	PA19	ISI_D3	PB3	GTX3	PB19	MCI1_CDA	PC3	ERX1	PC19	RK0
PA4	LCDDAT4	PA20	ISI_D4	PB4	GRX0	PB20	MCI1_DA0	PC4	ETXEN	PC20	RF0
PA5	LCDDAT5	PA21	ISI_D5	PB5	GRX1	PB21	MCI1_DA1	PC5	ECRSDV	PC21	RD0
PA6	LCDDAT6	PA22	ISI_D6	PB6	GRX2	PB22	MCI1_DA2	PC6	ECRSDV	PC22	SPI1_MISO
PA7	LCDDAT7	PA23	ISI_D7	PB7	GRX3	PB23	MCI1_DA3	PC7	EREFCK	PC23	SPI1_MOSI
PA8	LCDDAT8	PA24	LCDPWM	PB8	GTXCK	PB24	MCI1_CK	PC8	EMDC	PC24	SPI1_SPCK
PA9	LCDDAT9	PA25	LCDDISP	PB9	GTXEN	PB25	SCK1	PC9	EMDIO	PC25	SPI1_NPCS0
PA10	LCDDAT10	PA26	LCDVSYNC	PB10	INT_GETH	PB26	CTS1	PC10	LCDDAT20	PC26	SPI1_NPCS1/TWD1/ISI_D11
PA11	LCDDAT11	PA27	LCDHSYNC	PB11	GRXCK	PB27	RTS1	PC11	LCDDAT19	PC27	SPI1_NPCS2/TWCK1/ISI_D10
PA12	LCDDAT12	PA28	LCDPCK	PB12	INT_ETH	PB28	RXD1	PC12	LCDDAT18	PC28	SPI1_NPCS3/ISI_D9
PA13	LCDDAT13	PA29	LCDDEN	PB13	GRXER	PB29	TXD1	PC13	LCDDAT17	PC29	URXD0/ISI_D8
PA14	LCDDAT14	PA30	ISI_VSYNC/URXD1	PB14	CANRX1	PB30	DRXD	PC14	LCDDAT16	PC30	UTXD0/ISI_PCK
PA15	LCDDAT15	PA31	ISI_HSYNC/UTXD1	PB15	CANTX1	PB31	DTXD	PC15	LCDDAT21/PCK2	PC31	IRQ_PMIC

PIOD	USAGE	PIOD	USAGE	PIOE	USAGE	PIOE	USAGE
PD0	MCI0_CDA	PD16	SPI0_NPCS3	PE0	MCI0_CD	PE16	A16/CTS3
PD1	MCI0_DA0	PD17	RXD0	PE1	MCI1_CD	PE17	A17/RTS3
PD2	MCI0_DA1	PD18	TXD0	PE2	PWR_MCI0	PE18	A18/RXD3
PD3	MCI0_DA2	PD19	ADTRG	PE3	EN5V_USBB	PE19	A19/TXD3
PD4	MCI0_DA3	PD20	AD0	PE4	EN5V_USBC	PE20	A20/SCK2
PD5	MCI0_DA4	PD21	AD1	PE5	OVCUR_USB	PE21	A21/NANDALE
PD6	MCI0_DA5	PD22	AD2	PE6	RST_LCD	PE22	A22/NANDCLE
PD7	MCI0_DA6	PD23	AD3	PE7	IRQ1	PE23	1-Wire/User led1/A23/CTS2
PD8	MCI0_DA7	PD24	AD4	PE8	IRQ2	PE24	Power led/A24/RTS2
PD9	MCI0_CK	PD25	AD5	PE9	VBUS_SENSE/A9	PE25	A25/RXD2
PD10	SPI0_MISO	PD26	AD6	PE10	A10	PE26	NCS0/TXD2
PD11	SPI0_MOSI	PD27	AD7	PE11	A11	PE27	LCDDAT22
PD12	SPI0_SPCK	PD28	AD8	PE12	A12	PE28	LCDDAT23
PD13	SPI0_NPCS0	PD29	AD9	PE13	A13	PE29	NWR1/NBS1/TCLK2
PD14	SCK0/CANRX0	PD30	AD10/PCK0	PE14	A14	PE30	STA_PMIC
PD15	CTS0/CANTX0	PD31	/PCK1	PE15	A15/SCK3	PE31	ADTRG/PWML1

JUMPER DESCRIPTION

PART	DEFAULT	FUNCTION
JP1	SHORT	I_CORE Measurement
JP2	SHORT	I_IODDR Measurement
JP3	SHORT	I_IOP Measurement
JP4	SHORT	I_IOM Measurement
JP5	CLOSE	CS Nand flash memory
JP6	CLOSE	CS Serial flash memory

REV	MODIF	DES.	DATE
A	first	Embest	10-Feb-14
	INTEDIT	FPin	27-Sep-13
SCALE	1/1		

SAMA5D3 Xplained

PIO Assignment

REV.	SHEET
A	3/11

Figure 4-41. Power supplies

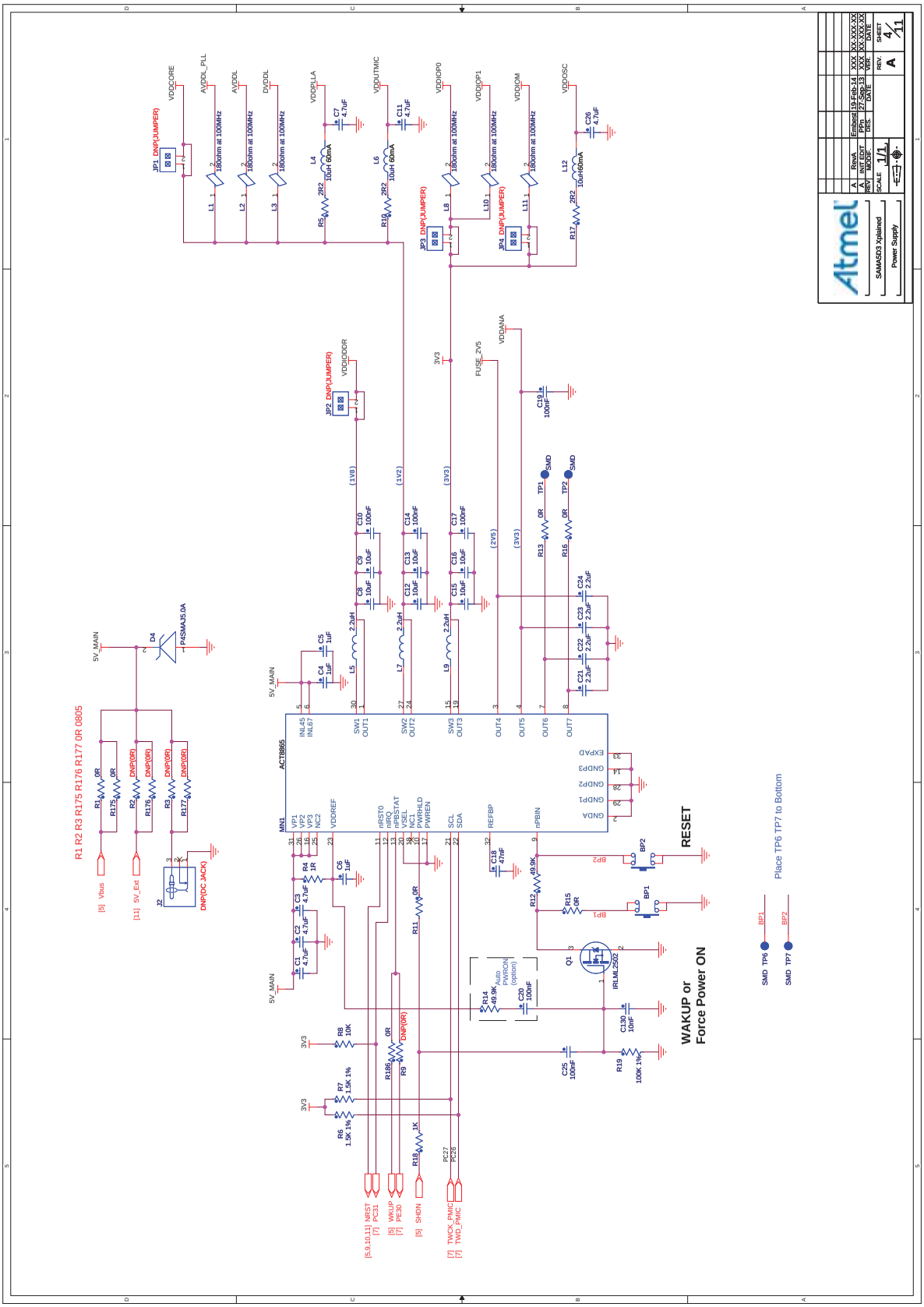


Figure 4-42. SAMA5D3 Device and USB Interfaces

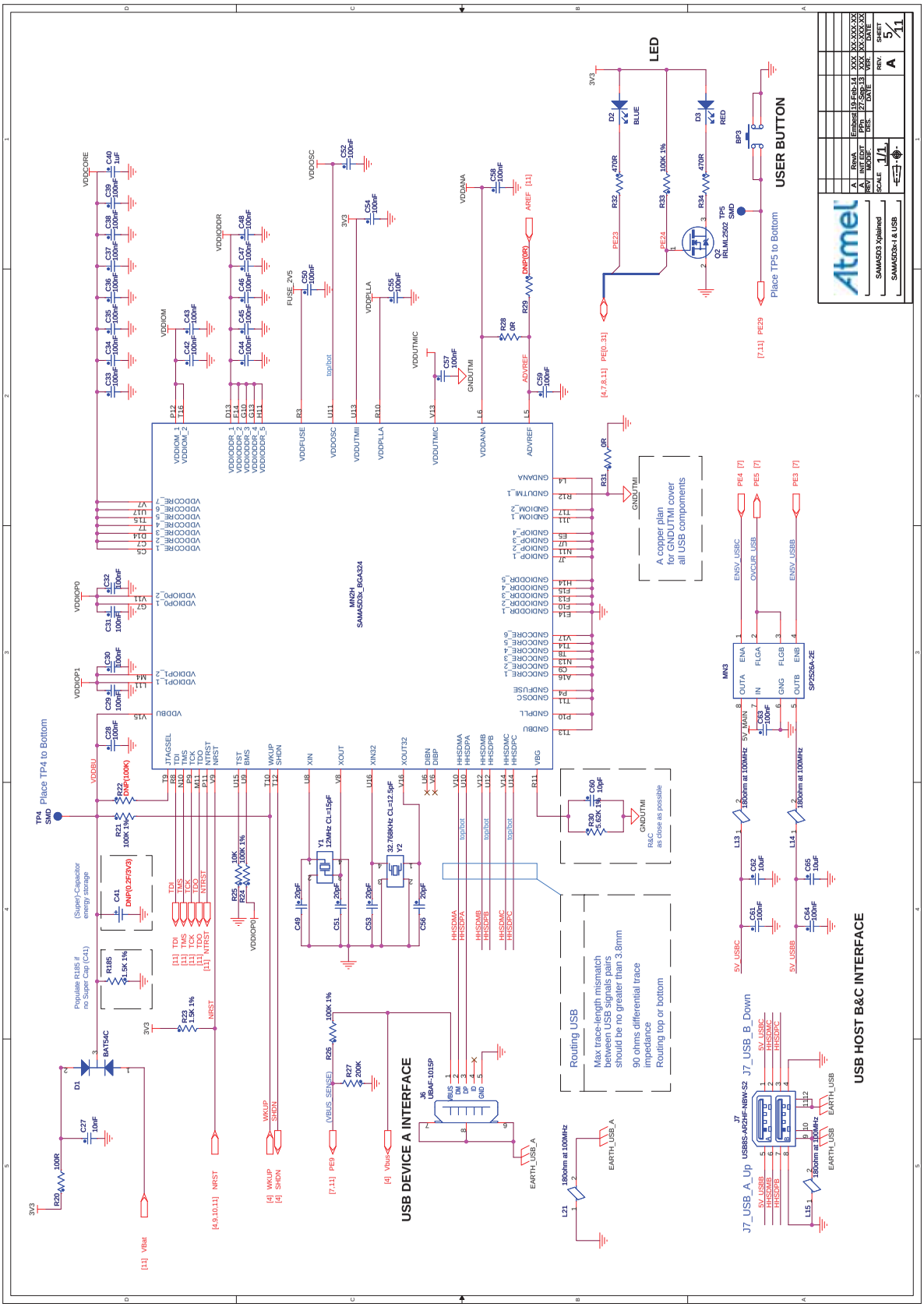


Figure 4-43. DDR2 Memory

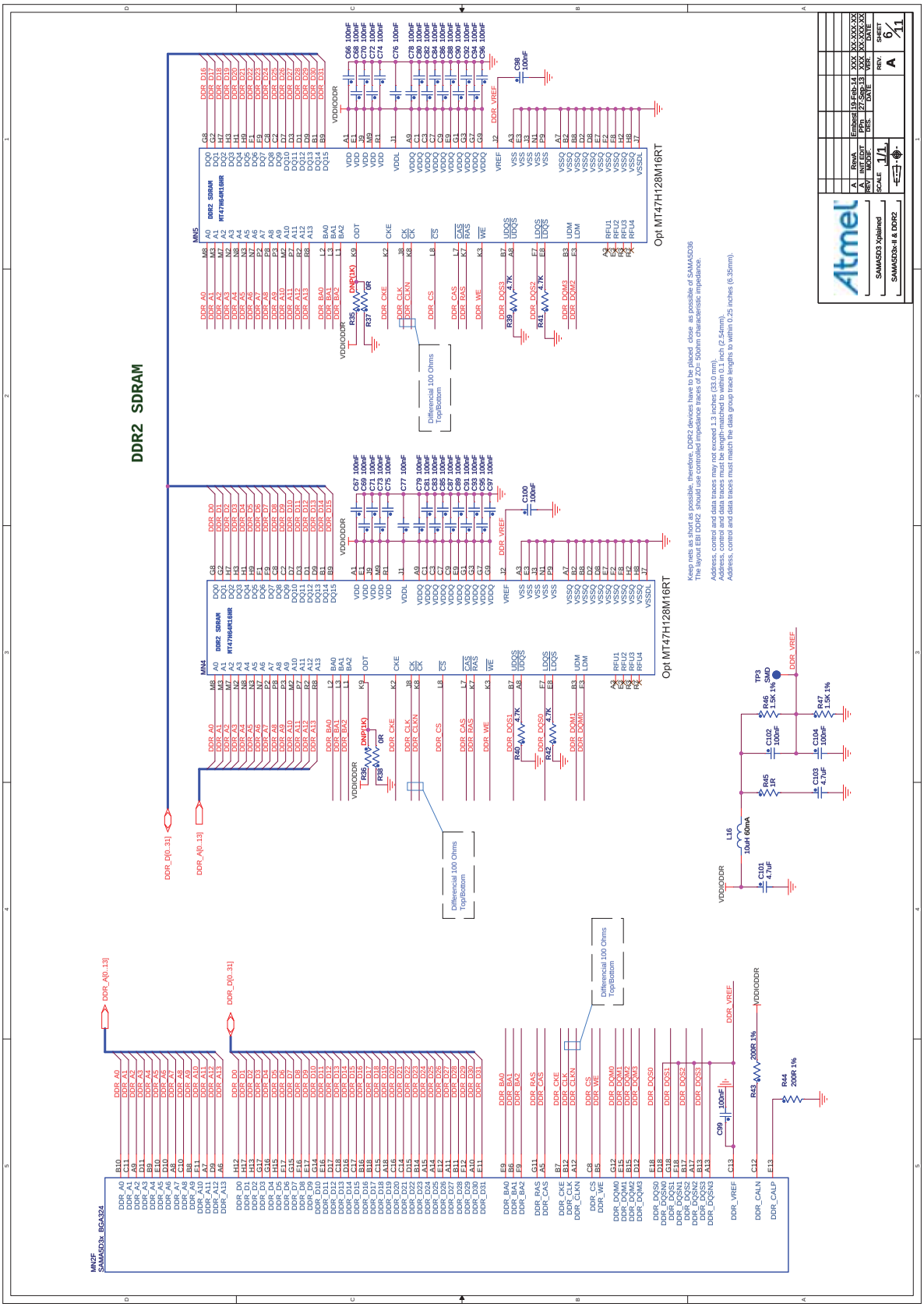


Figure 4-44. NAND Flash and Optional Memories

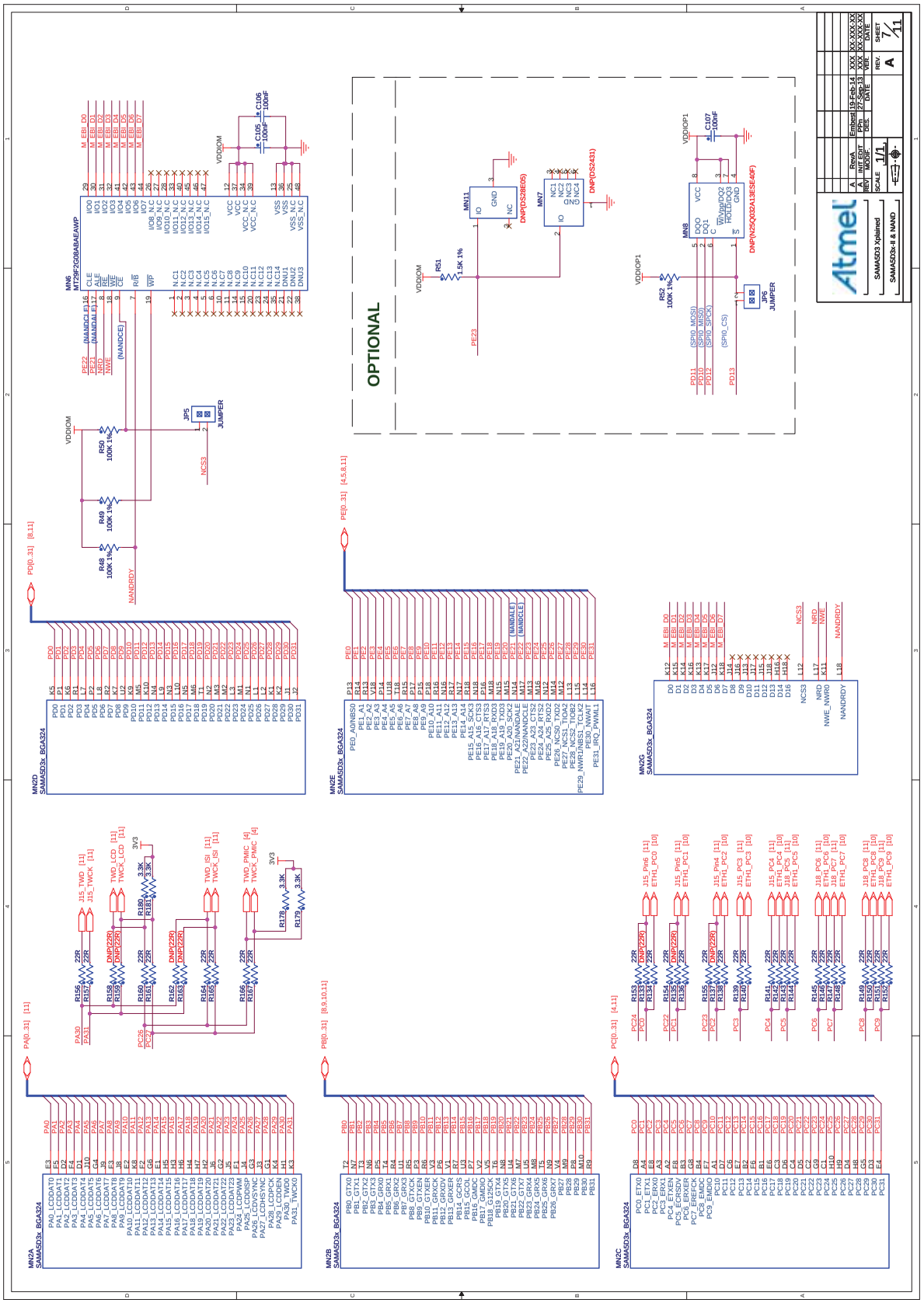


Figure 4-45. SD and Micro-SD Interfaces

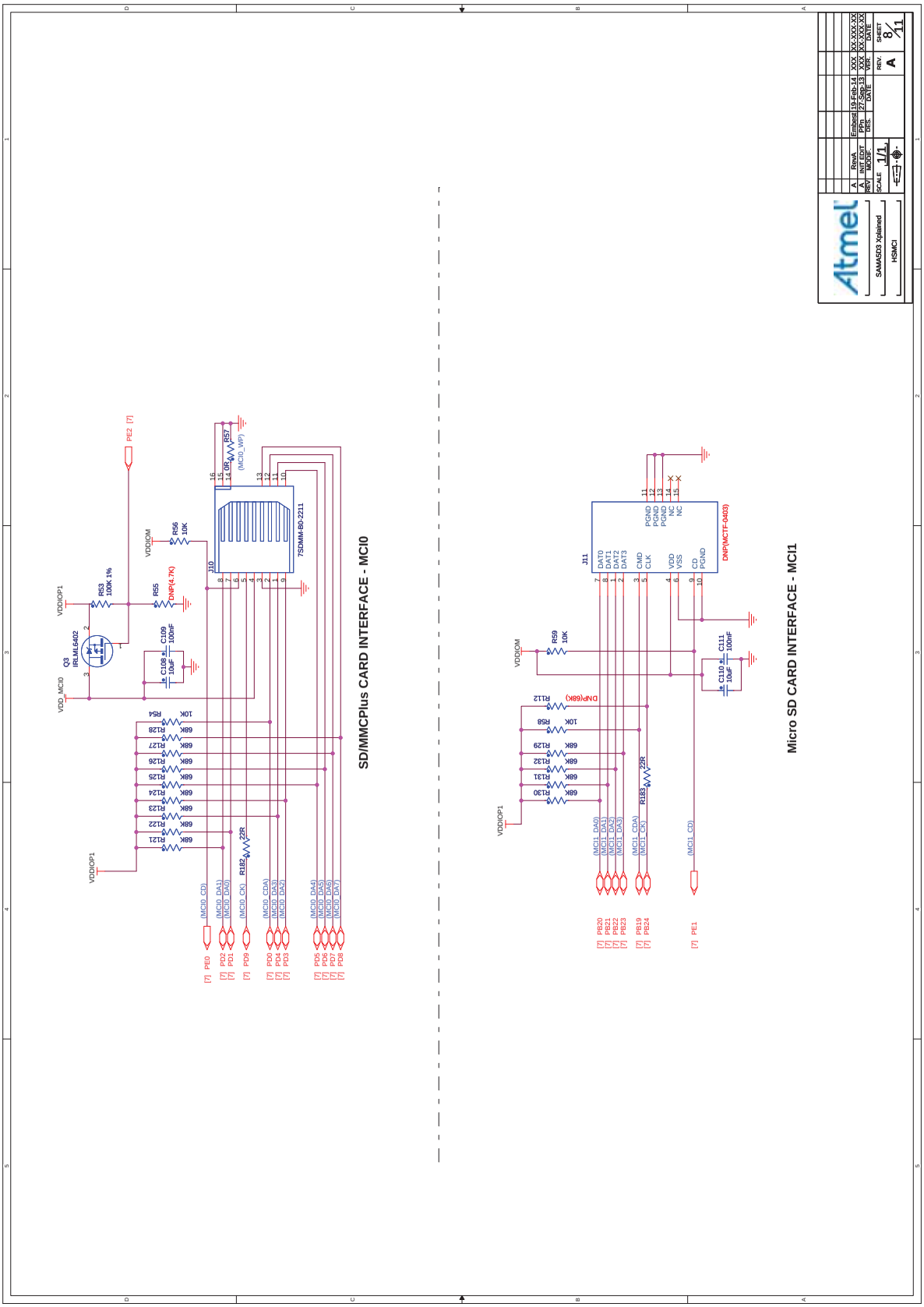


Figure 4-46. Gigabit Ethernet

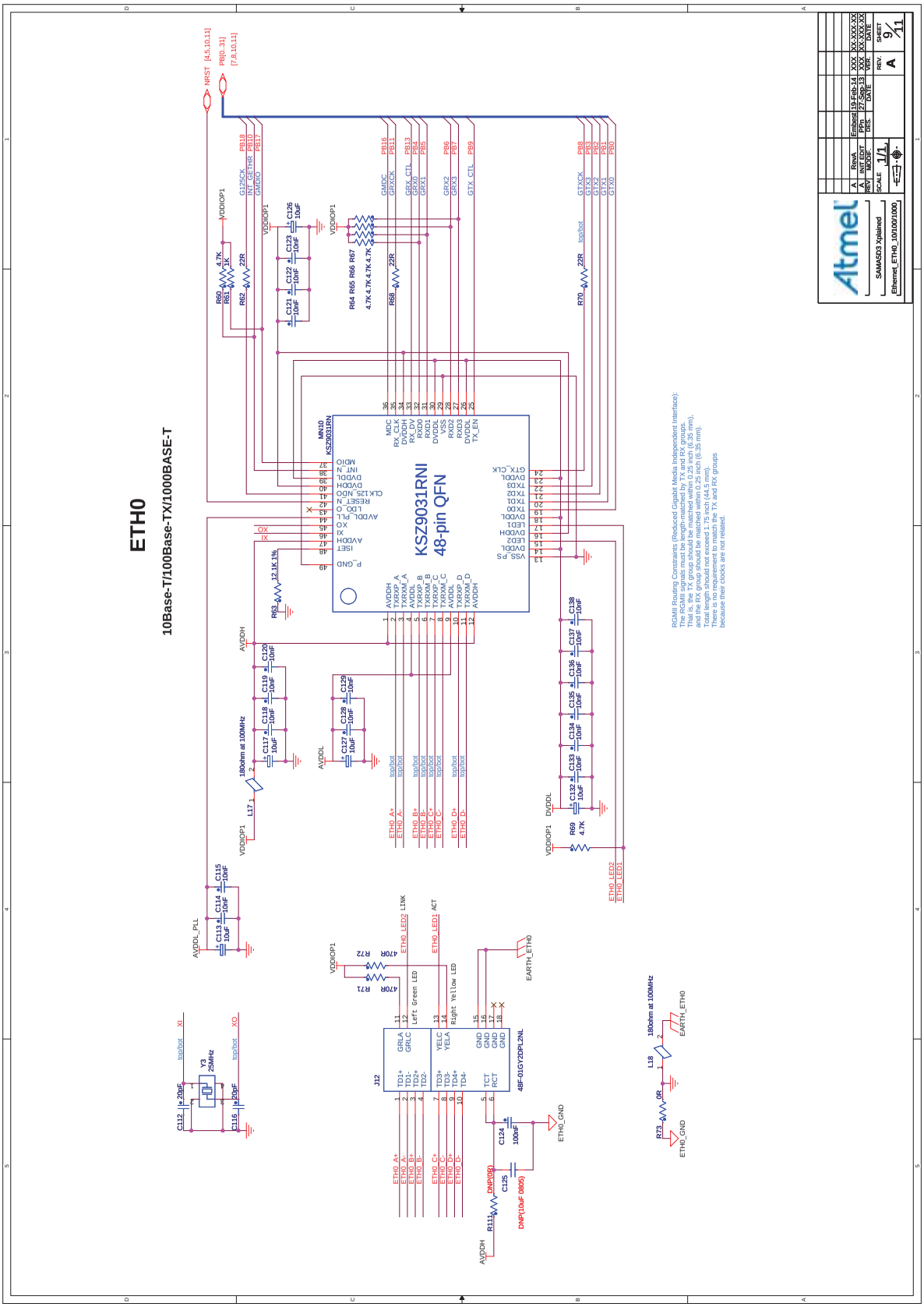


Figure 4-47. Ethernet 10/100

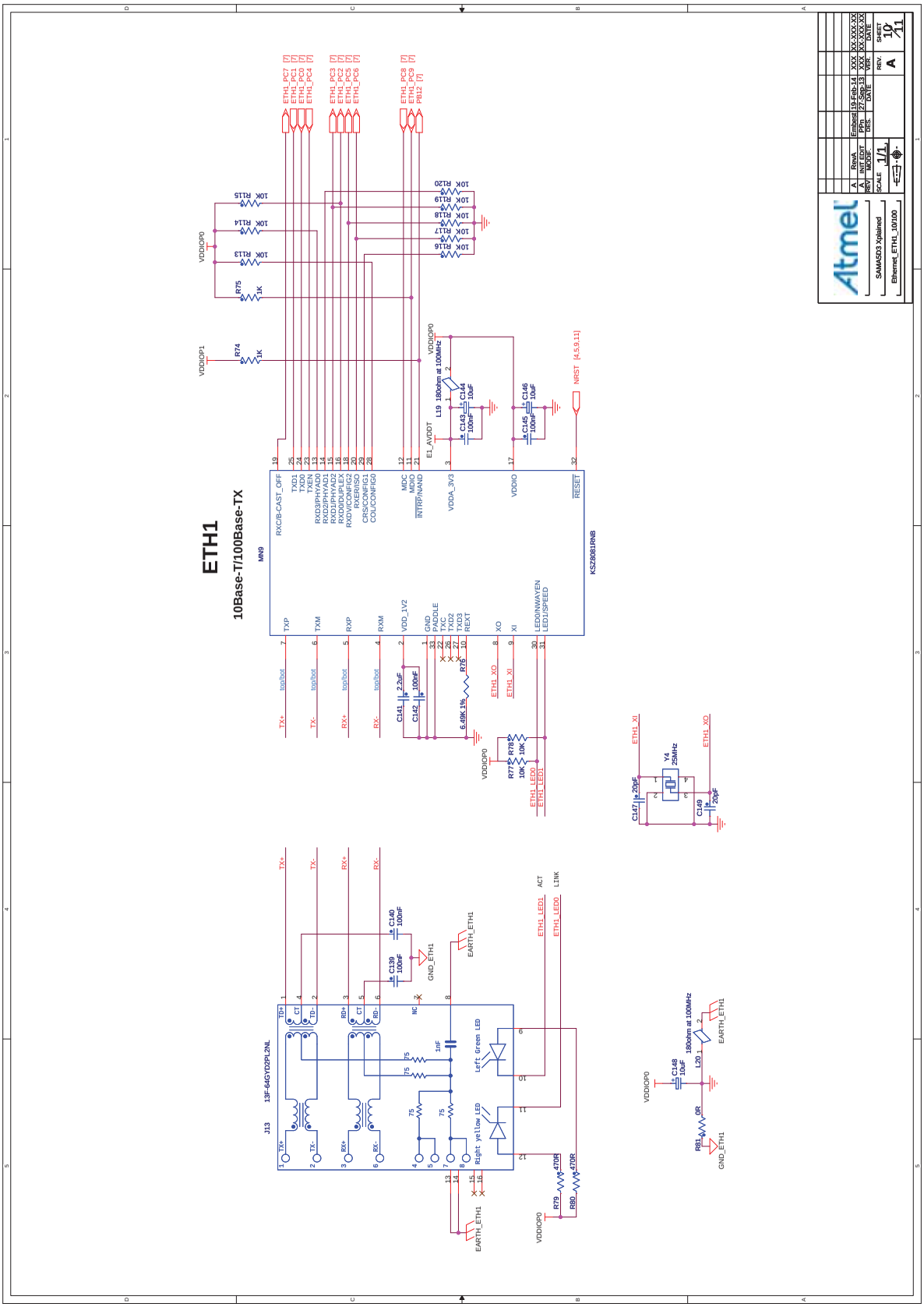
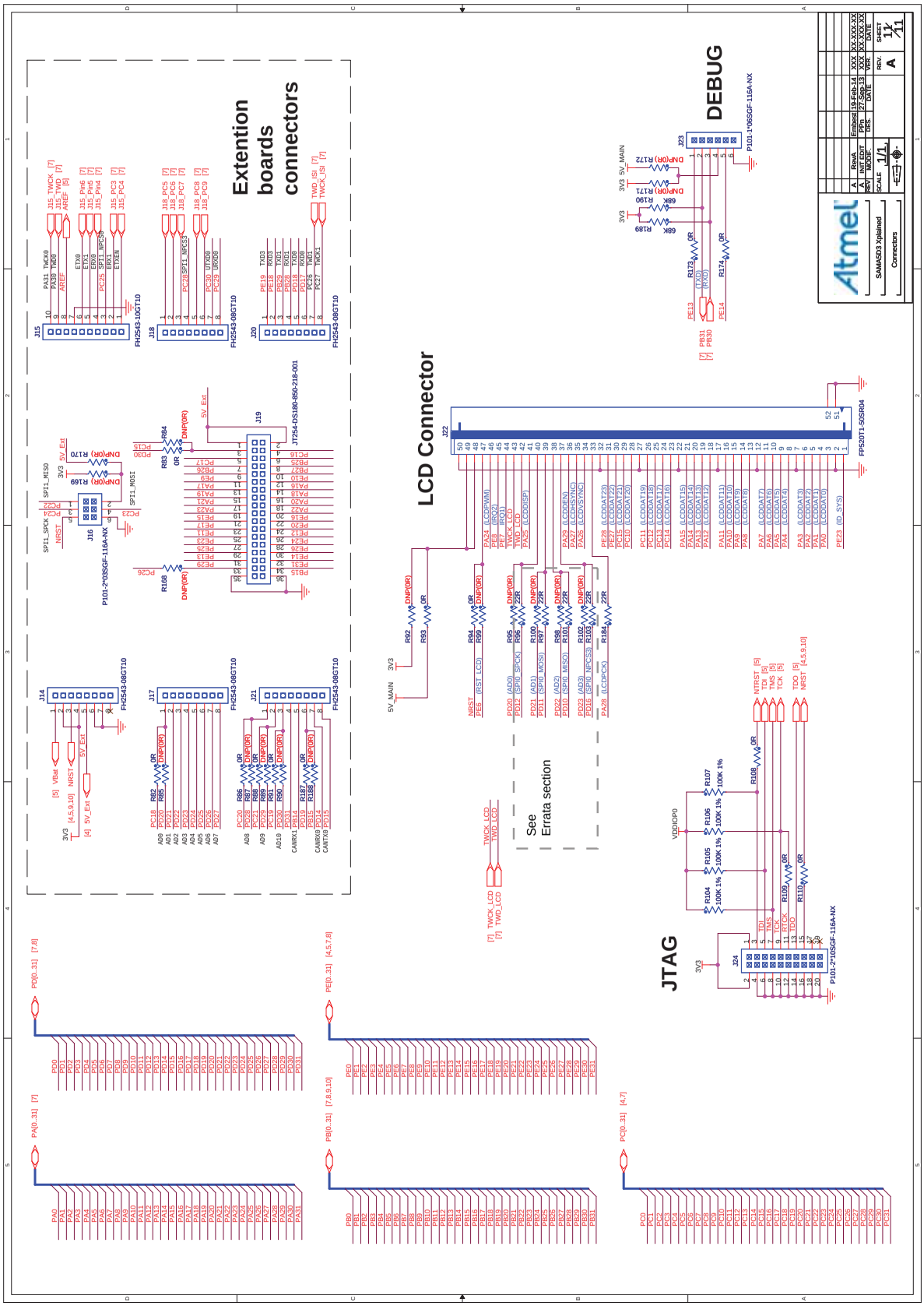


Figure 4-48. LCD, JTAG, DEBUG and Extended Connectors



5. Errata

5.1 The SPI lines available on the LCD connector J22 have been swapped.

Current implementation (wrong):

- Pin 37 = SPI0_NPCS3
- Pin 38 = SPI0_MISO
- Pin 39 = SPI0_MOSI
- Pin 40 = SPI0_SPCK

Correct implementation:

- Pin 37 = SPI0_SPCK
- Pin 38 = SPI0_MOSI
- Pin 39 = SPI0_MISO
- Pin 40 = SPI0_NPCS3

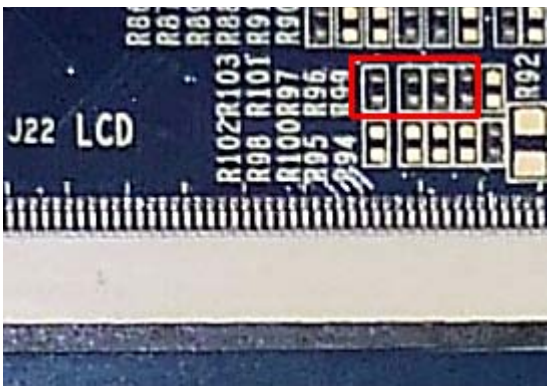
To date, there is no impact because no LCD screen available on the market uses the SPI bus on this connector, in particular the PDA Inc. TM430x and TM700x product series recommended by Atmel.

A potential problem exists only if the future "Xplained Pro" series LCD extensions are used because these extensions could require the SPI bus on this LCD connector.

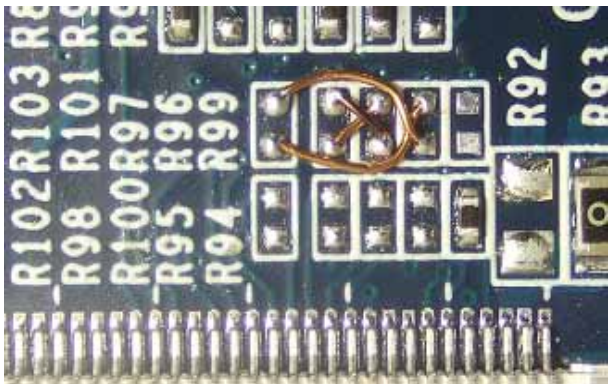
Also, for customers or third parties planning to develop their own extensions using a connection to J22, we strongly recommend following the correct implementation so as to guarantee a future consistency and compatibility with all Atmel tools.

Workaround:

1. Unsolder and remove resistors R96, R97, R101 and R103 located here:



2. Solder isolated pieces of wire as follows. Resin coated wires were used below. Make sure not to create any short-circuits between the wires and the other components.



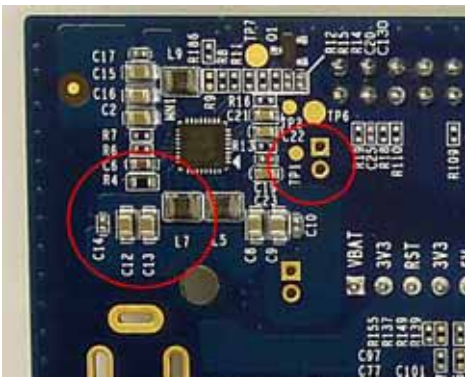
5.2 JP1 routing is incorrect and results in inaccurate VDDCORE current measurement

The jumper JP1 was incorrectly routed on the SAMA5D3 Xplained board. As a result, the on-board connections on the left and right sides of the jumper do not match the schematics and VDDCORE current measurement is incorrect.

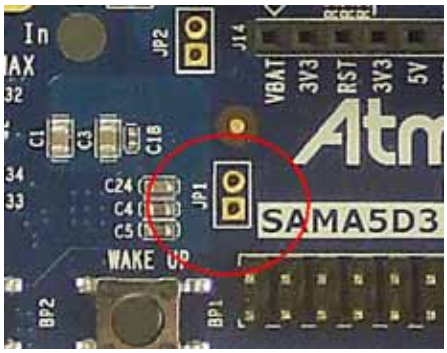
Workaround:

1. Locate C13, L7 and JP1 on the SAMA5D3 Xplained board.

C13, L7 and JP1 located on the bottom side

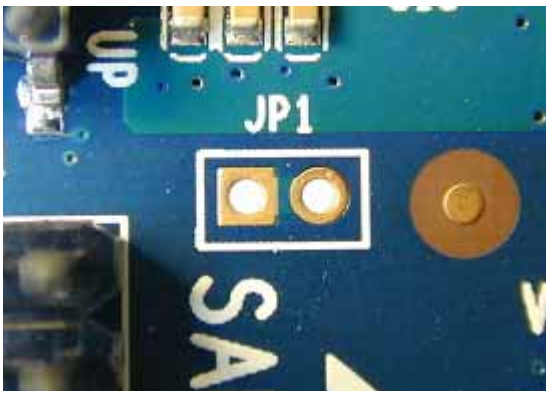


JP1 located on the top side

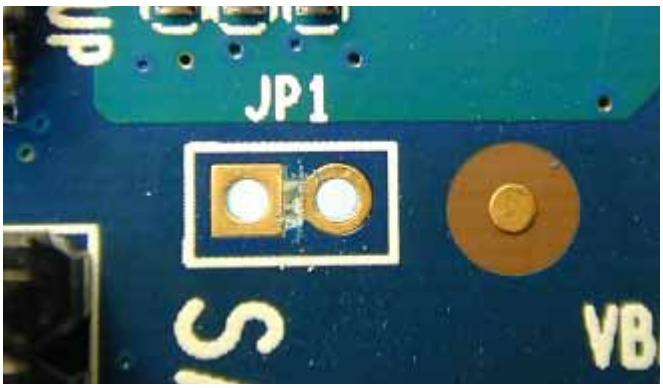


2. On the top side, cut the track between pins 1 and 2 of JP1.

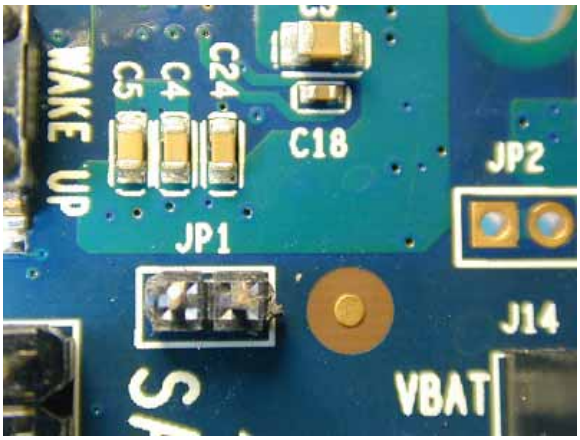
Before



After

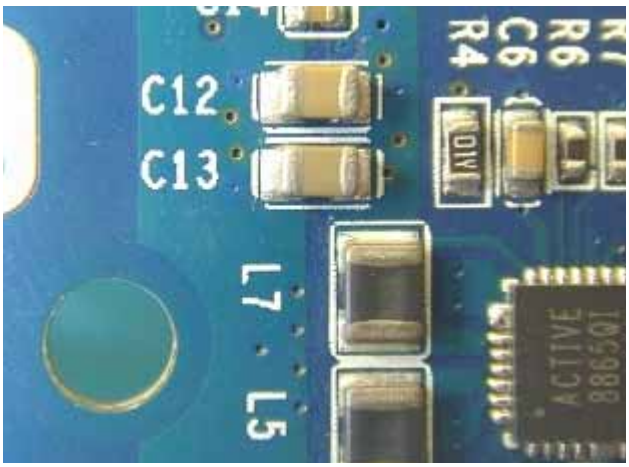


3. On the top side, solder a 2-pin header in the JP1 footprint.

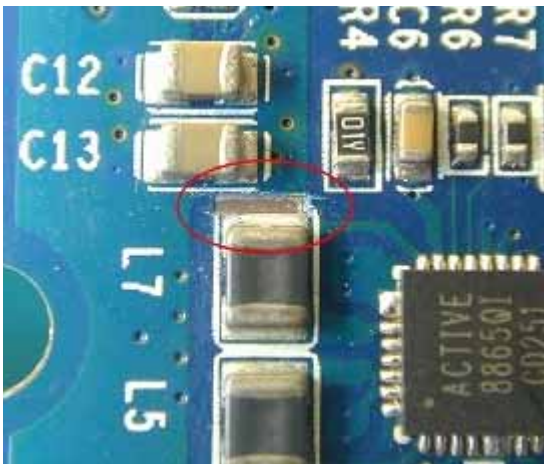


4. On the bottom side, cut the large track between C13 and L7.

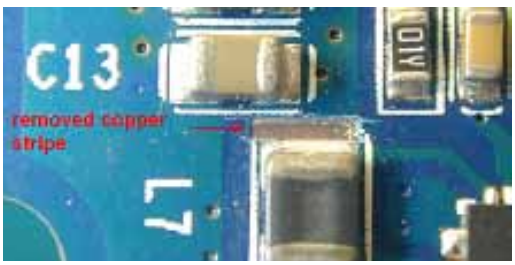
Before



After

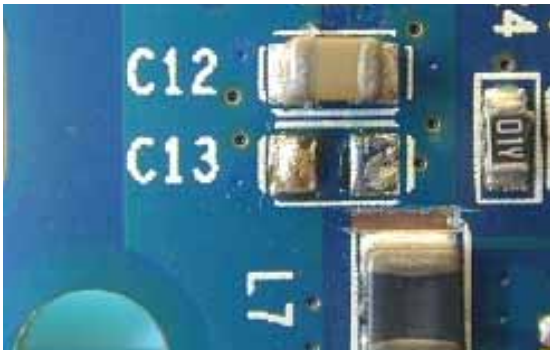


Zoom

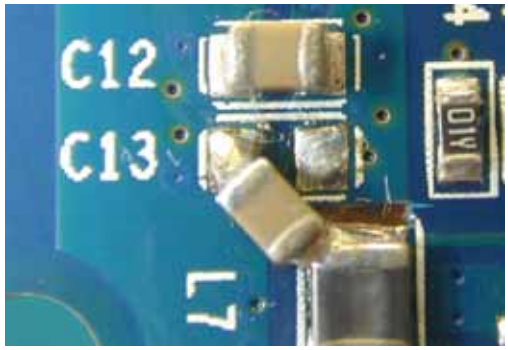


5. Unsolder C13 and re-solder it across the cut made in Step 3, directly to L7.

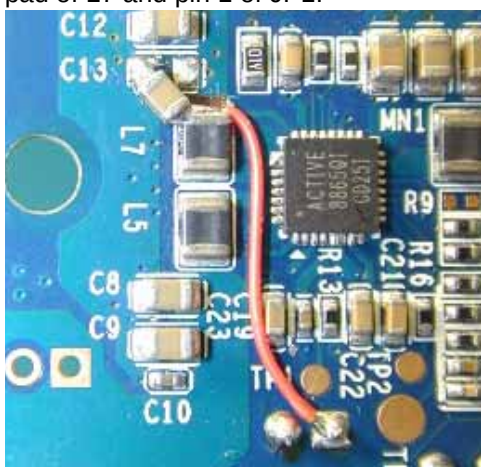
C13 Removed



C13 Re-soldered



6. Solder a wire between the top pad of L7 and pin 1 of JP1.



7. To complete the procedure, either:

   a) install a jumper across both JP1 pins for normal operation,

   or

   b) remove the jumper and connect an ammeter across both JP1 pins to measure VDDCORE current.

5.3 The TWI1 pull-up charge is excessive.

The pull-up charge on TWI1 data and clock lines is a bit too high and out of I²C specification.

Workaround:

Although the board proves to be functional as is, we recommend to fix this excessive pull-up charge by removing resistors R178 and R179. These are located near the J17 connector and the Atmel logo, as shown in the following figure:

Figure 5-1. Position of R178 and R179

6. Revision History

Table 6-1. SAMA5D3 Xplained User Guide Rev. 11269 Revision History

Doc. Rev.	Changes
11269D	"Errata" section: added Section 5.3 "The TWI1 pull-up charge is excessive."
11269C	Inserted Table 4-1 "SAMA5D3 Xplained Board Interface Connectors". Section 4.3.1 "Power Supply": added WARNING on known error on ACT8865 I²C implementation. Added Section 5.2 "JP1 routing is incorrect and results in inaccurate VDDCORE current measurement"
11269B	Added Section 5."Errata" . Added references to "Errata" in Figure 4-17 on page 21 and Figure 4-48 on page 59 and in Table 4-22, "LCD Socket J22 Signal Descriptions," on page 41 (added note 1)
11269A	First issue.

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