Revision History

32M (2M x 16 bit) PSEUDO STATIC RAM
48ball FPBGA Package

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Aug 2018

2Mb x16 Pseudo Static RAM Specification

GENERAL DESCRIPTION

The AS1C2M16P-70BIN is 33,554,432 bits of Pseudo SRAM which uses DRAM type memory cells, but this device has refresh-free operation and extreme low power consumption technology. Furthermore the interface is compatible to a low power Asynchronous type SRAM. The AS1C2M16P-70BIN is organized as 2,097,152 Words x 16 bit.

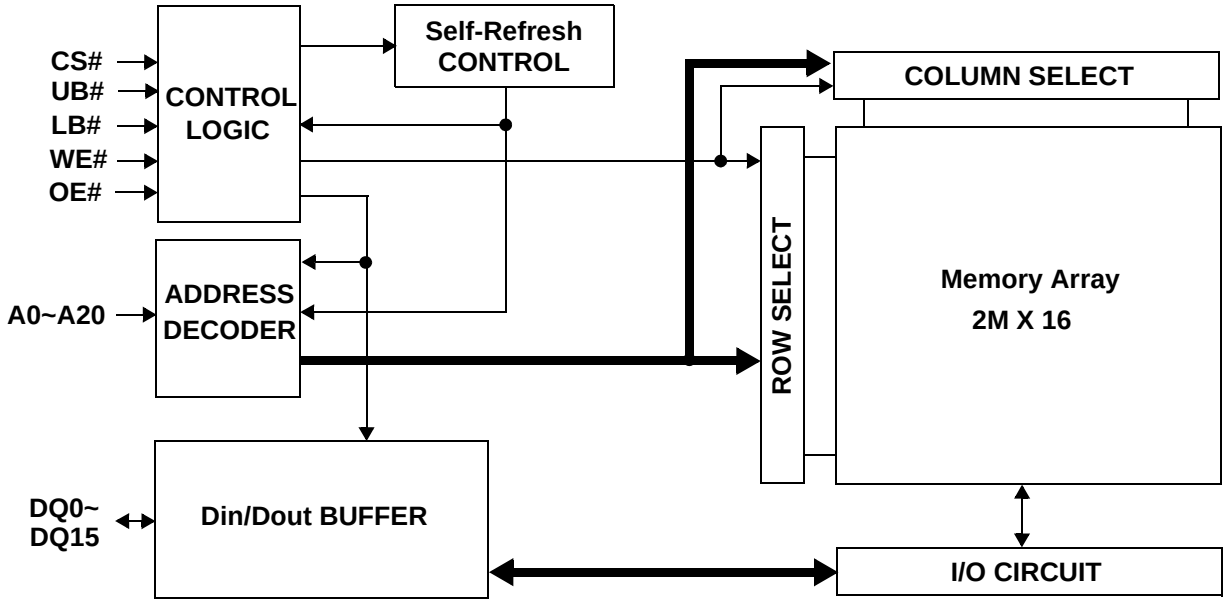
FEATURES

- Organization :2M x16
- Address access speed 70ns
- Power Supply Voltage : 2.6 ~ 3.3V
- Separated I/O power(VccQ) & Core power(Vcc)
- Three state outputs
- Byte read/write control by UB# / LB#
- Auto-TCSR for power saving
- Package type : 48ball-FPBGA (6.0x7.0)
- Operating Temperature
  . Industrial : -40 ℃ ~ 85 ℃

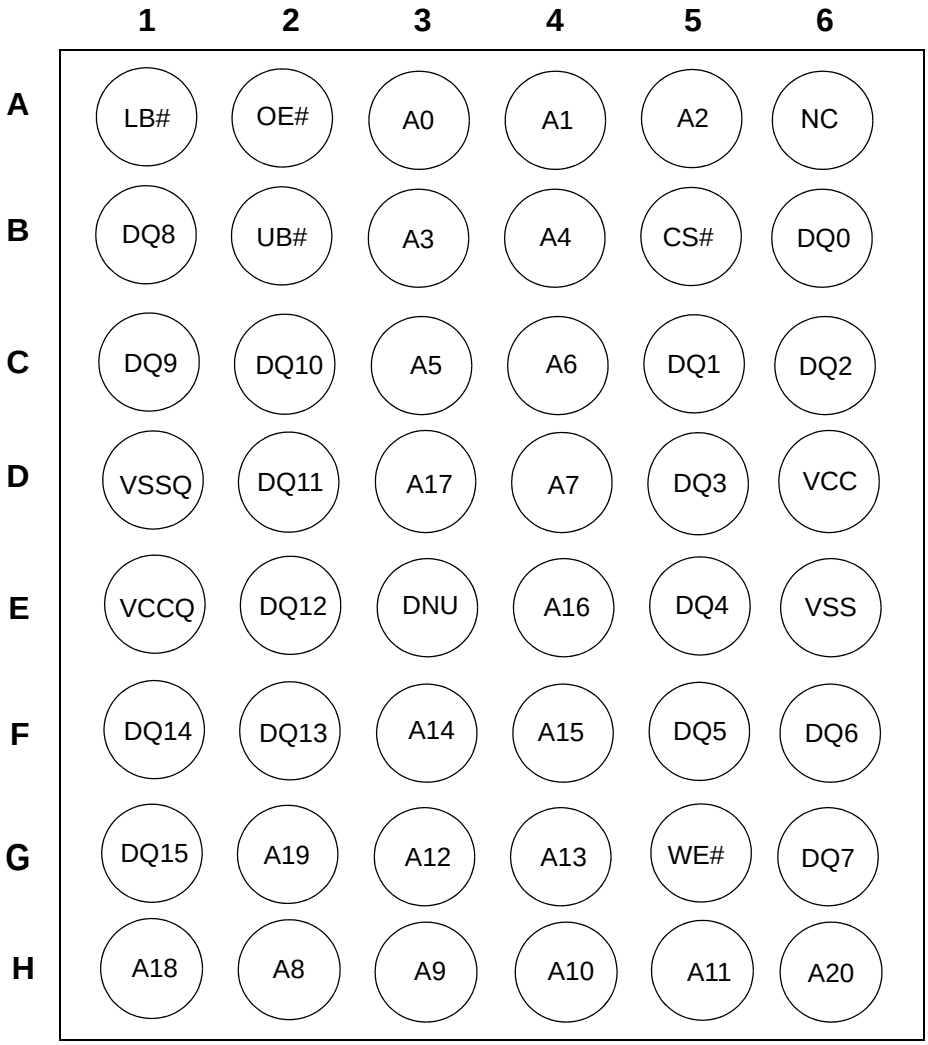
PRODUCT FAMILY

Part Number	Operating Temp.	Power Supply	Speed (t_{RC})	Power Dissipation		
				Standby (I_{SB}, Max.)	Operating I_{CC} (Max.)	
					I_{CC1} (f = 1MHz)	I_{CC2} (f = f_{max})
AS1C2M16P-70BIN	-40 ℃to 85 ℃	2.6V to 3.3V	70ns	120uA	5mA	25mA

FUNCTION BLOCK DIAGRAM



PIN DESCRIPTION (48ball-FPBGA-6.00x7.00)



TOP VIEW (Ball Down)

Name	Function	Name	Function
CS#	Chip select input	LB#	Lower byte ($DQ_{0\sim7}$)
OE#	Output enable input	UB#	Upper byte ($DQ_{8\sim15}$)
WE#	Write enable input	VCC	Power supply
DQ_{0-15}	Data in-out	VCCQ	I/O power supply
A_{0-20}	Address inputs	VSS(Q)	Ground
DNU	Do not use	NC	No connection

ABSOLUTE MAXIMUM RATINGS [1)]

Parameter		Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss		V_{IN}, V_{OUT}	-0.2 to V_{CCQ}+0.3V	V
Voltage on Vcc supply relative to Vss		V_{CC}, V_{CCQ}	-0.2[2)] V_{CCQ}+0.3V	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Industrial	T_A	-40 to 85	°C

1. Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Undershoot at power-off : -1.0V in case of pulse width $\leq$ 20ns

FUNCTIONAL DESCRIPTION

CS#	OE#	WE#	LB#	UB#	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	X	X	X	X	High-Z	High-Z	Deselected	Stand by
L	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	L	H	L	L	Data Out	Data Out	Word Read	Active
L	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	X	L	L	L	Data In	Data In	Word Write	Active

Note:
1. X means don't care. (Must be low or high state)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.6	3.0	3.3	V
	V_{CCQ}	2.6	3.0	3.3	V
Ground	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	0.8 * V_{CCQ}	-	V_{CCQ} + 0.2[1)]	V
Input low voltage	V_{IL}	-0.2[2)]	-	0.2 * V_{CCQ}	V

1. Overshoot: Vcc +1.0 V in case of pulse width ≤ 20ns
2. Undershoot: -1.0 V in case of pulse width ≤ 20ns
3. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f =1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

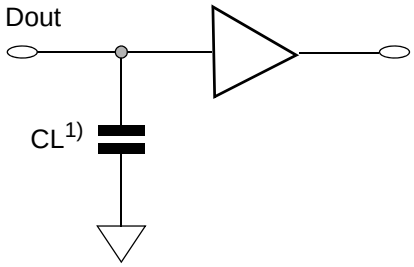
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=V_{SS} to V_{CCQ} , V_{CC}=V_{CCmax}	-1	-	1	uA
Output leakage current	I_{LO}	CS#=V_{IH} , OE#=V_{IH} or WE#=V_{IL} , V_{IO}=V_{SS} to V_{CCQ} , V_{CC}=V_{CCmax}	-1	-	1	uA
Average operating current	I_{CC1}	Cycle time = 1us, I_{IO}=0mA, 100% duty, CS#≤0.2V, , V_{IN}≤0.2V or V_{IN}≥V_{CCQ}-0.2V	-	-	5	mA
	I_{CC2}	Cycle time = Min, I_{IO}=0mA, 100% duty, CS#=V_{IL}, V_{IN}=V_{IL} or V_{IH}	-	-	25	mA
Output low voltage	V_{OL}	I_{OL} = 0.5mA, V_{CC}=V_{CCmin}	-	-	0.2*V_{CCQ}	V
Output high voltage	V_{OH}	I_{OH} = -0.5mA, V_{CC}=V_{CCmin}	0.8*V_{CCQ}	-	-	V
Standby current (CMOS)	I_{SB}	CS#≥V_{CCQ}-0.2V, Other inputs = 0 ~ V_{CCQ} (Typ. condition : V_{CC}=3.0V @ 25°C) (Max. condition : V_{CC}=3.3V @ 85°C)	-	-	120	uA

1. Maximum Icc specifications are tested with V_{CC} = V_{CCmax}.

AC OPERATING CONDITIONS

Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.2V to V_{CCQ}-0.2V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : $V_{CCQ}/2$
Output Load (See right) : $CL^{1)}$ = 30pF



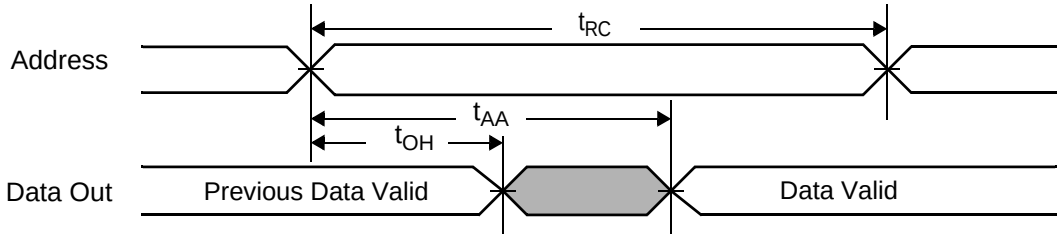
1. Including scope and Jig capacitance

AC CHARACTERISTICS

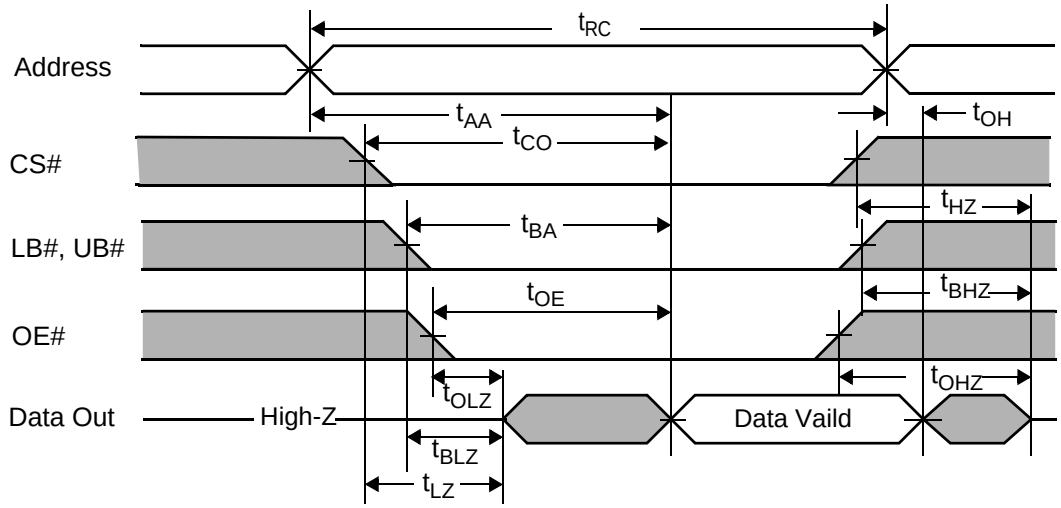
Parameter List		Symbol	Speed		Unit
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	10k	ns
	Address access time	t_{AA}	-	70	ns
	Chip enable to data output	t_{CO}	-	70	ns
	Output enable to valid output	t_{OE}	-	25	ns
	UB#, LB# enable to data output	t_{BA}	-	25	ns
	Chip enable to low-Z output	t_{LZ}	10	-	ns
	UB#, LB# enable to low-Z output	t_{BLZ}	0	-	ns
	Output enable to low-Z output	t_{OLZ}	0	-	ns
	Chip disable to high-Z output	t_{HZ}	0	20	ns
	UB#, LB# disable to high-Z output	t_{BHZ}	0	20	ns
	Output disable to high-Z output	t_{OHZ}	0	20	ns
	Output hold from Address change	t_{OH}	5	-	ns
Write	Write Cycle Time	t_{WC}	70	10k	ns
	Chip enable to end of write	t_{CW}	60	-	ns
	Address setup time	t_{AS}	0	-	ns
	Address valid to end of write	t_{AW}	60	-	ns
	UB#, LB# valid to end of write	t_{BW}	60	-	ns
	Write pulse width	t_{WP}	50	-	ns
	Write recovery time	t_{WR}	0	-	ns
	Write to output high-Z	t_{WHZ}	0	20	ns
	Data to write time overlap	t_{DW}	20	-	ns
	Data hold from write time	t_{DH}	0	-	ns
	End write to output low-Z	t_{OW}	5	-	ns

TIMING DIAGRAMS

READ CYCLE (1) (Address controlled, CS#=OE#=V_{IL}, WE#=V_{IH}, UB# or/and LB#=V_{IL})



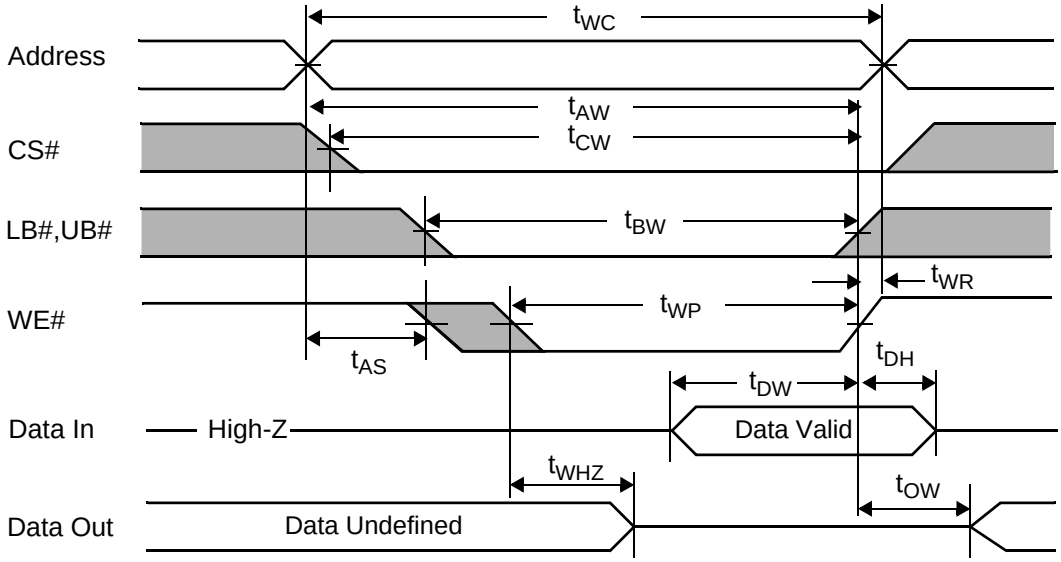
READ CYCLE (2) (WE#=V_{IH})



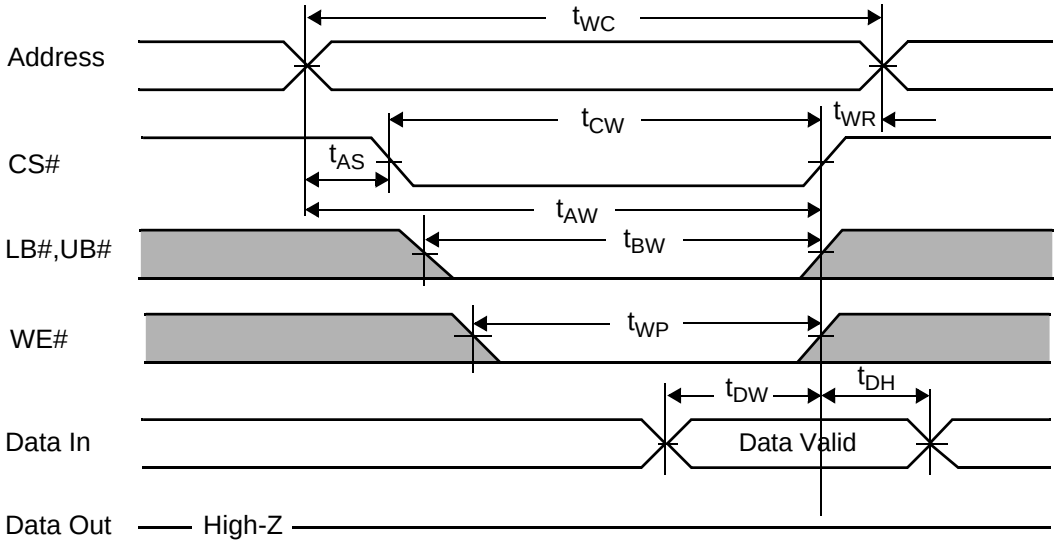
NOTES (READ CYCLE)

1. t_{HZ} , t_{BHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. Do not Access device with cycle timing shorter than t_{RC} for continuous periods > 10us.

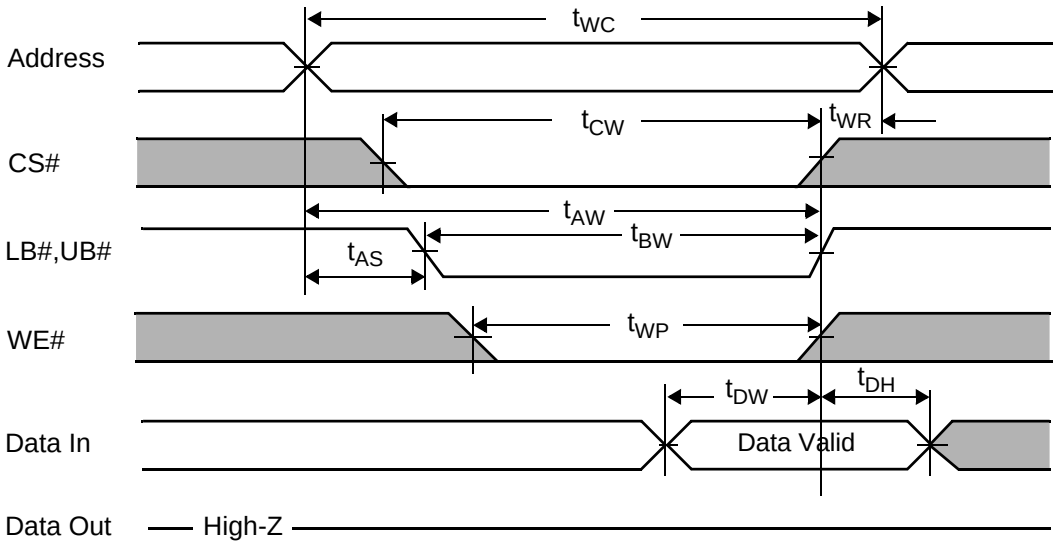
WRITE CYCLE (1) (WE# controlled)



WRITE CYCLE (2) (CS# controlled)



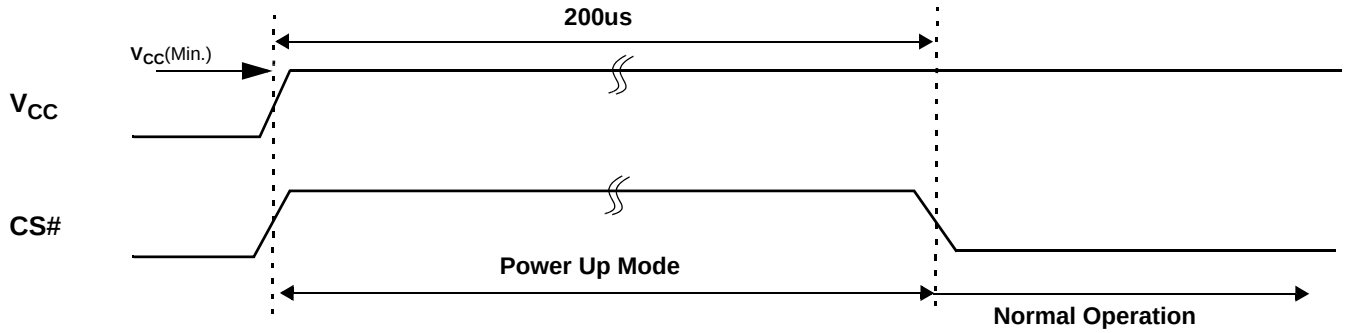
WRITE CYCLE (3) (UB#/LB# controlled)



NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low CS#, low WE# and low UB# or LB#. A write begins at the last transition among low CS# and low WE# with asserting UB# or LB# low for single byte operation or simultaneously asserting UB# and LB# low for word operation. A write ends at the earliest transition among high CS# and high WE#. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from CS# going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CS# or WE# going high.
5. Do not access device with cycle timing shorter than t_{WC} for continuous periods > 10us.

TIMING WAVEFORM OF POWER UP



NOTE (POWER UP)

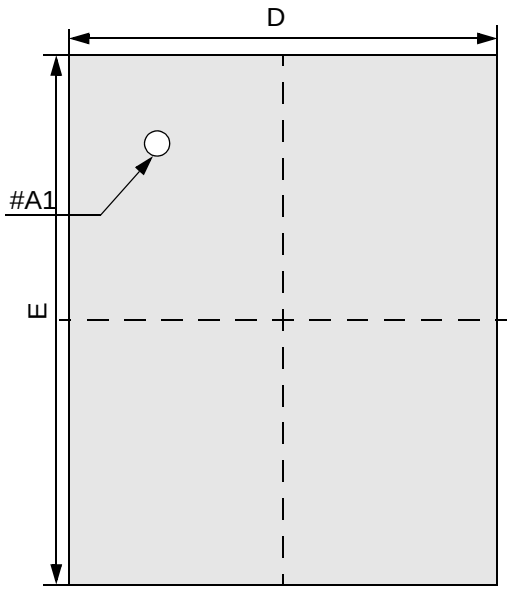
1. After Vcc reaches Vcc(Min.) , wait 200us with CS# high. Then you get into the normal operation.

Unit: millimeters

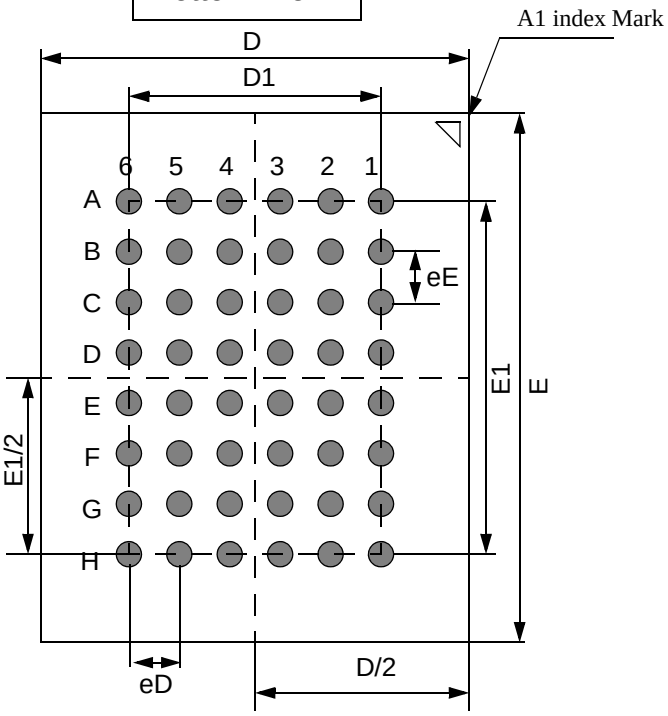
PACKAGE DIMENSION

48 Ball Fine Pitch BGA (0.75mm ball pitch)

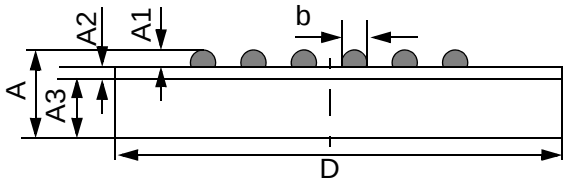
Top View



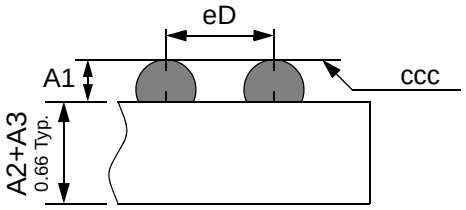
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.87	1.00
A1	0.22	-	0.32
A2	-	0.21	-
A3	-	0.45	-
b	0.35	-	0.45
D	5.90	6.00	6.10
E	6.90	7.00	7.10
D1	-	3.75	-
E1	-	5.25	-
eE	-	0.75	-
eD	-	0.75	-
ccc	-	-	0.08

NOTES.

1. Bump counts : 48(8row x 6column)
2. Bump pitch : (x,y)=(0.75x0.75) (typ.)
3. All tolerance are +/-0.050 unless otherwise specified.
4. Typ : Typical
5. ccc is coplanarity : 0.08(Max)
6.POST REFLOW ARE IN MILIMETER. (Pre Reflow Diameter : 0.35 +_ 0.02)
7. TOLERANCE INCLUDES WARPAGE.

PART NUMBERING SYSTEM

AS1C	2M16P	-70	B	I	N	XX
PSEUDO SRAM	2M16=2Mx16 P=PSEUDO SRAM	70ns	B = FBGA	I=Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free	PackingType None:Tray TR:Reel

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