Features

- Transient Protection for High-Speed Data Lines-to-GND and Lines-to-Lines.
- Provide Transient Protection for the Protected Differential Line Pair to
  IEC 61000-4-2 (ESD) ±30kV (contact/air)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 50A (8/20μs);
  IEC 61000-4-5 (Lightning) 1kV (10/700μs)
  Cable Discharge Event (CDE)
- DFN2525P10E (2.5x2.5mm) Package.
- Specific Pin Out For Easy Board Layout.
- Fast Turn-On and Low Clamping Voltage.
- Low Operating Voltage: 3.3V.
- Low Capacitance: 12pF Line-to-Line
- Low Leakage Current
- Solid-State Silicon-Avalanche and Active Circuit Triggering Technology.
- ***Green Part***

Applications

- WAN/LAN Device
- 10/100/1000 Ethernet
- Switching Systems
- Computers
- Instruments
- Differential Inputs

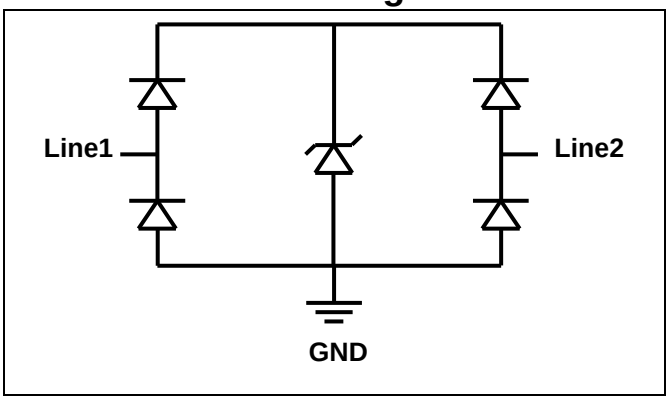
Description

AZ3233-02F is a design which includes surge rated clamping cells to protect high speed interfaces in an electronic systems. The AZ3233-02F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

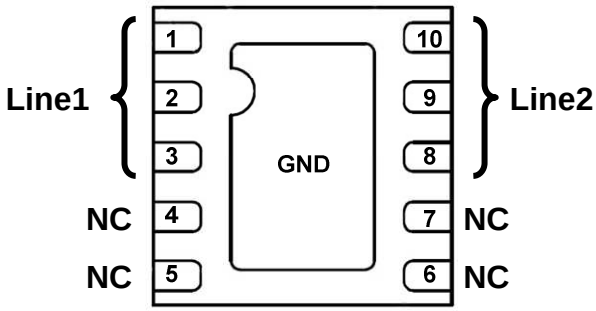
AZ3233-02F is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cells which is an equivalent TVS diode in a single package. During transient conditions, the proprietary clamping cells provide low clamping voltages to minimize the stress on the protected components.

AZ3233-02F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN2525P10E (2.5x2.5mm) (Top View)

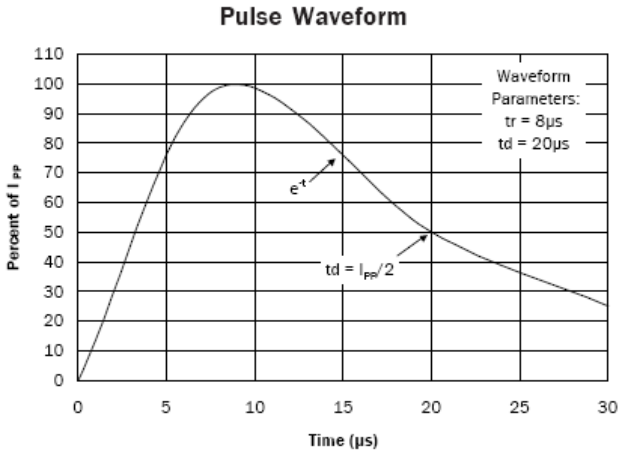
Pin Number	Description
1, 2, 3	I/O (Line1)
8, 9, 10	I/O (Line2)
4, 5, 6, 7	NC
Center Tab	Ground

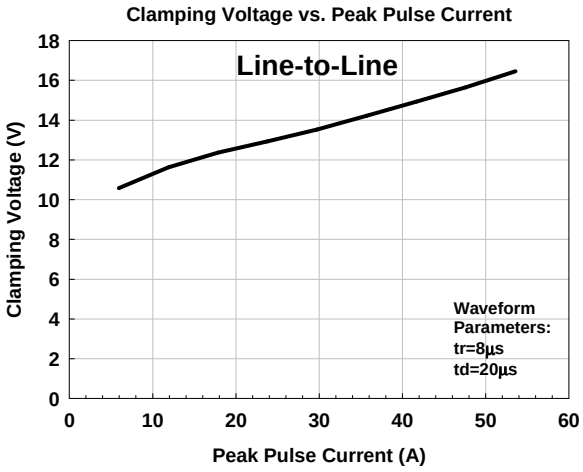
SPECIFICATIONS

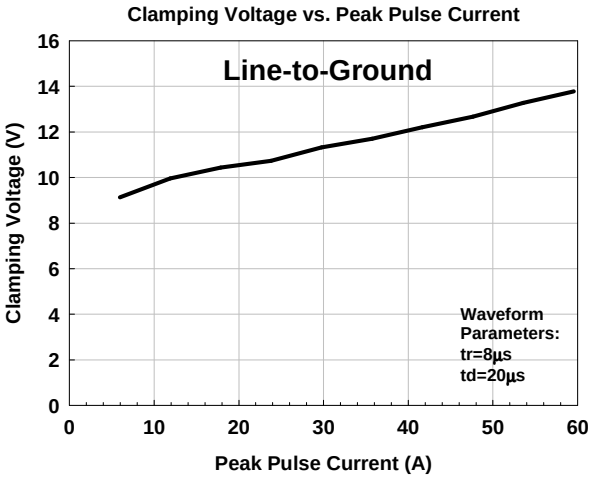
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20us)	I_{PP}	50	A
ESD per IEC 61000-4-2 (Contact /Air)	V_{ESD}	±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	^{o}C
Operating Temperature	T_{OP}	-55 to +125	^{o}C
Storage Temperature	T_{STO}	-55 to +150	^{o}C

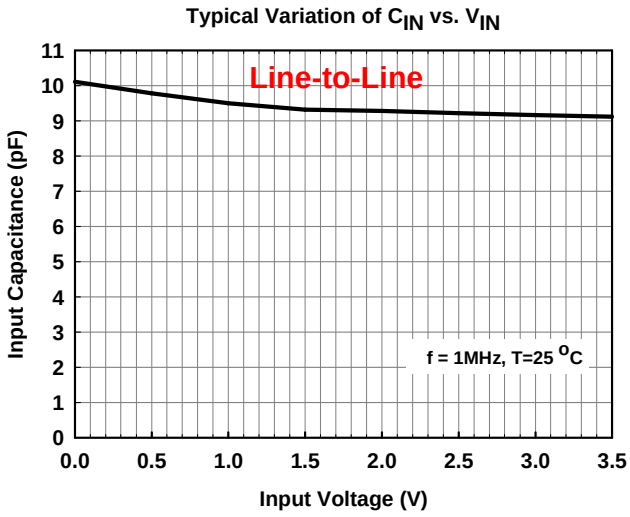
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Each Line to GND, T=25 ^{o}C.			3.3	V
Channel Leakage Current	I_{CH_Leak}	V_{RWM} = 3.3V, T=25 ^{o}C (Each Line to GND)			1	µA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 ^{o}C. (Each Line to GND)	3.9			V
Clamping Voltage	V_{CL}	I_{PP}=5A, tp=8/20us, T=25 ^{o}C. (Each Line to GND)		9.2	11	V
		I_{PP}=25A, tp=8/20us, T=25 ^{o}C. (Each Line to GND)		11	13	V
		I_{PP}=50A, tp=8/20us, T=25 ^{o}C. (Each Line to GND)		13	15	V
Channel Input Capacitance	C_{IN}	V_R = 0V, f = 1MHz, T=25 ^{o}C. (Each Line to GND)		20	25	pF
		V_R = 0V, f = 1MHz, T=25 ^{o}C. (Line to Line)		10	12	pF

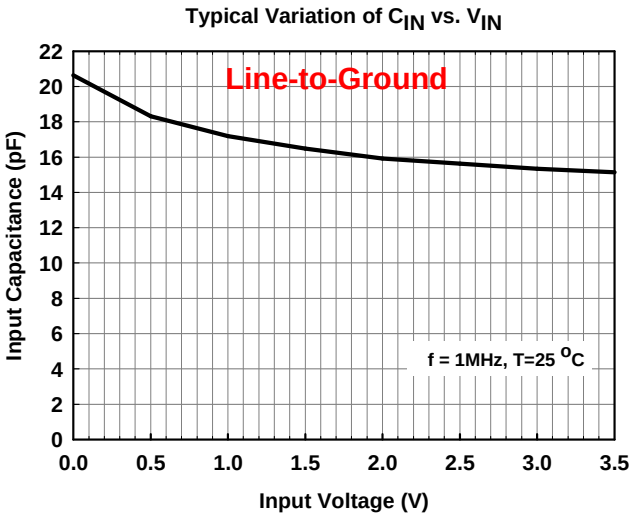
Typical Characteristics

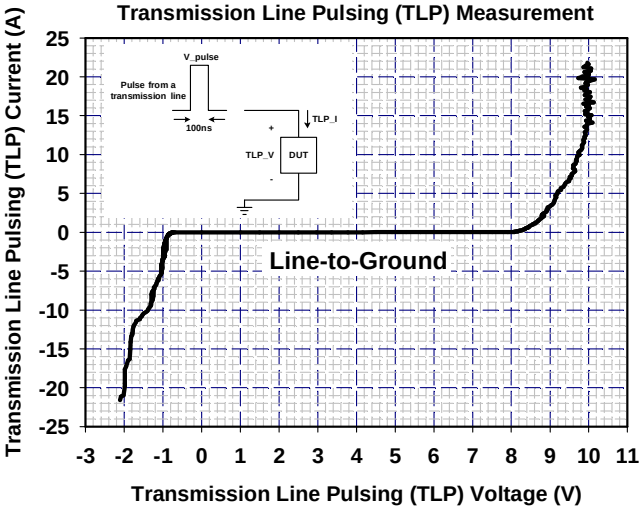












Applications Information

The AZ3233-02F is designed to protect two high speed data lines operating at 3.3 volts to against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The usage of the AZ3233-02F is shown in Fig. 1. It can be configured to protect one high speed line pair (two lines). The first line pair is connected to Pin-1, Pin-2, and Pin-3, simultaneously. The second line pair is connected to Pin-8, Pin-9, and Pin-10, simultaneously. The center tab of AZ3233-02F can be connected directly to a ground plane for lines-to-ground and lines-to-lines protection or floating for lines-to-lines protection only. To get minimum parasitic inductance, the path length should keep as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ3233-02F.
- Place the AZ3233-02F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transience easily injects to.

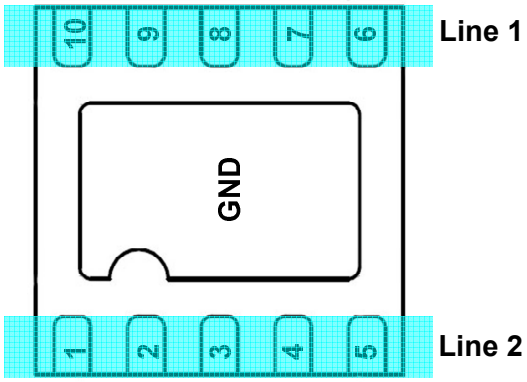
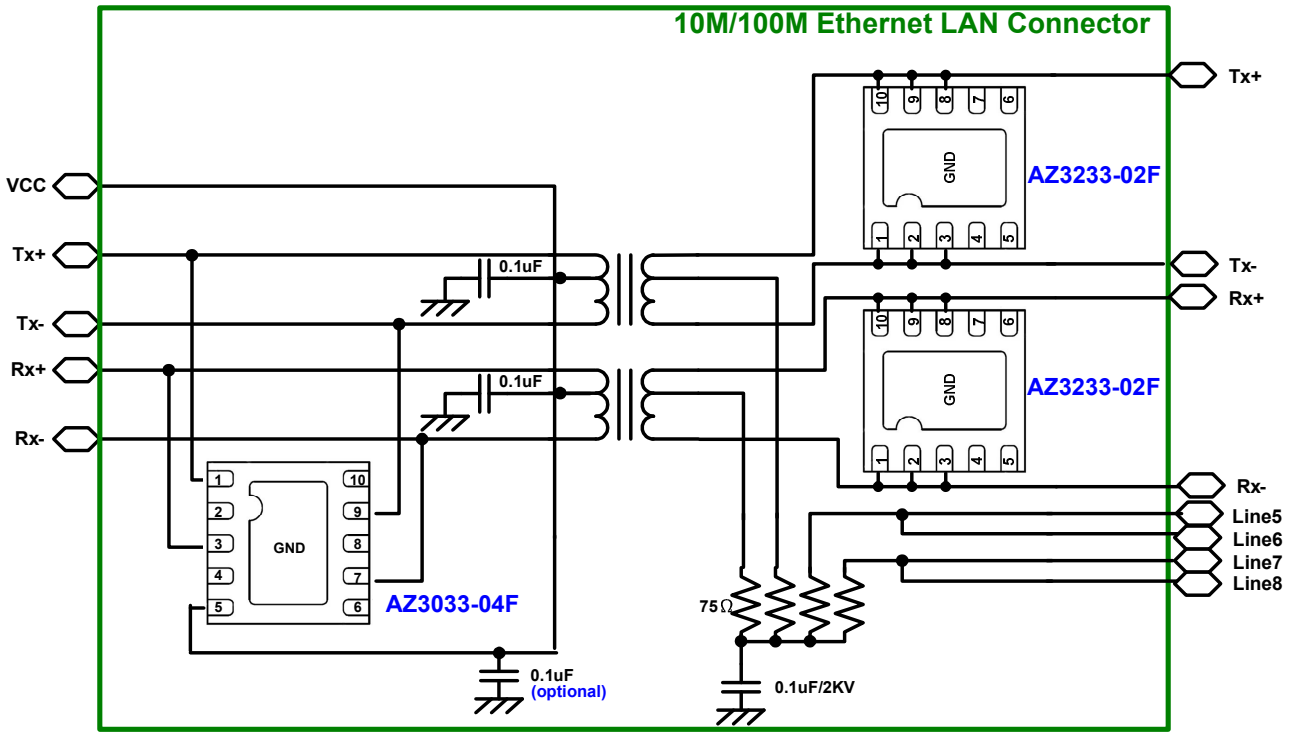
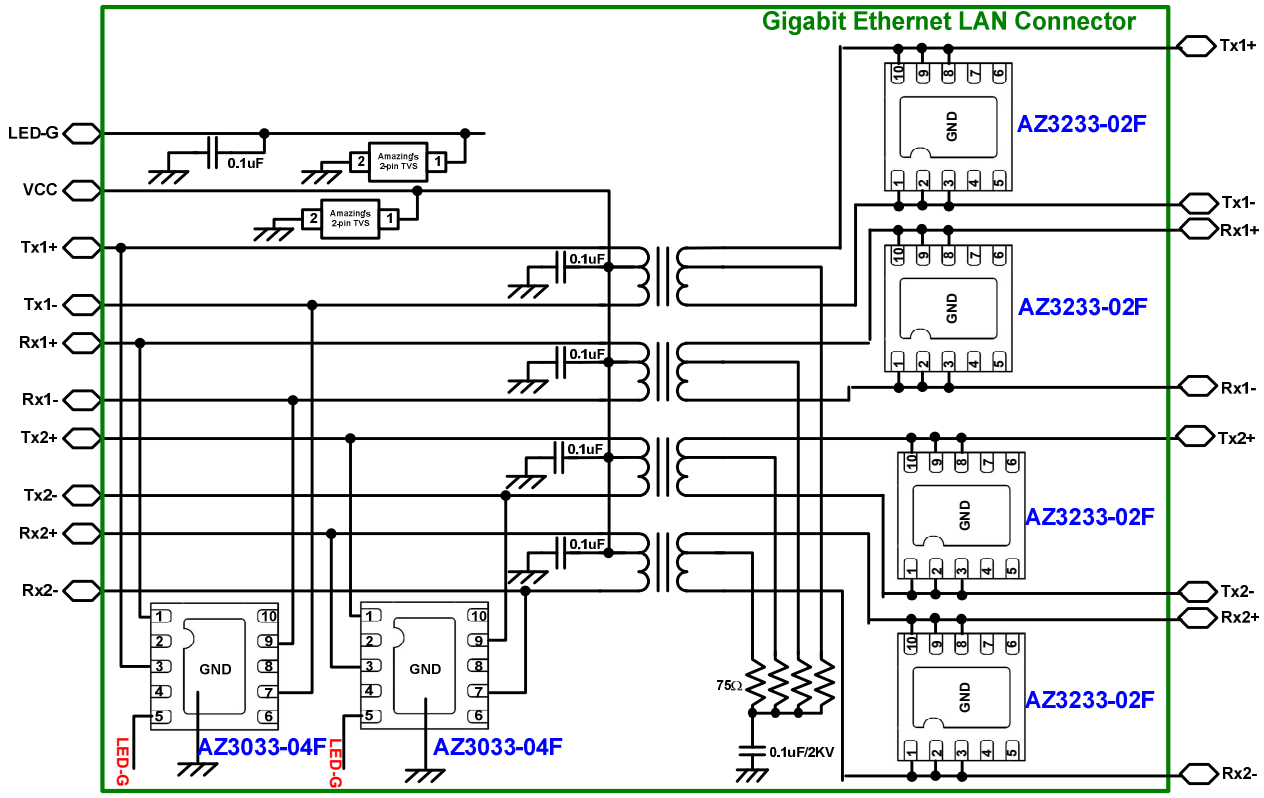


Fig. 1
Configuration for protecting differential line pairs

Typical Applications



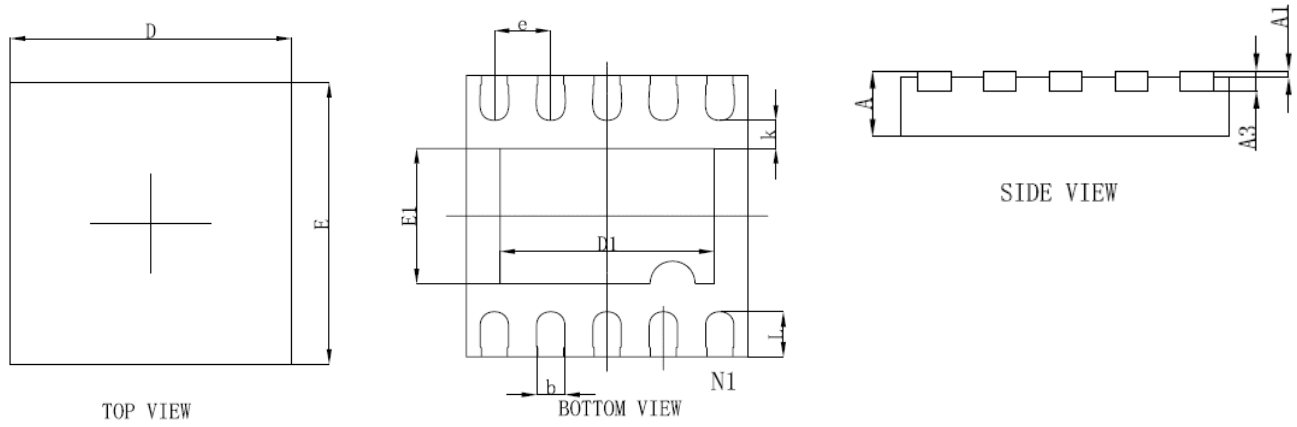
10M/100M Ethernet Protection Circuit



Gigabit Ethernet Protection Circuit

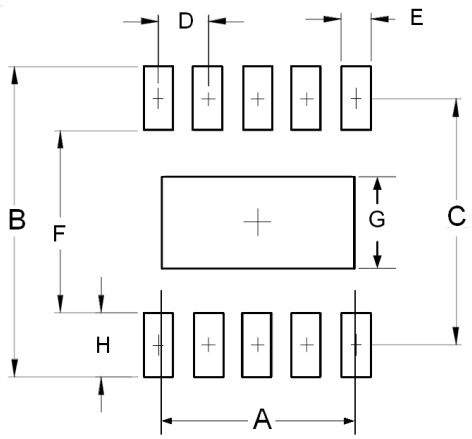
Mechanical Details

DFN2525P10E (2.5x2.5mm)
PACKAGE DIAGRAMS



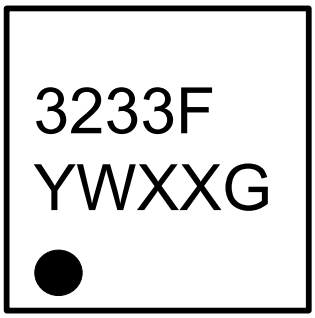
Symbol	Millimeters		Inches	
	min	max	min	max
A	0.45	0.60	0.018	0.024
A1	0.00	0.05	0.000	0.002
A3	0.152REF.		0.006 BSC	
D	2.45	2.55	0.096	0.100
E	2.45	2.55	0.096	0.100
D1	1.80	2.00	0.071	0.079
E1	1.10	1.30	0.043	0.051
b	0.20	0.30	0.008	0.012
e	0.5 BSC		0.019 BSC	
L	0.35	0.45	0.014	0.018

Land Layout



DIMENSIONS		
DIM	MILLIMETERS	INCHES
A	1.90	.075
B	3.10	.122
C	2.45	.096
D	0.50	.020
E	0.30	.012
F	1.80	.071
G	0.60	.024
H	0.65	.025

MARKING CODE



3233F = Device Code
YWXXG = Date Code

Part Number	Marking Code
AZ3233-02F (Green Part)	**3233F YWXXG**

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ3233-02F.R7G	Green	T/R	7 inch	3,000/reel	4 reel=12,000/box	6 box=72,000/carton

Revision History

Revision	Modification Description
Revision 2012/01/13	Preliminary Release.
Revision 2012/11/29	Formal Release.
Revision 2014/04/16	Add ordering information.