

## Au8014B: 3A Ultra Low Noise, Ultra Low Dropout Regulator

### General Description

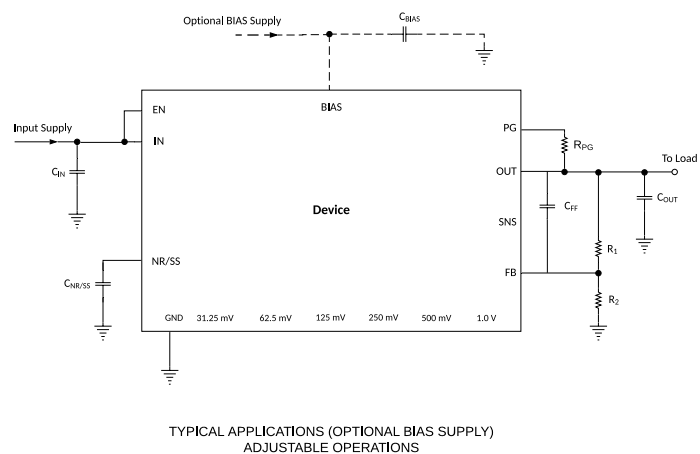
The Au8014B is a low-noise (4.3  $\mu$ VRMS), low-dropout linear regulator (LDO) capable of sourcing 3A with only 150 mV of dropout. The device output voltage is pin-programmable from 0.5 V to 2.468 V and adjustable from 0.5 V to 5.15 V using an external resistor divider.

Au8014B is the ideal choice to power noise-sensitive components found in high speed interfaces such as SERDES, 5G communication infrastructure such as High Speed ADCs, DACs and RF components due to its exceptional PSRR and low noise (4.3  $\mu$ VRMS) characteristics. The high PSRR and low noise combination of Au8014B limits power-supply induced phase noise and clock jitter.

The 5 V output capability of this device is well suited for RF amplifiers and RF front end. The Au8014B device is also well suited for digital loads such as ASICs, FPGAs, and DSPs that require a low-input voltage and low-output voltage to minimize power dissipation while providing excellent transient performance that caters to current steps in digital loads due to clock domain switching, dynamic power and frequency scaling. The soft-start capability minimizes in-rush current, thereby allowing for a smooth and reliable start-up at the system level.

### Features

- Low Dropout: 150 mV at 3 A
- 1.25% (max) Accuracy Over Line, Load, and Temperature
- Output Voltage Noise:
  - 4.3  $\mu$ VRMS at 0.5 V Output
  - 7.6  $\mu$ VRMS at 5.0 V Output
- Input Voltage Range:
  - Without BIAS: 1.4 V to 6.5 V
  - With BIAS: 1.1 V to 6.5 V
- Two Output Voltage Modes
  - 0.5 V to 5.15 V (Set by resistor divider)
  - 0.5 V to 2.468 V (Set via programming pins)
- Excellent PSRR of 38 dB at 1MHz
- Excellent Load Transient Response
- Adjustable Soft-Start In-Rush Control
- 3.5 mm x 3.5 mm, 20-Pin QFN



**Figure 1 Application Schematic**

### Applications

- 5G MIMO RF front end components
- Digital Loads: SerDes, FPGAs and DSPs
- High-speed Analog Circuits:
  - VCO, ADC, DAC, and LVDS

## Table of Contents

|   |    |
|---|----|
| General Description .....   | 1  |
| Features .....  | 1  |
| Applications.....   | 1  |
| 1 Pin Configuration.....  | 4  |
| 1.1 Pin Configuration Diagram.....  | 4  |
| 1.2 Pin Description.....  | 4  |
| 2 Electrical Specifications .....   | 5  |
| 2.1 Typical Characteristics.....  | 9  |
| 3 Detailed Description .....  | 10 |
| 3.1 Overview .....  | 10 |
| 3.2 Functional Block Diagram .....  | 11 |
| 3.3 Feature Description .....   | 11 |
| 3.3.1 Bias Rail.....  | 11 |
| 3.3.2 Power-Good Function .....   | 11 |
| 3.3.3 Programmable Soft-Start .....   | 11 |
| 3.3.4 Internal Current Limit (ILIM).....                                      | 11 |
| 3.3.5 Enable.....   | 12 |
| 3.3.6 Active Discharge Circuit.....   | 12 |
| 3.3.7 Undervoltage Lockout (UVLO).....  | 12 |
| 3.3.8 Thermal Protection.....   | 12 |
| 3.4 Device Functional Modes .....   | 12 |
| 3.4.1 Operation with $1.1\text{ V} \leq V_{IN} < 1.4\text{ V}$ .....          | 12 |
| 3.4.2 Operation with $1.4\text{ V} \leq V_{IN} \leq 6.5\text{ V}$ .....       | 12 |
| 3.4.3 Shutdown.....   | 12 |
| 4 Application and Implementation.....   | 13 |
| 4.1 Application Information .....   | 13 |
| 4.1.1 Recommended Capacitor Types .....                                       | 13 |
| 4.1.2 Input and Output Capacitor Requirements ( $C_{IN}$ and $C_{OUT}$ )..... | 13 |
| 4.1.3 Noise-Reduction and Soft-Start Capacitor ( $C_{NR/SS}$ ) .....          | 13 |
| 4.1.4 Feed-Forward Capacitor ( $C_{FF}$ ).....                                | 14 |
| 4.1.5 Optimizing Noise and PSRR.....  | 14 |
| 4.1.6 Adjustable Operation .....  | 14 |
| 4.1.7 Pin Programmable Output Configuration.....                              | 15 |
| 4.2 Typical Applications .....  | 15 |
| 4.2.1 Low-Input, Low-Output Voltage Conditions .....                          | 15 |
| 4.2.2 Typical Application for a 5.0-V Rail.....                               | 16 |
| 5 Package Information .....   | 18 |
| 18  |    |
| 6 Ordering Information .....  | 19 |
| 7 Revision History .....  | 20 |
| 8 Trademarks .....  | 20 |
| 9 Contact Information.....  | 20 |

## List of Tables

|  |   |
|--|---|
| Table 1 Pin Functions .....            | 4 |
| Table 2 Absolute Maximum Ratings ..... | 5 |

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|   |    |
|---|----|
| Table 3 ESD Ratings .....                           | 5  |
| Table 4 Recommended Operating Conditions .....      | 5  |
| Table 5 Thermal Information.....                    | 6  |
| Table 6 Electrical Specifications .....             | 6  |
| Table 7 Electrical Specifications (Continued) ..... | 7  |
| Table 8 Ordering Information .....                  | 19 |
| Table 9 Revision History .....                      | 20 |

**List of Figures**

|  |    |
|--|----|
| Figure 1 Application Schematic .....                   | 1  |
| Figure 2 Au8014B Pin Configuration .....               | 4  |
| Figure 3 PSRR vs Frequency and $I_{OUT}$ .....         | 9  |
| Figure 4 PSRR vs Frequency and $V_{IN}$ with Bias..... | 9  |
| Figure 5 PSRR vs Frequency and $V_{BIAS}$ .....        | 9  |
| Figure 6 Power On from EN .....                        | 9  |
| Figure 7 Load Transients .....                         | 10 |
| Figure 8 Noise PSD vs Frequency (CNRSS=10nF) .....     | 10 |
| Figure 9 Functional Block Diagram .....                | 11 |
| Figure 10 Adjustable Operation .....                   | 15 |
| Figure 11 Typical Application (Bias Supply) .....      | 16 |
| Figure 12 Typical Application.....                     | 17 |
| Figure 13 Package Information.....                     | 18 |

## 1 Pin Configuration

### 1.1 Pin Configuration Diagram

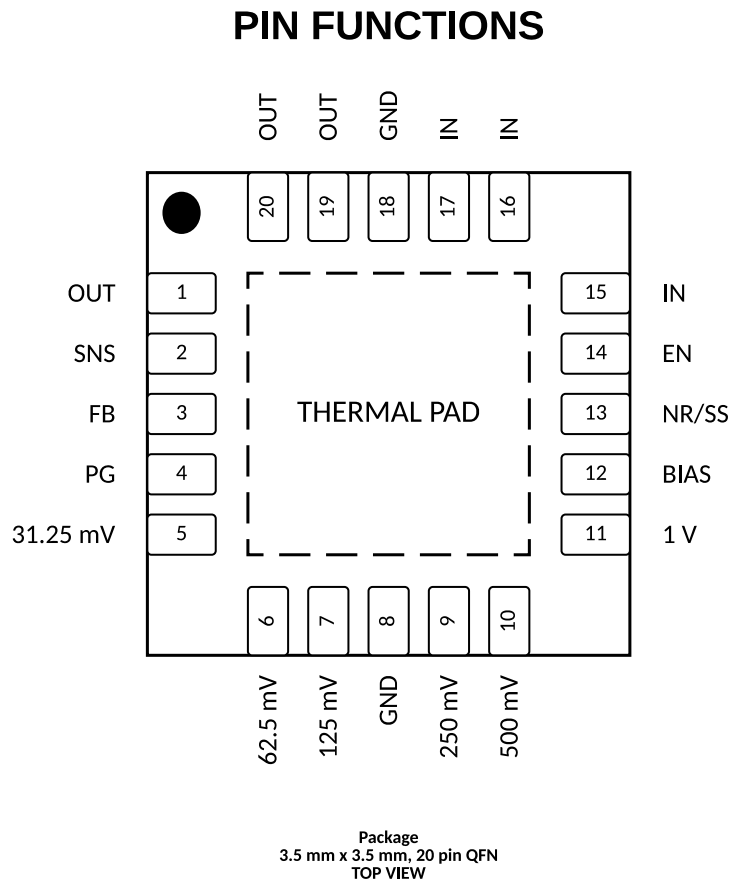


Figure 2 Au8014B Pin Configuration

### 1.2 Pin Description

Table 1 Pin Functions

| Pin Name | Pin No. | I/O | Description   |
|----------|---------|-----|---|
| 31.25 mV | 5       | I   | Programmable output voltage setting pins. Connect these pins to ground, SNS, or leave floating. Connecting these pins to ground increases the output voltage, whereas connecting these pins to SNS increases the resolution of the programmable network but decreases the range of the network; multiple pins can be simultaneously connected to GND or SNS to select the desired output voltage. Leave these pins floating (open) when not in use.         |
| 62.5 mV  | 6       |     |   |
| 125 mV   | 7       |     |   |
| 250 mV   | 9       |     |   |
| 500 mV   | 10      |     |   |
| 1.0 V    | 11      |     |   |
| BIAS     | 12      | I   | BIAS supply voltage. This pin enables the use of low-input voltage, low-output voltage conditions (that is, $V_{IN} = 1.1\text{ V}$ , $V_{OUT} = 0.5\text{ V}$ ) to reduce power dissipation across the die. The use of a BIAS voltage improves dc and ac performance for $V_{IN} \leq 1.4\text{ V}$ . A 10 $\mu\text{F}$ capacitor or larger must be connected between this pin and ground. If not used, this pin must be left floating or tied to ground. |
| EN       | 14      | I   | Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device. If enable functionality is not required, this pin must be connected to IN. If enable functionality is required, $V_{EN}$ must go high after $V_{IN}$ is established when a BIAS supply is used.   |

| Pin Name    | Pin No.   | I/O | Description  |
|-------------|-----------|-----|--|
| FB          | 3         | I   | Feedback pin connected to the error amplifier. Although not required, a 10 nF feed-forward capacitor from FB to OUT (as close to the device as possible) is recommended to maximize ac and noise performance.  |
| GND         | 8, 18     | —   | Ground pin. These pins must be connected to ground, the thermal pad, and each other with a low-impedance connection.   |
| IN          | 15-17     | I   | Input supply voltage pin. A 47 $\mu$ F or larger ceramic capacitor (25 $\mu$ F or greater of capacitance) from IN to ground is recommended to reduce the impedance of the input supply. Place the input capacitor as close to the input as possible.   |
| NR/SS       | 13        | —   | Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function. Although not required, a 10 nF or larger capacitor is recommended to be connected from NR/SS to GND (as close to the pin as possible) to maximize ac performance. |
| OUT         | 1, 19, 20 | O   | Regulated output pin. A 47 $\mu$ F or larger ceramic capacitor (25 $\mu$ F or greater of capacitance) from OUT to ground is required for stability and must be placed as close to the output as possible. Minimize the impedance from the OUT pin to the load.   |
| PG          | 4         | O   | Active-high, power-good pin. An open-drain output indicates when the output voltage reaches 89.3% of the target. The use of a feed-forward capacitor can disrupt PG (power good) functionality.  |
| SNS         | 2         | I   | Output voltage sense input pin. This pin connects the internal R <sub>1</sub> resistor to the output. Connect this pin to the load side of the output trace only if the programmable output feature is used.   |
| Thermal pad |           | —   | Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.  |

## 2 Electrical Specifications

**Table 2 Absolute Maximum Ratings**

Over junction temperature range (unless otherwise noted) <sup>[1]</sup>

| Parameter                                      | Pin  | Min                | Max                                  | Units |
|--|--|--------------------|--------------------------------------|-------|
| Voltage  | IN, BIAS, PG, EN                             | -0.3               | 7.0                                  | V     |
|  | SNS, OUT                                     | -0.3               | V <sub>IN</sub> + 0.3 <sup>[2]</sup> | V     |
|  | NR/SS, FB                                    | -0.3               | 3.6                                  | V     |
|  | 50 mV, 100 mV, 200 mV, 400 mV, 800 mV, 1.6 V | -0.3               | V <sub>OUT</sub> + 0.3               | V     |
| Current  | OUT  | Internally limited |                                      | A     |
|  | PG (sink current into device)                |                    | 5                                    | mA    |
| Operating junction temperature, T <sub>J</sub> |  | -40                | 125                                  | °C    |
| Storage temperature, T <sub>STG</sub>          |  | -55                | 160                                  | °C    |

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 3. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
- The absolute maximum rating is V<sub>IN</sub> + 0.3 V or 7.0 V, whichever is smaller.

**Table 3 ESD Ratings**

| Parameter                | Conditions         | Symbols          | Value | Units |
|--------------------------|--------------------|------------------|-------|-------|
| Electro Static Discharge | Human Body Model   | V <sub>ESD</sub> | ±2000 | V     |
|                          | Charged Body Model |                  | ±500  |       |

**Table 4 Recommended Operating Conditions**

Over junction temperature range (unless otherwise noted)

| Parameter                                | Symbol      | Min | Typ                              | Max      | Unit         |
|--|-------------|-----|----------------------------------|----------|--------------|
| Input supply voltage range               | $V_{IN}$    | 1.1 |                                  | 6.5      | V            |
| Bias supply voltage range <sup>[1]</sup> | $V_{BIAS}$  | 3.0 |                                  | 6.5      | V            |
| Output voltage range <sup>[2]</sup>      | $V_{OUT}$   | 0.5 |                                  | 5.15     | V            |
| Enable voltage range                     | $V_{EN}$    | 0   |                                  | $V_{IN}$ | V            |
| Output current                           | $I_{OUT}$   | 0   |                                  | 3        | A            |
| Input capacitor                          | $C_{IN}$    | 10  | 47                               |          | $\mu$ F      |
| Output capacitor                         | $C_{OUT}$   | 47  | $47 \parallel 10 \parallel 10^3$ |          | $\mu$ F      |
| Power-good pullup resistance             | $R_{PG}$    | 10  |                                  | 100      | k $\Omega$   |
| NR/SS capacitor                          | $C_{NR/SS}$ |     | 10                               |          | nF           |
| Feed-forward capacitor                   | $C_{FF}$    |     | 10                               |          | nF           |
| Operating junction temperature           | $T_J$       | -40 |                                  | 125      | $^{\circ}$ C |

Notes:

- BIAS supply is required when the  $V_{IN}$  supply is below 1.4 V. Conversely, no BIAS supply is required when the  $V_{IN}$  supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for  $V_{IN} \leq 1.4$  V.
- This output voltage range does not include device accuracy or accuracy of the feedback resistors.
- The recommended output capacitors are selected to optimize PSRR for the frequency range of 900 kHz to 1.1MHz. This frequency range is a typical value for DC-DC supplies.

**Table 5 Thermal Information**

| Thermal Metric                             | Symbol             | Au8014B QFN 20 PINS | Unit           |
|--|--------------------|---------------------|----------------|
| Junction-to-ambient thermal resistance     | $R_{\theta JA}$    | 35.4                | $^{\circ}$ C/W |
| Junction-to-case(top) thermal resistance   | $R_{\theta JC}$    | 27.9                | $^{\circ}$ C/W |
| Junction-to-board thermal resistance       | $R_{\theta JB}$    | 26.59               | $^{\circ}$ C/W |
| Junction-to-top characterization parameter | $\psi_{\theta JT}$ | 0.39                | $^{\circ}$ C/W |

**Table 6 Electrical Specifications**

Over operating junction temperature range ( $T_J = -40$   $^{\circ}$ C to  $+125$   $^{\circ}$ C),  $V_{IN} = 1.4$  V or  $V_{IN} = V_{OUT(nom)} + 0.4$  V (whichever is greater),  $V_{BIAS} = \text{open}$ ,  $V_{OUT(nom)} = 0.5$  V <sup>[1]</sup>,  $V_{EN} = 1.1$  V,  $C_{IN} = 10$   $\mu$ F,  $C_{OUT} = 47$   $\mu$ F,  $C_{NR/SS}$  without  $C_{FF}$ , and PG pin pulled up to  $V_{IN}$  with 100 k $\Omega$ , unless otherwise noted. Typical values are at  $T_J = 25$   $^{\circ}$ C.

| Parameter                                 | Condition  | Symbol   | Min       | Typ    | Max   | Units |
|---|--|--|-----------|--------|-------|-------|
| Input supply voltage range <sup>[2]</sup> |  | $V_{IN}$   | 1.1       |        | 6.5   | V     |
| Bias supply voltage range <sup>[2]</sup>  | $V_{IN} = 1.1$ V   | $V_{BIAS}$   | 3.0       |        | 6.5   | V     |
| Feedback voltage                          |  | $V_{FB}$   |           | 0.5    |       | V     |
| NR/SS pin voltage                         |  | $V_{NR/SS}$  |           | 0.5    |       | V     |
| Input supply UVLO with BIAS               | $V_{IN}$ rising with $V_{BIAS} = 3.0$ V                                      | $V_{UVLO1(IN)}$  |           | 1.02   | 1.085 | V     |
| $V_{UVLO1(IN)}$ hysteresis                | $V_{BIAS} = 3.0$ V   | $V_{HYS1(IN)}$   |           | 320    |       | mV    |
| Input supply UVLO without BIAS            | $V_{IN}$ rising  | $V_{UVLO2(IN)}$  |           | 1.31   | 1.39  | V     |
| $V_{UVLO2(IN)}$ hysteresis                |  | $V_{HYS2(IN)}$   |           | 250    |       | mV    |
| Bias supply UVLO                          | $V_{BIAS}$ rising, $V_{IN} = 1.1$ V  | $V_{ULOV(BIAS)}$   |           | 2.83   | 2.9   | V     |
| $V_{UVLO(BIAS)}$ hysteresis               | $V_{IN} = 1.1$ V   | $V_{HYS(BIAS)}$  |           | 290    |       | mV    |
| Output Voltage                            | Range  | Using pin programmability  | $V_{OUT}$ | 0.5    | 2.468 | V     |
|   |  | Using external resistors   | $V_{OUT}$ | 0.5    | 5.15  | V     |
|   | Accuracy <sup>[3][4]</sup>   | $0.5 \text{ V} \leq V_{OUT} \leq 5.15 \text{ V}$ ,<br>$5 \text{ mA} \leq I_{OUT} \leq 3 \text{ A}$ , over $V_{IN}$                                   | $V_{OUT}$ | -1.25% | 1.25% | %     |
|   | Accuracy with BIAS   | $1.1 \text{ V} \leq V_{IN} \leq 2.2 \text{ V}$ ,<br>$5 \text{ mA} \leq I_{OUT} \leq 3 \text{ A}$ ,<br>$3 \text{ V} \leq V_{BIAS} \leq 6.5 \text{ V}$ | $V_{OUT}$ | -1.25% | 1.25% |       |
| Line regulation                           | $I_{OUT} = 5 \text{ mA}$ ,<br>$1.4 \text{ V} \leq V_{IN} \leq 6.5 \text{ V}$ | $\Delta V_{OUT} / \Delta V_{IN}$   |           | 0.01   |       | mV/V  |

| Parameter                   | Condition   | Symbol  | Min | Typ  | Max | Units         |
|-----------------------------|---|---|-----|------|-----|---------------|
| Load regulation             | $5 \text{ mA} \leq I_{\text{OUT}} \leq 3 \text{ A}$ ,<br>$3.0 \text{ V} \leq V_{\text{BIAS}} \leq 6.5 \text{ V}$ ,<br>$V_{\text{IN}} = 1.1 \text{ V}$ | $\Delta V_{\text{OUT}} / \Delta I_{\text{OUT}}$ |     | 0.07 |     | mV/A          |
|                             | $5 \text{ mA} \leq I_{\text{OUT}} \leq 3 \text{ A}$   |   |     | 0.08 |     |               |
|                             | $5 \text{ mA} \leq I_{\text{OUT}} \leq 3 \text{ A}$ ,<br>$V_{\text{OUT}} = 5.0 \text{ V}$   |   |     | 0.4  |     |               |
| Dropout voltage             | $V_{\text{IN}} = 1.4 \text{ V}$ , $I_{\text{OUT}} = 3 \text{ A}$ ,<br>$V_{\text{FB}} = 0.5 \text{ V}$   | $V_{\text{DO}}$                                 |     | 150  | 250 | mV            |
|                             | $V_{\text{IN}} = 5.4 \text{ V}$ , $I_{\text{OUT}} = 3 \text{ A}$ ,<br>$V_{\text{FB}} = 0.5 \text{ V}$   |   |     | 115  | 250 |               |
|                             | $V_{\text{IN}} = 5.6 \text{ V}$ , $I_{\text{OUT}} = 3 \text{ A}$ ,<br>$V_{\text{FB}} = 0.5 \text{ V}$   |   |     | 120  | 250 |               |
|                             | $V_{\text{IN}} = 1.1 \text{ V}$ , $V_{\text{BIAS}} = 5.0 \text{ V}$ ,<br>$I_{\text{OUT}} = 3 \text{ A}$ , $V_{\text{FB}} = 0.5 \text{ V}$             |   |     | 110  | 180 |               |
| Output current limit        | $V_{\text{OUT}}$ forced at<br>$0.9 \times V_{\text{OUT(nom)}}$ ,<br>$V_{\text{IN}} = V_{\text{OUT(nom)}} + 0.4 \text{ V}$                             | $I_{\text{LIM}}$                                | 3.7 | 4.2  | 4.7 | A             |
| Short-circuit current limit | $R_{\text{LOAD}} = 20 \text{ m}\Omega$ , under<br>foldback operation  | $I_{\text{SC}}$                                 |     | 1    |     | A             |
| GND pin current             | $V_{\text{IN}} = 6.5 \text{ V}$ , $I_{\text{OUT}} = 5 \text{ mA}$   | $I_{\text{GND}}$                                |     | 1.95 |     | mA            |
|                             | $V_{\text{IN}} = 1.4 \text{ V}$ , $I_{\text{OUT}} = 3 \text{ A}$  |   |     | 2.4  |     | mA            |
|                             | Shutdown, PG = open,<br>$V_{\text{IN}} = 6.5 \text{ V}$ , $V_{\text{EN}} = 0.5 \text{ V}$   |   |     | 1.2  | 25  | $\mu\text{A}$ |

**Notes:**

- $V_{\text{OUT(nom)}}$  is the calculated  $V_{\text{OUT}}$  target value from the programmable pins in a fixed configuration. In an adjustable configuration,  $V_{\text{OUT(nom)}}$  is the expected  $V_{\text{OUT}}$  value set by the external feedback resistors.
- BIAS supply is required when the  $V_{\text{IN}}$  supply is below 1.4 V. Conversely, no BIAS supply is required when the  $V_{\text{IN}}$  supply is higher than or equal to 1.4 V. A BIAS supply helps improve dc and ac performance for  $V_{\text{IN}} \leq 1.4 \text{ V}$ .
- When the device is connected to external feedback resistors at the FB pin, external resistor tolerances are not included.
- The device is not tested under conditions where  $V_{\text{IN}} > V_{\text{OUT}} + 1.7 \text{ V}$  and  $I_{\text{OUT}} = 3 \text{ A}$ , because the power dissipation is higher than the maximum rating of the package.

**Table 7 Electrical Specifications (Continued)**

Over operating junction temperature range ( $T_{\text{J}} = -40 \text{ }^\circ\text{C}$  to  $+125 \text{ }^\circ\text{C}$ ),  $V_{\text{IN}} = 1.4 \text{ V}$  or  $V_{\text{IN}} = V_{\text{OUT(nom)}} + 0.4 \text{ V}$  (whichever is greater),  $V_{\text{BIAS}} = \text{open}$ ,  $V_{\text{OUT(nom)}} = 0.5 \text{ V}^{(1)}$ ,  $V_{\text{EN}} = 1.1 \text{ V}$ ,  $C_{\text{IN}} = 10 \text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 47 \text{ }\mu\text{F}$ ,  $C_{\text{NR/SS}}$  without  $C_{\text{FF}}$ , and PG pin pulled up to  $V_{\text{IN}}$  with  $100 \text{ k}\Omega$ , unless otherwise noted. Typical values are at  $T_{\text{J}} = 25 \text{ }^\circ\text{C}$ .

| Parameter  | Conditions   | Symbol               | Min                          | Typ                            | Max                          | Unit          |
|--|--|----------------------|------------------------------|--------------------------------|------------------------------|---------------|
| EN pin current                                     | $V_{\text{IN}} = 6.5 \text{ V}$ , $V_{\text{EN}} = 0 \text{ V}$<br>and $6.5 \text{ V}$   | $I_{\text{EN}}$      |                              |                                | 0.1                          | $\mu\text{A}$ |
| BIAS pin current                                   | $V_{\text{IN}} = 1.1 \text{ V}$ , $V_{\text{BIAS}} = 6.5 \text{ V}$ ,<br>$V_{\text{OUT(nom)}} = 0.5 \text{ V}$ ,<br>$I_{\text{OUT}} = 3 \text{ A}$ | $I_{\text{BIAS}}$    |                              | 2.3                            | 3.5                          | mA            |
| EN pin low-level input voltage<br>(disable device) |  | $V_{\text{IL(EN)}}$  | 0                            |                                | 0.5                          | V             |
| EN pin high-level input voltage<br>(enable device) |  | $V_{\text{IH(EN)}}$  | 1.1                          |                                | 6.5                          | V             |
| PG pin threshold                                   | For falling $V_{\text{OUT}}$   | $V_{\text{IT(PG)}}$  | $82\% \times V_{\text{OUT}}$ | $88.3\% \times V_{\text{OUT}}$ | $93\% \times V_{\text{OUT}}$ | V             |
| PG pin hysteresis                                  | For rising $V_{\text{OUT}}$  | $V_{\text{HYS(PG)}}$ |                              | $1\% \times V_{\text{OUT}}$    |                              | V             |
| PG pin low-level output voltage                    | $V_{\text{OUT}} < V_{\text{IT(PG)}}$ , $I_{\text{PG}} = -1 \text{ mA}$<br>(current into device)  | $V_{\text{OL(PG)}}$  |                              |                                | 0.4                          | V             |
| PG pin leakage current                             | $V_{\text{OUT}} > V_{\text{IT(PG)}}$ , $V_{\text{PG}} = 6.5 \text{ V}$   | $I_{\text{IKG(PG)}}$ |                              |                                | 0.1                          | $\mu\text{A}$ |
| NR/SS pin charging current                         | $V_{\text{NR/SS}} = \text{GND}$ ,<br>$V_{\text{IN}} = 6.5 \text{ V}$   | $I_{\text{NR/SS}}$   | 4.0                          | 6.2                            | 9.0                          | $\mu\text{A}$ |
| FB pin leakage current                             | $V_{\text{IN}} = 6.5 \text{ V}$  | $I_{\text{FB}}$      | -100                         |                                | 100                          | nA            |

| Parameter                      | Conditions   | Symbol   | Min | Typ | Max | Unit                |    |
|--------------------------------|--|----------|-----|-----|-----|---------------------|----|
| Power-supply ripple rejection  | $V_{IN} - V_{OUT} = 0.4\text{ V}$ ,<br>$I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$<br>$F = 10\text{ kHz}$ , $V_{OUT} = 0.5\text{ V}$ ,<br>$V_{BIAS} = 5.0\text{ V}$        | PSRR     |     | 55  |     | dB                  |    |
|                                | $V_{IN} - V_{OUT} = 0.4\text{ V}$ ,<br>$I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$<br>$F = 500\text{ kHz}$ , $V_{OUT} = 0.5\text{ V}$ ,<br>$V_{BIAS} = 5.0\text{ V}$       |          |     | 36  |     | dB                  |    |
|                                | $V_{IN} - V_{OUT} = 0.4\text{ V}$ ,<br>$I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$<br>$F = 1\text{ MHz}$ , $V_{OUT} = 0.5\text{ V}$ ,<br>$V_{BIAS} = 5.0\text{ V}$         |          |     |     | 38  |                     | dB |
|                                | $V_{IN} - V_{OUT} = 0.4\text{ V}$ ,<br>$I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$<br>$F = 10\text{ kHz}$ , $V_{OUT} = 5.0\text{ V}$                                       |          |     |     | 48  |                     | dB |
|                                | $V_{IN} - V_{OUT} = 0.4\text{ V}$ ,<br>$I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$<br>$F = 500\text{ kHz}$ ,<br>$V_{OUT} = 5.0\text{ V}$                                   |          |     |     |     | 36                  | dB |
|                                | $V_{IN} - V_{OUT} = 0.4\text{ V}$ ,<br>$I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$<br>$F = 1\text{ MHz}$ , $V_{OUT} = 5.0\text{ V}$  |          |     |     |     | 38                  | dB |
|                                | $V_{IN} - V_{OUT} = 0.4\text{ V}$ ,<br>$I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$   |          |     |     |     |                     |    |
| Output noise voltage           | $BW = 10\text{ Hz to }100\text{ kHz}$ ,<br>$V_{IN} = 1.1\text{ V}$ , $V_{OUT} = 0.5\text{ V}$ ,<br>$V_{BIAS} = 5.0\text{ V}$ , $I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$ | $V_N$    |     | 4.3 |     | $\mu\text{V}_{RMS}$ |    |
|                                | $BW = 10\text{ Hz to }100\text{ kHz}$ ,<br>$V_{OUT} = 5.0\text{ V}$ , $I_{OUT} = 3\text{ A}$ ,<br>$C_{NR/SS} = 100\text{ nF}$ ,<br>$C_{FF} = 10\text{ nF}$ ,<br>$C_{OUT} = 47\mu\text{F}  10\mu\text{F}  10\mu\text{F}$  |          |     |     | 7.6 |                     |    |
| Thermal shutdown temperature   | Shutdown, temperature increasing   | $T_{SD}$ |     | 150 |     | °C                  |    |
|                                | Reset, temperature decreasing  |          |     | 130 |     |                     |    |
| Operating junction temperature |  | $T_J$    | -40 |     | 125 | °C                  |    |

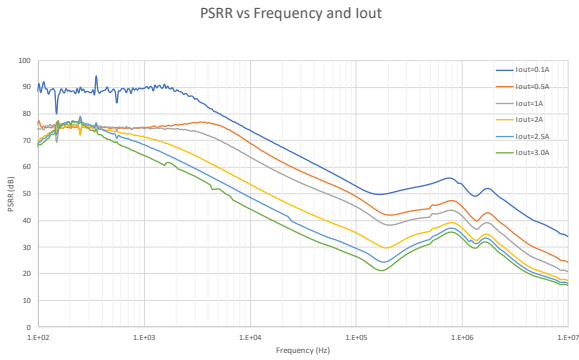
**Notes:**

- $V_{OUT(nom)}$  is the calculated  $V_{OUT}$  target value from the programmable pins in a fixed configuration. In an adjustable configuration,  $V_{OUT(nom)}$  is the expected  $V_{OUT}$  value set by the external feedback resistors.



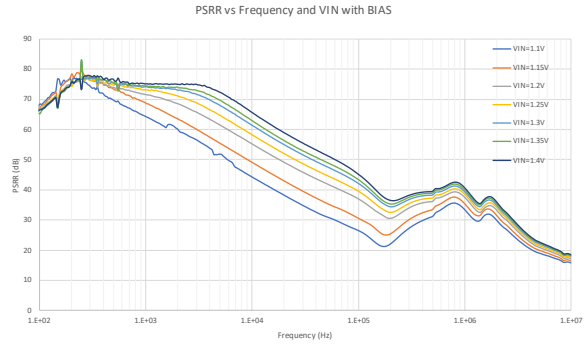
## 2.1 Typical Characteristics

The following graphs are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 1.4\text{ V}$  or  $V_{IN} = V_{OUT(NOM)} + 0.4\text{ V}$  (whichever is greater),  $V_{BIAS} = \text{open}$ ,  $V_{OUT(NOM)} = 0.5\text{ V}$ ,  $V_{EN} = 1.1\text{ V}$ ,  $C_{OUT} = 47\text{ }\mu\text{F}$ ,  $C_{NR/SS} = 0\text{ nF}$ ,  $C_{FF} = 0\text{ nF}$ , and PG pin pulled up to  $V_{IN}$  with  $100\text{ k}\Omega$  (unless otherwise noted).



$V_{IN}=1.1\text{V}$ ,  $V_{out}=0.5\text{V}$ ,  $V_{BIAS}=5\text{V}$ ,  $C_{OUT}=(47+10+10)\mu\text{F}$ ,  $C_{SS}=10\text{nF}$ ,  $C_{FF}=10\text{nF}$

Figure 3 PSRR vs Frequency and  $I_{out}$



$V_{out}=0.5\text{V}$ ,  $V_{BIAS}=5\text{V}$ ,  $I_{out}=3\text{A}$ ,  $C_{OUT}=(47+10+10)\mu\text{F}$ ,  $C_{SS}=10\text{nF}$ ,  $C_{FF}=10\text{nF}$

Figure 4 PSRR vs Frequency and  $V_{IN}$  with Bias

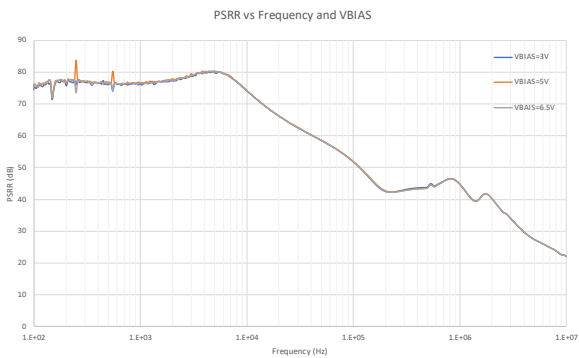


Figure 5 PSRR vs Frequency and  $V_{BIAS}$

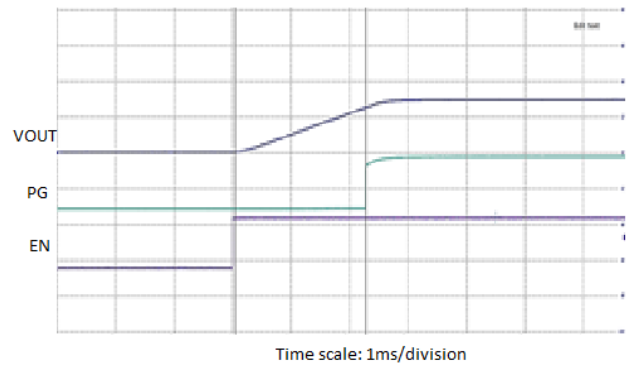


Figure 6 Power On from EN

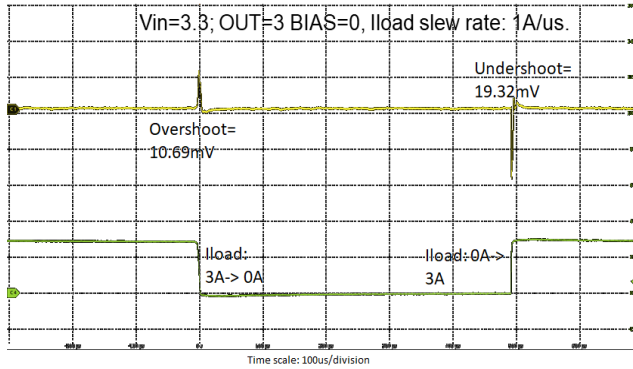


Figure 7 Load Transients

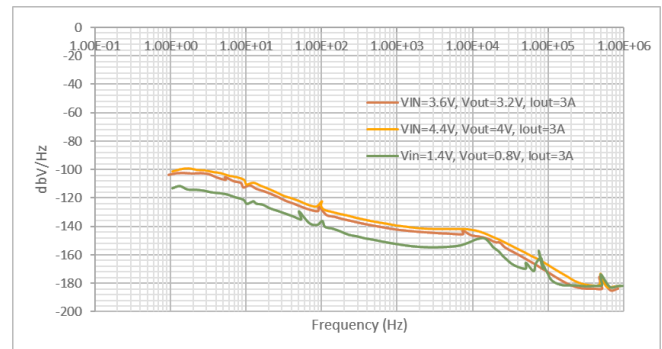


Figure 8 Noise PSD vs Frequency (CNRSS=10nF)

### 3 Detailed Description

#### 3.1 Overview

The Au8014B is a high-current (3 A), low-noise (4.3  $\mu$ V<sub>RMS</sub>), high accuracy (1%) low-dropout linear voltage regulator (LDO). These features make the device a robust solution to solve many challenging problems in generating a clean, accurate power supply.

The Au8014B has several features that make the device useful in a variety of applications. As detailed in the Functional Block Diagram section, these features include:

- Low-noise, high-PSRR output
- Programmable resistor network
- Optional bias rail
- Power-good output
- Programmable soft-start
- Foldback current limit
- Enable circuitry
- Active discharge
- Thermal protection

Overall, these features make the Au8014B the component of choice because of its versatility and ability to generate a supply for most applications.

### 3.2 Functional Block Diagram

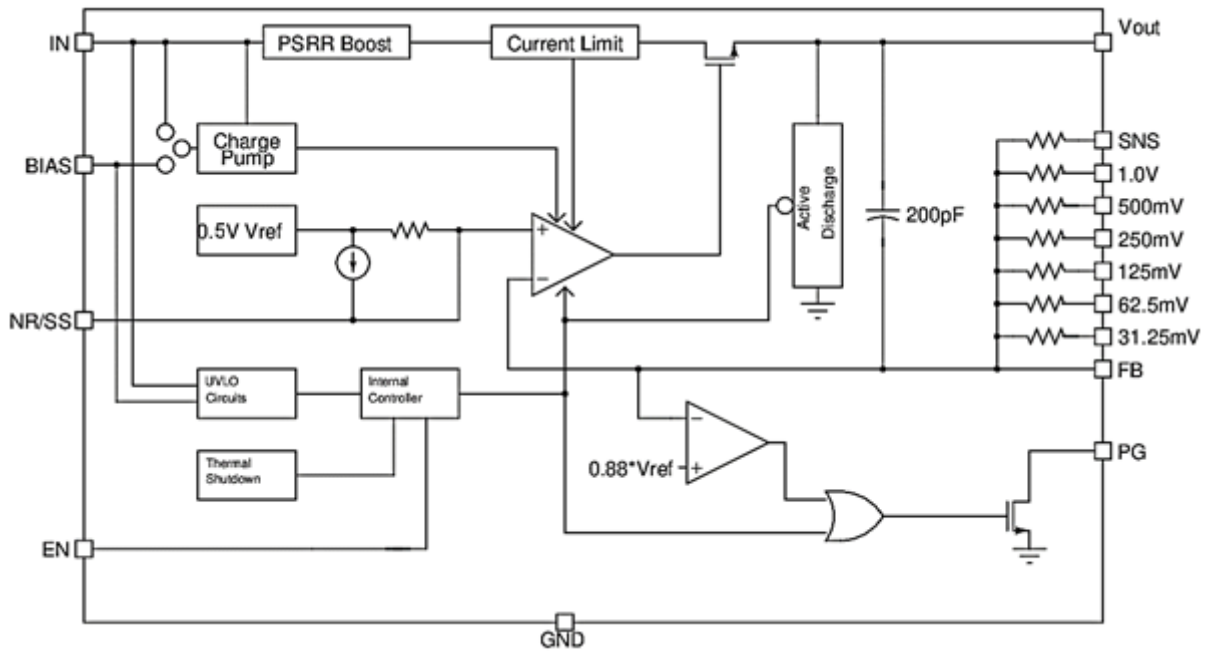


Figure 9 Functional Block Diagram

### 3.3 Feature Description

#### 3.3.1 Bias Rail

The device features a bias rail to enable low-input voltage, low-output voltage operation by providing power to the internal circuitry of the device. The bias rail is required for operation with  $V_{IN} < 1.4\text{ V}$ . An internal power MUX supplies the greater of either the input voltage or the bias voltage to an internal charge pump to power the internal circuitry.

#### 3.3.2 Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices. Using a pullup resistor from 10 k $\Omega$  to 100 k $\Omega$  is recommended. The use of a feed-forward capacitor ( $C_{FF}$ ) can cause glitches on start-up, and the power-good circuit may not function normally below the minimum input supply range.

#### 3.3.3 Programmable Soft-Start

Soft-start refers to the ramp-up time of the output voltage during LDO turn-on after EN and UVLO exceed the respective threshold voltage. The noise-reduction capacitor ( $C_{NR/SS}$ ) serves a dual purpose of both governing output noise reduction and programming the soft-start ramp time during turn-on. The start-up ramp is monotonic and linear in most conditions, however there is a small set of conditions that cause a small initial jump in output voltage.

#### 3.3.4 Internal Current Limit (ILIM)

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. During a current-limit event, the LDO sources constant current; therefore, the output voltage falls with decreased load impedance. Thermal shutdown can activate during a current limit event because of the high-power dissipation typically found in these conditions. To ensure proper operation of the current limit, minimize the inductances to the input and load. Continuous operation in current limit is not recommended.

### 3.3.5 Enable

The enable pin for the Au8014B is active high. The output of the Au8014B is turned on when the enable pin voltage is greater than its rising voltage threshold (1.1 V, max), and is turned off when the enable pin voltage is less than its falling voltage threshold (0.5 V, min). A voltage less than 0.5 V on the enable pin disables all internal circuits. At the next turn-on this voltage ensures a normal start up waveform with in-rush control, provided there is enough time to discharge the output capacitance.

When the enable functionality is not desired, EN must be tied to  $V_{IN}$ . However, when the enable functionality is desired, the enable voltage must come after  $V_{IN}$  is above  $V_{UVLO1(IN)}$  when a BIAS rail is used.

### 3.3.6 Active Discharge Circuit

The Au8014B has an internal pulldown MOSFET that connects a resistance of several hundred ohms to ground when the device is disabled to actively discharge the output voltage when the device is disabled.

Do not rely on the active discharge circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can possibly flow from the output to the input.

### 3.3.7 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit monitors the input and bias voltage ( $V_{IN}$  and  $V_{BIAS}$ , respectively) to prevent the device from turning on before  $V_{IN}$  and  $V_{BIAS}$  rise above the lockout voltage. The UVLO circuit also disables the output of the device when  $V_{IN}$  or  $V_{BIAS}$  fall below the lockout voltage. The UVLO circuit responds quickly to glitches on  $V_{IN}$  or  $V_{BIAS}$  and attempts to disable the output of the device if either of these rails collapse. As a result of the fast response time of the input supply UVLO circuit, fast and short line transients well below the input supply UVLO falling threshold can cause momentary glitches when asserted or when recovered from the transient.

### 3.3.8 Thermal Protection

The Au8014B contains a thermal shutdown protection circuit to disable the device when thermal junction temperature ( $T_J$ ) of the main pass-FET exceeds 150°C (typical). Thermal shutdown hysteresis assures that the LDO resets again (turns on) when the temperature falls to 130°C (typical). The thermal time constant of the semiconductor die is fairly short, and thus the device cycles on and off when thermal shutdown is reached until the power dissipation is reduced. For reliable operation, limit the junction temperature to a maximum of 125 °C. Operation above 125 °C can cause the device to exceed its operational specifications. Although the internal protection circuitry of the Au8014B is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the Au8014B into thermal shutdown or above a junction temperature of 125 °C reduces long-term reliability.

## 3.4 Device Functional Modes

### 3.4.1 Operation with $1.1\text{ V} \leq V_{IN} < 1.4\text{ V}$

The Au8014B requires a bias voltage on the BIAS pin greater than or equal to 3.0 V if the high-current input supply voltage is between 1.1 V to 1.4 V. The bias voltage pin consumes 2.4 mA, nominally.

### 3.4.2 Operation with $1.4\text{ V} \leq V_{IN} \leq 6.5\text{ V}$

If the input voltage is equal to or exceeds 1.4 V, no BIAS voltage is required. The Au8014B is powered from either the input supply or the BIAS supply, whichever is greater.

### 3.4.3 Shutdown

Shutting down the device reduces the ground current of the device to a maximum of 25  $\mu\text{A}$ .

## 4 Application and Implementation

NOTE: Information in the following applications sections is not part of the Aura Semiconductor component specification, and Aura Semiconductor does not warrant its accuracy or completeness. Aura Semiconductor's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 4.1 Application Information

The Au8014B is a linear voltage regulator with an input range of 1.1 V to 6.5 V and an output voltage range of 0.5 V to 5.0 V with a 1% accuracy and a 3 A maximum output current. The Au8014B has an integrated charge pump for ease of use and an external bias rail to allow for the lowest dropout across the entire output voltage range.

#### 4.1.1 Recommended Capacitor Types

The Au8014B is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and noise-reduction pin (NR, pin 13). Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high  $V_{IN}$  and  $V_{OUT}$  conditions (that is,  $V_{IN} = 5.5$  V to  $V_{OUT} = 5.0$  V) the derating can be greater than 50% and must be taken into consideration.

#### 4.1.2 Input and Output Capacitor Requirements ( $C_{IN}$ and $C_{OUT}$ )

The Au8014B is designed and characterized for operation with ceramic capacitors of 47  $\mu$ F or greater (22  $\mu$ F or greater of capacitance) at the output and 10  $\mu$ F or greater (5  $\mu$ F or greater of capacitance) at the input. Place the capacitors as close to the pins as possible to minimize ringing.

#### 4.1.3 Noise-Reduction and Soft-Start Capacitor ( $C_{NR/SS}$ )

The Au8014B features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ( $C_{NR/SS}$ ). The use of an external  $C_{NR/SS}$  is highly recommended, especially to minimize in-rush current into the output capacitors. This soft-start eliminates power-up initialization problems when powering field-programmable processors. The controlled voltage ramp of the output also reduces peak in-rush current during start-up, minimizing start-up transients to the input power bus.

Soft-start ramp time can be calculated with Equation 1:

$$t_{SS} = (V_{NR/SS} \times C_{NR/SS}) / I_{NR/SS} \quad (1)$$

Note that  $I_{NR/SS}$  is provided in [Table 6](#) and has a typical value of 6  $\mu$ A.

The noise-reduction capacitor, in conjunction with the noise-reduction resistor, forms a low pass filter (LPF) that filters out the noise from the reference before being gained up with the error amplifier, thereby reducing the device noise floor. The LPF is a single-pole filter and the cutoff frequency can be calculated with Equation 2. The typical value of  $R_{NR}$  is 1 M $\Omega$ . Increasing the  $C_{NR/SS}$  capacitor has a greater affect because the output voltage increases when the noise from the reference is gained up even more at higher output voltages. For low-noise applications, a 10 nF to 1  $\mu$ F  $C_{NR/SS}$  is recommended.

$$f_{cutoff} = 1 / (2 \times \pi \times R_{NR} \times C_{NR/SS}) \quad (2)$$

#### 4.1.4 Feed-Forward Capacitor ( $C_{FF}$ )

Although a feed-forward capacitor ( $C_{FF}$ ) from the FB pin to the OUT pin is not required to achieve stability, a 10 nF external feed-forward capacitor optimizes the transient, noise, and PSRR performance. A higher capacitance  $C_{FF}$  can be used; however, the start-up time is longer and the power-good signal can incorrectly indicate that the output voltage is settled.

#### 4.1.5 Optimizing Noise and PSRR

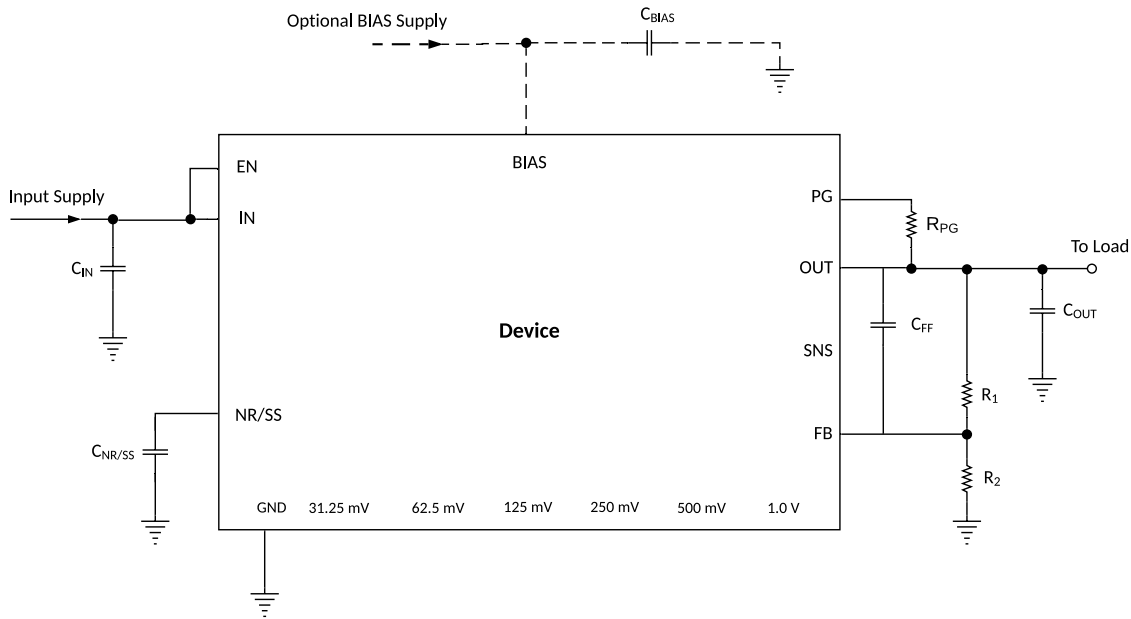
The ultra-low noise floor and PSRR of the device can be improved by careful selection of:

- $C_{NR/SS}$  for the low-frequency range
- $C_{FF}$  in the mid-band frequency range
- $C_{OUT}$  for the high-frequency range
- $V_{IN} - V_{OUT}$  for all frequencies, and

A larger noise-reduction capacitor improves low-frequency PSRR by filtering any noise coupling from the input into the reference. The feed-forward capacitor can be optimized to place a pole-zero pair near the edge of the loop bandwidth and push out the loop bandwidth, thus improving mid-band PSRR. Larger output capacitors and various output capacitors can be used to improve high-frequency PSRR.

#### 4.1.6 Adjustable Operation

The Au8014B can be used either with the internal programmable output network or by using external resistors. Using the programmable output network allows the Au8014B to be programmed from 0.5 V to 2.468 V. To extend this output voltage range to 5.0 V, external resistors must be used. This configuration is referred to as the adjustable configuration of the Au8014B throughout this document. Regardless of whether the internal resistor network or the external resistors are used, the output voltage is set by the two resistors, as shown in [Figure 10](#). Using the internal resistor ensures a 1% accuracy and minimizes the number of external components.



TYPICAL APPLICATIONS (OPTIONAL BIAS SUPPLY)  
ADJUSTABLE OPERATIONS

**Figure 10 Adjustable Operation**

R1 and R2 can be calculated for any output voltage range using Equation 3. This resistive network must provide a current equal to or greater than 5  $\mu$ A for dc accuracy. Using an R1 of 12.1 k $\Omega$  is recommended to optimize the noise and PSRR.

$$V_{OUT} = V_{NR/SS} \times (1 + R1 / R2) \tag{3}$$

#### 4.1.7 Pin Programmable Output Configuration

The output voltage of Au8014B can be set by an internal resistor network. The internal resistor network is accessed through pins 5,6,7,9,10,11. The default output voltage when all pin-programmable pins are floated is 0.5 V. Connecting the pin-programmable pins to GND raises the output voltage from 0.5V by the amount described in the pin’s name.

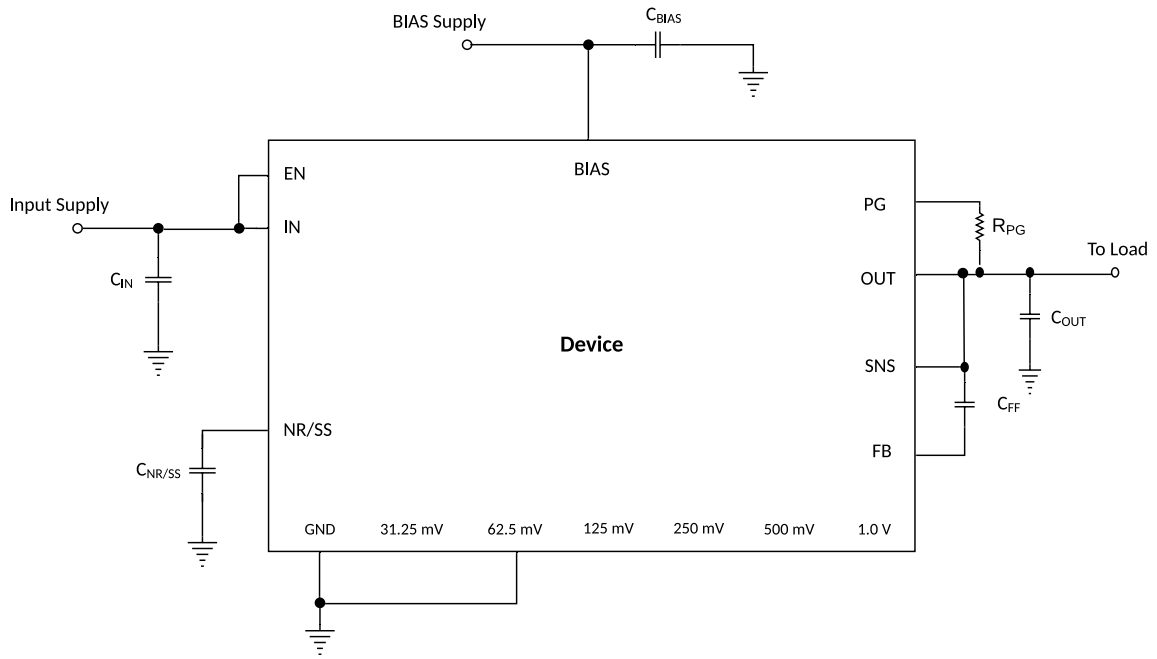
**Table 8 Pin Programmability vs Output Voltage**

| Pin             | Additive increment in output voltage |
|-----------------|--------------------------------------|
| Pin5 (31.25 mV) | 31.25 mV                             |
| Pin6 (62.5 mV)  | 62.5 mV                              |
| Pin7 (125 mV)   | 125 mV                               |
| Pin9 (250 mV)   | 250 mV                               |
| Pin10 (500 mV)  | 500 mV                               |
| Pin11 (1 V)     | 1 V                                  |

## 4.2 Typical Applications

### 4.2.1 Low-Input, Low-Output Voltage Conditions

This section discusses the implementation of the Au8014B using the programmable output configuration to regulate a 3.0 A load requiring good PSRR at high frequency with low-noise at 0.5 V using a 1.1 V input voltage and a 5.0 V bias supply. The schematic for this typical application circuit is provided in



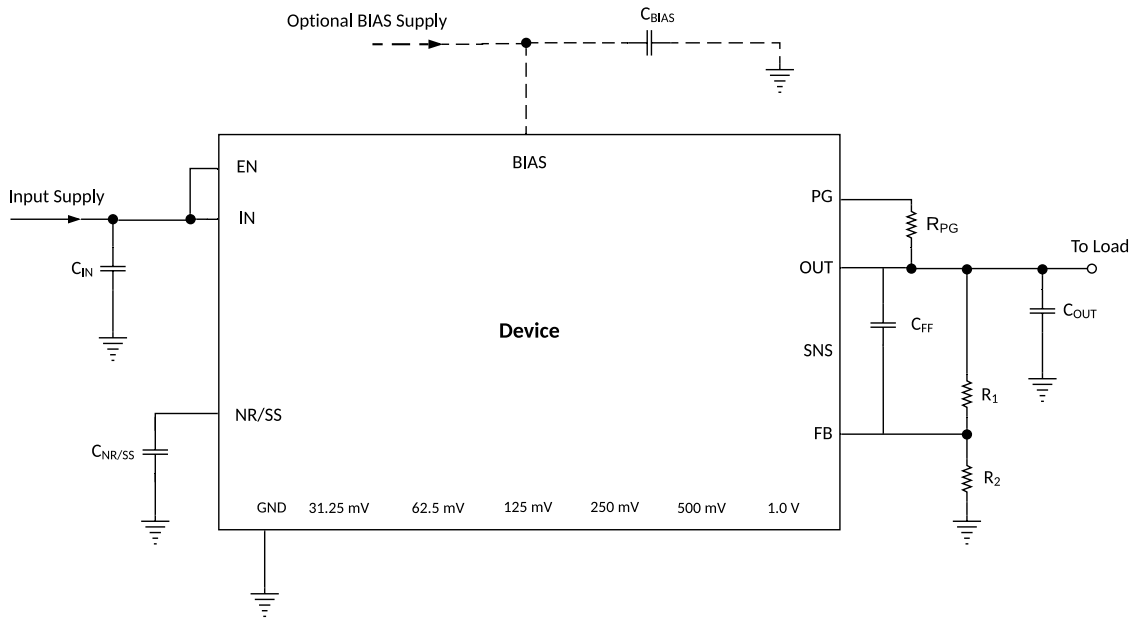
TYPICAL APPLICATION (BIAS SUPPLY)

**Figure 11 Typical Application (Bias Supply)**

#### 4.2.2 Typical Application for a 5.0-V Rail

This section discusses the implementation of the Au8014B using an adjustable feedback network to regulate a 3 A load requiring good PSRR at high frequency with low-noise at an output voltage of 5.0 V.





TYPICAL APPLICATIONS (OPTIONAL BIAS SUPPLY)  
ADJUSTABLE OPERATIONS

**Figure 12 Typical Application**

## 5 Package Information

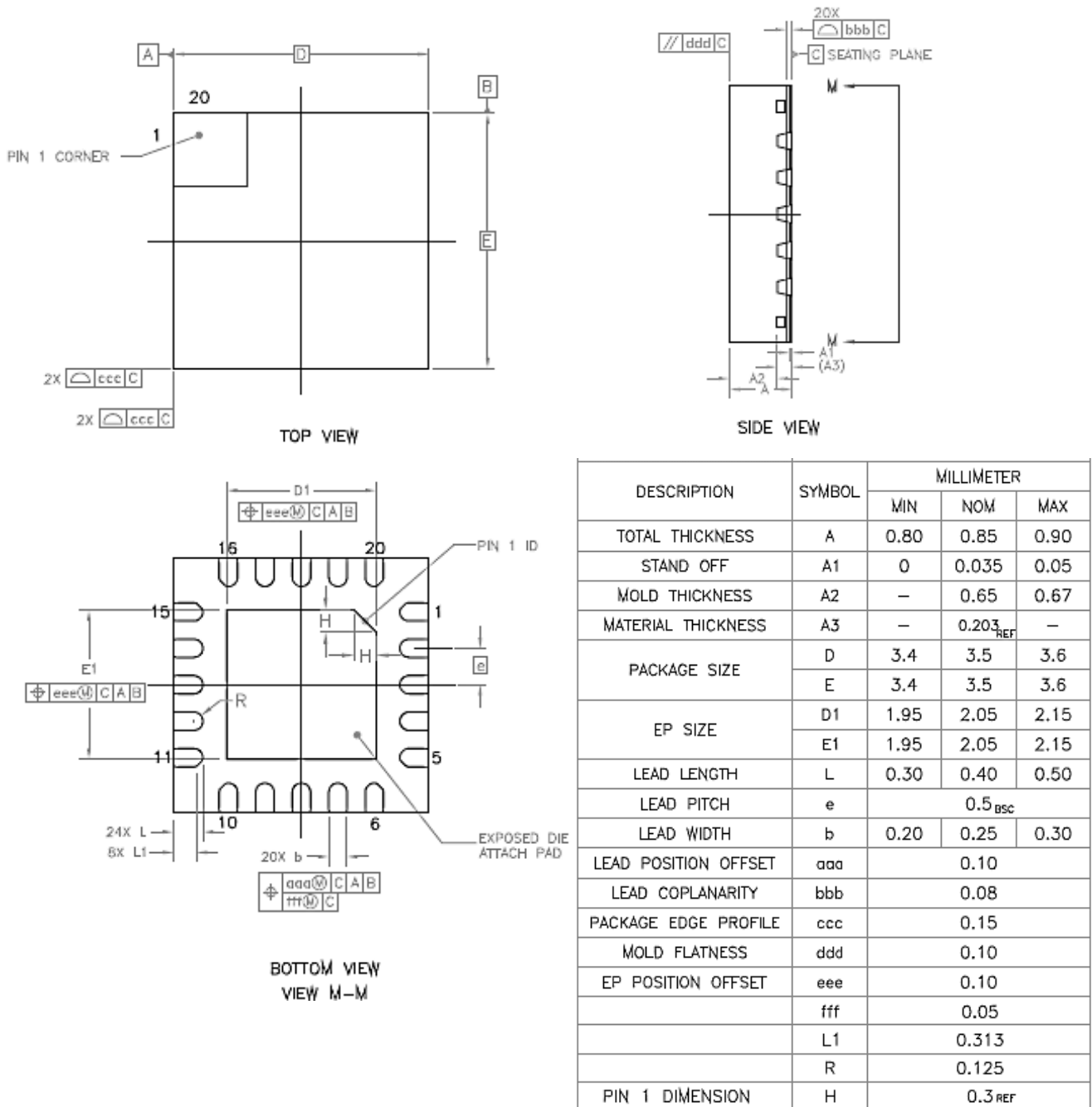


Figure 13 Package Information

Package MSL rating: MSL2.

### Tape and Reel Info:

| Device       | Package type   | Pins | SPQ<br>最小<br>包装<br>数量 | Reel<br>Diameter<br>(mm) | Reel<br>Width<br>W1<br>(mm) | A0<br>(mm) | B0<br>(mm) | K0<br>(mm) | P1<br>(mm) | W<br>(mm) | Pin1<br>Quadrant  |
|--------------|----------------|------|-----------------------|--------------------------|-----------------------------|------------|------------|------------|------------|-----------|-------------------|
| Au8014EB-QNR | QFN<br>3.5x3.5 | 20   | 4000                  | 330                      | 12.3                        | 3.8        | 3.8        | 1.15       | 8          | 12        | Q2 (Top<br>Right) |

## 6 Ordering Information

Table 8 Ordering Information

| Ordering Part Number (OPN) | Marking | Package    | Shipping Package | Temperature Range |
|----------------------------|---------|------------|------------------|-------------------|
| Au8014EB-QNR               | 8014EB  | 20-Pin QFN | Tape and Reel    | -40°C to 125°C    |
| Au8014EB-EVM               |         |            | Evaluation Board |                   |

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## 7 Revision History

**Table 9 Revision History**

| Version Number | Date                     | Description         | Author   |
|----------------|--------------------------|---------------------|----------|
| 1.0            | 4 <sup>th</sup> Dec 2021 | Release version 1.0 | AuraSemi |

## 8 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 9 Contact Information

For more information visit [www.aurasemi.com](http://www.aurasemi.com)

For sales related information please send an email to [sales@aurasemi.com](mailto:sales@aurasemi.com)

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