Au5424G: 1.8 V TO 3.3 V HIGH PERFORMANCE LVCMOS CLOCK BUFFER OUTPUT, ULTRA LOW JITTER BUFFER

General Description

The Au5424G is a high-performance LVCMOS clock buffer family of devices. It has an additive phase jitter of 50 fs RMS.

The Au5424G supports a synchronous glitch-free output enable (OE) function to eliminate any potential intermediate incorrect output clock cycles when enabling or disabling outputs. It can operate from a 1.8 V to 3.3 V supply.

Typical Applications:

- 5G, 4G Basestations
- Telecom Equipment
- Servers

Features

- High-performance 1:4
- LVCMOS clock buffer
- Very low pin-to-pin skew: <50 ps
- Very low additive jitter: <50 fs
- Supply voltage: 1.8 V to 3.3 V
- 3.3V tolerant input clock
- F_{MAX} = 200 MHz
- Integrated serial termination for 50 Ω channel
- Packaged in 8pin, 2 × 2 mm DFN packages

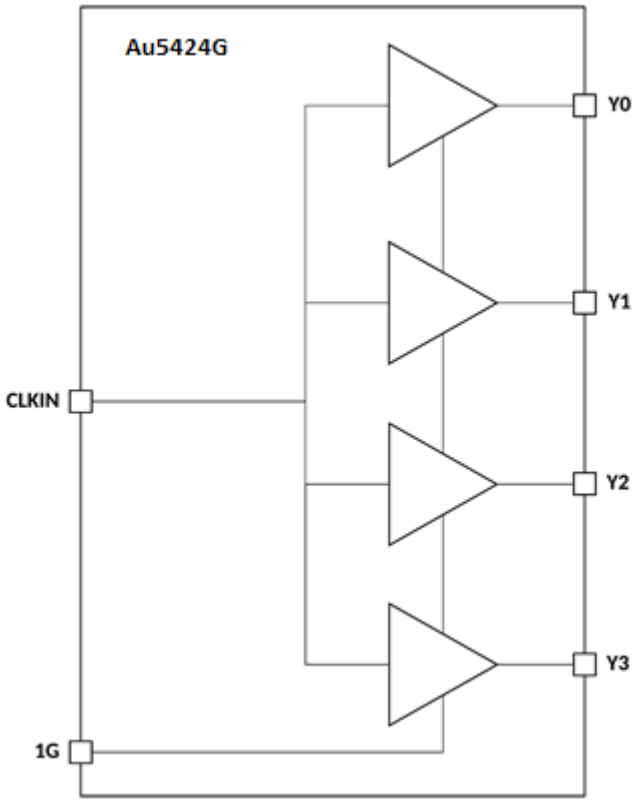

Figure 1 Functional Overview

Table of Contents

General Description 1
Features 1
Table of Contents 2
List of Tables 3
List of Figures 4
1 Pin Description 5
2 Functional Description 6
2.1 Output Logic Tables 6
3 Typical Application Diagram 7
4 Electrical Specifications 8
5 Package Information 12
6 Ordering Information 14
7 Revision History 15
8 Trademarks 16
9 Contact Information 17

List of Tables

Table 1 Detailed Pin Description 5
Table 2 Output Logic Tables.....6
Table 3 Absolute Maximum Ratings.....8
Table 4 Recommended Operating Supply and Temperature.....8
Table 5 DC Electrical Characteristics V_{DD} = 1.8 V ±5% 8
Table 6 DC Electrical Characteristics VDD = 2.5 V ±5%.....9
Table 7 DC Electrical Characteristics - VDD = 3.3 V ±5% 9
Table 8 AC Electrical Characteristics - VDD = 1.8 V ±5%..... 10
Table 9 AC Electrical Characteristics - VDD = 2.5 V ±5%..... 10
Table 10 AC Electrical Characteristics - VDD = 3.3 V ±5%..... 11
Table 11 Thermal Characteristics..... 11
Table 12 Ordering Information for Au5424G 14
Table 13 Revision History..... 15

List of Figures

Figure 1 Functional Overview 1
Figure 2 Au5424G Pin Configuration 5
Figure 3 Au5424G Typical Application Load 7
Figure 4 Au5424G Cross Sections 12
Figure 5 Recommended Land Pattern Dimension 13

1 Pin Description

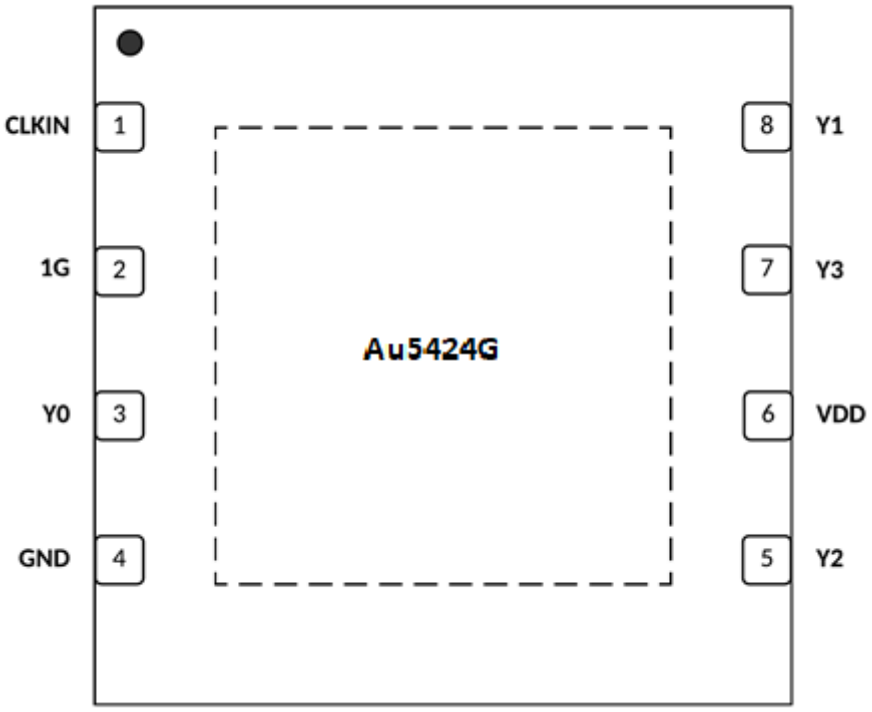

Figure 2 Au5424G Pin Configuration

Table 1 Detailed Pin Description

Pin Name	Pin Number	Functionality AU5424G
Y0	3	LVCMOS output 0
Y1	8	LVCMOS output 1
Y2	5	LVCMOS output 2
Y3	7	LVCMOS output 3
CLKIN	1	Single Ended Input Clock
1G	2	All outputs enable/disable
VDD	6	Core Supply Voltage, VDD
GND	4	Ground

2 Functional Description

2.1 Output Logic Tables

Table 2 Output Logic Tables

Inputs		Output
CLKIN	1G	Yn
X	L	L
L	H	L
H	H	H

3 Typical Application Diagram

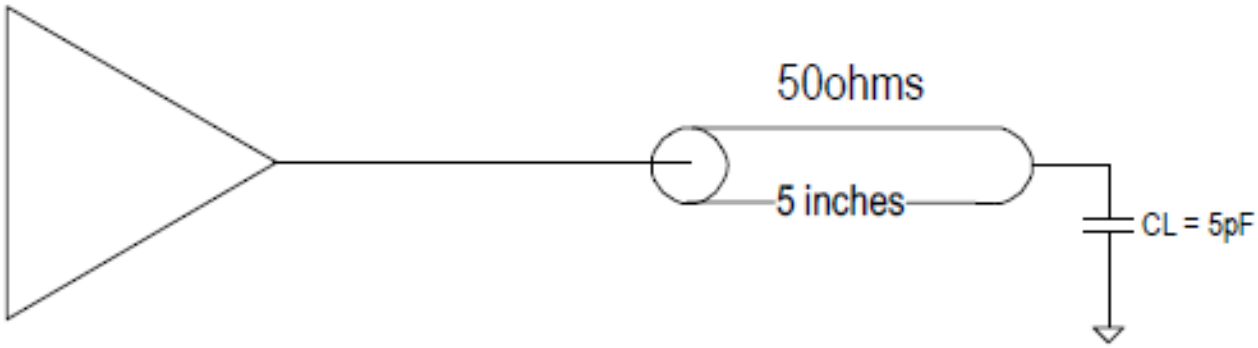

Figure 3 Au5424G Typical Application Load

4 Electrical Specifications

Table 3 Absolute Maximum Ratings

Parameters	Conditions	Sym	Min	Typ	Max	Units
Supply Voltage, VDD			3.6		3.6	V
Output Enable and All Outputs			-0.4		VDD+0.3	V
Input voltage, CLKIN			-0.4		3.465	V
Ambient Operating Temperature,			-40		+105	°C
Storage Temperature			-65		+150	°C
Junction Temperature					+150	°C
Soldering Temperature					+260	°C

Notes:

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

Table 4 Recommended Operating Supply and Temperature

Parameter	Sym	Min	Typ	Max	Units
Ambient Operating Temperature		-40		+105	°C
Power Supply Voltage (Measured in respect to GND)		+1.71		+3.465	V

Table 5 DC Electrical Characteristics V_{DD} = 1.8 V ±5%

Parameter	Conditions	Sym	Min	Typ	Max	Units
Operating Voltage		V_{DD}	1.71	1.8	1.89	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	1.6		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.6	V
Output High Voltage	I_{OH} = -5 mA.	V_{OH}	1.4			V
Output Low Voltage	I_{OL} = 5 mA.	V_{OL}			0.2	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin.	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF.	I_{DD}		0.7	1.7	mA
	0.008 MHz, C_L = 5 pF.			0.7	1.7	
	40 MHz, C_L = 5 pF.			11	13	
	100 MHz, C_L = 5 pF.			25	30	
	156.25 MHz, C_L = 5 pF.			37	47	
	200 MHz, C_L = 5 pF.			39	57	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +105 °C unless stated otherwise.

Table 6 DC Electrical Characteristics VDD = 2.5 V ±5%

Parameter	Conditions	Sym	Min	Typ	Max	Units
Operating Voltage		V_{DD}	2.375	2.5	2.625	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	1.8		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.7	V
Output High Voltage	I_{OH} = -8 mA.	V_{OH}	1.9			V
Output Low Voltage	I_{OL} = 8 mA.	V_{OL}			0.5	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin.	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF.	I_{DD}		0.9	2	mA
	0.008 MHz, C_L = 5 pF.			0.9	2	
	40 MHz, C_L = 5 pF.			15	17.2	
	100 MHz, C_L = 5 pF.			35	42	
	156.25 MHz, C_L = 5 pF.			52	67	
	200 MHz, C_L = 5 pF.			56	80	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +105 °C unless stated otherwise.

Table 7 DC Electrical Characteristics - VDD = 3.3 V ±5%

Parameter	Conditions	Sym	Min	Typ	Max	Units
Operating Voltage		V_{DD}	3.135	3.3	3.465	V
Input High Voltage, CLKIN[1]		V_{IH}	0.7×V_{DD}			V
Input Low Voltage, CLKIN[1]		V_{IL}			0.3×V_{DD}	V
Input High Voltage, 1G		V_{IH}	2.1		V_{DD}	V
Input Low Voltage, 1G		V_{IL}			0.8	V
Output High Voltage	I_{OH} = -12 mA.	V_{OH}	2.4			V
Output Low Voltage	I_{OL} = 12 mA.	V_{OL}			0.7	V
Nominal Output Impedance		Z_O		50		Ω
Input Capacitance	CLKIN, 1G pin.	C_{IN}		5		pF
Operating Supply Current[2]	0.001 MHz, C_L = 5 pF.	I_{DD}		1.2	2.2	mA
	0.008 MHz, C_L = 5 pF.			1.2	2.2	
	40 MHz, C_L = 5 pF.			19	23.3	
Operating Supply Current[2]	100 MHz, C_L = 5pF.	I_{DD}		45	54	
	156.25 MHz, C_L = 5pF.			67	87	
	200 MHz, C_L = 5pF.			75	107	

Notes:

1. Nominal switching threshold is VDD/2.
2. TA = -40 °C to +105 °C unless stated otherwise.

Table 8 AC Electrical Characteristics - VDD = 1.8 V ±5%

Parameter	Conditions	Sym	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Output Rise Time (5 pF load)[2]	0.36 V to 1.44 V, C_L = 5 pF.	t_{OR}		0.65	1.2	Ns
Output Fall Time (5 pF load)[2]	1.44 V to 0.36 V, C_L = 5 pF.	t_{OF}		0.65	1.2	Ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up.	$t_{START-UP}$			3	Ms
Propagation Delay[3]		t_{PD}	0.24		1.6	Ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t_{JIT}			0.06	Ps
Output to Output Skew	Rising edges at VDD/2.[1]	t_{SK}		35	50	Ps
Device to Device Skew	Rising edges at VDD/2.				200	Ps
Output Enable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{EN}			3	Cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{EN}			5	Cycles
Output Disable Time	C_L ≤ 5 pF. Frequency = 25Mhz	t_{DIS}			3	Cycles
	C_L ≤ 5 pF Frequency = 200Mhz	t_{DIS}			5	Cycles
Duty Cycle		t_{DC}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +105 °C unless stated otherwise.
3. With rail to rail input clock

Table 9 AC Electrical Characteristics - VDD = 2.5 V ±5%

Parameter	Conditions	Sym	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Output Rise Time (5 pF load)[2]	0.5 V to 2.0 V, C_L = 5 pF.	t_{OR}		0.63	1.2	ns
Output Fall Time (5 pF load)[2]	2.0 V to 0.5 V, C_L = 5 pF.	t_{OF}		0.63	1.2	ns
Start-up Time	Part start-up time for valid outputs after V_{DD} ramp-up.	$t_{START-UP}$			3	ms
Propagation Delay[3]		t_{PD}	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t_{JIT}			0.06	ps
Output to Output Skew	Rising edges at $V_{DD}/2$[1]	t_{SK}		35	50	ps
Device to Device Skew	Rising edges at $V_{DD}/2$	t_{SKD}			200	ps
Output Enable Time	C_L ≤ 5 pF Frequency = 25Mhz	t_{EN}			3	cycles

Parameter	Conditions	Sym	Min	Typ	Max	Units
	$C_L \leq 5$ pF Frequency = 200Mhz	t_{EN}			5	cycles
Output Disable Time	$C_L \leq 5$ pF. Frequency = 25Mhz	t_{DIS}			3	cycles
	$C_L \leq 5$ pF Frequency = 200Mhz	t_{DIS}			5	cycles
Duty Cycle		t_{DS}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +105 °C unless stated otherwise.
3. With rail to rail input clock

Table 10 AC Electrical Characteristics - VDD = 3.3 V ±5%

Parameter	Conditions	Sym	Min	Typ	Max	Units
Input Frequency			0		200	MHz
Output Rise Time (5 pF load)[2]	0.66 V to 2.64 V, CL = 5 pF.	t_{OR}		0.61	1.2	ns
Output Fall Time (5 pF load)[2]	2.64 V to 0.66 V, CL = 5 pF.	t_{OF}		0.61	1.2	ns
Start-up Time	Part start-up time for valid outputs after VDD ramp-up.	$t_{START-UP}$			3	ms
Propagation Delay[3]		t_{PD}	0.24		1.6	ns
Buffer Additive Phase Jitter, RMS	156.25 MHz, Integration Range: 12 kHz – 20 MHz.	t_{JIT}			0.05	ps
Output to Output Skew	Rising edges at VDD/2[1]	t_{SK}		35	50	ps
Device to Device Skew	Rising edges at VDD/2.	t_{SKD}			200	ps
Output Enable Time	$C_L \leq 5$ pF Frequency = 25Mhz	t_{EN}			3	cycles
	$C_L \leq 5$ pF Frequency = 200Mhz	t_{EN}			5	cycles
Output Disable Time	$C_L \leq 5$ pF. Frequency = 25Mhz	t_{DIS}			3	cycles
	$C_L \leq 5$ pF Frequency = 200Mhz	t_{DIS}			5	cycles
Duty Cycle		t_{DC}		50		%

Notes:

1. Between any 2 outputs with equal loading.
2. TA = -40 °C to +105 °C unless stated otherwise.
3. With rail to rail input clock

Table 11 Thermal Characteristics

Package	ΘJA	Units
8-DFN	75	°C/W; still air

5 Package Information

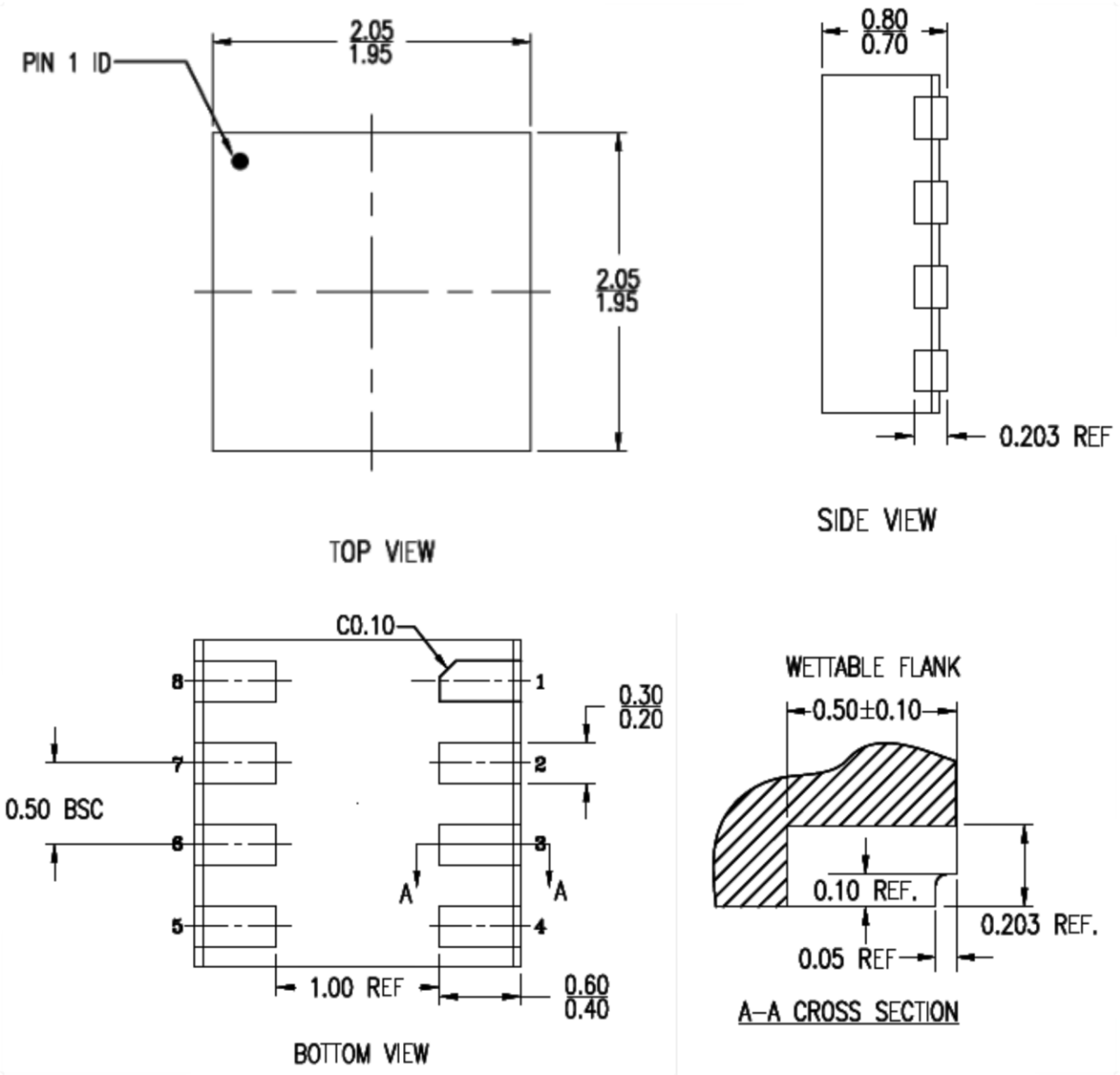

Figure 4 Au5424G Cross Sections

Note:

1. All Dimensions and Tolerancing Conform to ANSI Y14.5M -1982
2. All Dimensions are in Millimeters (mm)

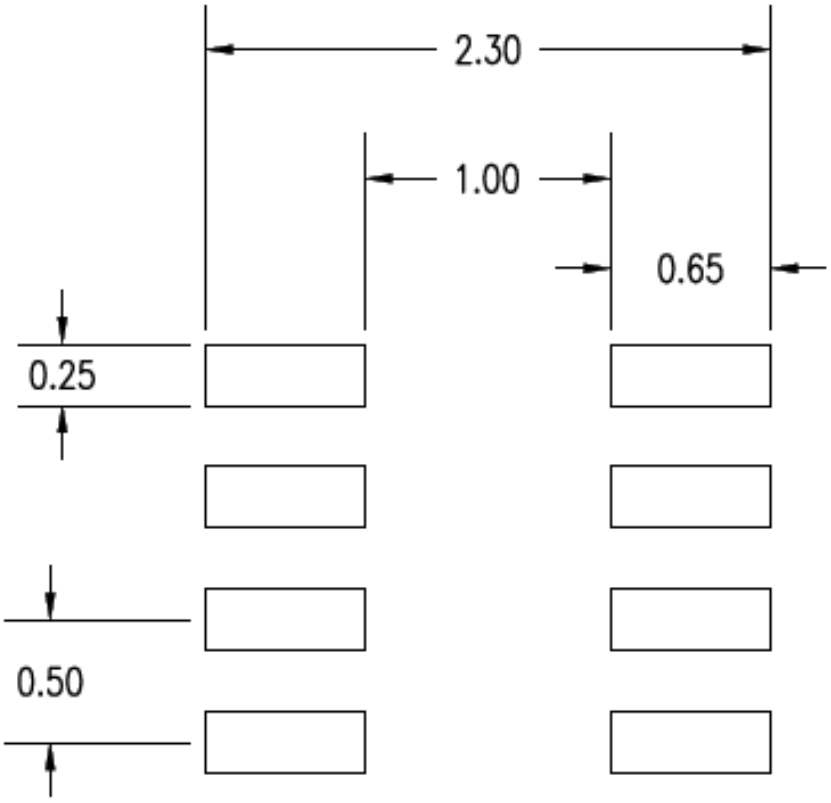

Figure 5 Recommended Land Pattern Dimension

Note:

1. All Dimensions are in Millimeters (mm)
2. All Angles are in Degrees
3. Land Pattern Recommendation per IPC-7351B Generic Requirement for Mount Design and Land Pattern

6 Ordering Information

Table 12 Ordering Information for Au5424G

Ordering Part Number (OPN)	Marking	Package	Shipping Package	Temp. Range
AU5424BG-DNR[1]	24BG	8 Lead DFN 2 mm x 2 mm	Tape and Reel	–40 to 105°C
AU5424BG-DMR[1]	24BG	8 Lead DFN 2 mm x 2 mm	Tape and Reel	–40 to 85°C
AU5424BG-EVB	—	—	Evaluation Board	—

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering option. Add a T at the end of the OPN to denote a tray option.

7 Revision History

Table 13 Revision History

Version	Date	Description	Author
0.1	8th March 2021	Au5424G Data Sheet First Draft	Aurasemi
0.2	5th July 2021	Table 11 Updated with the Ordering Information Details	Aurasemi
0.3	9th Aug 2021	Table 11 Updated with the Ordering Information Details	Aurasemi
0.4	17th Aug 2021	1) Table 1 Pin Description added 2) Max Supply current values corrected and updated 3) Timing parameters : Delay and Skew , min and max values are corrected and updated	Aurasemi
0.5	20th Sep 2021	Table 11 Updated with the Ordering Information Details	Aurasemi
0.6	29th Dec 2021	1) Table 3 updated with soldering temperature 2) Updated Specs for Voh / Vol 3) Updated specs for Output to Output Skew 4) Table 11 updated with thermal characterstics	Aurasemi
0.7	5th March,2022	Updated max electrical spec for Propagation Delay	Aurasemi

8 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

9 Contact Information

For more information visit www.aurasemi.com

For sales related information please send an email to sales@aurasemi.com