AT9917

Automotive LED Driver IC with High Current Accuracy

Features

- Switch Mode Controller for Boost, SEPIC and Buck Converters
- Closed-Loop Control of Output Current
- High PWM Dimming Ratio
- Internal 40V Linear Regulator
- Internal 3% Voltage Reference
- Constant Frequency Operation with Programmable Slope Compensation
- Linear and PWM Dimming
- Programmable Jitter to Reduce EMI
- +/–1A MOSFET Gate Driver
- Output Short-Circuit Protection
- Output Overvoltage Protection
- Programmable Hiccup Timer
- Soft Start
- Temperature Foldback with External NTC Resistor
- AEC-Q100 Compliant

Applications

- Automotive LED Driver Applications

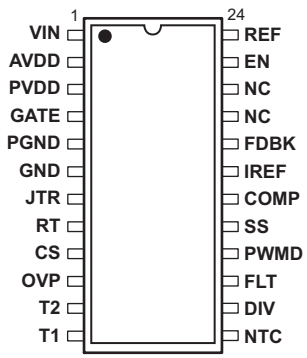
General Description

The AT9917 is an advanced fixed frequency PWM IC designed to control single-switch, boost, SEPIC and buck LED drivers in a Constant Current mode. The controller uses a Peak Current-mode control scheme with programmable slope compensation and includes an internal transconductance amplifier to control the output current with high accuracy. The IC includes a +/–1A gate driver that makes the AT9917 suitable for high-power applications. An internal 40V linear regulator powers the IC, eliminating the need for a separate power supply for the device. The IC provides a Fault output, which can be used to disconnect the LEDs in case of a Fault condition (such as an alternator load dump in automobiles) using an external disconnect FET. The AT9917 also provides a TTL-compatible, low-frequency PWM dimming input that can accept an external control signal with a duty ratio of 0% to 100% and a frequency of up to several kilohertz. Temperature foldback of the output current is possible, using an external NTC resistor.

The AT9917-based LED driver is suited for automotive LED driver applications. The AT9917-based LED lamp drivers can achieve efficiencies in excess of 90% when buck or boost topologies are used.

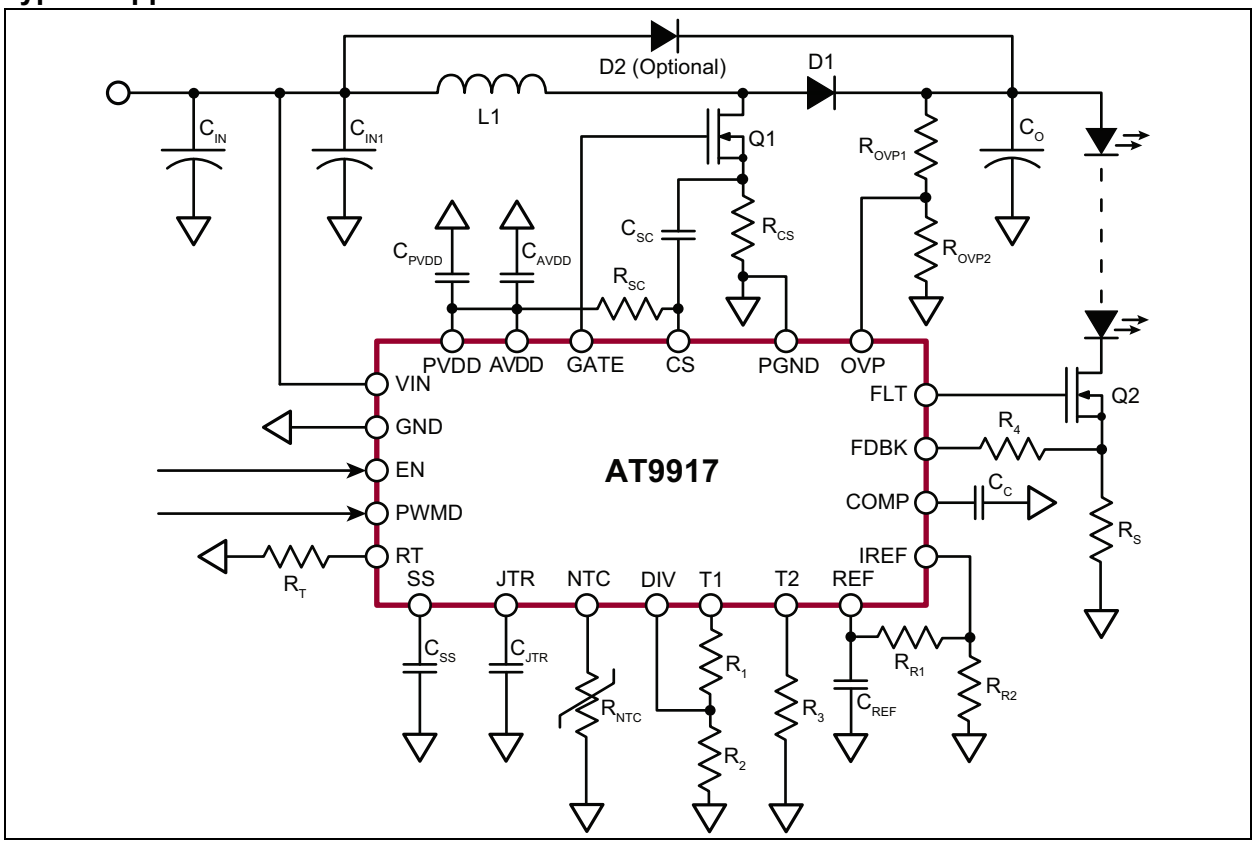
Package Type

24-lead TSSOP
(Top view)

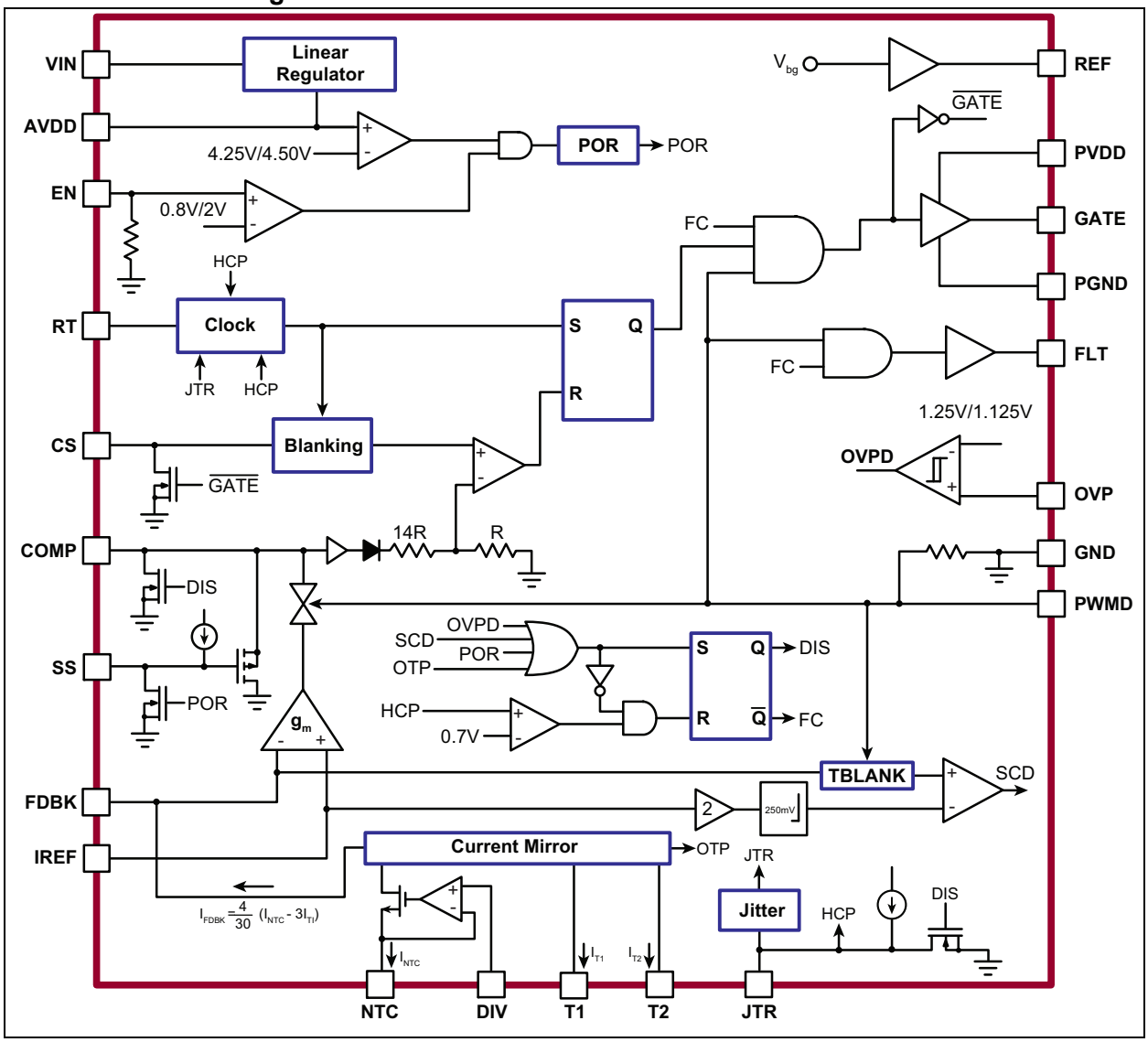


See Table 2-1 for pin information.

Typical Application



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN} to GND .....–0.5V to +45V
PV_{DD}, AV_{DD} to GND .....–0.3V to +6V
GATE to GND ..... –0.3V to (PV_{DD}+0.3V)
All other pins to GND .....–0.3V to (AV_{DD} +0.3V)
Continuous Power Dissipation (T_A= +25°C) ..... 1000 mW
Junction Temperature Range, T_J ..... –40°C to +150°C
Storage Temperature Range, T_S ..... –65°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, specifications are at T_A = 25°C. V_{IN} = 12V, PV_{DD} = AV_{DD} EN = PWMD = AV_{DD}, GATE = OPEN, C_{REF} = 0.1 µF, C_{AVDD} = C_{PVDD} = 1 µF, R_T = 200 kΩ, I_{T1} = I_{T2} = 100 µA.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
INPUT						
Input DC Supply Voltage Range	V_{INDC}	5.3	—	40	V	DC input voltage
Shutdown Mode Supply Current	I_{INDIS}	—	—	100	µA	EN = 0.8V, PWMD = GND (**Note 1**)
Input Current when Enabled	I_{INEN}	—	—	2	mA	EN = 2V, GATE OPEN, PWMD = GND (**Note 1**)
INTERNAL REGULATOR						
Internally Regulated Voltage	AV_{DD}	4.65	5	5.35	V	V_{IN} = 6V–40V, GATE OPEN, PWMD = GND, I_{DD} = 0 mA – 20 mA (**Note 1**)
AV_{DD} Undervoltage Lockout Upper Threshold	$AV_{DDUV,R}$	4.25	—	4.85	V	AV_{DD} rising (**Note 1**)
AV_{DD} Undervoltage Lockout Hysteresis	ΔAV_{DDUV}	—	250	—	mV	AV_{DD} falling
ENABLE INPUT						
Enable Input Low Voltage	$V_{EN(LO)}$	—	—	0.8	V	**Note 1**
Enable Input High Voltage	$V_{EN(HI)}$	2	—	—	V	**Note 1**
Pull-Down Resistor at EN	R_{EN}	—	100	—	kΩ	
REFERENCE						
REF Pin Voltage	V_{REF}	1.210	1.250	1.290	V	I_{REF} = 0 mA (**Note 1**)
REF Pin Voltage when Disabled	$V_{REF,DIS}$	—	0	—	mV	I_{REF} = 0 mA, EN = GND
Load Regulation of Reference Voltage	ΔV_{REF}	0	—	2	mV	I_{REF} = 0 mA –1 mA
GATE						
GATE Output Rise Time	T_{RISE}	—	20	35	ns	C_{GATE} = 4 nF, V_{IN} = AV_{DD} = PV_{DD} = 5V
GATE Output Fall Time	T_{FALL}	—	20	35	ns	C_{GATE} = 4 nF, V_{IN} = AV_{DD} = PV_{DD} = 5V
Maximum Duty Cycle	D_{MAX}	87	—	93	%	**Note 1**

Note 1: Specifications apply over the full operating ambient temperature range of –40ºC < T_A < +125ºC. Guaranteed by design and characterization.

2: Specifications are determined by characterization and are not 100% tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, specifications are at T_A = 25°C. V_{IN} = 12V, PV_{DD} = AV_{DD} EN = PWMD = AV_{DD}, GATE = OPEN, C_{REF} = 0.1 µF, C_{AVDD} = C_{PVDD} = 1 µF, R_T = 200 kΩ, I_{T1} = I_{T2} = 100 µA.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
PWM DIMMING						
PWMD Input Low Voltage	$V_{PWMD(LO)}$	—	—	0.8	V	**Note 1**
PWMD Input High Voltage	$V_{PWMD(HI)}$	2	—	—	V	**Note 1**
PWMD Pull-Down Resistance	R_{PWMD}	—	200	—	kΩ	
OVER VOLTAGE PROTECTION						
Overvoltage Rising Trip Point	$V_{OVP,RISING}$	1.15	1.25	1.35	V	OVP rising (**Note 1**)
Overvoltage Hysteresis	$V_{OVP,HYST}$	—	0.125	—	V	OVP falling
CURRENT SENSE						
Leading Edge Blanking	$T_{BLANK,CS}$	100	—	250	ns	**Note 1**
Delay to Output of Comparator	T_{DELAY1}	—	—	150	ns	V_{COMP} = AV_{DD} = PV_{DD} = 5V, V_{CS} = 0 mV – 400 mV step
Comparator Offset Voltage	V_{OFFSET}	–10	—	10	mV	**Note 1**
INTERNAL TRANSCONDUCTANCE OP-AMP						
Gainbandwidth Product	GBW	1	—	—	MHz	150 pF capacitance at COMP pin (**Note 1**)
Open-Loop DC Gain	A_V	65	—	—	dB	COMP OPEN
Input Common Mode Range	V_{CM}	–0.3	—	3	V	**Note 1**
Output Voltage Range	V_{COMP}	0.7	—	AV_{DD}	—	**Note 1**
Transconductance	g_m	—	950	—	µA/V	
Input Offset Voltage	V_{OFFSET}	–9	—	9	mV	**Note 1**
COMP Sink Current	$I_{COMP,SINK}$	0.2	—	—	mA	V_{FB} = 0.1V, V_{COMP} = 0V (**Note 1**)
COMP Source Current	$I_{COMP,SRC}$	–0.2	—	—	mA	V_{FB} = –0.1V, V_{COMP} = AV_{DD} (**Note 1**)
Input Bias Current	$I_{BIAS,AMP}$	—	0.5	1	nA	**Note 1**
OSCILLATOR						
Oscillator Frequency	f_{OSC1}	90	105	120	kHz	R_T = 1 MΩ (**Note 1**)
	f_{OSC2}	427	505	583	kHz	R_T = 200 kΩ (**Note 1**)
Output Frequency Range	f_{OSC}	100	—	800	kHz	**Note 1**
JITTER						
Jitter Frequency	F_{JTR}	—	50	—	Hz	C_{JTR} = 100 nF
		—	500	—	Hz	C_{JTR} = 10 nF
Change in the Switching Frequency	ΔF	±4.5	—	—	kHz	
HICCUP TIMER						
Hiccup Charging Current	I_{HICCUP}	—	10	—	µA	
Voltage Swing for Hiccup Timer	ΔV	—	0.6	—	V	
TEMPERATURE FOLDBACK CIRCUIT						
NTC Source Current Range	I_{NTC}	—	—	1	mA	**Note 1**
I_{FDBK}/I_{NTC} Current Gain	N_{NTC}	—	0.13	—	—	I_{NTC} = 0.5 mA
I_{NTC}/I_{T1} Current Gain	N_{T1}	—	3	—	—	I_{NTC} = 0.5 mA
I_{NTC}/I_{T2} Current Gain	N_{T2}	—	6	—	—	I_{NTC} = 0.5 mA
T1 and T2 Reference Voltage	V_{T1}, V_{T2}	—	3.5	—	V	
OUTPUT SHORT CIRCUIT						
Amplifier Gain at IREF Pin	G_{FAULT}	1.8	2	2.2	—	V_{IREF} = 400 mV

Note 1: Specifications apply over the full operating ambient temperature range of –40ºC < T_A < +125ºC. Guaranteed by design and characterization.

2: Specifications are determined by characterization and are not 100% tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, specifications are at T_A = 25°C. V_{IN} = 12V, PV_{DD} = AV_{DD} EN = PWMD = AV_{DD}, GATE = OPEN, C_{REF} = 0.1 µF, C_{AVDD} = C_{PVDD} = 1 µF, R_T = 200 kΩ, I_{T1} = I_{T2} = 100 µA.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Propagation Time for Short-Circuit Detection	$T_{D,SHORT}$	—	—	250	ns	V_{IREF} = 400 mV, V_{FDBK} steps from 0V –1V, V_{FLT} goes from high to low
Fault Output Rise Time	$T_{RISE,FAULT}$	—	—	300	ns	330 pF capacitor at FLT pin
Fault Output Fall Time	$T_{FALL,FAULT}$	—	—	200	ns	330 pF capacitor at FLT pin
Minimum Voltage at the Output of the Amplifier	V_{MIN}	250	—	—	mV	V_{IREF} = 0V (**Note 1**)
PWMD Blanking Time	$T_{BLANK,PWMD}$	200	—	900	ns	**Note 1**
SOFT START						
Soft-Start Charging Current	$I_{SS,CHG}$	10	15	25	µA	
Soft-Start Discharging Current	$I_{SS,DIS}$	1.0	—	—	mA	V_{SS} = 5V
Soft-Start Reset Voltage	$V_{SS,RST}$	—	—	100	mV	
SLOPE COMPENSATION						
On-Resistance of FET at CS Pin	$R_{ON,DFETCS}$	—	—	200	Ω	**Note 1**

Note 1: Specifications apply over the full operating ambient temperature range of –40ºC < T_A < +125ºC. Guaranteed by design and characterization.

2: Specifications are determined by characterization and are not 100% tested.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
TEMPERATURE RANGES						
Operating Ambient Temperature	T_A	–40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
24-lead TSSOP	θ_{JA}	—	125	—	°C/W	**Note 1**

Note 1: Mounted on an FR 4 board, 25 mm x 25 mm x 1.57 mm.

2.0 PIN DESCRIPTION

The details on the pins of AT9917 are listed in Table 2-1. Refer to **Package Type** for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	V_{IN}	This pin is the input of a 40V high-voltage regulator.
2	AV_{DD}	This is a power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1 µF).
3	PV_{DD}	This is the power supply pin for the gate driver. It should be connected externally to AV_{DD} and bypassed with a low ESR capacitor to PGND (at least 0.1 µF).
4	GATE	This pin is the output of gate driver for an external logic level N-channel power MOSFET.
5	PGND	Ground return for the gate drive circuitry
6	GND	Ground return for all the low-power analog internal circuitry. This pin must be connected to the return path from the input.
7	JTR	This pin controls the jitter of the clock programmed by a capacitor connected at this pin. This capacitor also determines the hiccup time.
8	RT	This pin sets the frequency of the power circuit. A resistor between RT and GND programs the circuit in Constant Frequency mode.
9	CS	This pin is used to sense the source current of the external power FET. It includes a built-in 100 ns (minimum) blanking time. Slope compensation is implemented by connecting an RC network to this pin as shown in the **Typical Application**.
10	OVP	This pin is the comparator input of the overvoltage protection circuit for the converter. When the voltage at this pin exceeds 1.25V, the gate output of the AT9917 is turned off and FLT goes low. Switching is enabled when the voltage at this pin goes below 1.125V.
11	T2	This pin programs the temperature at which the driver is shut off due to Overtemperature condition for the LED when using an external NTC resistor at the NTC pin.
12	T1	This pin programs the break temperature threshold which determines the start of the current derating when using an external NTC resistor at the NTC pin.
13	NTC	Users may connect an external NTC resistor to this pin for temperature fold back of the output current and overtemperature shutdown. The NTC pin should be connected to AVDD when output current thermal derating is not required.
14	DIV	This pin programs the voltage input for the transconductance at NTC pin.
15	FLT	This pin is pulled to ground when there is an Output Short-circuit condition or Output Overvoltage condition. This pin can be used to drive an external MOSFET in the case of boost converter configuration to disconnect the LED load from the power source. It is also controlled by the PWM dimming input to provide excellent PWM dimming response.
16	PWMD	When this pin is pulled to GND (or left open), switching of the AT9917 is disabled. When an external TTL high level is applied to it, switching will resume.
17	SS	Connecting a capacitor from this pin to GND programs the soft start time of the LED driver.
18	COMP	This pin is the output of the error amplifier. Stable closed-loop control can be accomplished by connecting a compensation network between COMP and GND. This pin is pulled internally to GND upon detection of a Fault condition and on startup.
19	IREF	The voltage at this pin sets the output current level. The current reference voltage can be set using a resistor divider from the REF pin to GND pin.
20	FDBK	This pin provides output current feedback to the AT9917 by using a current sense resistor. A resistor connected between the FDBK pin and the LED current sense resistor can be used to reduce the current at elevated temperatures.
21	NC	No connection
22	NC	

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
23	EN	Pulling EN to GND causes the AT9917 to go into a low-current Standby mode. A voltage greater than 2V enables the IC.
24	REF	This pin provides accurate reference voltage. It must be bypassed with a 0.01 µF to 0.1 µF capacitor to GND.

3.0 DETAILED DESCRIPTION

3.1 Power Topology

The AT9917 is a closed-loop, Switch-mode LED driver designed to control a buck, boost or SEPIC converter in a Constant Frequency mode. The IC includes an internal linear regulator, which operates from input voltages from 6V to 40V. It also possesses features typically required in LED drivers, such as open LED protection, output short-circuit protection, linear and PWM dimming, and accurate LED current control. In addition, the device includes a thermal derating circuit which can be used to reduce the LED current at high temperatures to prevent a thermal runaway. A high-current gate drive output enables the controller to be used in high power converters.

3.2 Power Supply to the IC (V_{IN}, AV_{DD}, PV_{DD})

The AT9917 can be powered directly from its V_{IN} pin that takes a voltage up to 40V. When a voltage is applied to the V_{IN} pin, the AT9917 tries to maintain a constant 5V (typical) at the AV_{DD} pin. The regulator also has a built-in undervoltage lockout which shuts off the IC if the voltage at the AV_{DD} pin falls below the UVLO lower threshold. This linear regulator also provides the power supply to the built-in gate driver.

The AV_{DD} pin must be bypassed by a low ESR capacitor (≥0.1 µF) to provide a low impedance path for the high-frequency current of the output gate driver. The PV_{DD} pin is used to provide power to the gate driver. It should also be bypassed with a low-ESR capacitor (≥0.1 µF) and should be shorted to the AV_{DD} pin.

The input current drawn from the external power supply (or V_{IN} pin) is the sum of the 2 mA (maximum) current drawn by the all the internal circuitry and the current drawn by the gate driver. The current drawn by the gate driver depends on the switching frequency and the gate charge of the external FET. Refer to Equation 3-1.

EQUATION 3-1:

$$I_{IN} = 2mA + Q_G \times f_S$$

Where:

f_S = Switching frequency of the converter

Q_G = Gate charge of the external FET (can be obtained from the FET data sheet)

The EN pin is a TTL-compatible input used to disable the IC. Pulling the EN pin to GND shuts down the IC and reduces the quiescent current drawn by the IC to be less than 100 µA. If the enable function is not required, the EN pin can be connected to AV_{DD}.

3.3 Reference Voltage (REF)

The AT9917 provides a 1.25V reference voltage at the REF pin. This voltage is used to derive the various internal voltages required by the IC and set the LED current externally. It should be bypassed with a low-impedance capacitor (0.01 µF to 0.1 µF).

3.4 Timing Resistor (RT)

The switching frequency of the converter is set by connecting a resistor between RT and GND. The resistor value can be determined with Equation 3-2.

EQUATION 3-2:

$$R_T = \frac{1}{f_S \times 9.5pF}$$

3.5 Current Sense (CS)

The CS input is used to sense the source current of the switching FET. The CS input of the AT9917 includes a built-in 100 ns (minimum) blanking time to prevent spurious turn-off due to the initial current spike when the FET turns on.

The IC includes an internal resistor divider network, which steps down the voltage at the COMP pins by a factor of 15. This voltage is used as the reference for the current sense comparators. Since the maximum voltage of the COMP pin is AV_{DD}, this voltage determines the maximum reference current for the current sense comparator and thus the maximum inductor current.

The switch current sense resistor R_{CS} should be chosen so that the input inductor current is limited to below the saturation current level of the input inductor. For Discontinuous Conduction mode of operation, no slope compensation is necessary. In this case, the current sense resistor is calculated with Equation 3-3.

EQUATION 3-3:

$$R_{CS} = \frac{AV_{DD} - 0.8V}{15 \times I_{SAT}}$$

Where I_{SAT} is the maximum desired peak inductor current

For Continuous Conduction mode converters operating in Constant Frequency mode, slope compensation becomes necessary to ensure stability of the Peak Current mode controller when the operating duty cycle is greater than 0.5. This factor must also be accounted for when determining R_{CS} as discussed in **Section 3.6 "Slope Compensation"**.

3.6 Slope Compensation

Choosing a slope compensation, which is one-half of the down slope of the inductor current, ensures that the converter is stable for all duty cycles.

As shown in Figure 3-1, slope compensation in AT9917 can be programmed by two external components. A resistor from AV_{DD} sets a current (which is almost constant since the AV_{DD} voltage is much larger than the voltage at the CS pin). This current flows into the capacitor and produces a ramp voltage across the capacitor. The voltage at the CS pin is then the sum of the voltage across the capacitor and the voltage across the current sense resistor, with the voltage across the capacitor providing the required slope compensation. When the GATE turns off, an internal pull-down FET discharges the capacitor, so that the capacitor can be charged up again to produce the same ramp voltage across the capacitor at each time the GATE turns on in each cycle

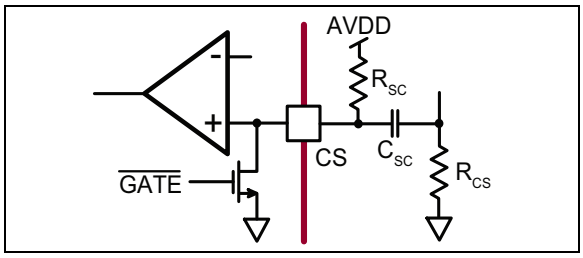


FIGURE 3-1: *Slope Compensation.*

The 200Ω maximum resistance of the internal FET will prevent the voltage at the CS pin from going all the way to zero. The minimum value of the voltage is computed in Equation 3-4:

EQUATION 3-4:

$$V_{CS,MIN} = \frac{AV_{DD}}{R_{SC}} \times 200\Omega$$

The slope compensation capacitor is chosen so that it can be completely discharged by the internal 200Ω (maximum) FET at the CS pin during the time the FET is off. Assuming the worst case switch duty cycle of 93%, C_{SC} is computed with Equation 3-5.

EQUATION 3-5:

$$C_{SC} = \frac{0.07}{3 \times 200\Omega \times f_S}$$

Assuming that there is a down slope of DS (A/µs) for the inductor current, the switch current sense resistor and the slope compensation resistor are calculated as shown in Equation 3-6 and Equation 3-7, respectively.

EQUATION 3-6:

$$R_{CS} = \frac{AV_{DD} - 0.8V}{15} \times \frac{1}{\left\{\frac{DS \times 10^6 \times 0.93}{2 \times f_S}\right\} + I_{SAT}}$$

EQUATION 3-7:

$$R_{SC} = \frac{2 \times AV_{DD}}{DS \times 10^6 \times C_{SC} \times R_{CS}}$$

3.7 Gate Driver Output (GATE, PGND)

The GATE output of the AT9917 is used to drive the gate of the switching FET. The PGND pin should be connected to the GND connection of the current sense resistor. In addition, the two grounds of the IC, PGND and GND, should be connected together at the input GND connection to minimize noise.

3.8 FLT Output

The FLT pin is used to drive a disconnect FET while operating in boost or SEPIC converter configuration. In the case of boost converters, when there is a short-circuit fault at the output, there is a direct path from the input source to ground which can cause high currents to flow. The disconnect switch is used to interrupt this path and prevent damage to the converter.

The disconnect switch also helps to disconnect the output filter capacitors from the LED load in the boost or SEPIC converter configuration during PWM dimming without discharging the output filter capacitors. This enables a very high PWM dimming ratio.

3.9 Control of the LED Current (IREF, FDBK and COMP)

The LED current in the AT9917 is controlled in a closed-loop manner. The current reference voltage at the IREF pin which sets the LED current is programmed using a resistor divider from the REF pin to the GND pin. The current reference voltage can also be set externally with a low-voltage source. This reference voltage is compared to the voltage at the FDBK pin, which senses the LED current through the LED current sense resistor. The AT9917 includes a 1 MHz transconductance amplifier with a tri-state output, which is used to close the feedback loops and provide accurate current control. The compensation network is connected from the COMP pin to the GND pin.

The output of the op-amp is buffered and connected to the current sense comparator using a 14R:1R resistor divider.

The output of the op-amp is also controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the op-amp is connected to the COMP pin. When PWMD is low, the output is left open. This enables the integrating capacitor to hold the charge when the PWMD signal has turned off the gate drive. When the IC is enabled, the voltage on the integrating capacitor almost instantaneously forces the converter into a steady state.

3.10 Linear Dimming

Linear dimming can be accomplished by varying the voltages at the IREF pin. Note that since the AT9917 is a Peak Current mode controller, it has a minimum on-time for the GATE output. This minimum on-time will prevent the converter from completely turning off even when the IREF pin is pulled to GND. Thus, linear dimming in this device cannot accomplish true zero-LED current. To get zero-LED current, PWM dimming has to be used.

Due to the offset voltage of the short-circuit comparator and the non-linearity of the X2 gain stage, pulling the IREF pin very close to GND might cause the internal short-circuit comparator to trigger and shut down the IC. To overcome this, the output of the gain stage is limited to 250 mV (minimum), allowing the IREF pin to be pulled all the way to 0V without triggering the short-circuit comparator. Therefore, the minimum voltage for a short-circuit detection is 250 mV.

3.11 PWM Dimming (PWMD)

PWM dimming in the AT9917 can be accomplished using a TTL-compatible square wave source at the PWMD pin.

When the PWM signal is high, the GATE and FLT pins are enabled and the output of the transconductance op-amp is connected to the external compensation network. Thus, the internal amplifier controls the output current. When the PWMD signal goes low, the output of the transconductance amplifier is disconnected from the compensation network. Thus, the integrating capacitor maintains the voltage across it. The GATE is disabled, so the converter stops switching and the FLT pin goes low, turning off the disconnect switch.

Note that disconnecting the LED load during PWM dimming causes the energy stored in the inductor to be dumped into the output capacitor. The filter capacitor that is chosen should be large enough so that it can absorb the inductor energy without a significant change in voltage across it. If the capacitor voltage change is significant, it would cause a turn-on spike in the inductor current when PWMD goes high.

3.12 Jitter and Hiccup Timer (JTR)

The JTR pin is a multipurpose pin on the AT9917. It is used to set the jitter frequency, wherein the switching frequency swings between its limits. It is also used to set the hiccup time for Fault conditions.

The value of the capacitor required for the jitter frequency is derived with Equation 3-8.

EQUATION 3-8:

$$C_{JTR} = \frac{5\mu F}{F_{JTR}(Hz)}$$

Note that the jitter frequency must be chosen to be significantly lower than the crossover frequency of the closed-loop control. If not, the controller will not be able to reject the jitter frequency, and the LED current will have a current ripple at the jitter frequency.

The same capacitor is used to determine the hiccup time. Equation 3-9 illustrates the computation for hiccup time.

EQUATION 3-9:

$$t_{HICCUP} = \frac{C_{JTR} \times 0.6V}{10\mu A}$$

If the actual hiccup time is lower than desired, the capacitor at the pin can be increased at the cost of a lower jitter frequency.

3.13 Fault Conditions

The AT9917 is a robust controller which can protect the LEDs and the LED driver in case of Fault conditions. The device includes both open LED protection and output short-circuit protection. In both cases, the AT9917 shuts down and attempts to restart. The hiccup time is programmed by the capacitor at the JTR pin.

When a Fault condition is detected, both GATE and FLT outputs are disabled, while the COMP pins and JTR pins are pulled to GND. Once the voltage at the JTR pin falls below 0.1V and the Fault condition(s) has disappeared, the capacitor at the JTR pin is released and is charged slowly by a 10 µA current source. Once the capacitor is charged to 0.7V, the COMP pins are released and GATE and FLT pins are allowed to turn on. If the hiccup time is long enough, it ensures that the compensation networks are all completely discharged and that the converters start at minimum duty cycle.

3.14 Short-Circuit Protection

When a Short-circuit condition is detected (output current becomes higher than twice the Steady-state current), the GATE and FLT outputs are pulled low. As soon as the disconnect FET is turned off, the output current goes to zero and the Short-circuit condition disappears. At this time, the hiccup timer is started. Once the timing is complete, the converter attempts to restart. If the Fault condition still persists, the converter shuts down and goes through the cycle again. If the Fault condition is cleared due to a momentary output short, the converter just resumes the normal output regulation. This allows the LED driver to recover from accidental shorts without having to reset the IC.

During Short-circuit conditions, there are two conditions that determine the hiccup time.

The first is the time required to discharge the compensation capacitors. Assuming a pole-zero R-C network at the COMP pin (series combination of RZ and CZ in parallel with CC), t_{COMP} is computed as shown in Equation 3-10.

EQUATION 3-10:

$$t_{COMP} = 3 \times R_Z \times C_Z$$

In case the compensation networks are only type 1 (single capacitor), Equation 3-11 should be used.

EQUATION 3-11:

$$t_{COMP} = 3 \times 300\Omega \times C_C$$

The second is the time required for the inductors to completely discharge following a short circuit. This time can be computed as demonstrated in Equation 3-12.

EQUATION 3-12:

$$t_{IND} = \frac{\Pi}{4}\sqrt{L \times C_O}$$

Where L and C_O are the input inductor and output capacitor of the power stage

The hiccup time is then chosen as indicated in Equation 3-13.

EQUATION 3-13:

$$t_{HICCUP} > max(t_{COMP}, t_{IND})$$

Note that the power rating of the LED current sense resistor has to be chosen properly if it has to survive a persistent Fault condition. The power rating can be determined as shown in Equation 3-14.

EQUATION 3-14:

$$P_{RS} \geq \frac{I^2_{SAT} \times R_S(t_{FALL,FAULT} + t_{OFF})}{t_{HICCUP}}$$

Where I_{SAT} is the saturation current of the disconnect FET. For AT9917, "$t_{FALL,FAULT} + t_{OFF}$" is 450 ns (maximum)

3.15 False Triggering of the Short-Circuit Comparator During PWM Dimming

During PWM dimming, the parasitic capacitance of the LED string might cause a spike in the output current when the disconnect FET is turned on. If this spike is detected by the short-circuit comparator, it will cause the IC to falsely detect an Over Current condition and shut down.

To prevent false trigger, there is a built-in 500 ns blanking network for the short-circuit comparator. This blanking network is activated when the PWMD input goes high. Thus, the short-circuit comparator will not see the spike in the LED current during the PWM dimming turn-on transition. Once the blanking timer has completed its task, the short-circuit comparator will start monitoring the output current. Thus, the total delay time for detecting a short circuit will depend on the condition of the PWMD input.

If the output short circuit exists before the PWM dimming signal goes high, the total detection time is computed as demonstrated in Equation 3-15.

EQUATION 3-15:

$$t_{DETECT} = t_{PWMD} + t_{FALL,FAULT} + t_{OFF} \approx 950ns(max)$$

If short circuit occurs when the PWM dimming signal is already high, the time to detect is calculated as shown in Equation 3-16:

EQUATION 3-16:

$$t_{DETECT} = t_{FALL,FAULT} + t_{OFF} \approx 450ns(max)$$

3.16 Overvoltage Protection

The AT9917 provides hysteretic overvoltage protection, allowing the IC to recover in case the LED load is momentarily disconnected.

When the load is disconnected from a boost converter, the output voltage rises as the output capacitor starts charging with the inductor's stored energy dump. When the output voltage reaches the OVP rising threshold, the AT9917 detects an Overvoltage condition and turns off the converter. The converter is turned back on only when the output voltage falls below the OVP falling threshold, which is 10% lower than the rising threshold. The OVP and recovery time duration is mostly dictated by the R-C time constant of the output capacitor C_O and the resistor network used to sense over voltage (R_{OVP1} + R_{OVP2}). In case of a persistent Open Circuit condition, this cycle repeats and maintains the output voltage within a 10% band.

In most designs, the lower threshold voltage of the over voltage protection (V_{OVP} –10%) at which the AT9917 attempts to restart will be more than the LED string voltage. Thus, when the LED load is reconnected to the output of the converter, the voltage differential between the actual output voltage and the LED string voltage will cause a spike in the output current. This causes a short circuit to be detected and the device triggers short-circuit protection. This behavior continues until the output voltage becomes lower than the LED string voltage, at which point no fault will be detected and normal operation of the circuit will commence.

3.17 Thermal Derating

The reference voltage used to set the LED current is programmed using two resistors—R_{r1} and R_{r2}, which are connected as shown in Figure 3-2.

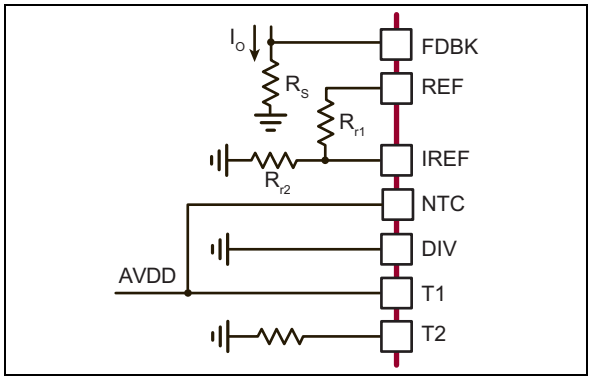


FIGURE 3-2: *No Thermal Derating.*

Thermal derating is programmed using four pins—NTC, DIV, T1 and T2. When no temperature foldback is required, NTC and T1 should be connected to AV_{DD}, and DIV should be connected to GND. T2 still requires a resistor to GND (10 kΩ ~100 kΩ). No pins should be left floating as shown in Figure 3-2.

The output LED current I_O without thermal derating or output LED current I_1 with thermal derating enabled at temperature below T_1 in the thermal derating curve can be calculated with Equation 3-17.

EQUATION 3-17:

$$I_O = I_1 = \frac{V_{REF}}{R_S} \times \frac{R_{r2}}{R_{r1} + R_{r2}}$$

Where I_O is the output LED current without thermal derating, I_1 is the output LED current at temperature below T_1 in the thermal derating curve, V_{REF} is the reference voltage at REF pin, and R_S is the LED current sense resistor.

When thermal derating needs to be implemented, four resistors are used to set the various points to obtain the thermal derating curve shown in Figure 3-3.

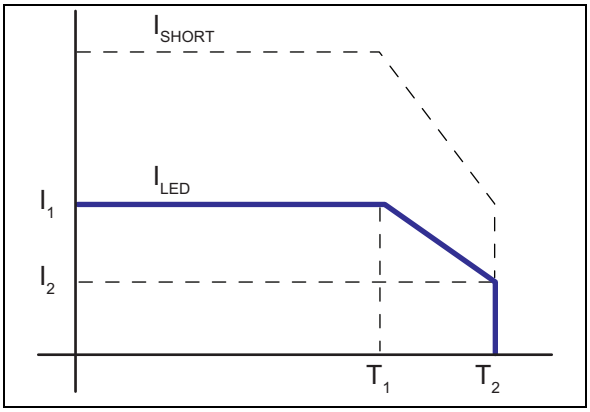


FIGURE 3-3: *Thermal Derating Curve.*

When an external NTC resistor is connected as illustrated in Figure 3-4, both temperatures T_1 and T_2, as well as the current I_2 can be accurately programmed to optimize the light output of the LED lamp for safe operation over the entire operating temperature range.

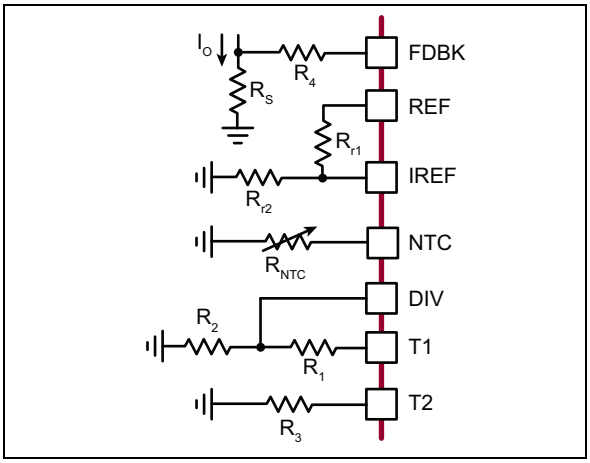


FIGURE 3-4: *With Thermal Derating.*

The ratio of the resistor divider $R_2/(R_1 + R_2)$ programs the voltage at the NTC pin. The voltage V_{T1} at T1 pin is approximately 3.5V. The current sourced by NTC pin and T1 pin is mirrored out of FDBK pin in accordance with Equation 3-18.

EQUATION 3-18:

$$I_{FDBK} = \frac{4}{30}(I_{NTC} - 3I_{T1})$$

When:

$$I_{NTC} > I_{T1}$$

I_{FDBK}, I_{NTC}, and I_{T1} are the currents sourced from pins FDBK, NTC, and T1, respectively.

Temperature T_1 is programmed by selecting R_2 as demonstrated in Equation 3-19.

EQUATION 3-19:

$$R_2 = 3 \times R_{NTC(T1)}$$

Where $R_{NTC(T1)}$ is the resistance of the NTC resistor at temperature T_1.

As illustrated in Equation 3-20, R_1 can be computed using the maximum current (≤1 mA) that will flow through the NTC resistor at temperature T_2.

EQUATION 3-20:

$$R_1 = \frac{V_{T1}}{I_{NTC,MAX}} \times \left\{\frac{R_2}{R_{NTC(T2)}}\right\} - R_2$$

Where $I_{NTC,MAX}$ is the maximum NTC current, and $R_{NTC(T2)}$ is the resistance of the NTC resistor at temperature T_2.

Further reduction of the NTC resistance R_{NTC} will create a proportional offset of the current feedback reference voltage at FDBK, and hence will cause a drop in LED current. To program the desired LED current I_2 at the temperature T_2, resistor R_4 at FDBK should be calculated as shown in Equation 3-21.

EQUATION 3-21:

$$R_4 = \frac{(I_1 - I_2) \times R_S \times (R_1 + R_2)}{V_{T1} \times \frac{4}{30}\left\{\frac{R_2}{R_{NTC(T2)}} - 3\right\}}$$

Where V_{T1} is the voltage at the T1 pin (V_{T1} = 3.5V), and $R_{NTC(T2)}$ is the resistance of the NTC resistor at temperature T_2.

The overtemperature shutdown is triggered at temperature T_2 when the current from the NTC pin I_{NTC} > [3 x I_{T1} + 6 x I_{T2}]. The voltage at T2 pin is approximately equal to the voltage at T1 pin which is 3.5V. The turn-off of the converter at the desired thermal shutdown temperature T_2 is programmed using R_3 connected from the T2 pin to GND pin. Refer to Equation 3-22.

EQUATION 3-22:

$$R_3 = \frac{6(R_1 + R_2)}{\left\{\frac{R_2}{R_{NTC(T2)}} - 3\right\}}$$

The overtemperature recovery threshold is independent of the current at the T_2 pin. AT9917 recovers from thermal shutdown at the break temperature T_1 when the current from the NTC pin I_{NTC} < $3I_{T1}$.

3.18 Soft Start (SS)

The soft-start feature controls the initial ramp-up of the error voltage at the COMP pin. Connecting a single soft-start capacitor between SS pin and GND pin can program the soft-start time. Upon the first applying voltage to the AVDD pin, a current source of typical 15 µA is supplied from the SS pin, gradually charging the soft-start capacitor. The COMP pin voltage tracks the SS pin voltage until regulation of the output current is reached. When AVDD voltage falls below the undervoltage lower threshold, the soft-start capacitor is discharged rapidly by an internal MOSFET. The soft-start time can be estimated by the Equation 3-23.

EQUATION 3-23:

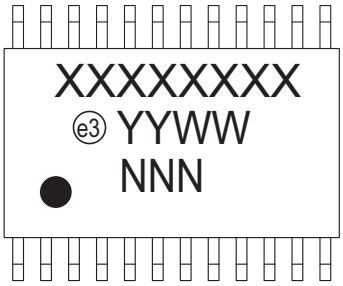
$$t_{SS} = \frac{C_{SS} \times V_{COMP}}{I_{SS,CHG}}$$

Where C_{SS} is the capacitance of the soft-start capacitor, V_{COMP} is the COMP pin voltage at normal regulation, (V_{COMP} ≈ 2.5V), and $I_{SS,CHG}$ is the soft-start charging current.

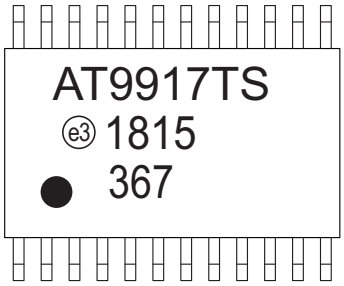
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

24-lead TSSOP



Example

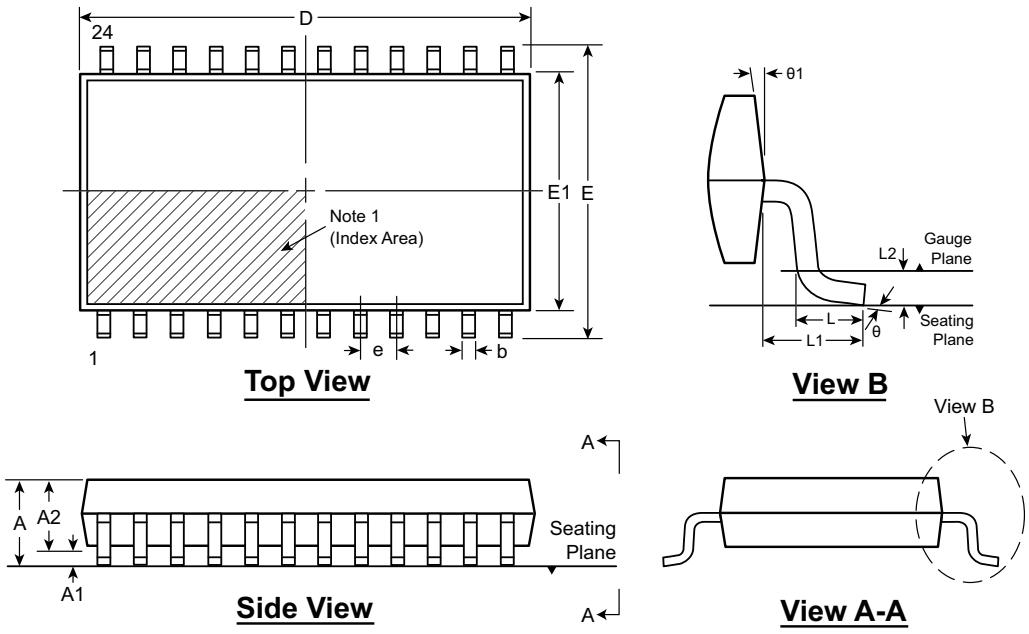


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

24-Lead TSSOP Package Outline (TS)

7.80x4.40mm body, 1.20mm height (max), 0.65mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.85*	0.05	0.80	0.19	7.70	6.20*	4.30	0.65 BSC	0.45	1.00 REF	0.25 BSC	0°	12° REF
	NOM	-	-	1.00	-	7.80	6.40	4.40		0.60			-	
	MAX	1.20	0.15	1.15†	0.30	7.90	6.60*	4.50		0.75			8°	

JEDEC Registration MS-153, Variation AD, Issue F, May 2001.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (September 2018)

- Converted Supertex Doc #s DSFP-AT9917 to Microchip DS20005557A
- Created a Detailed Description section and included **Section 3.18 “Soft Start (SS)”**
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	AT9917	=	Automotive LED Driver IC with High Current Accuracy
Package:	TS	=	24-lead TSSOP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	2500/Reel for TS Package

Example:

a) AT9917TS-G: Automotive LED Driver IC with High Current Accuracy, 24-lead TSSOP Package, 2500/Reel

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