

## Description

The AP43776Q is a highly integrated, dual-channel, USB Type-C®, PD3.1 / PPS, BC 1.2 and QC protocol decoder. It passes certification of USB Type-C power delivery specification Rev 3.1 with PPS and Quick Charge™ QC5 protocol.

The device can support the full range of PPS APDO (augmented power data object) from 3.3V to 21V with 20mV/step voltage resolution and up to 6A current with 50mA/step resolution for power management. To enable output current beyond 3A, the AP43776Q supports e-Marker cable detection with built-in VCONN switch with 30mA driving capability and over-current protection (OCP). Cable-loss compensations are also embedded.

During the power charging, AP43776Q can support Display Port Alternate Mode by decoding out the CC signal and deliver the routing signal to the mux switch through I2C interface. Meanwhile, the AP43776Q also supports BC1.2 CDP handshaking.

The AP43776Q provides an embedded MCU and built-in ADC converters for voltage and temperature measurement, where over-temperature protection (OTP) and other specific functions can be implemented through I2C pins and rich GPIO pins. Working in conjunction with two I2C-equipped Buck-Boost controllers or converters which have PD3.1 PPS output circuitry, the AP43776Q serves as the I2C master and supports two independent PD3.1 PPS charging applications without using additional output enable MOS chips for each PD3.1 output port.

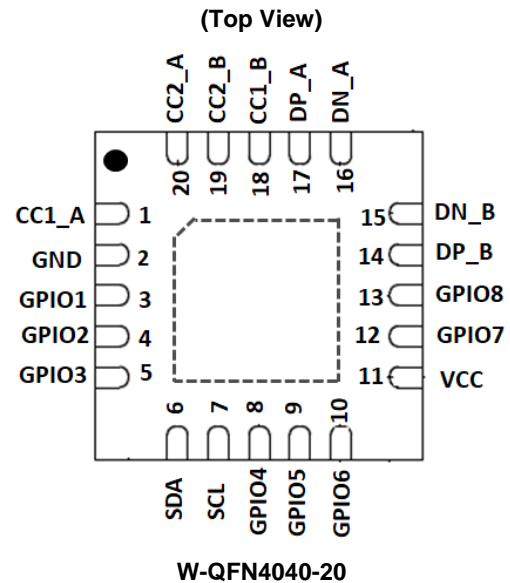
With built-in firmware, the AP43776Q can support various smart power-management functions such as power-sharing scheme between two attached USB Type-C PD devices, low-battery power de-rating, thermal power de-rating, LED light indication, etc. Two AP43776Q devices can also be interconnected through a UART (GPIO) pin to implement smart power-sharing scheme for all four connected USB Type-C ports attached to a fixed power source.

## Features

- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to +125°C TA Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C5
- Dual-channel independent USB Type-C PD3.1/PPS decoder
- USB-IF PD3.1/PPS certified TID: 9440
- Quick Charge™ QC5 certified No.: QC20211008263
- PD3.1/ full range of PPS VOUT (3.3V to 21V)
- Compliant with BC1.2 DCP mode for QC2.0/3.0/4/4+/5
- Type-C PD Display Port Alternative mode
- BC 1.2 CDP (Charging Downstream Port) mode for Charging Downstream device and allow data transfer
- Built-in ADC and multi-channel multiplexer for voltage and temperature measurement
- e-Marker detection and VCONN 30mA capability
- Cable-loss compensations
- I2C Interface and Interrupt
- Multi-purpose I/Os to support different applications
- CC1/CC2 to VBUS short protection up to 24V
- Moisture detection between DP and DN
- Thermal protection through external NTC
- Output power de-rating for low battery
- Built-in MCU with 12KB OTP ROM for main application program with multi-time-programmable ROM (MTP ROM) blocks for customization
- W-QFN4040-20(SWP) (4x4, 0.5mm pitch) package

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Assignments



## Features (continued)

- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AP43776Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**  
<https://www.diodes.com/quality/product-definitions/>

## Applications

- In-vehicle multi-port USB PD3.1 charging systems

## Typical Applications Circuit

### Application 1:

Two USB Type-C ports car charger based on one AP43776Q + two DC/DC, where I2C bus is used for communications between AP43776Q and two DC/DC controllers. It is shown that the USB Type-C output MOS switch is not needed.

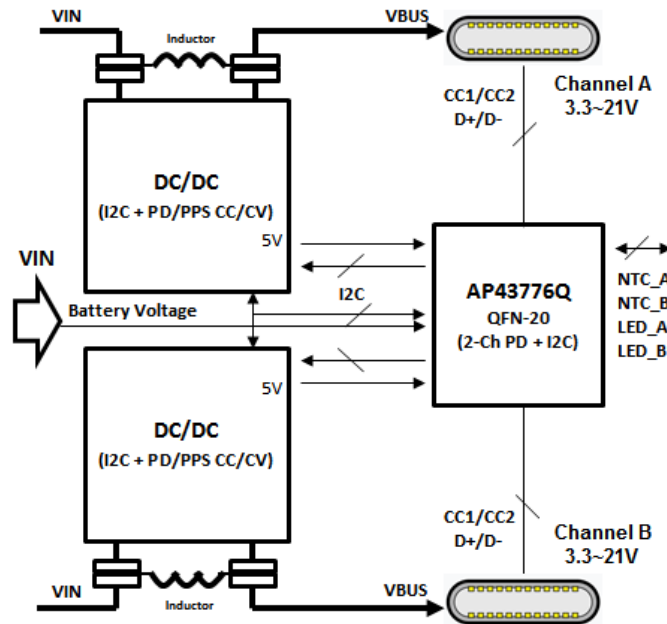


Figure 1. A two-channel car charger

### Application 2:

Four USB Type-C ports car charger based on two AP43776Q + four DC/DC controllers, where the smart power sharing is performed through I2C and UART buses.

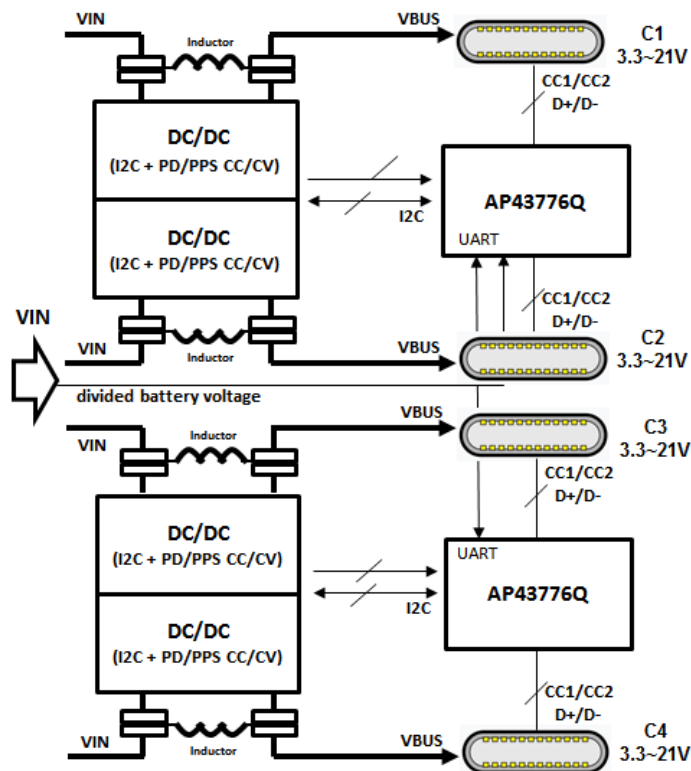
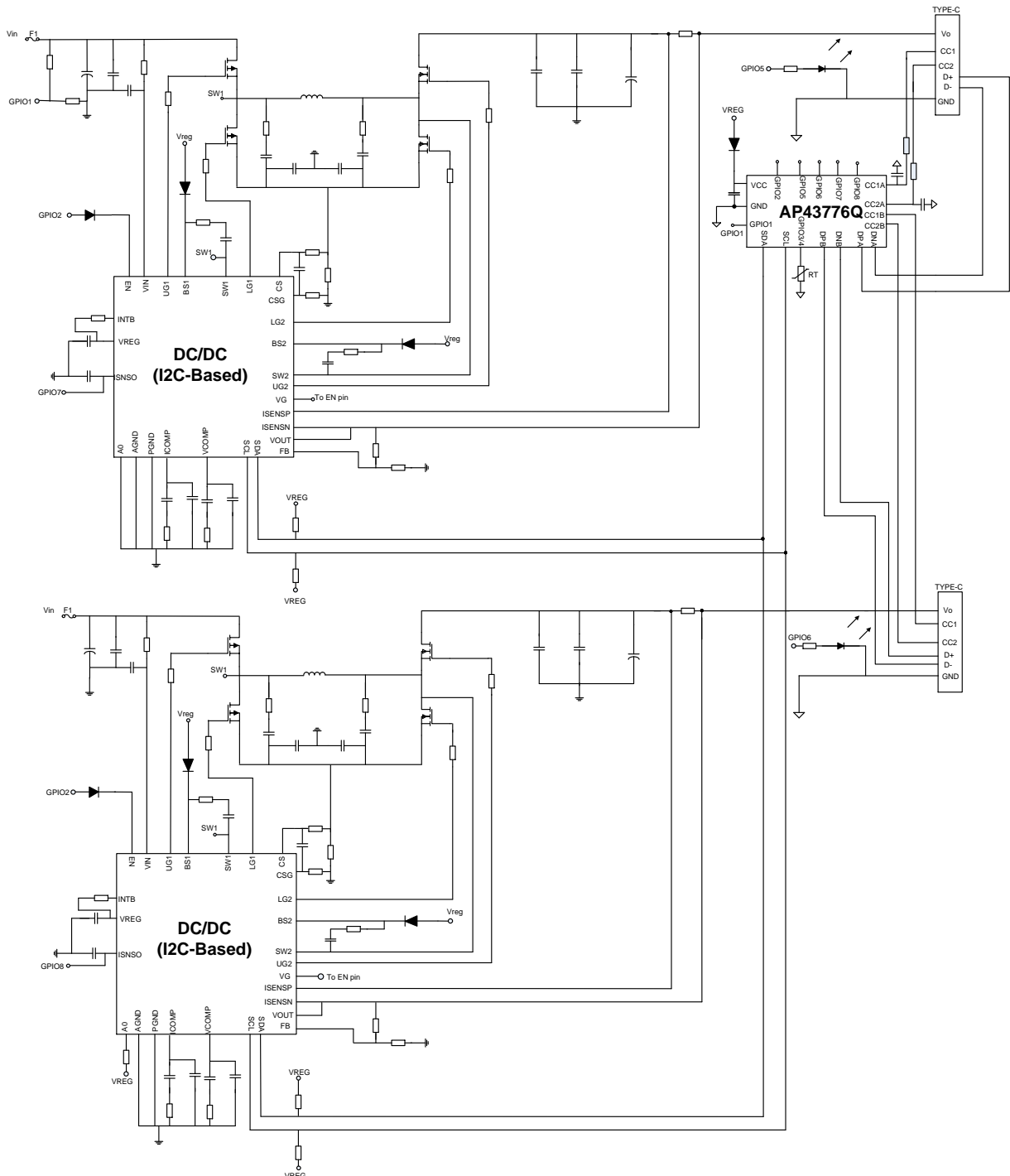


Figure 2. A four-channel car charger

**Typical Applications Circuit** (continued)

An example of the 120W Dual-port Type C PD3.1 PPS car charger is shown in Figure 3. Powered by the VREG pin (internal 5V regulator output) for the attached DC-DC controller and detecting the Vin through GPIO1, the AP43776Q may enter standby mode to disable DC/DC stage by controlling the GPIO2 pin. All PD decoded information and measured parameters of the operating conditions are processed through the CC1 and CC2 pins. The AP43776Q conveys necessary actions, such as constant voltage output, constant current output, and protection functions through the I2C interface. With built-in application firmware, VBUS MOS switches are not needed, and GPIO pins are used for battery detection, power sharing, temperature detection, LED indicators, and so on.



**Figure 3. A 120W 2C PD3.1 PPS car charger design based on 2\*DC/DC+1\*AP43776Q**

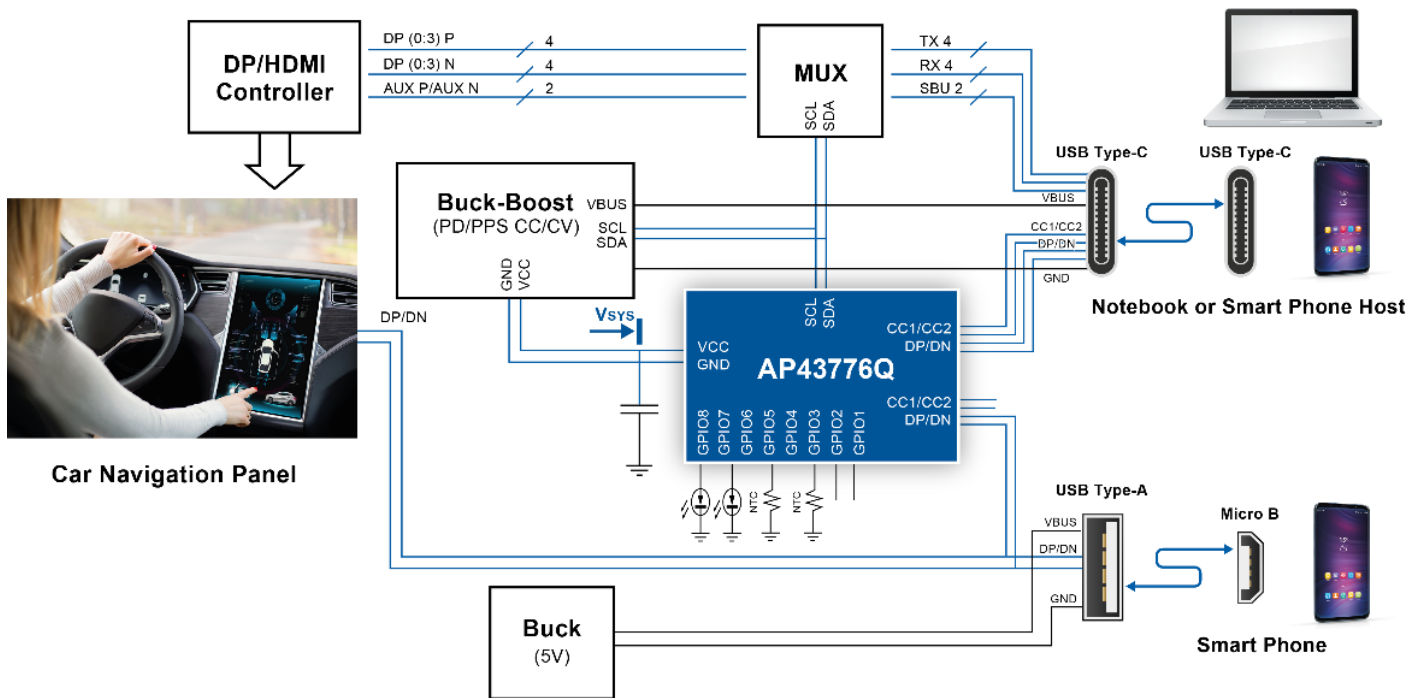
**Typical Applications Circuit** (continued)

**Application 3: Alternate Mode and BC 1.2 CDP Mode Support**

The AP43776Q not only supports power protocol decoding, but also provides data link capability. Figure 4 illustrates an AP43776Q application scenario of power source and data link.

One of the ports is used as a Type-C connector, which is connected to the Notebook host or smart phone device. The power from Down Facing Port (DFP) is sourced out to the Notebook/device, and the video data from Up Facing Port (UFP) is linked to the car navigation system through the AP43776Q supporting alternative mode. During the handshake, the AP43776Q decodes the alternative mode information of the Notebook host's or device's CC commands, and then the information is sent to the high-speed mux to switch the data path accordingly.

The other ports may be used as a Type-A connector supporting BC 1.2 CDP mode, where not only power is sourced out for the device, but also data may be linked to the car navigator at the same time.



**Figure 4. The AP43776Q supports DP alternative mode and BC 1.2 CDP mode for data link during power sourcing**

## Pin Descriptions

Pin Number	Pin Name	Function
1	CC1_A	Output to channel A Type-C CC or VCONN pin.
2	GND	Ground pin.
3	GPIO1	Multipurpose I/O pin. (define for UART application)
4	GPIO2	Multipurpose I/O pin. (define for UART application)
5	GPIO3	Multipurpose I/O pin. (define for NTC application)
6	SDA	Data pin of I2C. (define for communication with I2C-based Buck-Boost or Buck IC)
7	SCL	Clock pin of I2C. (define for communication with I2C-based Buck-Boost or Buck IC)
8	GPIO4	Multi-purpose I/O pin with current source. (defined for NTC application)
9	GPIO5	Multipurpose I/O pin. (define for LED indicator light)
10	GPIO6	Multipurpose I/O pin. (define for LED indicator light)
11	VCC	Power supply pin
12	GPIO7	General-purpose I/O pin. (define for V/I report of Buck-Boost or Buck IC)
13	GPIO8	General-purpose I/O pin. (define for V/I report of Buck-Boost or Buck IC)
14	DP_B	Connected to channel B Type-C DP pin.
15	DN_B	Connected to channel B Type-C DN pin.
16	DN_A	Connected to channel A Type-C DN pin.
17	DP_A	Connected to channel A Type-C DP pin.
18	CC1_B	Output to channel B Type-C CC or VCONN pin.
19	CC2_B	Output to channel B Type-C CC or VCONN pin.
20	CC2_A	Output to channel A Type-C CC or VCONN pin.
—	Exposed Pad	Connected to PCB Ground.

**Functional Block Diagram**

The AP43776Q is an MCU-based, dual-channel, USB Type-C, PD3.1/PPS and QC5 protocol decoder. The device's functional block diagram is shown below. With its hardware transceivers and multiplexed ADC, the rich multipurpose GPIOs can support many different kinds of applications.

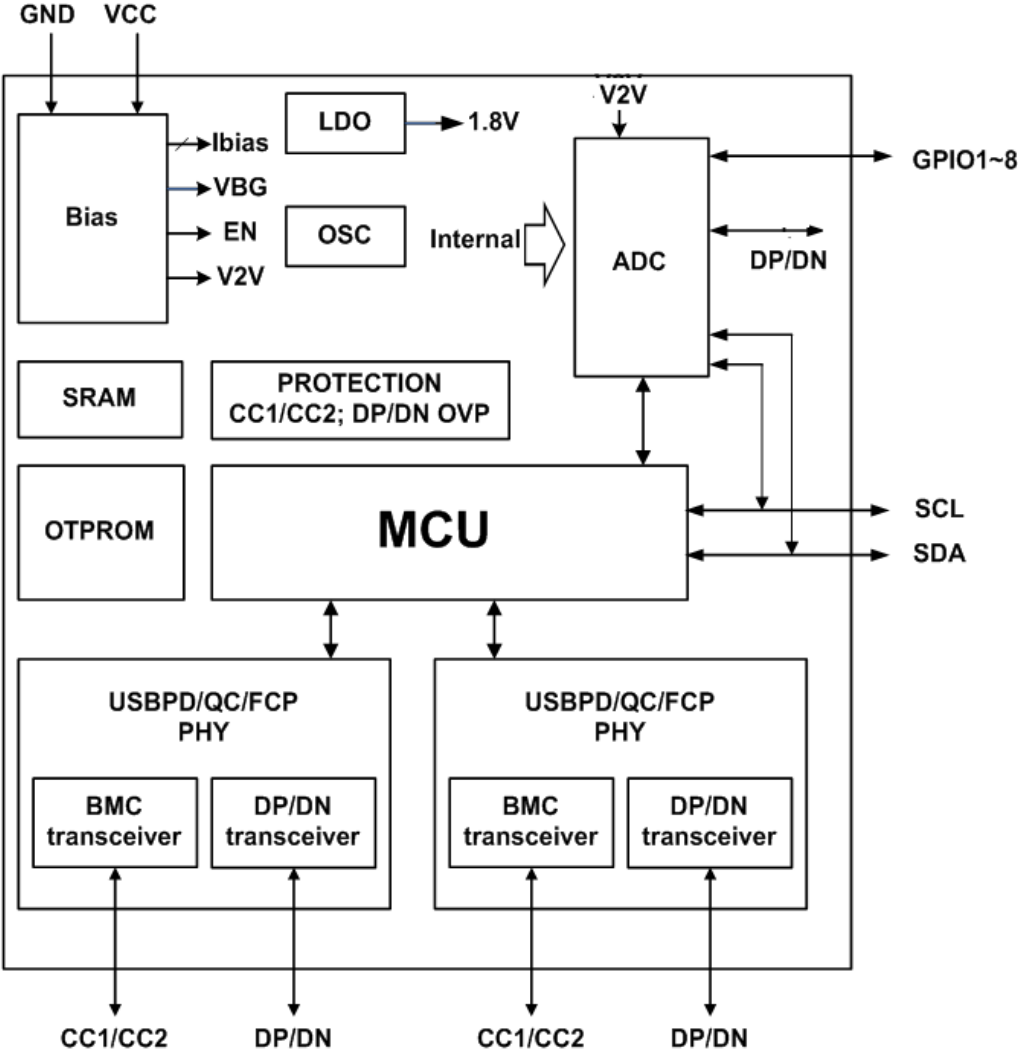


Figure 5. The functional block diagram of the AP43776Q

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## Functional Overview

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### Function Description

The AP43776Q is a highly integrated, dual-channel, USB Type-C PD3.1/PPS/QC5 protocol decoder, and has passed the certification of USB-IF PD3.1/PPS and Qualcomm™ QC5.0. To ensure two independent PD3.1 PPS protocol decoding operations are in full compliance with critical USB Power Delivery specification rev 3.1, the AP43776Q implements a combination of hardware and MCU firmware to leverage quick response times from the hardware and maintain software flexibility. To reduce noise interference during chip application, I2C communication is used between the PD controller and DC/DC converter.

### USB Type-C CC Logic & PD 3.1 Engine

The AP43776Q supports the latest USB Power Delivery Specification Revision 3.1, and is compliant to USB Type-C Cable and Connector Specification Revision 2.1. The device can support the full range of PPS APDO (augmented power data object) from 3.3V to 21V with 20mV/step voltage resolution and up to 6A current with 50mA/step resolution for power management.

The device has two independent protocol decoders and plays as two DFPs (providers only). To leverage quick response times from the hardware circuitry, it consists of USB Type-C baseband transceivers, physical-layer logic, and DP/DM transceivers for supporting QC and FCP protocols. All communications are half-duplex, and the Physical Layer provides collision avoidance to minimize communication errors during handshake. These transceivers perform the BMC and the 4b/5b encoding and decoding functions as well as the analog front end.

To perform the CC detection logic, the current sources and switches are integrated to perform the RP resistors, as required by USB Type-C specifications to implement connection detection, plug orientation detection, and to establish USB DFP role. Also, it can be programmed to indicate the complete range of current capacity on VBUS.

The built-in VCONN power switch is provided to the cable e-Marker over the CC pin that is determined not to be connected to the CC wire as soon as a cable is plugged in. The maximum output power of VCONN is 150mW.

### USB BC 1.2 DCP(Dedicated Charging Port) Mode and Quick Charging Legacy

The AP43776Q integrates the USB dedicated charging port auto detect function to recognize most of mainstream portable devices. It supports the following charging schemes like BC1.2 DCP mode, Apple mode, Chinese Telecommunications Industry Standard YD/T 1591-2009, FCP Class A, and Qualcomm Quick Charging HVDCP mode (QC2.0/3.0/4/4+/5).

### DisplayPort Alternate Mode Support

The AP43776Q supports DisplayPort Alternate Mode on USB Type-C standard with DP mode Discovery, Enter, Exit included by decoding out the control signals from CC handshaking, and delivering to the mux switches through I2C interface, and then the USB Type-C data stream can be routed to the DP/HDMI receiver correctly. Also, the DP configuration, status update, and source/sink connection detection are provided.

### USB BC1.2 CDP Mode

The AP43776Q also supports BC 1.2 CDP (Charging Downstream Port) Mode. It can be enabled by I2C communication. When CDP is enabled, QC/Apple and DCP modes on DP and DM will be turned off.

### Bias and Power

The AP43776Q operates from a single external supply source, VCC. VCC is used for analog circuitry and goes through internal regulators to generate all of the voltage and current references for chip operation, without the need for external capacitor decoupling. The AP43776Q has two different power modes: normal and sleep. During normal operation, the AP43776Q consumes less than 3mA. During sleep mode, its current can be reduced to around 0.5mA automatically.

### I2C Interface

For USB Type-C PD charging system, the I2C interface pins (SCK, SDA) are used to communicate between the PD decoder and DC/DC controller/converter to replace analog signal feedback with much higher noise immunity. The AP43776Q is in charge of the CC1/CC2 or DP/DN protocol handshake with the attached device, and deliver the voltage and current request to DC/DC controller/converter through I2C bus.

The AP43776Q, working as an I2C master device, keeps track of charging capability of each USB Type-C port through I2C interface pins at the same time. Based on the user-specified and desired smart power-sharing options for the two charging ports, the AP43776Q decides the final charging profiles for each port.

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**Functional Overview** (continued)

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**MCU and OTP/MTP ROM**

The AP43776Q has an MCU subsystem, which integrates an 8-bit 8051 processor, SRAM, and OTP ROM. The MCU subsystem is optimized for user configurability of different topologies, support of different protocols, and low-power consumption at a low cost. With the embedded hardware PHY transceivers offloading MCU processing, the AP43776Q can handle two channels of PD handshakes efficiently through an MCU simultaneously, and be compliant with critical USB Power Delivery specifications.

An OTP ROM is provided to store PD, QC, and FCP protocol firmware, and an MTP ROM is provided for user configuration table. Either in-system programming or offline socket programming are provided for the OTP ROM and MTP ROM.

**ADC**

The AP43776Q contains a 10-bit SAR (successive approximation register) ADC and multi-channel multiplexer for analog to digital conversions. All GPIO inputs can be connected to the internal analog multiplex busses through a switch. With the ADC voltage reference, VREF, being set at 2V, any input voltage,  $V_{in}$ , on the GPIO can be digitized into a 10-bit digital code proportional to  $V_{in}/V_{REF}$ . The sampling rate of ADC is 100KHz, but the firmware re-samples the ADC output by 1ms/time, and some longer de-glitch time is used to qualify the ADC output code. Meanwhile, ADC is used to detect and monitor analog signals on the non-GPIO pins like CC1/CC2/VCONN and DP/DN, and then come out the associated OVP protections.

**GPIO Support**

There are many GPIO pins that can be used to support customization features, like low-voltage battery, power de-rating, thermal power de-rating, LED light indication, fault status, and so on. The GPIO pin can also be used for UART communication to support four USB Type-C ports, and some GPIOs support current sources for external NTC temperature detection.



### Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V <sub>CC</sub>	Input Voltage at V <sub>CC</sub> Pin	6.0	V
V <sub>CC1A</sub> , V <sub>CC2A</sub> , V <sub>CC1B</sub> , V <sub>CC2B</sub>	Input Voltage at CC1_A, CC2_A, CC1_B, CC2_B Pins	24	V
V <sub>DPA</sub> , V <sub>DNA</sub> , V <sub>DPB</sub> , V <sub>DNB</sub> , SDA, SCL and GPIO <sub>x</sub>	Input Voltage at DPA, DNA, DPB, DNB, SDA, SCL, and GPIO <sub>x</sub> Pins	6.0	V
T <sub>J</sub>	Operating Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
T <sub>LEAD</sub>	Lead Temperature (Soldering, 10s)	+300	°C
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient) (Note 5)	122	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case) (Note 5)	27	°C/W
ESD	ESD (Human Body Model) Voltage on D+, D- Pins	±6	kV
	ESD (Human Body Model) Voltage on other Pins	±4	kV
	ESD (Charged Device Model)	±1000	V

- Notes:
- Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
  - Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with the minimum footprint.

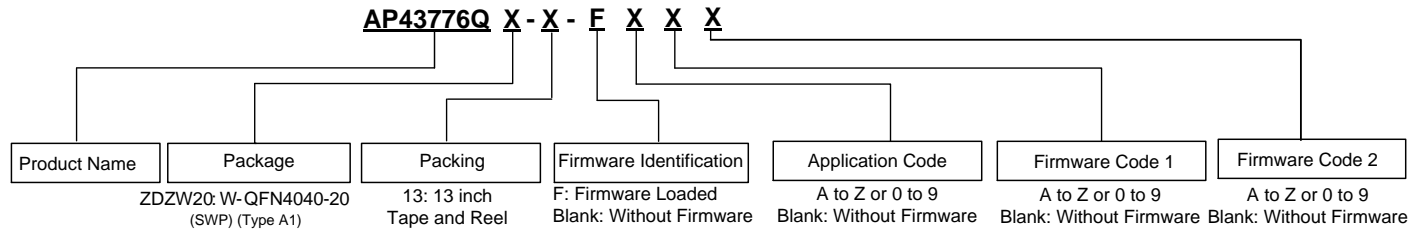
### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Power Supply Voltage	3	5.5	V
T <sub>OP</sub>	Operating Temperature Range	-40	+125	°C

**Electrical Characteristics** ( $-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$ ,  $V_{CC} = 5\text{V}$ , unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
<b>VCC PIN &amp; INTERNAL BIAS SECTION</b>						
$V_{CC\_OP}$	VCC Operation Range	—	3	—	5.5	V
$V_{CC\_POR}$	VCC Power-on Reset Voltage	—	2.0	—	3.1	V
$V_{CC\_POR\_HYS}$	VCC Power-on Hysteresis	—	—	0.1	—	V
$I_{SM}$	Sleep Mode Current	$V_{CC} = 5\text{V}$ @ sleep mode	150	—	1200	$\mu\text{A}$
$I_{CC\_OP}$	Operating Supply Current	—	1.1	—	3.0	mA
$I_{S\_SCL}$	Sink Current of SCL for impedance check	$V_{SCL} = 1\text{V}$	760	840	920	$\mu\text{A}$
$V_{2V}$	Internal Reference Voltage	$2.046 \pm 5\%$	1.944	2.046	2.148	V
$CLK_{12M}$	Internal Clock Frequency	$12\text{MHz} \pm 10\%$	10.8	12	13.2	MHz
<b>CC1/CC2 PIN SECTION</b>						
$V_{OH\_open}$	Pull High Voltage of CCx	—	3.4	3.6	3.8	V
$I_{rp\_330}$	Source Current of CCx	$R_D = 5.1\text{k}\Omega$	305	330	355	$\mu\text{A}$
$V_{SW\_TxDC}$	Voltage Swing of CCx for BMC Tx	$R_D = 5.1\text{k}\Omega$	1.05	1.125	1.2	V
$V_{SW\_TxDCL}$	Low Voltage Swing of CCx for BMC Tx	$R_D = 5.1\text{k}\Omega$	0	—	75	mV
$R_{VCONN}$	Rds_on of internal Vconn switch	—	—	15	—	$\Omega$
<b>DN/DP PIN SECTION</b>						
$V_{DP\_APP}$	DP Apple mode output voltage	—	2.52	2.8	3.08	V
$V_{DN\_APP}$	DN Apple mode output voltage	—	2.52	2.8	3.08	V
$DP\_DWM20K$	DP 20K pull down resistor	—	18	20	22	k $\Omega$
$DN\_DWM20K$	DN 20K pull down resistor	—	18	20	22	k $\Omega$
$DP\_DWM900K$	DP 900K pull down resistor	—	600	—	1400	k $\Omega$
$DN\_DWM900K$	DN 900K pull down resistor	—	600	—	1400	k $\Omega$
$R_{DPDN\_short}$	DPDN short resistor	—	5	20	40	$\Omega$
$R_{DN\_IMP}$	Impedance check of DN for attach function	—	100	—	350	$\Omega$
<b>DIGITAL I/O PIN SECTION (DP/DN/GPIO1~GPIO8)</b>						
$V_{OH}$	Logic Output High Level Voltage	Source Current 4mA	$V_{CC}-0.2$	—	—	V
$V_{OL}$	Logic Output Low Level Voltage	Sink Current 4mA	—	—	200	mV
$I_{S\_OTP}$	Source Current for OTP Pins (GPIO3 and GPIO4)	—	126	140	154	$\mu\text{A}$
<b>ADC SECTION</b>						
$V_{ADC\_REF}$	ADC Reference Voltage	—	—	2.046	—	V
$V_{OFFSET}$	ADC Offset Voltage	—	—	$\pm 4.0$	—	mV
<b>PROTECTION SECTION</b>						
$V_{DP\_OVP}$	$V_{ABCV_{DP\_OVP}}$	$V_{DP\_OVP}$	4.1	4.35	4.6	V
$V_{DN\_OVP}$	$V_{DN\_OVP}$	$V_{DN\_OVP}$	4.1	4.35	4.6	V
$I_{VCONN\_OCP}$	VCONN Overcurrent Protection	—	32	48	56	mA

**Ordering Information**

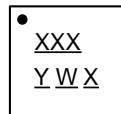


Orderable Part Number	Package (Note 6)	Marking ID	Packing		
			Quantity	Carrier	Part Number Suffix
AP43776QZDZW20-13	W-QFN4040-20(SWP)	B4Q	3,000	13" Tape and Reel	-13

Note: 6. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

**Marking Information**

**(Top View)**

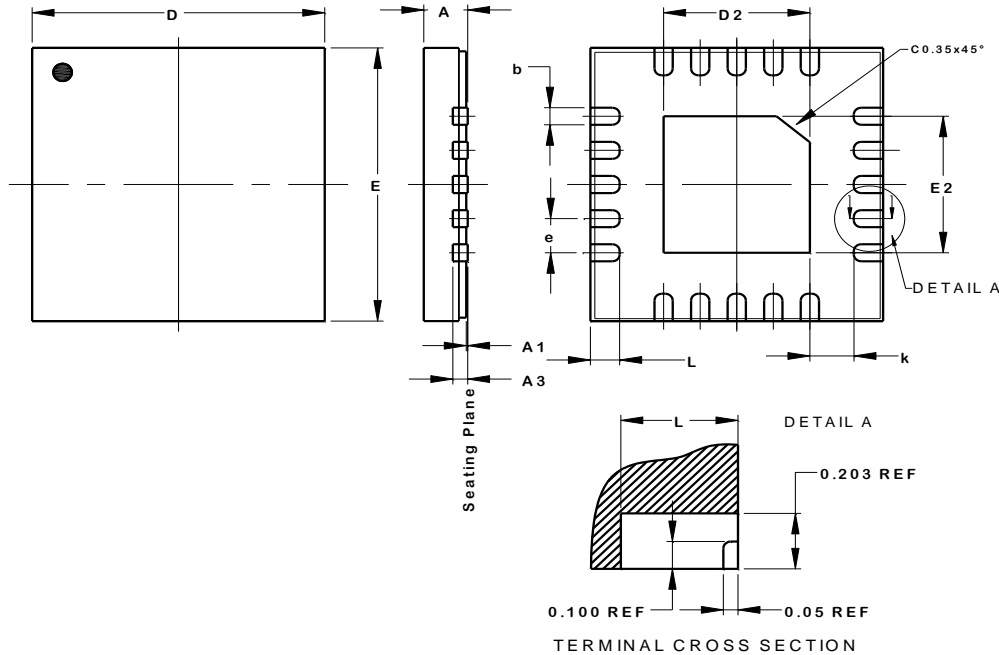


- XX : Identification Code
- Y : Year : 0~9
- W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents  
52 and 53 week
- X : Internal Code

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-QFN4040-20 (SWP) (Type A1)

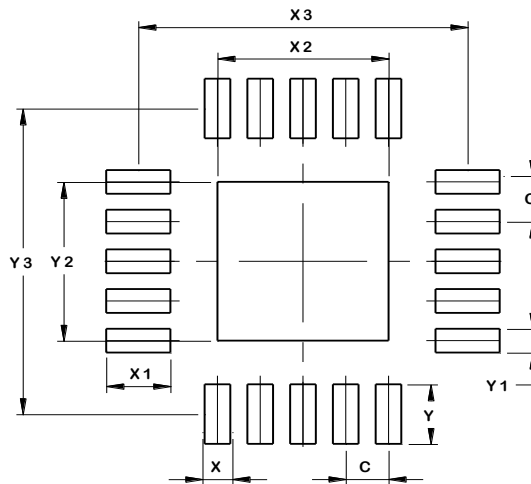


W-QFN4040-20 (SWP) (Type A1)			
Dim	Min	Max	Typ
A	0.70	0.80	0.75
A1	0.00	0.05	0.02
A3	0.203 REF		
b	0.20	0.30	0.25
D	4.00 BSC		
D2	1.95	2.05	2.00
E	4.00 BSC		
E2	1.95	2.05	2.00
e	0.50 BSC		
k	0.20	--	--
L	0.30	0.50	0.40
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

W-QFN4040-20 (SWP) (Type A1)



Dimensions	Value (in mm)
C	0.500
X	0.300
X1	0.750
X2	2.000
X3	3.850
Y	0.750
Y1	0.300
Y2	2.000
Y3	3.850

## Mechanical Data

- Moisture Sensitivity: Level 1 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 Ⓔ3
- Weight: 0.0408 grams (Approximate)

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