

Description

The AP22654Q and AP22655Q are single channel precision adjustable current-limit switches optimized for applications that require precision current limiting, or to provide up to 3.1A of continuous load current during heavy loads/short circuits. These devices offer a pin-strapped current-limit threshold between 0.4A and 3.56A (typ) via an external resistor. Current limit accuracy $\pm 12\%$ can be achieved at high current-limit settings. The rise and fall times are controlled to minimize current surges during turn on/off.

The devices have fast short-circuit response time for improved overall system robustness. They provide a complete protection solution for applications subject to heavy capacitive loads and the prospect of short circuit, offering reverse current blocking and limiting, overcurrent, overtemperature and short-circuit protections, as well as controlled rise time and undervoltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false overcurrent reporting and does not require any external components.

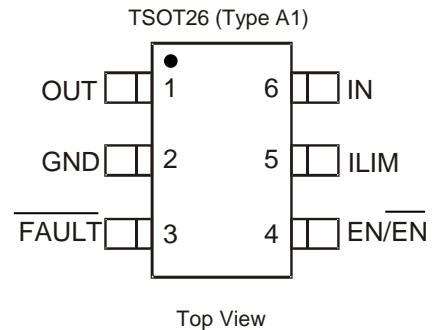
AP22654Q and AP22655Q limit the output current to a safe level when the output current exceeds current-limit threshold.

Both devices are available in TSOT26 (Type A1) package.

Applications

- Automotive ECU supply rail power distribution and switching
- Automotive ECU supply rail precision current limiting

Pin Assignments

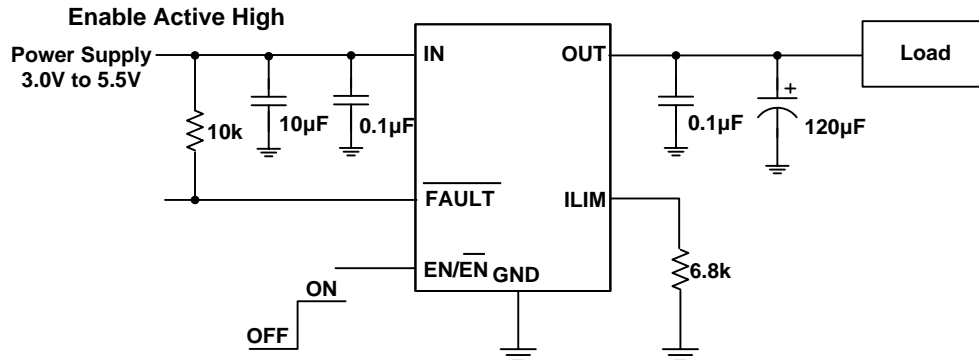


Features

- AEC Qualified to AEC-Q100 Grade 1 Offering -40°C to +125°C Ambient Operating Temperature Range
- Up to 3.1A Maximum Load Current
- Accurate Adjustable Current Limit, 0.4A to 3.56A
- $\pm 12\%$ Accurate Adjustable Current Limit, 1.0A with $R_{LIM} = 6.8k\Omega$
- Constant Current During Overcurrent
- Fast Short-Circuit Response Time: 5 μ s (typ)
- Reverse Current Blocking During Shutdown and Reverse Current Limiting During Enable
- Operating Range: 3.0V to 5.5V
- Built-in Soft-Start with 1.0ms Typical Rise Time
- Overcurrent, Reverse Output Current/Voltage and Thermal Protection
- Fault Report (FAULT) with Blanking Time
- ESD Protection: 2kV HBM, 1.5kV CDM
- Active Low (AP22654Q) or Active High (AP22655Q) Enabled
- TSOT26 (Type A1) Package: Available in "Green" Molding Compound (No Br, Sb)
- 15kV ESD Protection per IEC 61000-4-2 (With Ext. Capacitance)
- UL Recognized, File Number E322375, Vol. 1
- IEC62368-1 CB Scheme Certified
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. "Green" Device (Note 3)**
- The AP22654Q and AP22655Q are suitable for automotive applications requiring specific change control; these parts are AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**

<https://www.diodes.com/quality/product-definitions/>

- Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 - See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit (Note 4)


Note: 4. 120µF output capacitance is a requirement of USB.

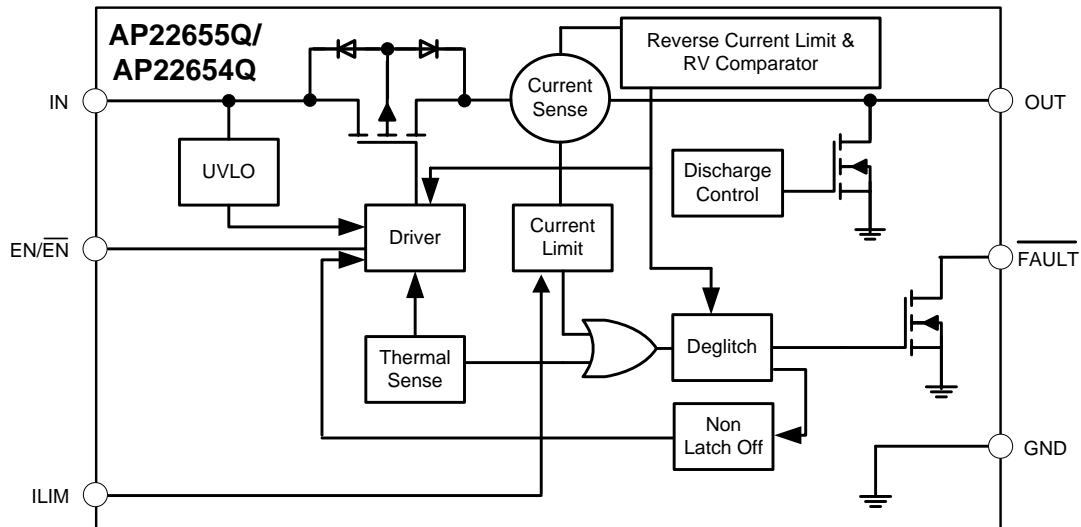
Available Options

Part Number	Channel	Enable Pin (EN)	Recommended Maximum Continuous Load Current (A)	Current-Limit Protection	Package
AP22654Q	1	Active Low	3.1	Constant-Current	TSOT26 (Type A1)
AP22655Q	1	Active High			TSOT26 (Type A1)

Pin Descriptions

Pin Name	Pin Number		I/O	Function
	AP22654Q	AP22655Q		
IN	6	6	I	Input, connect a 0.1µF bypass capacitor and a high-value capacitor to GND close to IC as possible. (At least 10µF in Input voltage.)
GND	2	2	—	Ground, connect to external exposed pad.
$\overline{\text{EN}}$	4	—	I	Enable input, logic low turns on power switch.
EN	—	4	I	Enable input, logic high turns on power switch.
$\overline{\text{FAULT}}$	3	3	O	Active-low open-drain output, asserted during overcurrent, overtemperature, or reverse-voltage conditions.
ILIM	5	5	O	Use external resistor to set current-limit threshold; recommended $1.91\text{k}\Omega \leq R_{\text{LIM}} \leq 16.9\text{k}\Omega$. $\text{ILIM} = 6800/R_{\text{LIM}}(\text{k}\Omega)$
OUT	1	1	O	Voltage output pin. Connecting 0.1µF bypass capacitor and a high-value capacitor to GND close to IC. (At least 10µF in USB application)
Exposed Pad	—	—	—	Internal connection to GND; connect to GND externally for improved power dissipation. It should not be used as electrical ground conduction path.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Ratings	Unit	
ESD	HBM	Human Body Model ESD Protection (Note 5)	2	kV
	CDM	Charged Device Model ESD Protection	1.5	kV
	IEC System Level	Surges per EN61000-4-2. 1999 Applied to Output Terminals of EVM (Note 6)	15	kV
V _{IN} , V _{OUT} , V _{FAULT} , V _{ILIM} , V _{EN} , V _{EN-bar}	Voltage on IN, OUT, FAULT, ILIM, EN, EN-bar	-0.3 to +6.0	V	
—	Continuous FAULT Sink Current	25	mA	
—	ILIM Source Current	1	mA	
I _{LOAD}	Maximum Continuous Load Current	Internal Limited	A	
T _{J(MAX)}	Maximum Junction Temperature	+150	°C	
T _{ST}	Storage Temperature Range (Note 7)	-65 to +150	°C	
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 8)	89	°C/W	
R _{θJC}	Thermal Resistance, Junction to Case (Note 8)	45	°C/W	

- Notes:
- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
 - External capacitors need to be connected to the output, EVM board was tested with external capacitor. This level is a pass test only and not a limit.
 - UL recognized rating from -30°C to +70°C (Diodes Incorporated qualified T_{ST} from -65°C to +150°C).
 - The JEDEC high-K (2s2p) board used to derive this data was a 3inch x 3inch, multilayer board with 1oz internal power and ground planes with 2oz copper traces on top and bottom of the board.

Caution: Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Recommended Operating Conditions (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	3.0	5.5	V
I_{OUT}	Output Current, $4.0\text{V} \leq V_{IN} \leq 5.5\text{V}$ ($-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$)	0	2.0	A
	Output Current, $4.0\text{V} \leq V_{IN} \leq 5.5\text{V}$ ($-40^\circ\text{C} \leq T_J \leq +105^\circ\text{C}$)	0	2.4	A
	Output Current, $4.0\text{V} \leq V_{IN} \leq 5.5\text{V}$ ($-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$)	0	3.1	A
$V_{EN}, V_{\overline{EN}}$	Enable Voltage	0	V_{IN}	V
V_{IH}	High-Level Input Voltage on EN or \overline{EN}	1.5	V_{IN}	V
V_{IL}	Low-Level Input Voltage on EN or \overline{EN}	0	0.4	V
R_{LIM}	Current-Limit Threshold Resistor Range (1% Initial Tolerance)	1.91	16.9	k Ω
I_o	Continuous FAULT Sink Current	0	10	mA
—	Input De-Coupling Capacitance, IN to GND	0.1	—	μF
T_J	Operating Junction Temperature $I_{OUT} \leq 2.0\text{A}$	-40	+125	$^\circ\text{C}$
	Operating Junction Temperature $I_{OUT} \leq 2.4\text{A}$	-40	+105	$^\circ\text{C}$
	Operating Junction Temperature $I_{OUT} \leq 3.1\text{A}$	-40	+85	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{IN} = 3.0\text{V}$ to 5.5V , $V_{EN} = 0\text{V}$ or $V_{EN} = V_{IN}$, $R_{FAULT} = 10\text{k}\Omega$, unless otherwise specified.)

Symbol	Parameter	Test Conditions (Note 9)	Min	Typ	Max	Unit	
Supply							
V_{UVLO}	Input UVLO	V_{IN} Rising	—	2.25	2.65	V	
ΔV_{UVLO}	Input UVLO Hysteresis	V_{IN} Decreasing	—	100	—	mV	
I_{SHDN}	Input Shutdown Current	$V_{IN} = 5.0\text{V}$, Disabled, by EN = V_{IN} or GND, OUT = Open	—	0.1	1	μA	
I_Q	Input Quiescent Current	$V_{IN} = 5.0\text{V}$, Enabled, by EN = V_{IN} or GND, OUT = Open	—	90	120	μA	
I_{REV}	Reverse Leakage Current	Disabled, $V_{IN} = 0\text{V}$, $V_{OUT} = 5.0\text{V}$, I_{REV} at V_{IN}	—	0.01	1	μA	
Power Switch							
$R_{DS(ON)}$	Switch On-Resistance	TSOT26 (Type A1) Package	$T_A = +25^\circ\text{C}$, $V_{IN} = 5.0\text{V}$	—	50	75	m Ω
			$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	—	—	85	
t_R	Output Turn-On Rise Time	$V_{IN} = 5.0\text{V}$, $C_L = 1\mu\text{F}$, $R_{LOAD} = 100\Omega$ (See Figure 1)	—	1	1.5	ms	
		$V_{IN} = 3.3\text{V}$, $C_L = 1\mu\text{F}$, $R_{LOAD} = 100\Omega$	—	0.6	1	ms	
t_F	Output Turn-Off Fall Time	$V_{IN} = 5.0\text{V}$, $C_L = 1\mu\text{F}$, $R_{LOAD} = 100\Omega$ (See Figure 1)	0.1	—	0.5	ms	
		$V_{IN} = 3.3\text{V}$, $C_L = 1\mu\text{F}$, $R_{LOAD} = 100\Omega$	0.1	—	0.5	ms	
Current Limit							
I_{LIMIT}	Current-Limit Threshold (Maximum DC Output Current) $V_{IN} = 5\text{V}$, $V_{OUT} = 4.5\text{V}$	$R_{LIM} = 1.91\text{k}\Omega$	3133	3560	3987	mA	
		$R_{LIM} = 2.7\text{k}\Omega$	2217	2519	2821		
		$R_{LIM} = 4.53\text{k}\Omega$	1321	1501	1681		
		$R_{LIM} = 6.8\text{k}\Omega$	880	1000	1120		
		$R_{LIM} = 12.1\text{k}\Omega$	478	562	646		
		$R_{LIM} = 16.9\text{k}\Omega$	322	402	482		
I_{SHORT}	Short-Circuit Current Limit, OUT Connected to GND	$R_{LIM} = 1.91\text{k}\Omega$	—	890	—	mA	
		$R_{LIM} = 2.7\text{k}\Omega$	—	630	—		
		$R_{LIM} = 4.53\text{k}\Omega$	—	375	—		
		$R_{LIM} = 6.8\text{k}\Omega$	—	250	—		
		$R_{LIM} = 12.1\text{k}\Omega$	—	141	—		
		$R_{LIM} = 16.9\text{k}\Omega$	—	101	—		
Enable Pin							
$I_{LEAK-EN}$	EN Input Leakage Current	$V_{IN} = 5\text{V}$, $V_{EN} = 0\text{V}$ and 5.5V	-2	—	2	μA	
t_{ON}	Turn-On Time	$C_L = 1\mu\text{F}$, $R_L = 100\Omega$ (See Figure 1)	—	—	4	ms	
t_{OFF}	Turn-Off Time	$C_L = 1\mu\text{F}$, $R_L = 100\Omega$ (See Figure 1)	—	—	1	ms	
Output Discharge							
R_{DIS}	Discharge Resistance	$V_{IN} = 5\text{V}$, Disabled, $I_{OUT} = 1\text{mA}$	—	500	—	Ω	

Note: 9. Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

Electrical Characteristics (continued)

(@T_A = +25°C, V_{IN} = 3.0V to 5.5V, V_{EN} = 0V or V_{EN} = V_{IN}, R_{FAULT} = 10kΩ, unless otherwise specified.)

Symbol	Parameter	Test Conditions (Note 9)	Min	Typ	Max	Unit
Reverse Voltage Protection						
V _{RV} P	Reverse-Voltage Comparator Trip Point	V _{OUT} – V _{IN}	—	65	—	mV
I _{ROCP}	Reverse Current Limit	V _{OUT} – V _{IN} = 150mV	—	0.32	—	A
t _{TRIG}	Time from Reverse-Voltage Condition to MOSFET Turn Off	V _{IN} = 5V	2	7	20	ms
Fault Flag						
V _{OL}	FAULT Output Low Voltage	I _{FAULT} = 1mA	—	—	180	mV
I _{FOH}	FAULT Off Current	V _{FAULT} = 5.5V	—	—	1	μA
t _{blank}	FAULT Blanking Time	Assertion or Deassertion due to Overcurrent and Overtemperature Conditions	2	7	20	ms
Thermal Shutdown						
T _{SHDN}	Thermal Shutdown Threshold	Enabled	—	+155	—	°C
T _{HYS}	Thermal Shutdown Hysteresis	—	—	+35	—	°C

Typical Performance Characteristics

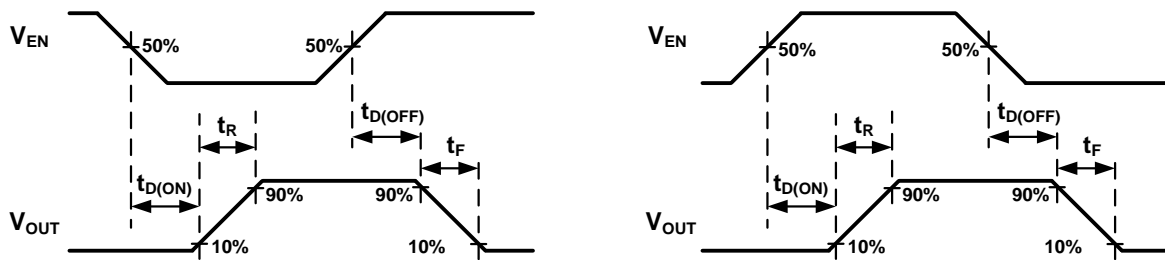
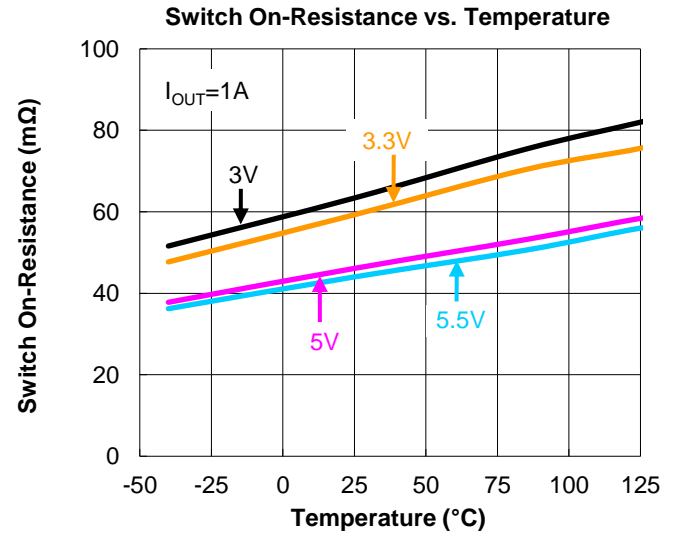
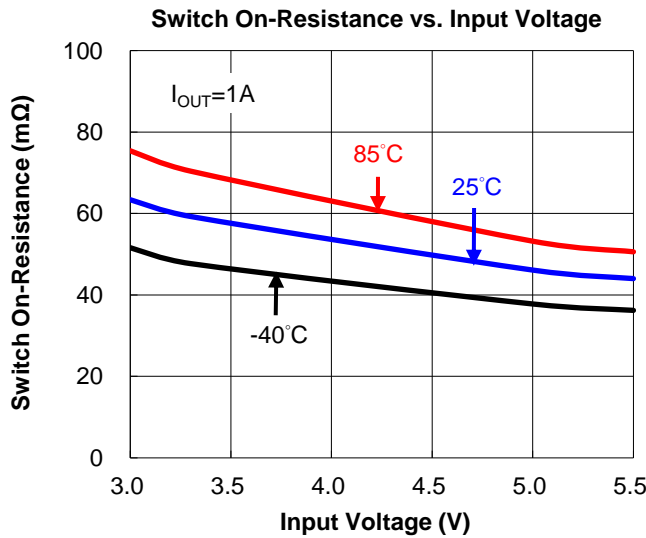
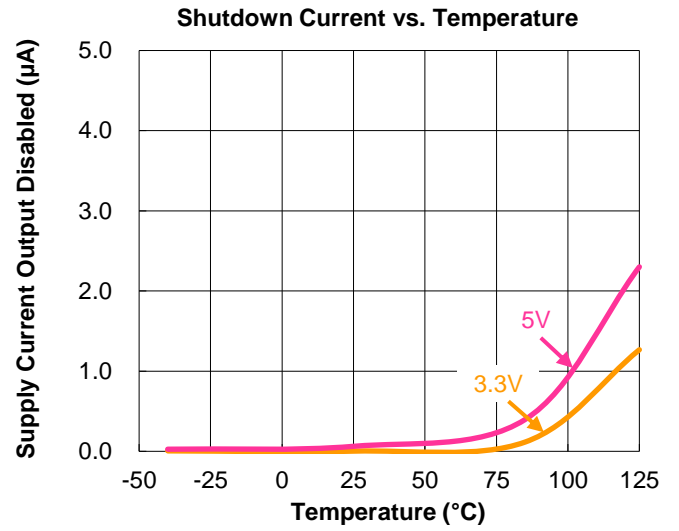
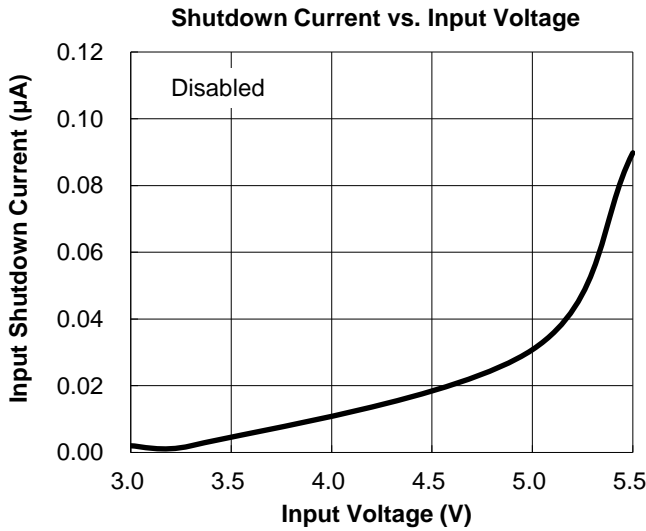
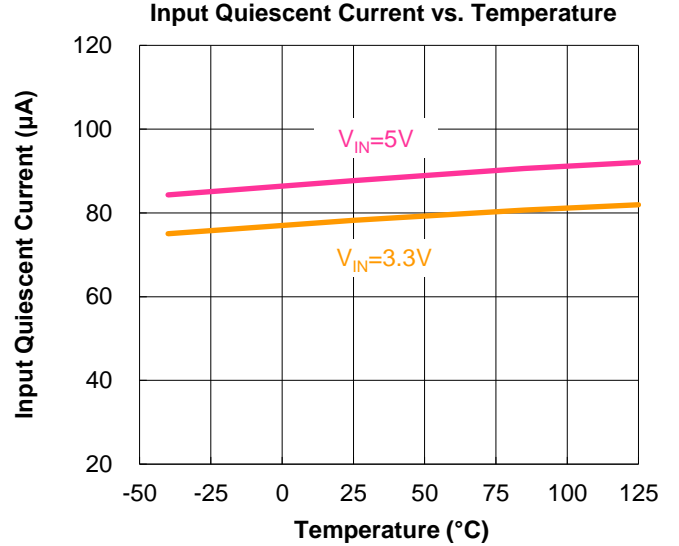
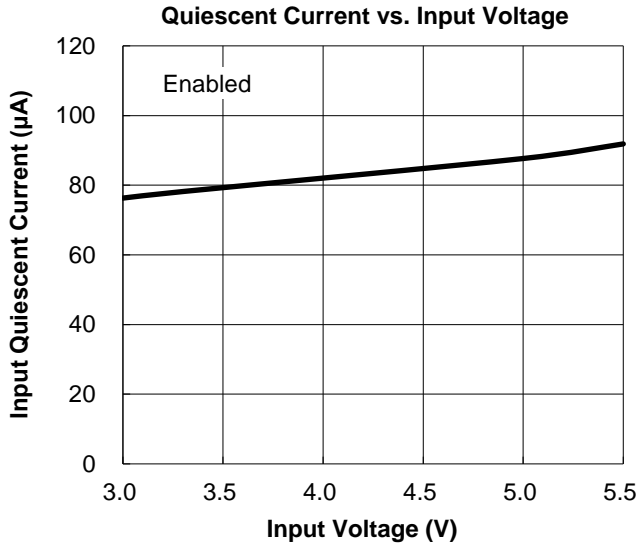
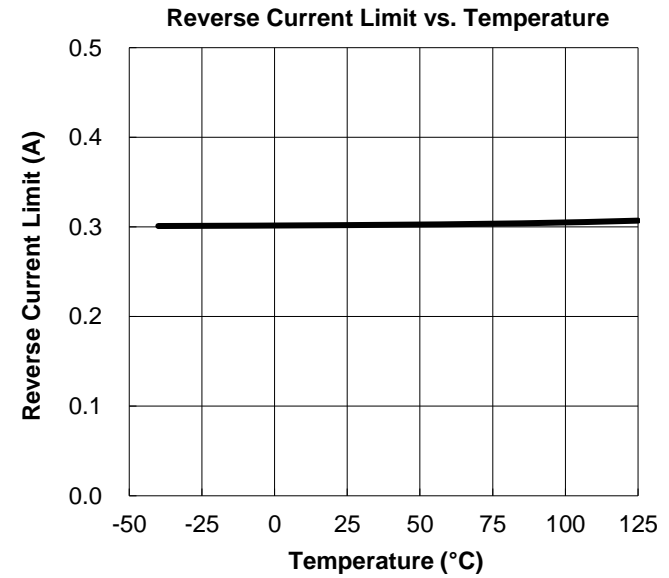
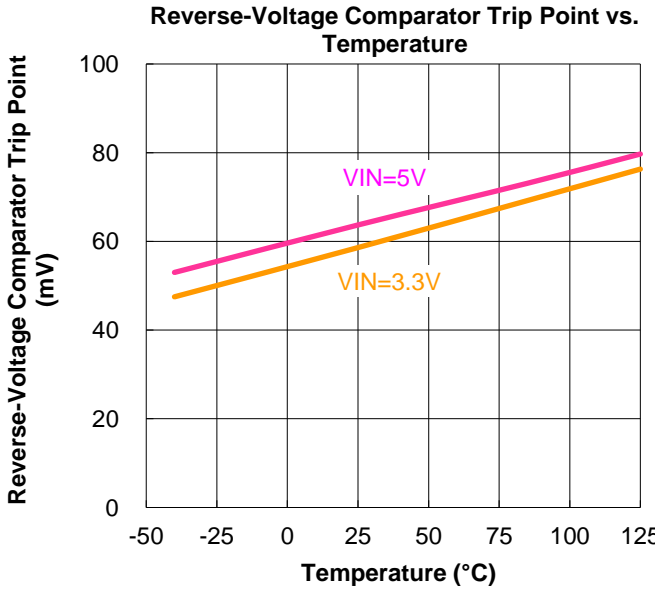
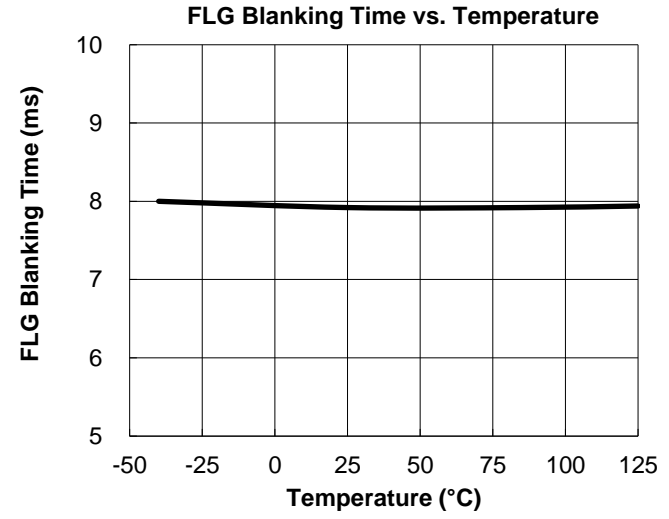
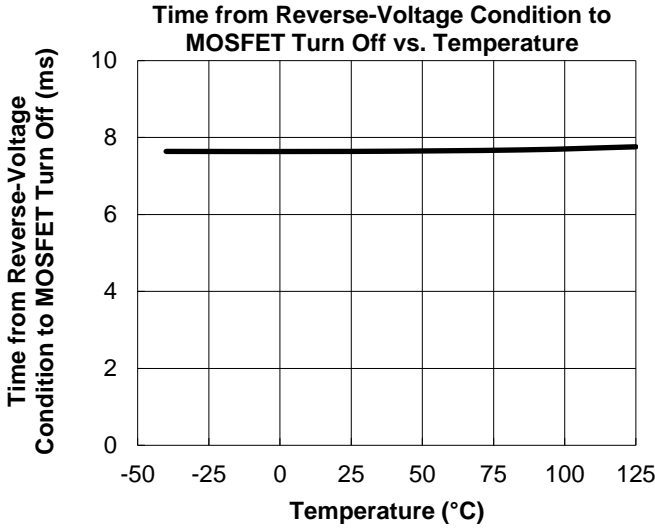
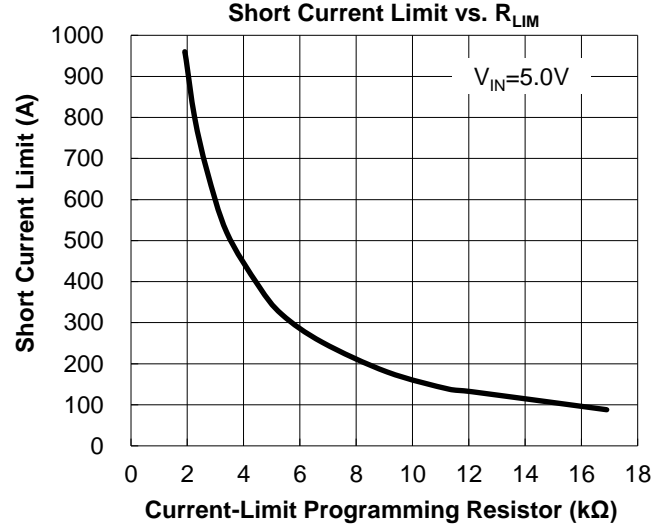
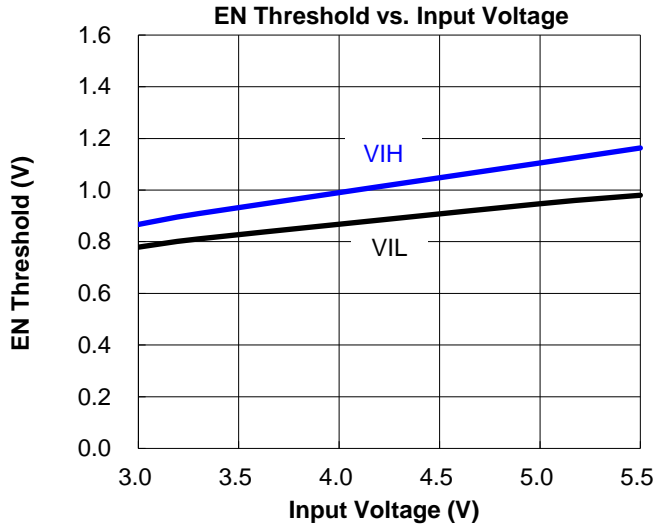


Figure 1. Voltage Waveforms: AP22654Q (Left), AP22655Q (Right)

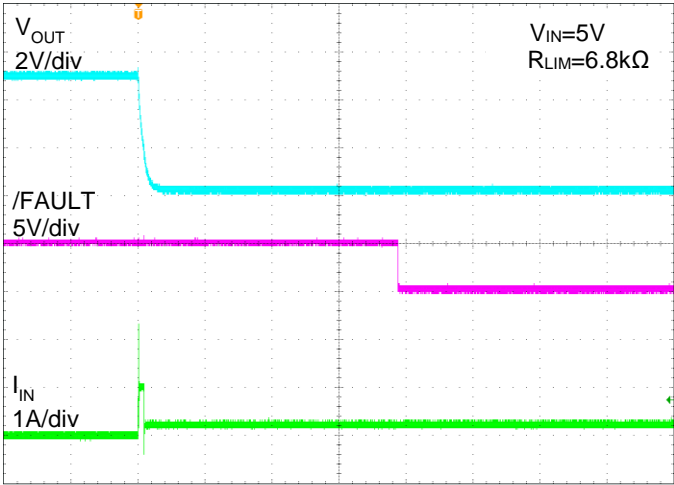
Typical Performance Characteristics (continued)



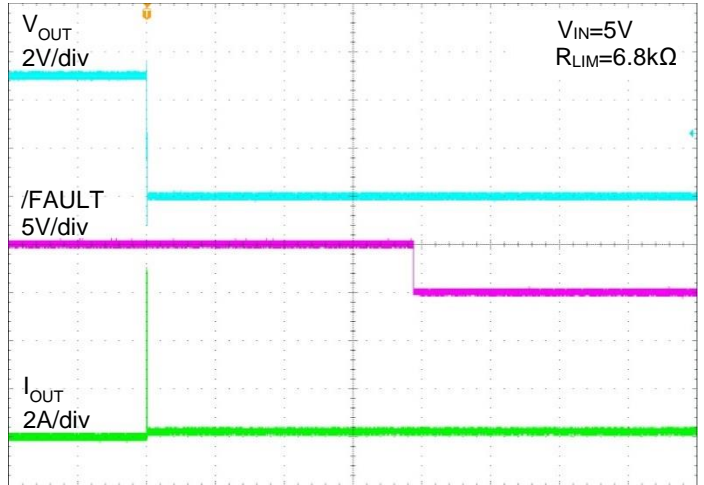
Typical Performance Characteristics (continued)



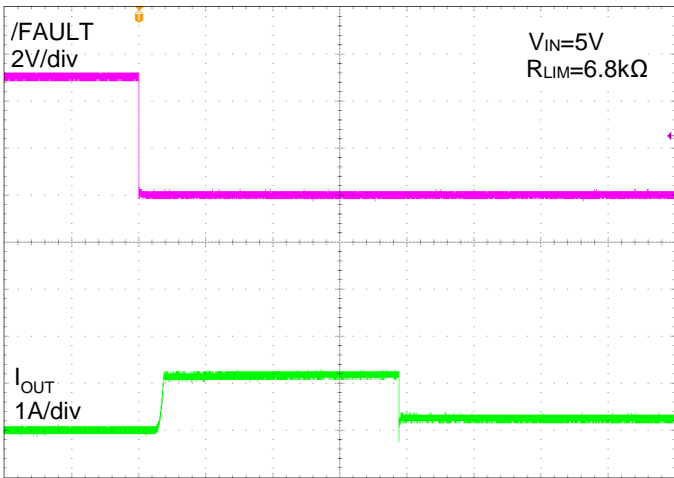
Typical Performance Characteristics (continued)



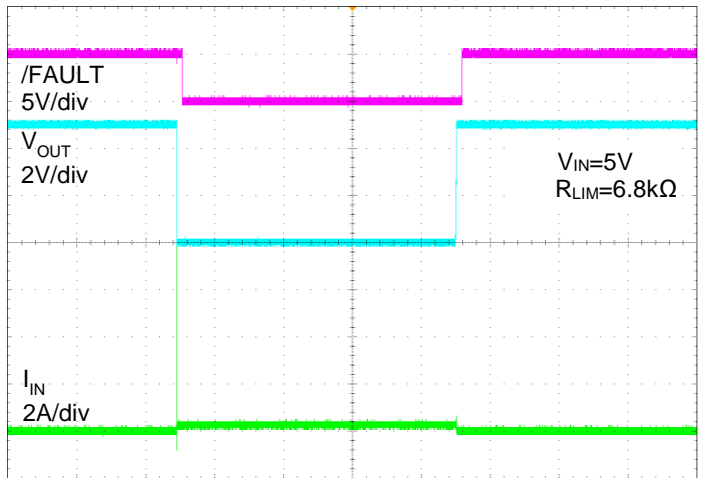
No Load to 1Ω Transient Response



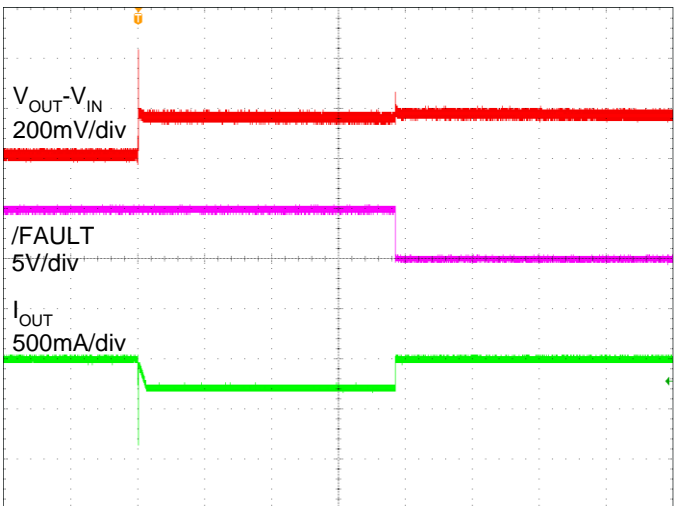
Short-Circuit Current Limit Response



Device Enabled into Short-Circuit



Short-Circuit with Blanking Time and Recovery



Reverse Current Limit Response

Application Information

The AP22654Q and AP22655Q are integrated high-side power switches optimized for Universal Serial Bus (USB) that requires protection functions. The power switches are equipped with a driver that controls the gate voltage and incorporates slew-rate limitation. This, along with the various protection features and special functions, makes these power switches ideal for hot-swap or hot-plug applications.

Protection Features

Undervoltage Lockout (UVLO)

Whenever the input voltage falls below UVLO threshold (to 2.1V), the power switch is turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

Overcurrent and Short-Circuit Protection

An internal sensing FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, AP22654Q and AP22655Q maintain a constant output current and reduce the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

The different overload conditions and the corresponding response of the AP22654Q and AP22655Q are outlined below:

No.	Conditions	Explanation	Behavior of the AP22654Q and AP22655Q
1	Short-circuit condition at startup	Output is shorted before input voltage is applied or before the part is enabled.	The IC senses the short circuit and immediately clamps output current to a certain safe level namely I _{SHORT} .
2	Short-circuit or overcurrent condition	Short-circuit or overload condition that occurs when the part is enabled.	<ul style="list-style-type: none"> At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the overcurrent trip threshold), the device switches into current limiting mode and the current is clamped at I_{SHORT}/I_{LIMIT}.
3	Gradual increase from nominal operating current to I _{LIMIT}	Load increases gradually until the current-limit threshold (I _{TRIG}).	The current rises until I _{LIMIT} or thermal limit. Once the threshold has been reached, the device switches into its current limiting mode and is set at I _{LIMIT} .

Overcurrent FAULT Signal

The FAULT signal will be asserted in response to OCP before the device reaches its current limit. The output current upon FAULT signal triggered will be lower than the I_{limit} value. To implement FAULT signal for precision system protection control, it is recommended to leave enough margin from maximum continuous operating current for each R_{LIM} value condition.

Current-Limit Threshold Programming

The current-limit threshold can be programmed using an external resistor. The current-limit threshold is proportional to the current sourced out of I_{LIM}.

The recommended 1% resistor range for R_{LIM} is 1.91kΩ ≤ R_{LIM} ≤ 16.9kΩ. Figure 2 includes current-limit tolerance due to variations caused by temperature and process. This graph does not include the external resistor tolerance. The traces routing the R_{LIM} resistor to the AP22654Q and AP22655Q should be as short as possible to reduce parasitic effects on the current-limit accuracy.

To design below a maximum current-limit threshold, find the intersection of R_{LIM} and the maximum desired load current on the I_{LIMIT_max} curve and choose a value of R_{LIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to drop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{LIM} and the I_{LIMIT_min} curve.

Best Fit Current-Limit Threshold Equations (I_{LIMIT_typ}):

$$I_{LIM_min}(mA) = 6237.3/[R_{LIM}(k\Omega)]^{1.036}$$

$$I_{LIM_typ}(mA) = 6800/R_{LIM}(k\Omega)$$

$$I_{LIM_max}(mA) = 7393.3/[R_{LIM}(k\Omega)]^{0.974}$$

Application Information (continued)

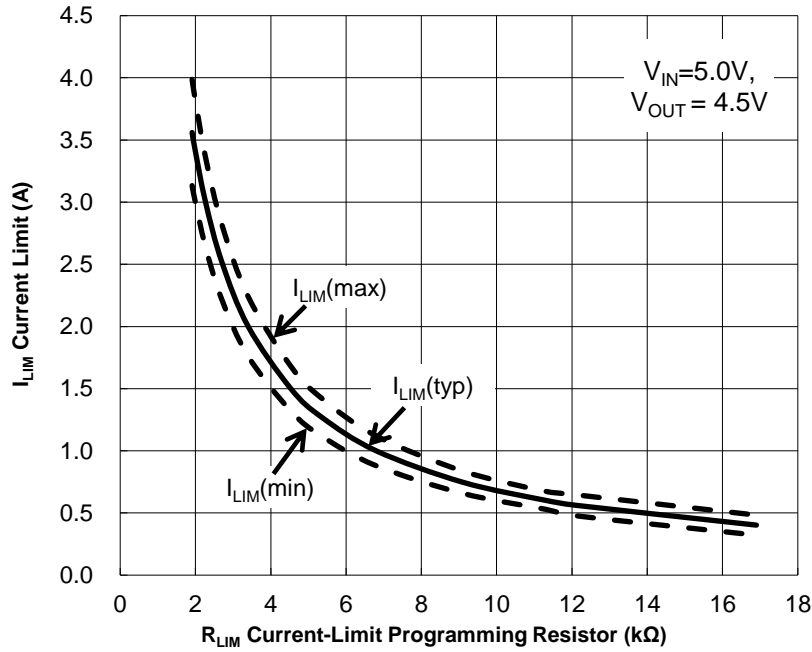


Figure 2. R_{LIMIT} vs. Overload Current Limit

Thermal Protection

Thermal protection prevents the IC from damage when the die temperature exceeds safe margins. This mainly occurs when heavy-overload or short-circuit faults are present for extended periods of time. The AP22654Q and AP22655Q implement a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately +155°C, the thermal protection feature will be activated as follows: The internal thermal sense circuitry turns the power switch off and the FAULT output is asserted, thus preventing the power switch from damage. Hysteresis in the thermal sense circuit allows the device to cool down by approximately +35°C before the output is turned back on. This built-in thermal hysteresis feature is an excellent feature, as it avoids undesirable oscillations of the thermal protection circuit.

Reverse-Current and Reverse-Voltage Protection

The USB specification does not allow an output device to source current back into the USB port. In a normal MOSFET switch, current will flow in reverse direction (from the output side to the input side) when the output side voltage is higher than the input side. A reverse-current limit (**ROCP**) feature is implemented in the AP22654Q and AP22655Q to limit such back currents. The ROCP circuit is activated when the output voltage is higher than the input voltage. After the reverse current circuit has tripped (reached the reverse current trip threshold), the current is clamped at this IROCP level.

In addition to ROCP, reverse overvoltage protection (**ROVP**) is also implemented. The ROVP circuit is activated by the **reverse voltage comparator trip point**; i.e., the difference between the output voltage and the input voltage.

For AP22654Q and AP22655Q, once ROVP is activated, FAULT assertion occurs at a de-glitch time of 7ms. Recovery from ROVP is automatic when the fault is removed. FAULT deassertion de-glitch time is same as the deassertion time.

Application Information (continued)

Special Functions

Discharge Function

When $V_{IN} > V_{OUT}$, and when enable is deasserted or when the input voltage is under UVLO level, the discharge function is active. The output capacitor is discharged through an internal NMOS that has a discharge resistance of 500Ω. Hence, the output voltage drops down to zero. The time taken for discharge is dependent on the RC time constant of the resistance and the output capacitor.

FAULT Response

The FAULT open-drain output goes active low for any of the following faults: overcurrent, OUT pin short-circuit, reverse-voltage condition or thermal shutdown. The time from when a fault condition is encountered to when the FAULT output goes low is 7ms (typ). The FAULT output remains low until overcurrent, OUT pin short-circuit and overtemperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary overcurrent condition, which does not trigger the FAULT due to the 7ms deglitch timeout. This 7ms timeout is also applicable for overcurrent recovery and overtemperature recovery. The AP22654Q and AP22655Q are designed to eliminate erroneous overcurrent reporting without the need for external components, such as an RC delay network.

For the AP22654Q and AP22655Q, when the reverse voltage condition is triggered, FAULT output goes low after 7ms (typ). This 7ms (typ) timeout is also applicable for the recovery from reverse voltage fault.

Power Supply Considerations

A 0.1μF X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. This limits the input voltage drop during line transients. Placing a high-value electrolytic capacitor on the input (10μF minimum) and output pin (120μF) is recommended when the output load is heavy. This precaution also reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the device output with a 0.1μF to 4.7μF ceramic capacitor improves the immunity of the device to short-circuit transients. This capacitor also prevents output from going negative during turn-off due to parasitic inductance.

Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature (T_A) and $R_{DS(ON)}$, the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times \theta_{JA} + T_A$$

Where:

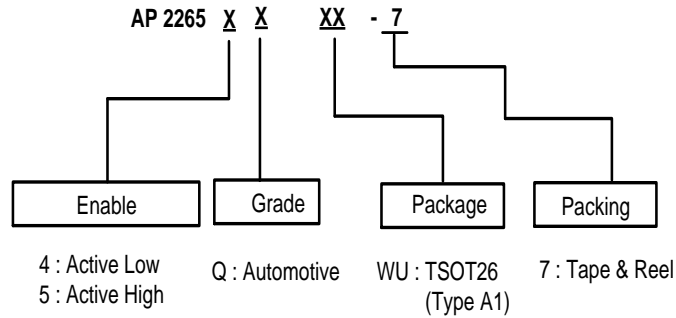
- T_A = Ambient temperature °C
- θ_{JA} = Thermal resistance
- P_D = Total power dissipation

Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or PC boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise and fall times of the AP22654Q and AP22655Q, these devices can be used to provide a softer startup to devices being hot-plugged into a powered system. The UVLO feature of the AP22654Q and AP22655Q also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP22654Q and AP22655Q between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

Ordering Information

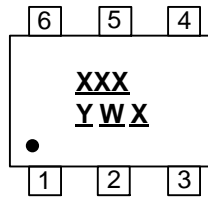


Part Number	Part Number Suffix	Enable Active	Output Fault Condition	Package Code	Package	Packing	
						Qty.	Carrier
AP22654QWU-7	-7	Low	Output Current Limits	WU	TSOT26 (Type A1)	3000	Tape & Reel
AP22655QWU-7	-7	High		WU	TSOT26 (Type A1)	3000	Tape & Reel

Marking Information

TSOT26 (Type A1)

(Top View)



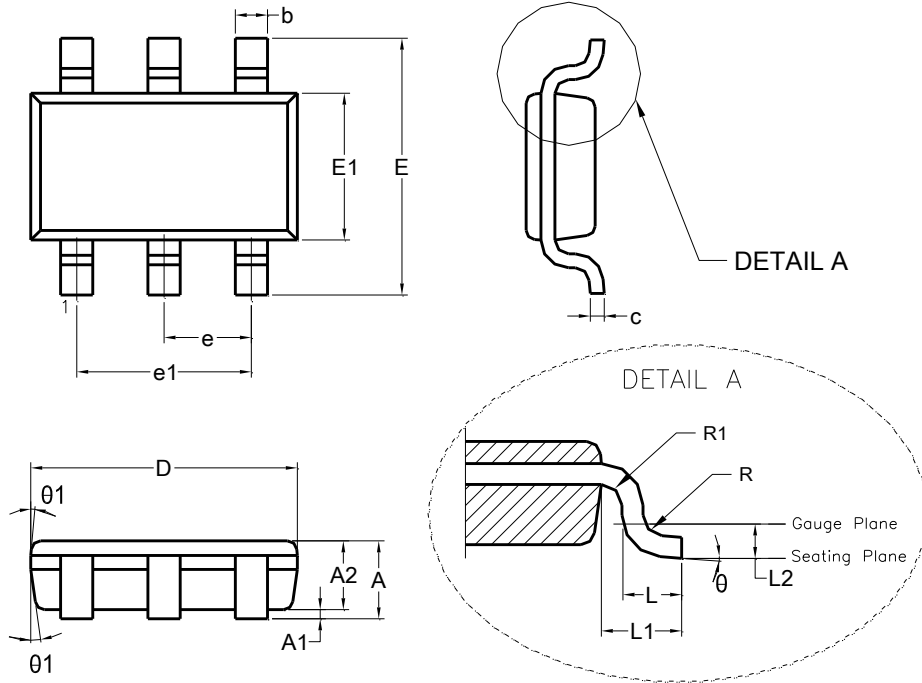
XXX : Identification Code
Y : Year 0 to 9 (ex: 3 = 2023)
W : Week : A to Z : Week 1 to 26;
 a to z : Week 27 to 52; z represents Week 52 and 53
X : Internal Code

Part Number	Package	Identification Code
AP22654QWU-7	TSOT26 (Type A1)	FMQ
AP22655QWU-7	TSOT26 (Type A1)	FNQ

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

TSOT26 (Type A1)

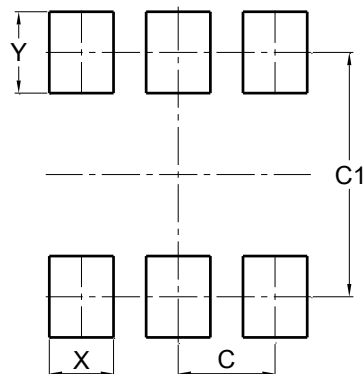


TSOT26 (Type A1)			
Dim	Min	Max	Typ
A	0.700	0.825	--
A1	0.000	0.050	--
A2	0.700	0.775	0.750
b	0.350	0.500	--
c	0.100	0.200	--
D	2.800	3.000	2.900
E	2.600	3.000	2.800
E1	1.500	1.700	1.600
e	0.95 BSC		
e1	1.900 BSC		
L	0.370	0.600	0.450
L1	0.600 REF		
L2	0.250 BSC		
R	0.100	--	--
R1	0.100	0.250	--
theta	0°	8°	4°
theta1	4°	12°	10°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

TSOT26 (Type A1)



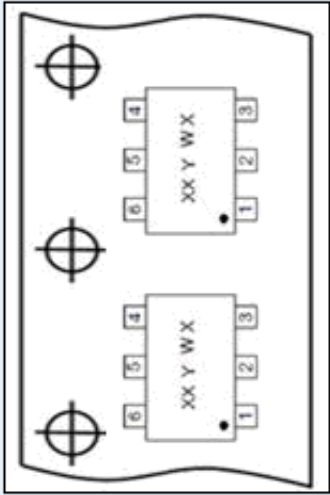
Dimensions	Value (in mm)
C	0.950
C1	2.400
X	0.630
Y	0.800

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.0145 grams (Approximate)

Taping Orientation (Note 10)

Package Type: TSOT26 (Type A1)



Note: 10. The taping orientation of the other package type can be found on our website at <https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf>.

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