AK9723AJ

LED Driver and Sensor AFE for NDIR Gas Sensing

1. General Description

The AK9723AJ is the IR LED driver and Analog Front End (AFE) IC for signal processing of IR photo detector. The AK9723AJ has dual channel AFE and an ADC for digital output, and IR photo detector output signals can be obtained at the same time. The AK9723AJ can communicate with HOST MCU through I^2C bus. The AK9723AJ is suitable for NDIR gas sensing processing using IR LED and IR photo detector.

2. Features

- Integrated LED Driver with Programmable Constant Current Circuit
- Dual Channel Input AFE
- Interrupt Function
- Power Supply Voltage Range: 2.7V to 3.6V
- Small and Thin Package: 16-pin QFN 4.0mm x 4.0mm x t0.7mm

3. Applications

- NDIR gas sensor

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5. Block Diagram and Functions

5.1. Block Diagram

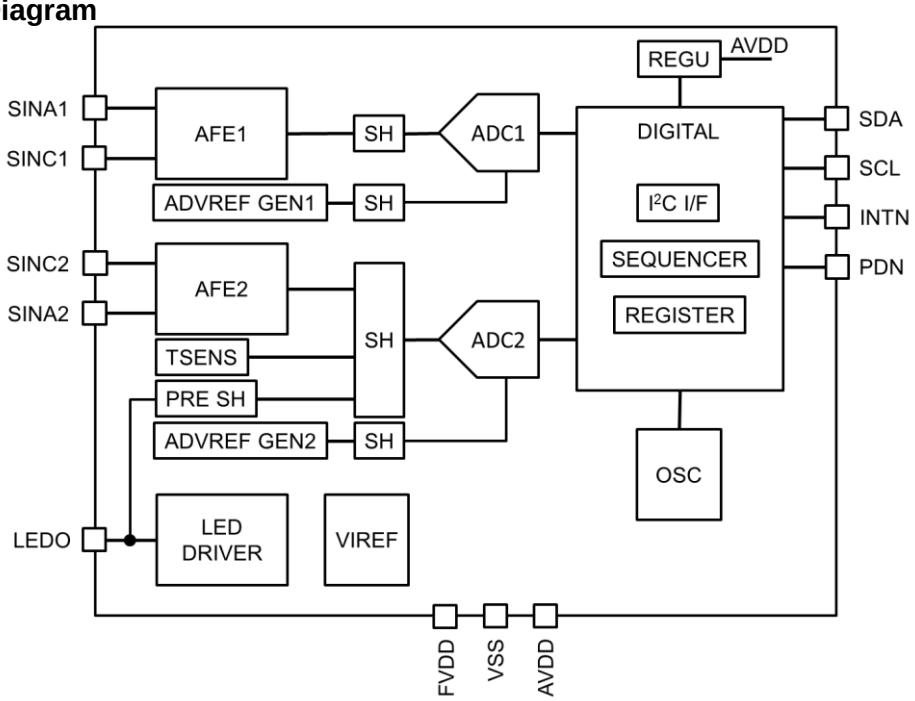


Figure 5.1 Block Diagram

5.2. Functions

Table 5.1 Block Functions

Block	Function
OSC	Oscillator
VIREF	Reference voltage and reference current generator
TSENS	Temperature sensor
AFE1	Convert the IR photo detector output current path1 (IR1 path) to voltage. Cancel the offset of IR photo detector.
AFE2	Convert the IR photo detector output current path2 (IR2 path) to voltage. Cancel the offset of IR photo detector.
ADC1 / 2	Sigma delta 2nd order analog-to-digital converter
LED DRIVER	LED constant current driver
REGU	Generate 1.6V for digital circuit
I^2C I/F	Communicate with MCU by SCL and SDA in I^2C protocol. Support 400kHz fast mode.
SEQUENCER	Control of analog circuit
REGISTER	Register to store the measurement data, operation mode, timing value
ADVREF GEN1 / 2	Reference voltage generator for ADC
SH	Sample and hold circuit
PRE SH	Sample and hold circuit

6. Pin Configurations and Functions

6.1. Pin Configurations

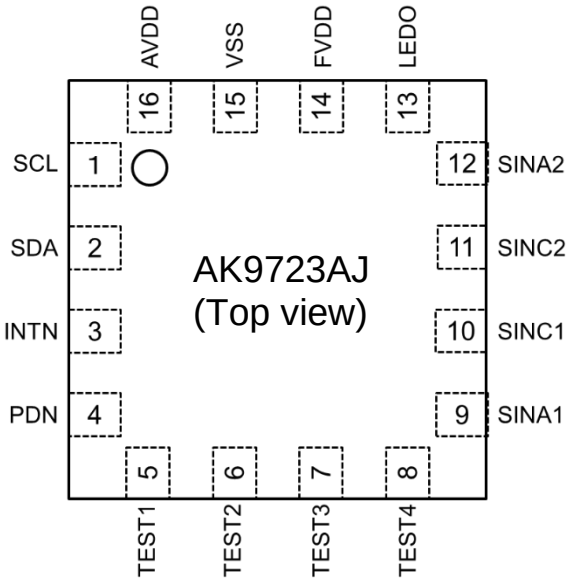


Figure 6.1 Pin Configurations

6.2. Functions

Table 6.1 Pin Functions

Pin No.	Name	I/O	Functions
1	SCL	I	I^2C clock input pin. This pin is open drain pin output (NMOS type).
2	SDA	I/O	I^2C data input/output pin. This pin is open drain pin output (NMOS type).
3	INTN	O	Interrupt pin. INTN pin is active low at the ADC output is ready for read. This pin is open drain output (NMOS type).
4	PDN	I	Power down pin. When PDN pin = “H”, The AK9723AJ can operate.
5	TEST1	I	TEST pin. TEST pin must be connected to VSS
6	TEST2	I	TEST pin. TEST pin must be connected to VSS
7	TEST3	I	TEST pin. TEST pin must be connected to VSS
8	TEST4	I	TEST pin. TEST pin must be connected to VSS
9	SINA1	I	IR photo ditector1 connection pin (anode)
10	SINC1	I	IR photo ditector1 connection pin (cathode)
11	SINC2	I	IR photo ditector2 connection pin (cathode)
12	SINA2	I	IR photo ditector2 connection pin (anode)
13	LEDO	O	LED driver output pin
14	FVDD	-	LED driver power supply pin
15	VSS	-	Ground pin
16	AVDD	-	Power supply pin

7. Absolute Maximum Ratings

Table 7.1 Absolute Maximum Ratings

VSS = 0V

Parameter		Symbol	Min.	Max.	Unit
Power supply	AVDD, FVDD pins	V+	-0.3	4.3	V
Input voltage	All pins	Vin	-0.3	4.3	V
Input current	All pins (Except for power supply)	Iin	-10	10	mA
Storage temperature		Tstg	-40	125	°C

Notes

Operation exceeding the absolute maximum ratings may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

8. Operating Conditions

Table 8.1 Operating Conditions

VSS = 0V

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power supply	AVDD, FVDD pins	V+	2.7	3.0	3.6	V
Operation temperature		Ta	-40	-	85	°C

Notes

Operation outside the recommended operating conditions is not guaranteed.
Power supply and temperature monitor is recommended.

9. Power Supply Conditions

Table 9.1 Power Supply Conditions

Unless otherwise specified, AVDD = FVDD = 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power supply	PDN pin	PSUP	200	-	-	μs

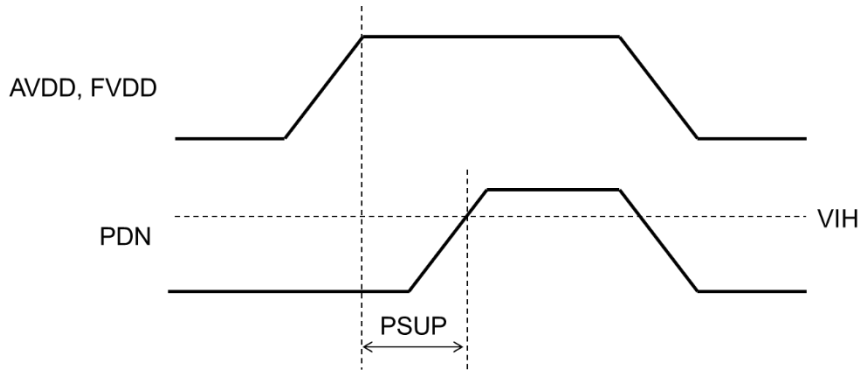


Figure 9.1 Power supply conditions

10. Electrical Characteristics

10.1. Analog Characteristics

Table 10.1 Electrical Characteristics

Unless otherwise specified, AVDD = FVDD= 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter		Symbol	Min.	Typ.	Max.	Unit
IR sensor maximum input current 1	IR1 path IR1_AFE_GAIN [1:0] bits = “01” ITIME [7:0] bits = “00101010”	SIR1	24	30	37	nA
IR sensor maximum input current 2	IR2 path ITIME [7:0] bits = “00101010”	SIR2	2.0	2.5	3.1	μA
IR sensor output noise 1	IR1 path MLOOP [3:0] bits= “0000” IR1_AFE_GAIN [1:0] bits = “00” ITIME [7:0] bits = “00101010” R01 = 33kΩ Ta = 25 ºC	SON1	-	27000	40500	LSB rms
IR sensor output noise 2	IR2 path ITIME [7:0] bits = “00101010” R02 = 33kΩ Ta = 25 ºC	SON2	-	2000	3000	LSB rms
Sensor resistance measurement range 1	IR1 path Sensor resistance measurement mode	SRMR1	675	750	-	kΩ
Sensor resistance measurement range 2	IR2 path Sensor resistance measurement mode	SRMR2	405	450	-	kΩ
LED forward voltage measurement range		VFMR	0.55	-	FVDD-0.5	V
LED terminal voltage range	LEDADJ [4:0] bits= “11000”	LTVR	0.55	-	FVDD-0.5	V
LED current accuracy	LEDADJ [4:0] bits= “11000” LEDO pin = 1.5V Ta = 25 ºC	LCA	97	100	103	mA
LED current step	LEDO pin = 1.5V AVDD, FVDD pins = 2.7V Ta = 25 ºC	LCS	1.5	3.0	4.5	mA
Current consumption	PDN pin = AVDD MODE [1:0] bits = “00”	IDD0	-	0.45	3.0	μA
	PDN pin = AVDD MODE [1:0] bits = “10” MTIME [7:0] bits = “00000000” ITIME [7:0] bits = “01011100” LEDADJ [4:0] bits = “11000”	IDD1	-	560	750	μA

10.1.1. Connection device specification

Table 10.2 Connection device specification

Unless otherwise specified, AVDD = 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter		Symbol	Min.	Typ.	Max.	Unit
Input current 1	IR1 path	ISIN1	1.0	8.5	51.0	nA
Input current 2	IR2 path	ISIN2	0.4	3.0	18.0	μA

10.2. Digital Characteristics

10.2.1. DC Characteristics

Table 10.3 DC Characteristics

Unless otherwise specified, AVDD = 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter			Symbol	Min.	Typ.	Max.	Unit
High level input voltage1		PDN, SCL, SDA pins	VIH	70%AVDD	-	AVDD+0.3	V
Low level input voltage		PDN, SCL, SDA pins	VIL	-	-	30%AVDD	V
Input current	Vin = VSS or AVDD	PDN, SCL, SDA pins	Iin	-10	-	10	μA
Hysteresis voltage (*1)		SCL, SDA pins	VHS	5%AVDD	-	-	V
Low level output voltage	IOL ≤ 3mA	SDA, INTN pins	VOL	-	-	20%AVDD	V

Note

* 1. Reference data only, not tested

10.2.2. AC Characteristics

Table 10.4 AC Characteristics (Standard Mode: fSCL ≤ 100kHz)

Unless otherwise specified, AVDD = 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL	-	-	100	kHz
SCL clock high period	tHIGH	4.0	-	-	µs
SCL clock low period	tLOW	4.7	-	-	µs
SDA and SCL rise time (*2)	tR	-	-	1.0	µs
SDA and SCL fall time (*2)	tF	-	-	0.3	µs
Start condition hold time	tHD:STA	4.0	-	-	µs
Start condition setup time	tSU:STA	4.7	-	-	µs
SDA hold time (vs. SCL falling edge)	tHD:DAT	0	-	-	µs
SDA setup time (vs. SCL rising edge)	tSU:DAT	250	-	-	ns
Stop condition setup time	tSU:STO	4.0	-	-	µs
Bus free time	tBUF	4.7	-	-	µs

Note

*2. Reference data only, not tested

Table 10.5 AC Characteristics (Fast Mode: 100kHz ≤ fSCL ≤ 400kHz)

Unless otherwise specified, AVDD = 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	fSCL	-	-	400	kHz
SCL clock high period	tHIGH	0.6	-	-	µs
SCL clock low period	tLOW	1.3	-	-	µs
SDA and SCL rise time (*3)	tR	-	-	0.3	µs
SDA and SCL fall time (*3)	tF	-	-	0.3	µs
Start condition hold time	tHD:STA	0.6	-	-	µs
Start condition setup time	tSU:STA	0.6	-	-	µs
SDA hold time (vs. SCL falling edge)	tHD:DAT	0	-	-	µs
SDA setup time (vs. SCL rising edge)	tSU:DAT	100	-	-	ns
Stop condition setup time	tSU:STO	0.6	-	-	µs
Bus free time	tBUF	1.3	-	-	µs
Noise suppression pulse width	tSP	-	-	50	ns

Note

*3. Reference data only, not tested.

[I²C bus interface timing]

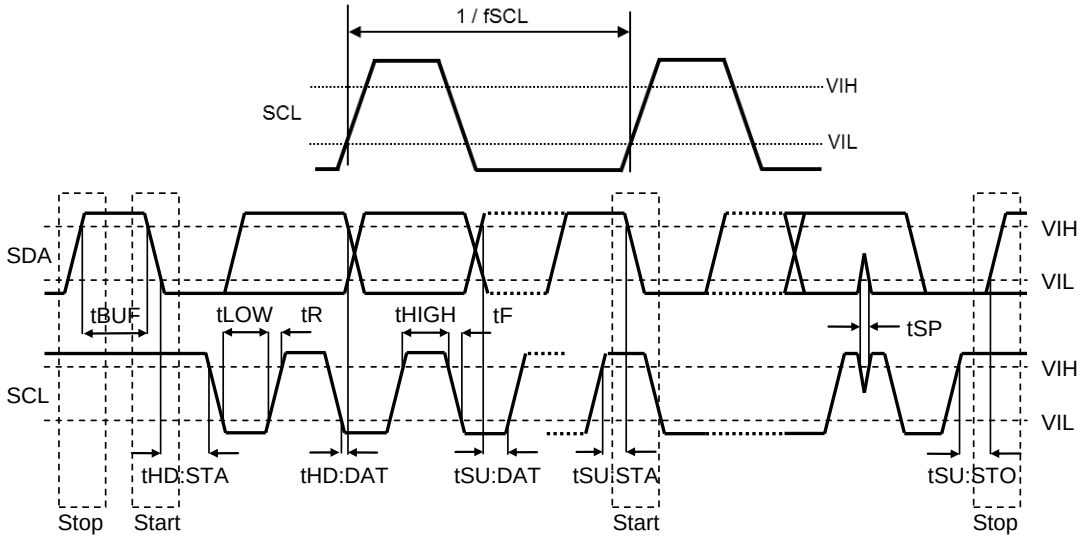


Figure 10.1 Bus Timing

Table 10.6 AC Characteristics of the INTN pin
Unless otherwise specified, AVDD = 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter		Symbol	Min.	Typ.	Max.	Unit
Rise time (*4)	INTN pin RL = 24kΩ CL = 50pF	tRINTN	-	-	2.0	μs
Fall time (*4)		tFINTN	-	-	0.25	μs

Note
*4. Reference data only, not tested

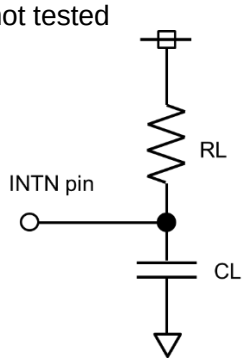


Figure 10.2 INTN load circuit

Table 10.7 AC Characteristics of the PDN pin
Unless otherwise specified, AVDD = 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter		Symbol	Min.	Typ.	Max.	Unit
PDN pulse width	PDN pin	TPDN	1	-	-	μs
Command input disable time		TCIE	10	-	-	μs

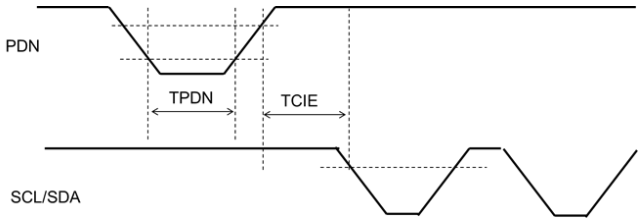


Figure 10.3 TPDN and TCIE condition

Table 10.8 Measurement interval condition
Unless otherwise specified, AVDD = 2.7 ~ 3.6V, Ta = -40 ~ 85ºC

Parameter		Symbol	Min.	Typ.	Max.	Unit
Measurement interval		TMI	1.5	-	-	ms

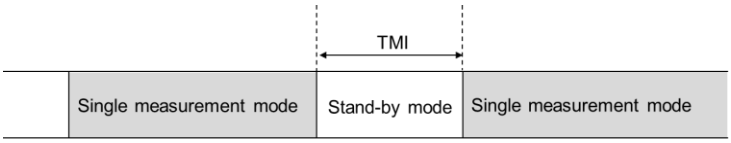


Figure 10.4 Measurement interval condition

11. Functional Descriptions

11.1. Power Supply States

Table 11.1 Power Supply States and Functions

State	AVDD pin, FVDD pin	PDN pin	I²C	Analog Circuit
1	OFF(0V)	"L"	Disable	Power Down
2	2.7 ~ 3.6V	"L"	Disable	Power Down
3	2.7 ~ 3.6V	"H"	Enable	Only the regulator circuit operates

11.2. Reset Functions

The AK9723AJ has two reset functions.

(1) Hardware reset
The AK9723AJ is reset by PDN pin = VSS.

(2) Soft reset
The AK9723AJ is reset by setting SRST bit.

When the AK9723AJ is reset, all registers are set to initial values.

11.3. Operating Mode

The AK9723AJ has following three operation modes.

(1) Power Down Mode
(2) Stand-by Mode
(3) Single Measurement Mode

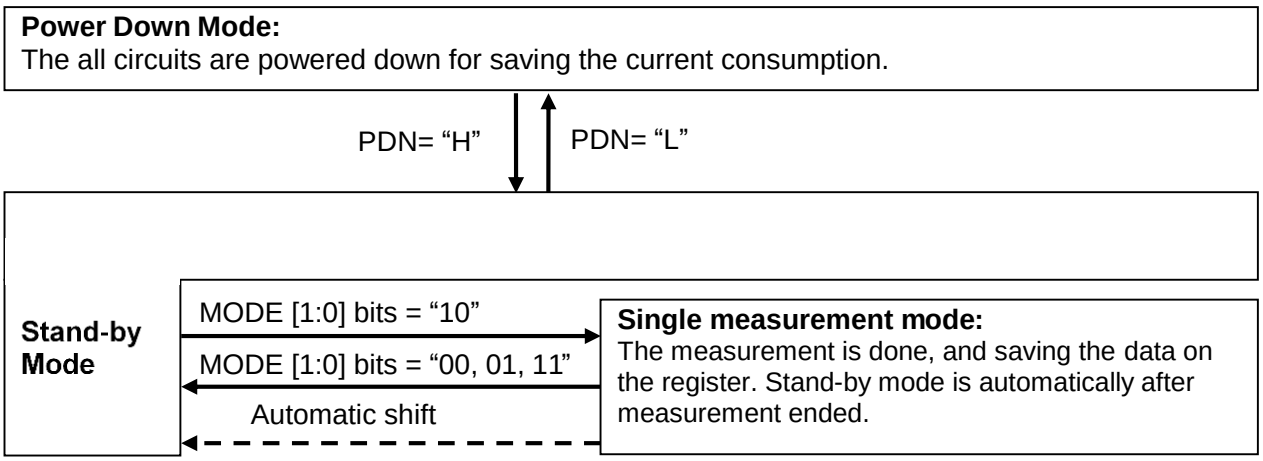


Figure 11.1 Operating Mode

11.4. Descriptions for Each Operating Mode

11.4.1. Power Down Mode

All circuits are powered off. The all functions of the AK9723AJ does not work in this mode.

11.4.2. Stand-by Mode (MODE [1:0] bits = “00”)

Power to the circuits except for the regulator is off. All registers can be accessed in this mode. Read / write register data are retained, and reset by software reset.

11.4.3. Single Measurement Mode (MODE [1:0] bits = “10”)

When the AK9723AJ is set to single measurement mode (MODE [1:0] bits = “10”), measurement is done once, and the measurement data is stored to the measurement data registers (IR1L to VFH). After completing measurement, The AK9723AJ outputs “Low” from INTN pin and goes to stand-by mode (MODE [1:0] bits = “00”) automatically.

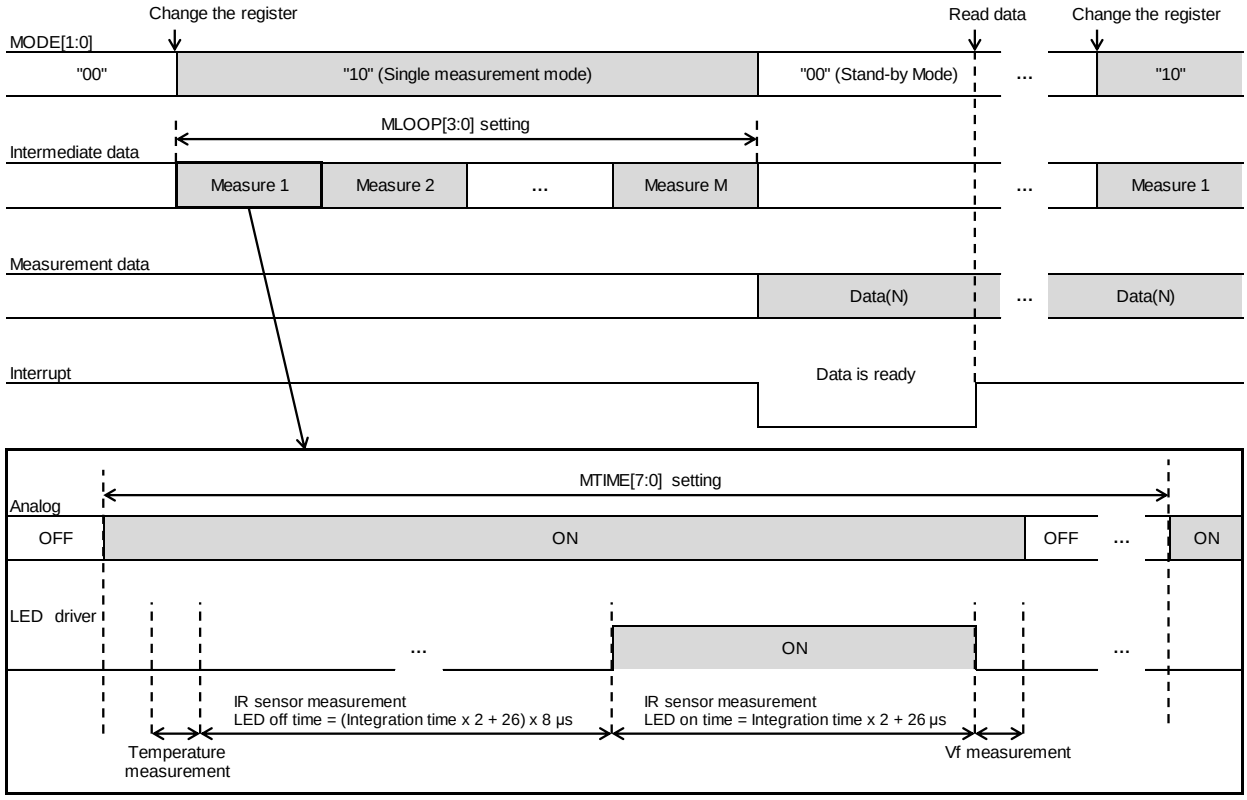


Figure 11.2 Single Measurement Mode

11.5. Read Measurement Data

After measurement data is set to internal buffer and ready to read, “DRDY” bit in ST1 register is set to “1”. This state is called “Data Ready”. When the DRDY bit is "1", the output of the INTN pin becomes "L". When the ST1 read is complete, the DRDY bit is set to "0" and INTN pin output becomes "H".

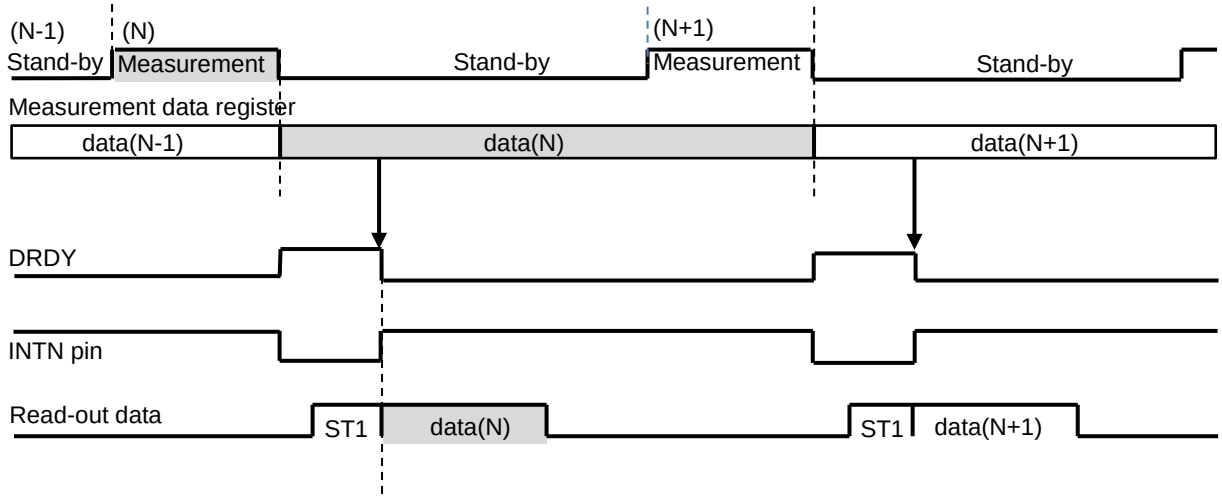


Figure 11.3 Read-out Procedure

The AK9723AJ recommends monitoring the INTN pin.

When you do not use the INTN pin, please note the following points.
If the measurement is completed while reading ST1, the DRDY bit may not be updated properly.
Therefore, secure 10% or more margin for the set measurement time and execute DRDY bit read.

11.5.1. Recommended Measurement Procedure

Recommended measurement procedure of AK9723AJ is shown below.

(1) Setting before measurement
Confirm INTN pin = “H” and write the data to the following registers.
- Soft Reset: Write FFh to register address 18h
- Measurement number of intermediate data setting
- Measurement time of intermediate data setting
- Integration time
- LED current adjustment setting
- Test mode: Write 00h to register address 17h

(2) Start measure
Measurement is executed by writing 02h to the Measurement mode setting register.

(3) Read measurement data
INTN pin output turns to “L” (Active) after completion of data ready.
Read measurement data in the following order.
- Status 1
- Measurement data of IR sensor
- Measurement data of temperature sensor
- Measurement data of LED forward voltage

INTN pin turns to “H” when reading the Status 1 register.

(4) Wait 1.5ms or more

For measurement again, execute from (1).

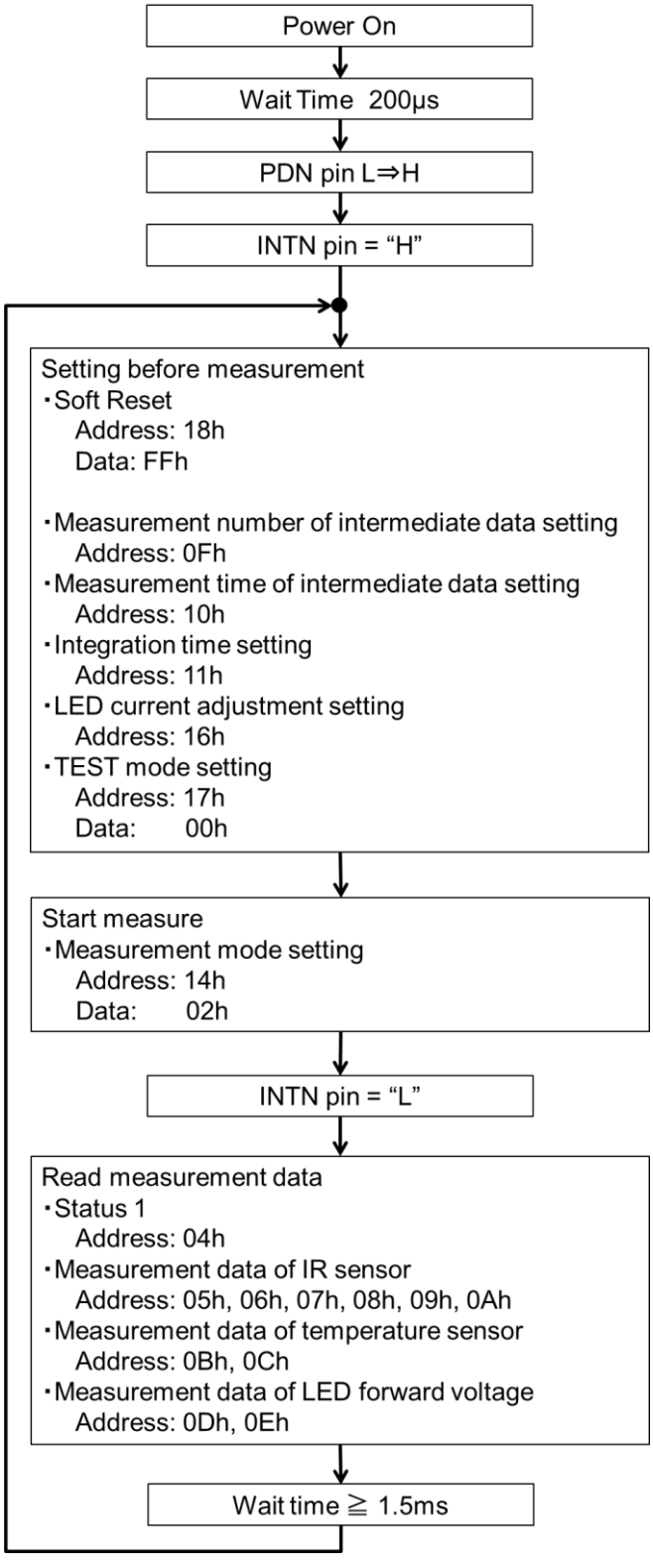


Figure 11.4 Recommended Measurement Procedure

12. Serial Interface

The I²C bus interface of the AK9723AJ supports standard mode (Max, 100kHz) and high-speed mode (Max. 400kHz).

12.1. Data Transfer

Initially the start condition should be input to access the AK9723AJ through the bus. Next, send a one byte slave address, which includes the device address. The AK9723AJ compares the slave address, and if these addresses match, the AK9723AJ generates an acknowledge signal and executes a read / write command. The stop condition should be input after executing a command.

12.1.1. Changing state of the SDA line

The SDA line state should be changed only while the SCL line is “L”. The SDA line state must be maintained while the SCL line is “H”. The SDA line state can be changed while the SCL line is “H”, only when a start condition or a stop condition is input.

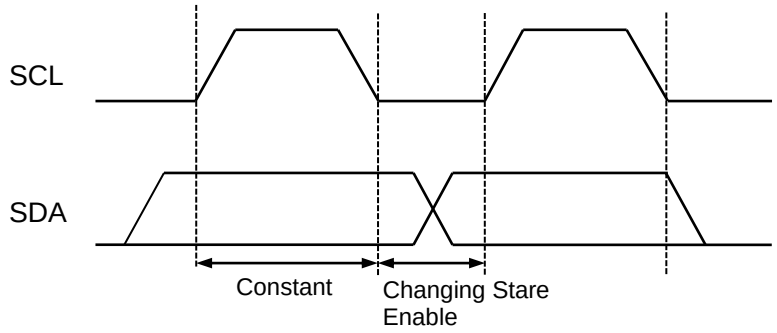


Figure 12.1 Changing State of SDA Line

12.1.2. Start / Stop Conditions

A start condition is generated when the SDA line state is changed from “H” to “L” while the SCL line is “H”. All commands start from a start condition.
A stop condition is generated when the SDA line state is changed from “L” to “H” while the SCL line is “H”. All commands end after a stop condition.

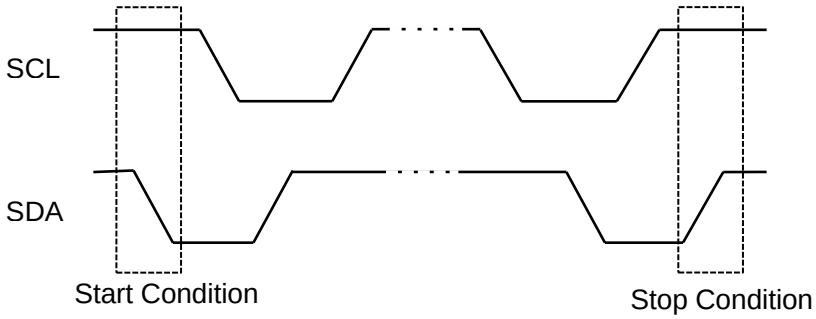


Figure 12.2 Start / Stop Conditions

12.1.3. Acknowledge

The device transmitting data will release the SDA line after transmitting one byte of data (SDA line state is “H”). The device receiving data will pull the SDA line to “L” during the next clock. This operation is called “Acknowledge”. The acknowledge signal can be used to indicate successful data transfers.

The AK9723AJ will output an acknowledge signal after receiving a start condition and slave address.

The AK9723AJ will output an acknowledge signal after receiving each byte, when the write instruction is transmitted.

The AK9723AJ will transmit the data stored in the selected address after outputting an acknowledge signal, when read instruction is transmitted. Then the AK9723AJ will monitor the SDA line after releasing the SDA line. If the master device generates an acknowledge instead of stop condition, the AK9723AJ transmits an 8-bit data stored in the next address. When the acknowledge is not generated, transmitting data is terminated.

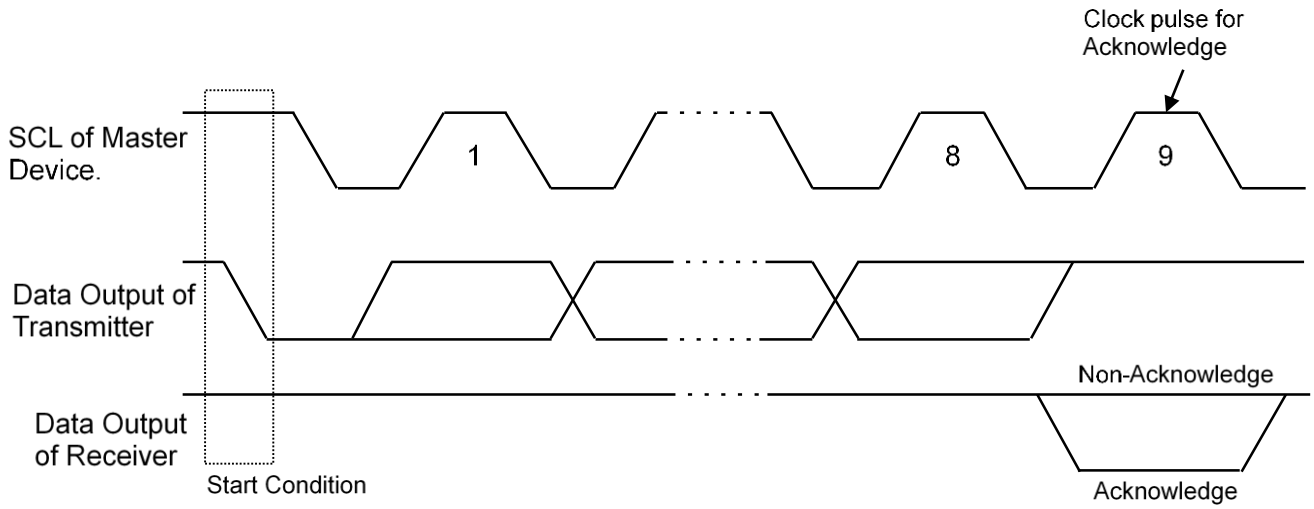


Figure 12.3 Acknowledge

12.1.4. Slave Address

The slave address of the AK9723AJ is 65h.

MSB							LSB
1	1	0	0	1	0	1	R/W

Figure 12.4 Slave Address

When the first one byte data including the slave address is transmitted after a start condition, the device, which is specified as the communicator by the slave address on bus, selected.

After transmitting the slave address, the device that has the corresponding device address will execute a command after transmitting an acknowledge signal. The 8-bit (Least Significant bit-LSB) of the first one byte is the R/W bit.

When the R/W bit is set to “1”, a read command is executed. When the R/W bit is set to “0”, a write command is executed.

12.1.5. Write Command

When the R/W bit set to “0”, the AK9723AJ executes a write operation. The AK9723AJ will out an acknowledge signal and receive the second byte, after receiving a start condition and first one byte (slave address) in a write operation. The second byte has an MSB-first configuration, and specifies the address of the internal control register.

MSB							LSB
A7	A6	A5	A4	A3	A2	A1	A0

Figure 12.5 Register Address

The AK9723AJ will generate an acknowledge and receive the third byte after receiving the second byte (register address).

The data after the third byte is the control data. The control data consists of 8-bit and has an MSB-first configuration. The AK9723AJ generates an acknowledge for each byte received. The data transfer is terminated by a stop condition, generated by the master device.

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Figure 12.6 Control Data

Two or more bytes can be written at once. The AK9723AJ generates an acknowledge and receives the next data after receiving the third byte (control data). When the following data is transmitted without a stop condition, after transmitting one byte, the internal address counter is automatically incremented, and data is written in the next address.

The automatic increment function works in the address from 0Fh to 17h. When the start address is “0Fh”, the address is repeatedly incremented as. “0Fh -> 10h -> … -> 17h -> 0Fh -> 10h…”

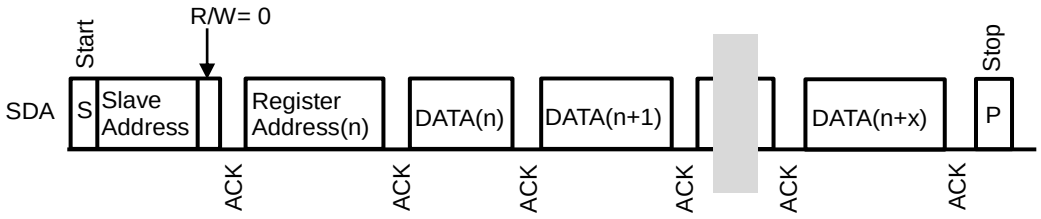


Figure 12.7 Write Operation

12.1.6. Read Command

When the R/W bit is set to “1”, the AK9723AJ executes a read operation. When the AK9723AJ transmits data from the specified address, the master device generates an acknowledge instead of a stop condition and the next address data can be read-out.
Address can be 00h to 0Eh, 0Fh to 17h. When the address is 00h to 0Eh, the address is incremented 00h -> 01h -> … -> 0Eh, and the address goes back to 04h after 0Eh. When the address is 0Fh to17h, the address goes back to 0Fh after 17h.
The AK9723AJ supports both current address read and random address read.

(1) Current Address Read

The AK9723AJ has an integrated address counter. The data specified by the counter is read-out in the current address read operation. The internal address counter retains the next address which is accessed at last. For example, when the address which was accessed last is “n”, the data of address “n+1” is read-out by the current address read instruction.
The AK9723AJ generates an acknowledge after receiving a read instruction (R/W bit = “1”). Then the AK9723AJ will start to transmit the data specified by the internal address counter at the next clock, and will increment the internal address counter by one. The read operation terminates when the master device generates a stop condition instead of an acknowledge after the AK9723AJ transmits one byte data.

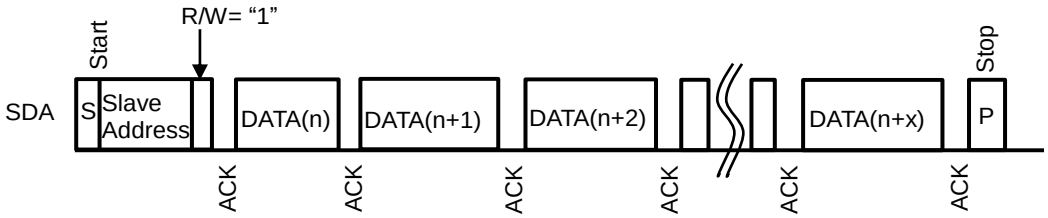


Figure 12.8 Current Address Read

(2) Random Read

Data from an arbitrary address can be read-out by a random read operation. A random read requires the input of a dummy write instruction before the input of a slave address of a read instruction (R/W bit = “1”).
To execute random read, the master device generates a start condition, and then the slave address (R/W bit = “0”) of the write instruction and the read address are sequentially input. The AK9723AJ generates an acknowledge after receiving the write instruction. After that, the master device input a start condition and a slave address of the read instruction (R/W bit = “1”). The AK9723AJ generates an acknowledge in response to the input of this slave address. Next, the AK9723AJ outputs the data at the specified address, then increments the internal address counter by one. The read operation terminates when the master device generates a stop condition instead of an acknowledge after the AK9723AJ transmits the data.

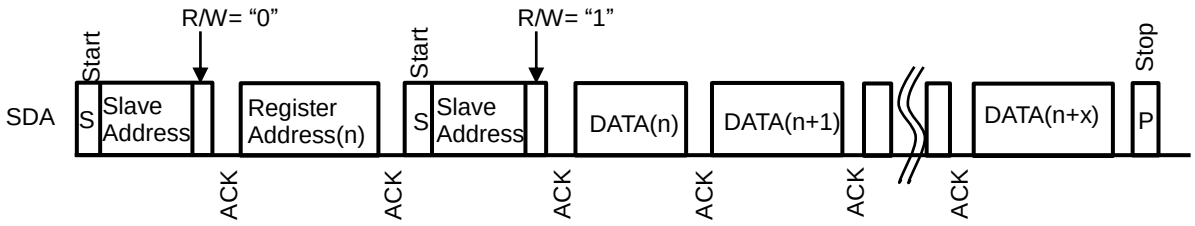


Figure 12.9 Random Read

13. Registers

13.1. Description of Registers

The AK9723AJ has registers of 25 addresses as indicated in Table 13.1 Every address consists of 8-bit data. Data is transferred to or received from the external MCU via the serial interface described previously.

Table 13.1 Register Table

Name	Address	SRST	R/W	Data	
				Content	bit
WIA1	00h	Disable	R	Company Code	8
WIA2	01h	Disable	R	Device ID	8
INFO1	02h	Disable	R	Information	8
INFO2	03h	Disable	R	Information	8
ST1	04h	Enable	R	Status 1	3
IR1L	05h	Enable	R	Measurement data of IR1 (Low)	8
IR1M	06h	Enable	R	Measurement data of IR1 (Middle)	8
IR1H	07h	Enable	R	Measurement data of IR1 (High)	8
IR2L	08h	Enable	R	Measurement data of IR2 (Low)	8
IR2M	09h	Enable	R	Measurement data of IR2 (Middle)	8
IR2H	0Ah	Enable	R	Measurement data of IR2 (High)	8
TMPL	0Bh	Enable	R	Measurement data of temperature sensor(Low)	8
TMPH	0Ch	Enable	R	Measurement data of temperature sensor(High)	8
VFL	0Dh	Enable	R	Measurement data of LED forward voltage(Low)	8
VFH	0Eh	Enable	R	Measurement data of LED forward voltage (High)	8
CNTL1	0Fh	Enable	R/W	Measurement number of intermediate data	4
CNTL2	10h	Enable	R/W	Measurement time of intermediate data	8
CNTL3	11h	Enable	R/W	Integration time	8
CNTL4	12h	Enable	R/W	IR2 integrated time setting	8
CNTL5	13h	Enable	R/W	INTN pin output setting	2
CNTL6	14h	Enable	R/W	Mode setting	2
CNTL7	15h	Enable	R/W	Detection range switching	7
CNTL8	16h	Enable	R/W	LED current setting	5
CNTL9	17h	Enable	R/W	Resistance measurement mode setting	1
CNTL10	18h	Enable	R/W	Soft reset	1

Addresses 00h to 0Eh, 0Fh to 17h are compliant with automatic increment function of serial interface respectively. When the address is in 00h to 0Eh, the address is incremented 00h -> 01h -> 02h -> … -> 0Eh, and the address goes back to 04h after 0Eh. When the address is in 0Fh to 17h, the address goes back to 0Fh after 17h.

13.2. Register Map

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	WIA1	0	1	0	0	1	0	0	0
01h	WIA2	0	0	1	0	0	0	1	1
02h	INFO1	0	0	0	0	0	0	0	0
03h	INFO2	0	0	0	0	0	0	0	0
04h	ST1	1	1	1	1	1	OVCUR_DET	ERR_FLAG	DRDY
05h	IR1L	IR1L_7	IR1L_6	IR1L_5	IR1L_4	IR1L_3	IR1L_2	IR1L_1	IR1L_0
06h	IR1M	IR1M_15	IR1M_14	IR1M_13	IR1M_12	IR1M_11	IR1M_10	IR1M_9	IR1M_8
07h	IR1H	IR1H_23	IR1H_22	IR1H_21	IR1H_20	IR1H_19	IR1H_18	IR1H_17	IR1H_16
08h	IR2L	IR2L_7	IR2L_6	IR2L_5	IR2L_4	IR2L_3	IR2L_2	IR2L_1	IR2L_0
09h	IR2M	IR2M_15	IR2M_14	IR2M_13	IR2M_12	IR2M_11	IR2M_10	IR2M_9	IR2M_8
0Ah	IR2H	IR2H_23	IR2H_22	IR2H_21	IR2H_20	IR2H_19	IR2H_18	IR2H_17	IR2H_16
0Bh	TMPL	TMPL_7	TMPL_6	TMPL_5	TMPL_4	TMPL_3	TMPL_2	TMPL_1	TMPL_0
0Ch	TMPH	TMPH_15	TMPH_14	TMPH_13	TMPH_12	TMPH_11	TMPH_10	TMPH_9	TMPH_8
0Dh	VFL	VFL_7	VFL_6	VFL_5	VFL_4	VFL_3	VFL_2	VFL_1	VFL_0
0Eh	VFH	VFH_15	VFH_14	VFH_13	VFH_12	VFH_11	VFH_10	VFH_9	VFH_8
0Fh	CNTL1	1	1	1	1	MLOOP_3	MLOOP_2	MLOOP_1	MLOOP_0
10h	CNTL2	MTIME_7	MTIME_6	MTIME_5	MTIME_4	MTIME_3	MTIME_2	MTIME_1	MTIME_0
11h	CNTL3	ITIME_7	ITIME_6	ITIME_5	ITIME_4	ITIME_3	ITIME_2	ITIME_1	ITIME_0
12h	CNTL4	IR2INT_7	IR2INT_6	IR2INT_5	IR2INT_4	IR2INT_3	IR2INT_2	IR2INT_1	IR2INT_0
13h	CNTL5	1	1	1	1	1	1	ERR_DIS	DRDY_DIS
14h	CNTL6	1	1	1	1	1	1	MODE_1	MODE_0
15h	CNTL7	1	IR2_MSRIUP	IR1_MSRIUP	IR2_SH_GAIN	IR1_ADC_RNG	IR1_SH_GAIN	IR1_AFE_GAIN_1	IR1_AFE_GAIN_0
16h	CNTL8	1	1	1	LEDADJ_4	LEDADJ_3	LEDADJ_2	LEDADJ_1	LEDADJ_0
17h	CNTL9	1	1	1	1	1	1	1	TST
18h	CNTL10	1	1	1	1	1	1	1	SRST

The ERR_FLAG bit is reset in the single measurement mode setting.
At this time, the DRDY bit is not reset.

The DRDY bit is reset by reading the ST1 register.
At this time, the ERR_FLAG bit is not reset.

13.3. Detailed Description of Register

13.3.1. WIA1: Company code

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	WIA1	0	1	0	0	1	0	0	0

1 Byte fixed code as Company code of AKM.

13.3.2. WIA2: Device ID

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
01h	WIA2	0	0	1	0	0	0	1	1

1 Byte fixed code as AKM device ID.

13.3.3. INFO1, INFO2: Information

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
02h	INFO1	0	0	0	0	0	0	0	0
03h	INFO2	0	0	0	0	0	0	0	0

INFO1 [7:0]: Reserved register for AKM.
INFO2 [7:0]: Reserved register for AKM.

13.3.4. ST1: Status 1

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
04h	ST1						OVCUR_DET	ERR_FLAG	DRDY
Reset		1	1	1	1	1	0	0	0

OVCUR_DET: Error flag
“0”: Normal state
“1”: Error state

Error flag is set when LED overcurrent is detected.

ERR_FLAG: Error flag
“0”: Normal state
“1”: Error state

The ERR_FLAG bit is "1" when register setting satisfies the following conditions.

Error judgment condition: (Integration time) x 18 > (Measurement time)

DRDY: Data ready
“0”: Normal state
“1”: Data ready

When data can be read, the DRDY bit becomes “1”. This bit returns to “0” when reading of ST1 register is completed.

13.3.5. IRxL, IRxM, IRxH: Measurement data of IR sensor (x=1,2)

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
05h	IR1L	IR1L_7	IR1L_6	IR1L_5	IR1L_4	IR1L_3	IR1L_2	IR1L_1	IR1L_0
06h	IR1M	IR1M_15	IR1M_14	IR1M_13	IR1M_12	IR1M_11	IR1M_10	IR1M_9	IR1M_8
07h	IR1H	IR1H_23	IR1H_22	IR1H_21	IR1H_20	IR1H_19	IR1H_18	IR1H_17	IR1H_16
08h	IR2L	IR2L_7	IR2L_6	IR2L_5	IR2L_4	IR2L_3	IR2L_2	IR2L_1	IR2L_0
09h	IR2M	IR2M_15	IR2M_14	IR2M_13	IR2M_12	IR2M_11	IR2M_10	IR2M_9	IR2M_8
0Ah	IR2H	IR2H_23	IR2H_22	IR2H_21	IR2H_20	IR2H_19	IR2H_18	IR2H_17	IR2H_16
Reset		0	0	0	0	0	0	0	0

Measurement data of IR sensor
IR1L [7:0]: IR1 measurement data lower 8-bit
IR1M [15:8]: IR1 measurement data middle 8-bit
IR1H [23:16]: IR1 measurement data upper 8-bit
IR2L [7:0]: IR2 measurement data lower 8-bit
IR2M [15:8]: IR2 measurement data middle 8-bit
IR2H [23:16]: IR2 measurement data upper 8-bit

24-bit data is stored in two's complement and little endian format.

Table 13.1 Measurement data of IR sensor

IRx [23:0] (x=1,2)		IR Sensor output [mV]
Hex	Decimal	
7FFFFF	8388607	750
⋮	⋮	⋮
555555	5592405	500
⋮	⋮	⋮
111111	1118481	100
⋮	⋮	⋮
000001	1	8.94×10^{-5}
000000	0	0
FFFFFF	-1	-8.94×10^{-5}
⋮	⋮	⋮
EEEEEF	-1118481	-100
⋮	⋮	⋮
AAAAAB	-5592405	-500
⋮	⋮	⋮
800001	-8388607	-750

13.3.6. TMPL, TMPH: Measurement data of temperature sensor

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0Bh	TMPL	TMPL_7	TMPL_6	TMPL_5	TMPL_4	TMPL_3	TMPL_2	TMPL_1	TMPL_0
0Ch	TMPH	TMPH_15	TMPH_14	TMPH_13	TMPH_12	TMPH_11	TMPH_10	TMPH_9	TMPH_8
Reset		0	0	0	0	0	0	0	0

Measurement data of temperature sensor
TMPL [7:0]: Temperature data lower 8-bit
TMPH [15:8]: Temperature data upper 8-bit

16-bit data is stored in two's complement and little endian format.
By two-point calibration, it is possible to can accurately detect the temperature of -40 ºC to 85 ºC. For details, refer to the application note "Calibrating the Temperature sensor".

13.3.7. Vf: Measurement data of LED forward voltage

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0Dh	VFL	VFL_7	VFL_6	VFL_5	VFL_4	VFL_3	VFL_2	VFL_1	VFL_0
0Eh	VFH	VFH_15	VFH_14	VFH_13	VFH_12	VFH_11	VFH_10	VFH_9	VFH_8
Reset		0	0	0	0	0	0	0	0

Measurement data of LED forward voltage
VFL [7:0]: Vf data lower 8-bit
VFH [15:8]: Vf data upper 8-bit

16-bit data is stored in two's complement and little endian format.

Table 13.3 Measurement data of LED forward voltage

Vf [15:0]		LED forward voltage [mV]
Hex	Decimal	
7FFF	32767	2900
⋮	⋮	⋮
4444	17476	2200
⋮	⋮	⋮
2222	8738	1800
⋮	⋮	⋮
0001	1	1400.05
0000	0	1400
FFFF	-1	1399.95
⋮	⋮	⋮
DDDE	-8738	1000
⋮	⋮	⋮
BBBC	-17476	600
⋮	⋮	⋮
8001	-32767	-100

13.3.8. CNTL1: Control1

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
0Fh	CNTL1					MLOOP_3	MLOOP_2	MLOOP_1	MLOOP_0
Reset		1	1	1	1	0	0	0	0

MLOOP [3:0]: Measurement number of intermediate data setting

Table 13.4 Measurement number of intermediate data

MLOOP [3:0]		Number of measurements [times]
Hex	Decimal	
A, B, C, D, E, F	10,11,12,13,14,15	1024
9	9	512
8	8	256
⋮	⋮	⋮
3	3	8
2	2	4
1	1	2
0	0	1

13.3.9. CNTL2: Control2

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
10h	CNTL2	MTIME_7	MTIME_6	MTIME_5	MTIME_4	MTIME_3	MTIME_2	MTIME_1	MTIME_0
Reset		0	0	0	0	0	0	0	0

MTIME [7:0]: Measurement time of intermediate data setting

Table 13.5 Measurement time of intermediate data

MTIME [7:0]		Measurement time [ms]
Hex	Decimal	
FF	255	515
⋮	⋮	⋮
51	81	167
⋮	⋮	⋮
03	3	11
02	2	9
01	1	7
00	0	5

13.3.10. CNTL3: Control3

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
11h	CNTL3	ITIME_7	ITIME_6	ITIME_5	ITIME_4	ITIME_3	ITIME_2	ITIME_1	ITIME_0
Reset		0	0	0	0	0	0	0	0

ITIME [7:0]: Integration time setting

The light emission time of the LED can be obtained by the following formula.
LED light emission time = Integration time x 2 + 26 [μs]

Table 13.6 Integration time

ITIME [7:0]		Integration time [μs]
Hex	Decimal	
FF	255	520.9
⋮	⋮	⋮
2A	42	100.0
29	41	98.0
28	40	96.1
⋮	⋮	⋮
02	2	21.0
01	1	19.0
00	0	17.0

13.3.11. CNTL4: Control4

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
12h	CNTL4	IR2INT_7	IR2INT_6	IR2INT_5	IR2INT_4	IR2INT_3	IR2INT_2	IR2INT_1	IR2INT_0
Reset		0	0	0	0	0	0	0	0

IR2INT [7:0]: Integration time adjustment of IR2

Since the input ranges of IR1 and IR2 are different, the integration time of IR2 can be adjusted to match the measurement range of IR1.
The integration time of IR2 is shown below.

IR2 integration time = Integration time – IR2 mask time [μs]

Table 13.7 Integration time adjustment

IR2INT [7:0]		IR2mask time [μs]
Hex	Decimal	
FF	255	503.9
⋮	⋮	⋮
82	130	256.9
⋮	⋮	⋮
03	3	5.9
02	2	4.0
01	1	2.0
00	0	0

13.3.12. CNTL5: Control5

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
13h	CNTL5							ERR_DIS	DRDY_DIS
Reset		1	1	1	1	1	1	0	0

DRDY_DIS: DRDY interrupt setting
“0”: Enable
“1”: Disenable

ERR_DIS: Error flag interrupt setting
“0”: Enable
“1”: Disenable

If you do not want to interrupt the HOST from the INTN pin, set the above bit to "1".

13.3.13. CNTL6: Control6

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
14h	CNTL6							MODE_1	MODE_0
Reset		1	1	1	1	1	1	0	0

MODE [1:0]: Measurement mode setting
“00, 01, 11”: Stand-by Mode
“10”: Single Measurement Mode

13.3.14. CNTL7: Control7

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
15h	CNTL7		IR2_ MSRIUP	IR1_ MSRIUP	IR2_SH _GAIN	IR1_ADC _RNG	IR1_SH _GAIN	IR1_AFE _GAIN_1	IR1_AFE _GAIN_0
Reset		1	0	0	0	0	0	0	0

IR1_AFE_GAIN [1:0]: Selection of AFE gain of IR1 measurement path
“00”: 2 times
“01”: 1 times
“10”: 2/3 times
“11”: 1/2 times

IR1_SH_GAIN: Selection of SH gain of IR1 measurement path
“0”: 1 times
“1”: 2 times

IR1_ADC_RNG: Selection of ADC range of IR1 measurement path
“0”: 1000 mV
“1”: 500 mV

IR2_SH_GAIN: Selection of SH gain of IR2 measurement path
“0”: 0.5 times
“1”: 0.33 times

IR1_MSRIUP: Resolution selection in IR1 resistance measurement mode
“0”: 1 times (Measurement range: Maximum 750kΩ)
“1”: 4 times (Measurement range: Maximum 187.5kΩ)

IR2_MSRIUP: Resolution selection in IR2 resistance measurement mode
“0”: 1 times (Measurement range: Maximum 450kΩ)
“1”: 4 times (Measurement range: Maximum 112.5kΩ)

13.3.15. CNTL8: Control8

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
16h	CNTL8				LEDADJ_4	LEDADJ_3	LEDADJ_2	LEDADJ_1	LEDADJ_0
Reset		1	1	1	0	0	0	0	0

LEDADJ [4:0]: LED current adjustment

Table 13.8 LED current adjustment

LEDADJ [4:0]		LED current [mA]
Hex	Decimal	
1F	31	121
1E	30	118
⋮	⋮	⋮
19	25	103
18	24	100
17	23	97
⋮	⋮	⋮
01	1	31
00	0	28

13.3.16. CNTL9: Control9

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
17h	CNTL9								TST
Reset		1	1	1	1	1	1	1	0

TST:
“0”: Normal mode
“1”: TEST mode

This bit is for analysis. It is not used during normal measurement. Please be sure to set “0”.

13.3.17. CNTL10: Control10

Address	Name	D7	D6	D5	D4	D3	D2	D1	D0
18h	CNTL10								SRST
Reset		1	1	1	1	1	1	1	0

SRST: Soft reset
“0”: Normal state
“1”: Reset

All registers are reset by setting SRST bit to “1”. SRST bit automatically returns to “0” after reset is activated.

14. Recommended External Circuits

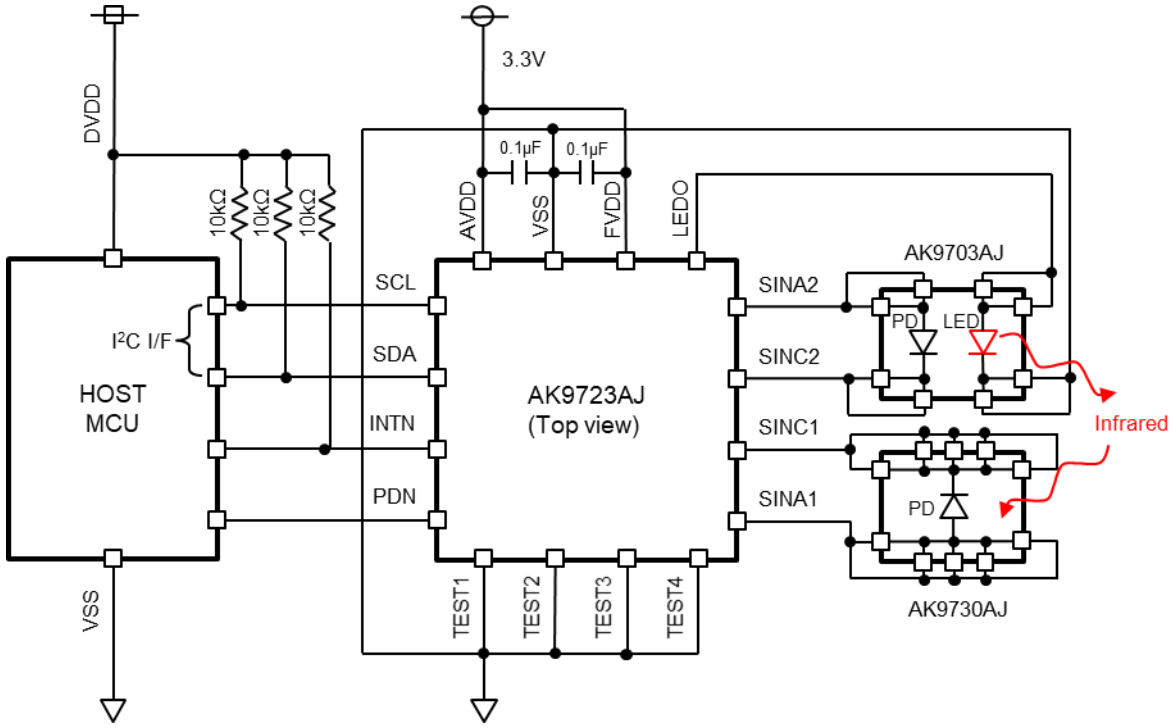


Figure 14.1 Recommended External Circuits

Pull-up resistance of SDA, SCL and INTN should be connected to DVDD. Please refer the I²C bus specification Ver2.1 and select the suitable resistance value. The resistance value in Figure 14.1 is reference.

In order to stabilize the operation of AK9723AJ, it is preferable to put a capacitor (0.1~1.0μF) between AVDD and VSS and another capacitor (0.1~1.0μF) between FVDD and VSS. In addition, the TESTx pin (x = 1, 2, 3, 4) must be connected to VSS.

Specification can not be guaranteed if each pin is open / short resulting in a state different from the above configuration.

15. Package

15.1. Outline Dimensions

Unit: mm

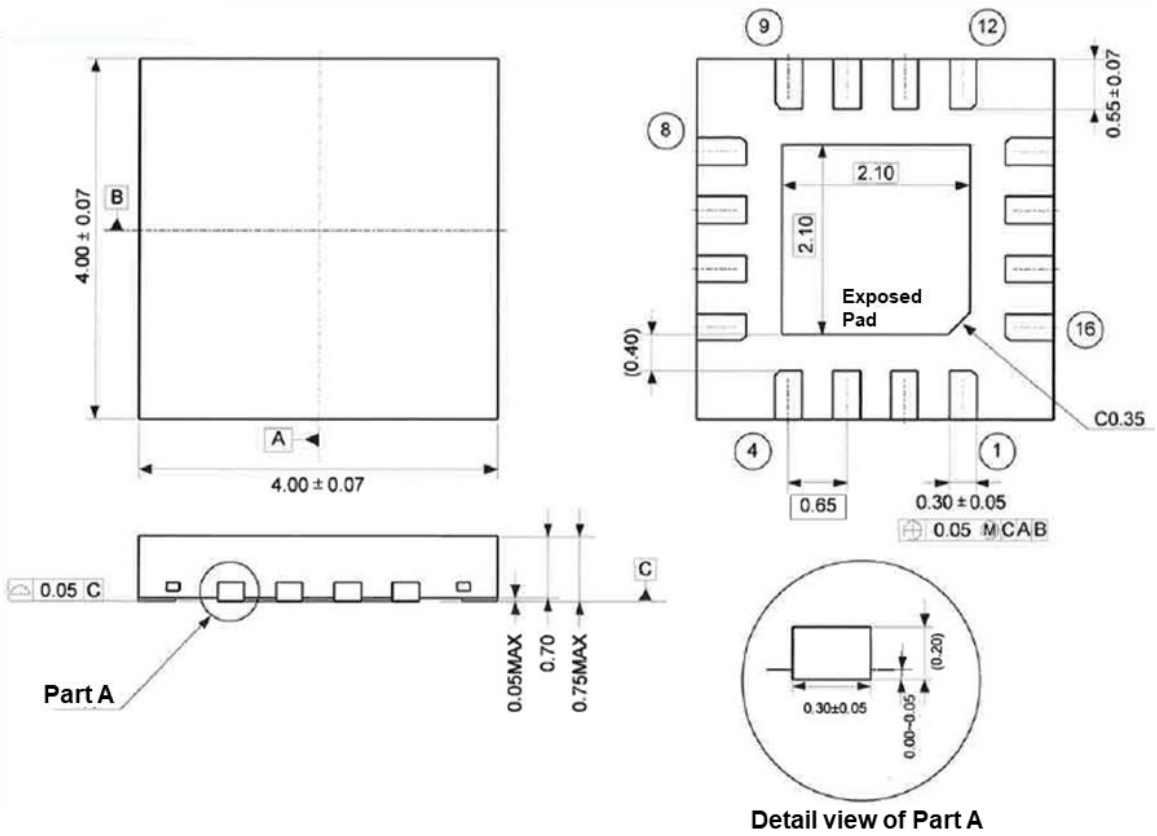


Figure 15.1 Outline Dimensions

15.2. Pad Dimensions

Unit: mm

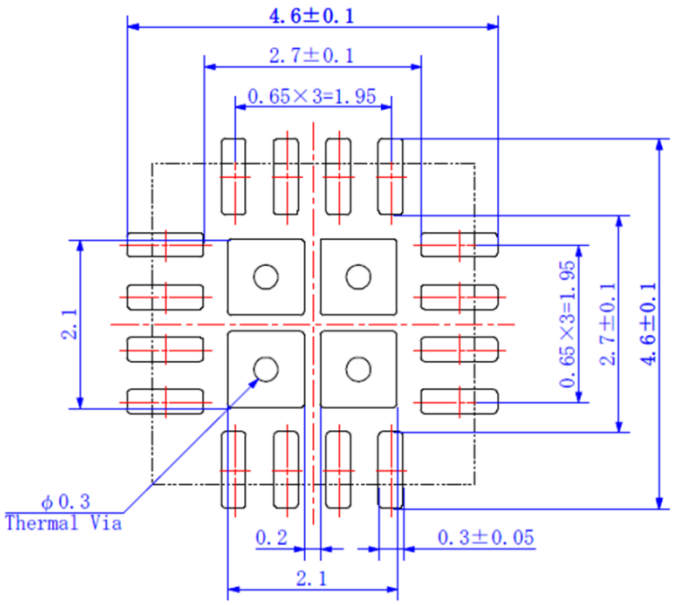
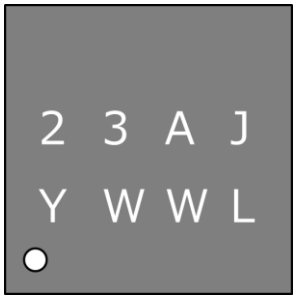


Figure 15.2 Pad Dimensions

The exposed pad must be electrically disconnected.
Do not connect a land for the exposed pad to land of other pins.

15.3. Marking



Y: Year		W W: Week				L: Lot	
Mark	Year	Mark	Week	Mark	Week	Mark	Lot
0	2020	01	1	32	32	A	1
1	2021	02	2	33	33	B	2
2	2022	03	3	34	34	C	3
3	2023	04	4	35	35	D	4
4	2024	05	5	36	36	E	5
5	2025	06	6	37	37	F	6
6	2026	07	7	38	38	G	7
7	2027	08	8	39	39	H	8
8	2028	09	9	40	40	J	9
9	2019	10	10	41	41	K	10
		11	11	42	42	L	11
		12	12	43	43	M	12
		13	13	44	44	N	13
		14	14	45	45	P	14
		15	15	46	46	Q	15
		16	16	47	47	R	16
		17	17	48	48	T	17
		18	18	49	49	U	18
		19	19	50	50	V	19
		20	20	51	51	W	20
		21	21	52	52	X	21
		22	22	53	53	Y	22
		23	23			Z	23
		24	24			1	24
		25	25			2	25
		26	26			3	26
		27	27			4	27
		28	28			5	28
		29	29			6	29
		30	30			7	30
		31	31			8	31
						9	32

16. Ordering Guide

AK9723AJ -40 ~ 85ºC 16-pin QFN Industrial Grade

17. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
19/3/8	00	First Edition		
19/8/23	01	Updated	4, 5	Figure and table numbers
		Updated	7	ITME [7:0] and MLOOP [3:0] value in Table 10.1
		Updated	9	Symbol name of "Bus free time" in Table 10.4 and Table 10.5
		Added	10	Table 10.8 Measurement interval condition
		Updated	11	Analog circuit status in Table 11.1
		Updated	12	MLOOP [3:0] in Figure 11.2
		Updated	13	Text of Section 11.5
		Updated	14	Added wait time in Figure 11.4
		Updated	19	Text of Section 12.1.6 (1) and (2)

		Updated	20	Changed the number of bits in ST1 and CNTL1 registers in Table 13.1
		Updated	23, 24, 25, 26, 27, 28	Section number
		Updated	24	LED forward voltage in Table 13.3
21/9/8	02	Updated	7	Current consumption
		Updated	30	Outline dimensions

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