AK5483

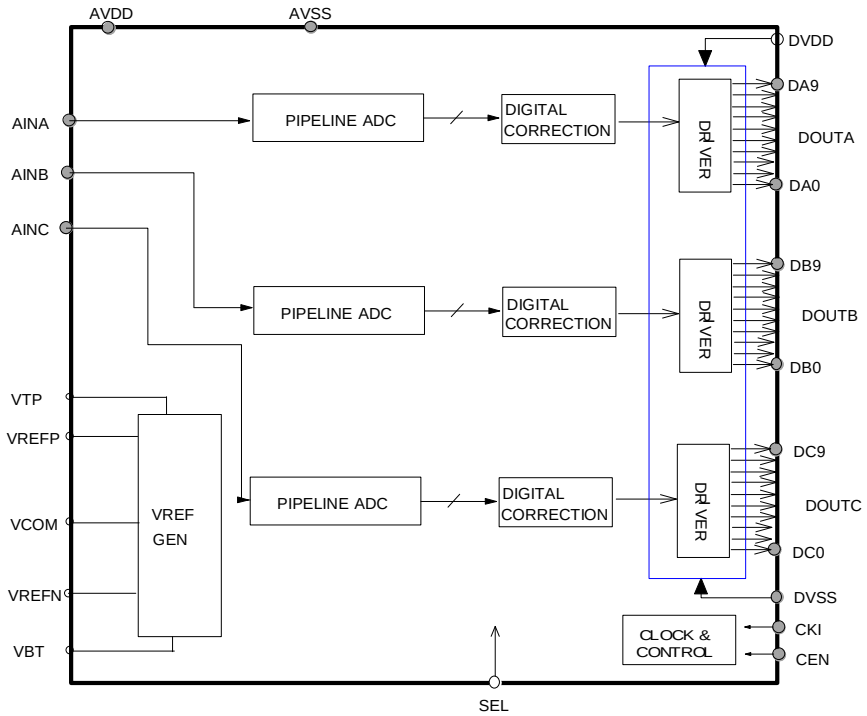
10Bit 20MHz 3CH A/D Converter

Outline

AK5483 is a Cmos, 20MSPS(MAX)、 10bit,Analog to Digital(A/D) Converter.
Three Channels of high Performance ADCs are integrated into a tiny package.
Employing Full-Pipeline A/D Conversion Architecture, AK5483 Converts Single End 1Vpp Analog Input into 10bit Straight Binary Format Digital Data.
The analog Input Range is determined by external reference input pins[VTP,VBT]. The range is common for the three channels.

Features

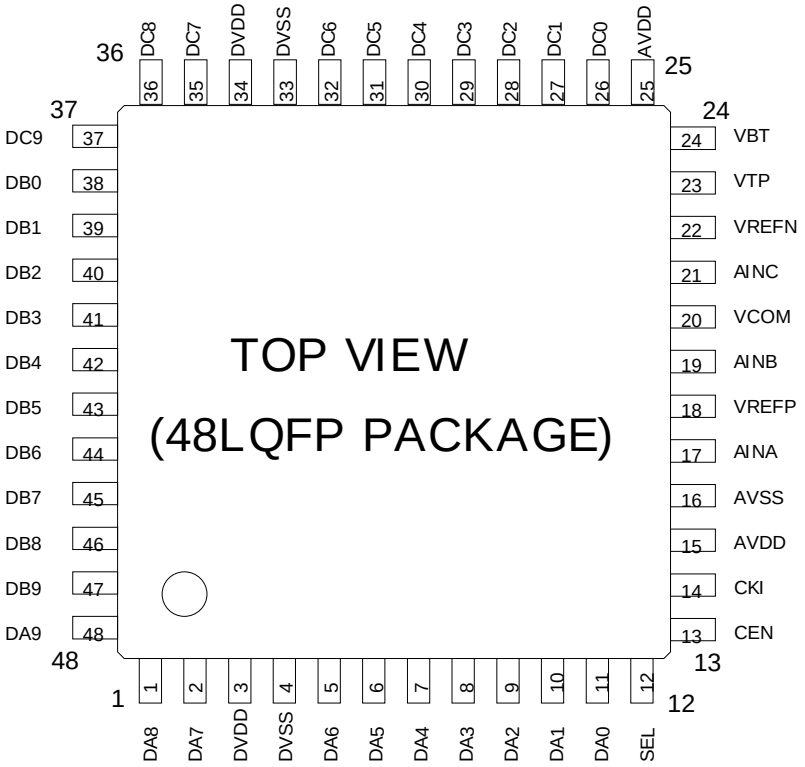
* CMOS 3Channel A/D Converter
* Sampling Rate : 20 MSPS
* Number of Channels : 3Channels(Simultaneous Sampling)
* Single Low Supply Voltage : 3.0V.... +3.6V
* Analog Input Range,Vref Range : Adaptive to Power Supply Voltage
  Single End Analog Input : 1 Vp-p [VBOT=1.3V VTOP=2.3V] (@VDD=3.0V)
* Digital Output Format : Straight Binary (BOTTOM=000H , TOP=3FFH)
  3CH * 10BIT (All data in Parallel)
* Stand-by mode
* Low Power Consumption : 135 mW(15MHz mode @3V)
  165 mW(20MHz mode @3V)
* High Isolation between Channels : 55dB
* Linearity : Differential(DNL) +-0.6 LSB(TYP.)
  : Integral (INL) +-1.5 LSB(TYP.)
* Small Package : 48pin LQFP-0707



* Ordering Guide

AK5483 -20deg...+85deg 48 Pin LQFP

* Pin Assignment



ALL SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

* Pin Descriptions [48LQFP]

PIN NO.	Symbol	Type	Description & Function
1	DA8	O	CH A OUTPUT D8
2	DA7	O	CH A OUTPUT D7
3	DVDD	P	Digital Supply(3.3V[TYP.])
4	DVSS	P	Digital Ground 0V
5	DA6	O	CH A OUTPUT D6
6	DA5	O	CH A OUTPUT D5
7	DA4	O	CH A OUTPUT D4
8	DA3	O	CH A OUTPUT D3
9	DA2	O	CH A OUTPUT D2
10	DA1	O	CH A OUTPUT D1
11	DAO	O	CH A OUTPUT D0(LSB)
12	SEL	I	Sampling Frequency SELECT Upper Limit of Sampling Clock(CKI) Frequency is determined by this pin. Low : 15MHz mode High : 20MHz mode Always connect to High or Low.
13	CEN	I	CHIP ENABLE(Power Down Control) LOW:Normal Operating Mode High: Power down & All Digital Output= High-Z
14	CKI	I	CLOCK Input Input Pin for Sampling Clock
15	AVDD	P	Analog Supply (3.3V[TYP.])
16	AVSS	P	Analog Ground 0V
17	AINA	I	ANALOG INPUT(CH A)
18	VREFP	O	VREF Voltage for internal circuit Place 0.1uF Ceramic Cap. between AVSS.
19	AINB	I	ANALOG INPUT(CH B)
20	VCOM	O	VREF Voltage for internal circuit Place 0.1uF Ceramic Cap. between AVSS.
21	AINC	I	ANALOG INPUT(CH C)
22	VREFN	O	VREF Voltage for internal circuit Place 0.1uF Ceramic Cap. between AVSS.
23	VTP	I	VREF Top Voltage Input Pin[To set Analog Input Range] VIN Full Scale Reference pin.
24	VBT	I	VREF Bottom Voltage Input Pin[To set Analog Input Range] VIN Zero Scale Reference pin.

* Pin Descriptions

PIN NO.	Symbol	Type	Description & Function
25	AVDD	P	Analog Supply (3.3V[TYP.])
26	DC0	O	CH C OUTPUT D0(LSB)
27	DC1	O	CH C OUTPUT D1
28	DC2	O	CH C OUTPUT D2
29	DC3	O	CH C OUTPUT D3
30	DC4	O	CH C OUTPUT D4
31	DC5	O	CH C OUTPUT D5
32	DC6	O	CH C OUTPUT D6
33	DVSS	P	Digital Ground 0V
34	DVDD	P	Digital Supply(3.3V[TYP.])
35	DC7	O	CH C OUTPUT D7
36	DC8	O	CH C OUTPUT D8
37	DC9	O	CH C OUTPUT D9(MSB)
38	DB0	O	CH B OUTPUT D0(LSB)
39	DB1	O	CH B OUTPUT D1
40	DB2	O	CH B OUTPUT D2
41	DB3	O	CH B OUTPUT D3
42	DB4	O	CH B OUTPUT D4
43	DB5	O	CH B OUTPUT D5
44	DB6	O	CH B OUTPUT D6
45	DB7	O	CH B OUTPUT D7
46	DB8	O	CH B OUTPUT D8
47	DB9	O	CH B OUTPUT D9(MSB)
48	DA9	O	CH A OUTPUT D9(MSB)

ABSOLUTE MAXIMUM RATINGS

AVSS,DVSS=0V,All voltages are with respect to GND

Parameter	Symbol	Conditions	Ratings	Units
Power Supply Voltage				V
	AVDD		-0.3 ..... 6.0	V
	DVDD		-0.3 ..... 6.0	
		(# 1)	or (AVDD+0.3)	V
Voltage Difference	Vdlt	DVDD - AVDD	0.3	V
Input Current	IIN	Except Power Pins	+-10	mA
Analog Input Voltage Range	VINA		AVSS - 0.3 ..... AVDD + 0.3	V
Digital Input Voltage [Input Pins]	VINL		AVSS - 0.3 ..... AVDD + 0.3	V
Digital Input Voltage [Output Pins]	VONL	(#2)	AVSS - 0.3 .... AVDD + 0.3	V
Ambient Temperature	TA		-20 ..... +85	deg
Storage Temperature	Tstg		-40 .....+125	deg

(# 1) The higher voltage of 6.0V and AVDD + 0.3V specifies Max. value of DVDD absolute maximum rating.

(# 2) The VONL limits the excess voltage applied to digital output pins.

WARNING Operation at or beyond these limits may result in permanent damage to the device. Normal Operating Specifications are not guaranteed at these extremes.

Recommended Operating Conditions

1.Power Supply Requirements
(DVSS,AVSS=0V,(#1))

Parameter	Symbol	Condition	min	typ	max	Units
Supply Voltage [Analog]	AVDD	(#2)	3.0	3.3	3.6	V
[Digital]	DVDD		3.0	3.3	AVDD	V

(#1) All voltages are with respect to GND
(#2) At start-up , power-on AVDD before(or at the same time to) DVDD power-on.

2.Reference Input

Applicable Voltage to Top/Bottom Reference Voltage(TOP,BOTTOM is proportional to Power Supply Voltage[AVDD].

The Analog Input Range[Conversion D-range] is determined based on TOP & BOTTOM Voltage [which is applied to VTP/VBT pins] . Note that the AINFS[Analog Input Range] must satisfy the following range.

Parameter	Symbol	Conditions	SPEC	Values	Unit
Analog Input Range	AINFS	#1	min.	VDD/3 - VDD/30	Vpp
			typ.	VDD/3	
			max.	VDD/3 + VDD/30	
Reference Bottom Voltage	VBTE	#2	min.	1.3 * VDD/3 - VDD/30	V
			typ.	1.3 * VDD/3	
			max.	1.3 * VDD/3 + VDD/30	
Reference Top Voltage	VTPE	#2	min.	2.3 * VDD/3 - VDD/30	V
			typ.	2.3 * VDD/3	
			max	2.3 * VDD/3 + VDD/30	
Reference Input Impedance	ZTBE	VBT -VTP	min.		KOHM
			typ.	100	

(#1) : AINFS=VTPE - VBTE
Note that AFINFS is not the ADC operating input voltage range (Analog Characteristics are not always guaranteed.)
(#2) : Adjust both of these voltages[VBTE/VTPE] to satisfy the AINFS spec. regarding the voltage difference VTPE-VBTE.
(Notice : Acceptable external VREF voltage varies according to the Power Supply Voltage[AVDD].
Example : In case of VDD=AVDD=DVDD=3.0V
VBTE=1.20...1.398V VTPE=2.199...2.397V
AINFS= 0.9 .... 1.08 Vpp

Specifications

1) Analog Specifications

(AVDD=DVDD=3.3V, VBT=1.43V,VTP=2.53V, Ta=25deg,
Fs=20MHz @20MHz mode , Fs=15MHz @15MHz mode
Signal frequency Fin=1MHz Signal level =-1dB , unless otherwise noted)

Parameter	Symbol	Conditions	min	typ	max	Units
Resolution	RES				10	BITS
Integral Nonlinearity[INL]	INL			+-1.5	+-2.5	LSB
Differential Nonlinearity[DNL]	DNL			+-0.6	+-1.0	LSB
Offset Voltage	EOB EOT	TO VBT TO VTP (#1)	-30 -40		+30 +40	mV mV
Cross-talk	CT	@Fs=20MHz(#2)		-65	-55	dB
Input Resistance	RIN	@Fs=20MHz(#3)		50		KOHM
Input Capacitance	CIN	@Fs=20MHz		10		pF
Input Bandwidth	BW	-3dB@20MHz		100		MHz

(#1)Offset Voltage is the difference of Transition input voltage to All Zero [All One] and VBT[VTP].

(#2)Cross-talk[CT] is the isolation between each ADC.
The value is specified as the cross talk from any one channel[Ain=1MHz ,-1dB] to the other two channels[no signal input].

(#3)Input Resistance[RIN] is specified as the equivalent impedance from Analog Input Pins[AINA,AINB,AINC] to ADC common voltage[center voltage between VTP & VBT]. RIN is proportional to 1/FS.

2)Power Supply

(Ta=25 deg ;AVDD=DVDD=3.3V; VTP=2.53V,VBT=1.43V)

Parameter	Symbol	Condition	min	typ	max	Units
Analog Operating Current (@CEN=LOW)	IA+	Fin=1MHz @Fs=15MHz(#3) @Fs=20MHz		45 55	60 70	mA mA
Digital Output Driver Operating Current (@CEN=LOW)	ID+	Fin=1MHz (#1) @Fs=15MHz(#3) @Fs=20MHz		10 15	15 21	mA mA
Stand-by Current (@CEN=HIGH)	IAS IDS	Analog (#2) Digital			0.1 0.1	mA mA

(#1)Capacitor Loads [CL=10pF] are attached to all digital output pins[D0..D9].
Analog Input Signal 1MHz Sine Wave.

(#2)The Stand-by Current is measured under
*No Analog Input *CKI= Low fixed

(#3)15MHz mode is selected by SEL=Low.

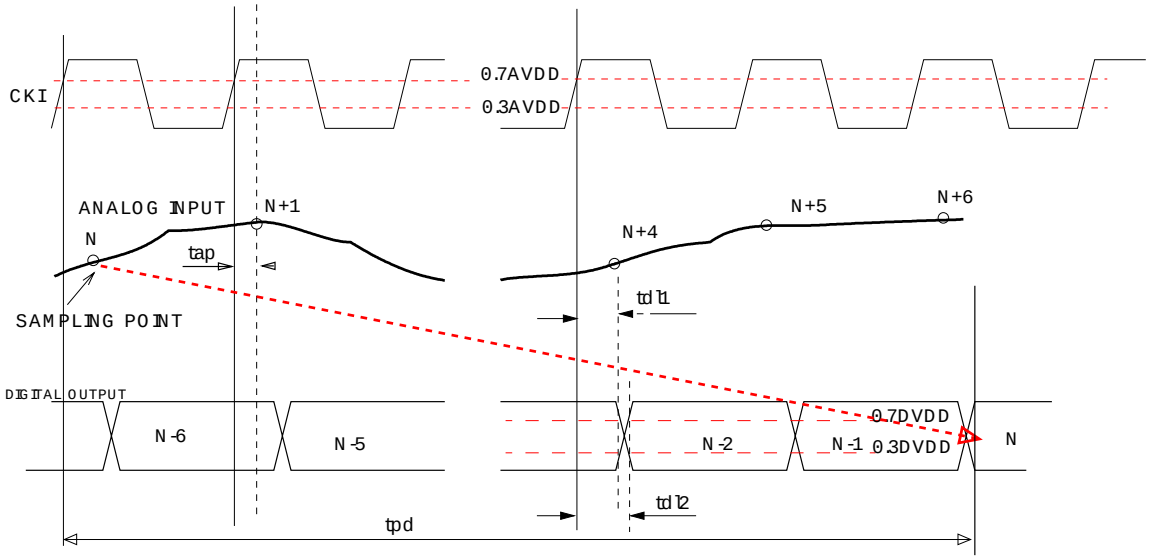
3)Timing Specifications

(AVDD,DVDD=3.0V....3.6 V, AVSS,DVSS=0V, Ta=TAMIN.....TAMAX deg,CL<10pF)

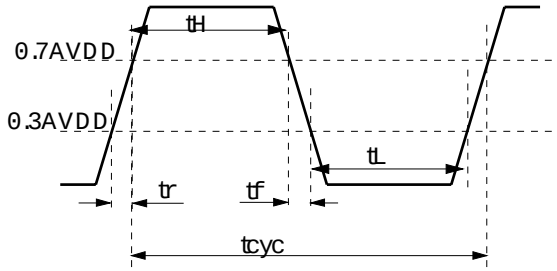
Parameters	Symbo l	Conditon	min	typ	max	Units
Conversion Speed	Fc	15MHz mode 20MHz mode	0.5 0.5		15 20	MHz MHz
Clock Cycle	tcy	15MHz mode 20MHz mode	66 50			ns ns
Clock Rise Time	tr	[30%->70%]VDD			2	ns
Clock Fall Time	tf	[70%->30%]VDD			2	ns
Clock Duty Cycle	DUTY	(#1)		50		%
Clock Low Period	tL	15MHz mode 20MHz mode	31 23			ns ns
Clock High Period	tH	15MHz mode 20MHz mode	31 23			ns ns
Pipeline Delay	tpd			6		CLKIN
Sampling Delay	tap			3		ns
Data Output Delay	tdl1 tdl2		2		35	ns ns

(#1)Acceptable DUTY should be calculated from clock HIGH/LOW period and operating Frequency(Fc).

Timing Diagram



Clock Timing Chart



4)Digital DC Specifications

(AVDD=DVDD=3.0...3.6V , AVSS=DVSS=0V, Ta=TAMIN...TAMAX deg
Specified as static characteristics)

Parameter	Symbol	Condition	min	typ	max	Units
High Input Voltage	VIH		0.7AVDD			V
Low Input Voltage	VIL				0.3AVDD	V
High Output Voltage	VOH	IOH=-3mA	0.7DVDD			V
Low Output Voltage	VOL	IOL=3mA			0.3DVDD	V
High Level Input Current (CKI,CEN)	ILIKG				+-10	uA
HIGH-Z Output Current (DA0:9,DB0:9,DC0:9)	IOZ	CEN=HIGH			+-10	uA

Theory of operation

* Analog Input Range

External Reference Voltage fed through VTP/VBT determine the analog input range of all three channels of 10 Bit AD converter.

The Zero level of analog input(AINA,AINB,AINC) is VBT and the Full Scale is VTP.

* Converted Digital Output Code

The converted Digital Output Code is Straight Binary format.

For Zero Scale(AIN=VBT), the output code is all zero.

For Full Scale(AIN=VTP), the output code is all one.

The deviation from these ideal voltage is expressed by Offset[EOB,EOT].

* Sampling Frequency Select

Reduction of power consumption is realized for sampling frequency less than 15MHz.

20MHz mode : SEL=High Normal current is consumed to operate at Fc=20MHz.

15MHz mode] : SEL=Low Current is reduced with restriction of Fcmax=15MHz.

* Chip Enable Function

By setting CEN=High, whole chip of AK5483 powers down.

Under the power down state, all digital output are High-Impedance and Vref related circuit also powers down.

The internal reference voltage is generated with input of CEN=LOW & supply of external VREF voltage. Depending on the state of external capacitors, some period is required to charge them.

* CKI,Pipeline delay,Data Output Timing

Feed A/D converter sampling clock through CKI pin.

Rising edges of CKI track and hold the analog input signal.

After 6clock pipeline delay, 10 bit digital output code is obtained.

* Caution for Power Supply

It is recommended to supply both AVDD and DVDD supply from single regulator.

(Please observe absolute maximum rating spec. DVDD<=(AVDD+0.3V) even at the start-up sequence of the power.)

Control Logic

Digital Output

The following chart describes relation between analog input and the digital Output

Analog Input						Digital Output Code									
						MSB									LSB
VTP						1	1	1	1	1	1	1	1	1	1
:										:					
:						1	0	0	0	0	0	0	0	0	0
:						0	1	1	1	1	1	1	1	1	1
:										:					
VBT						0	0	0	0	0	0	0	0	0	0

(note VTP.VBT are common for all three channels
Input Range of VINA,B,C is determined by VTP,VBT)

The output code by CEN[Power Down] is as follows

CEN		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
LO		P	P	P	P	P	P	P	P	P	P
HI		Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

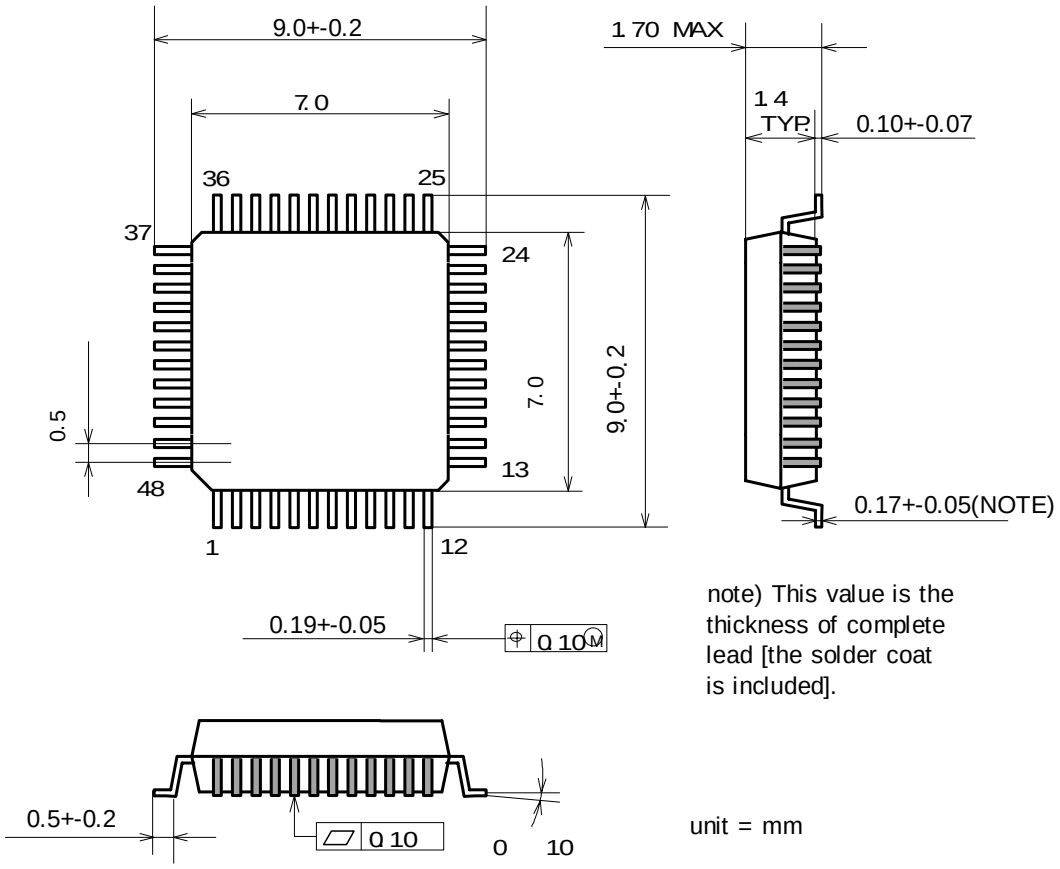
NOTE: P: Normal Output code
Z: High Impedance

Frequency mode Select by SEL

SEL	mode	Fcmax	Power
LO	15MHz mode	15MHz	Reduced
HI	20MHz mode	20MHz	Normal

Outline Dimensions

48LQFP-0707



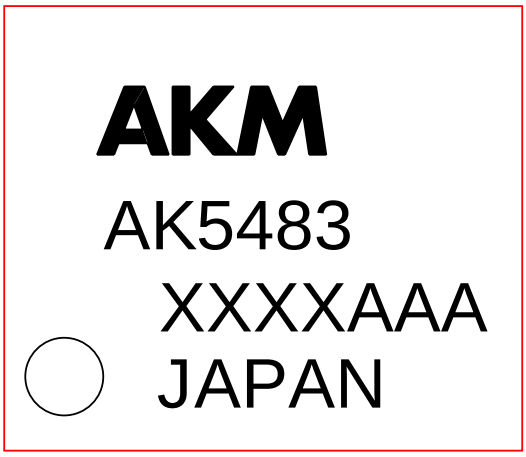
note) This value is the thickness of complete lead [the solder coat is included].

unit = mm

* Package & Lead frame material

Package molding compound	:	Epoxy
Lead frame material	:	Cu
Lead frame surface treatment:	:	Solder plate

Marking



Contents of XXXXAAA

XXXX : Production date (numbers)

AAA : lot number (alphabet)

Reference Circuit

The following schematic is the Reference circuit for system design.
Please optimize capacitance/resistance according to the system environment.