

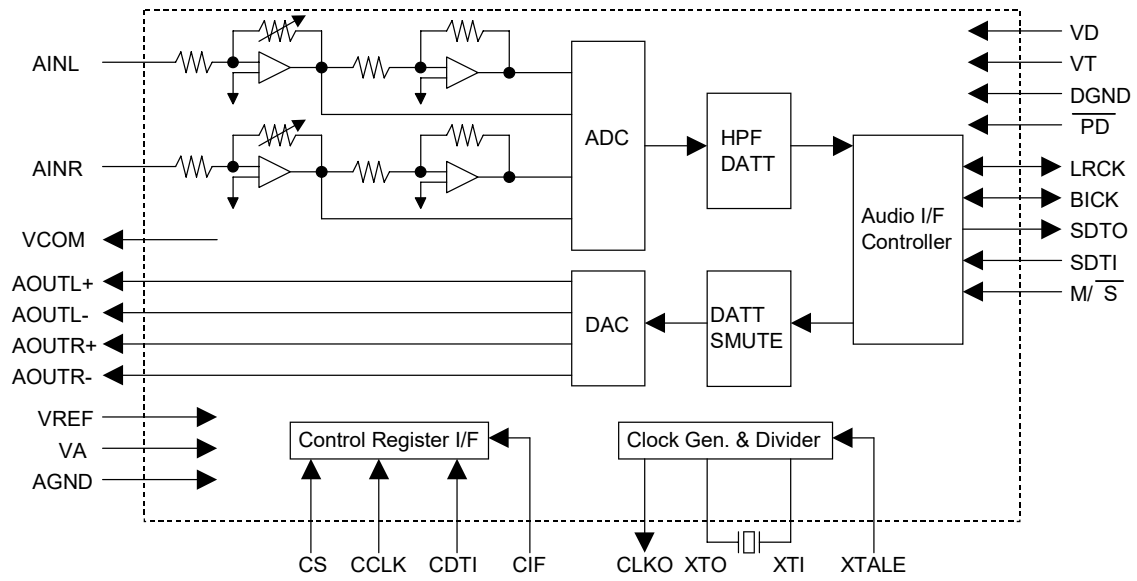
**AK4524****24Bit 96kHz Audio CODEC****GENERAL DESCRIPTION**

The AK4524 is a high performance 24bit CODEC for the 96kHz recording system. The ADC has an Enhanced Dual Bit architecture with wide dynamic range. The DAC uses the new developed Advanced Multi Bit architecture and achieves low outband noise and high jitter tolerance by use of SCF (switched capacitor filter) techniques. The AK4524 has an input PGA and is well-suited MD, DVTR system and musical instruments.

**FEATURES**

- **24bit 2ch ADC**
  - 64x Oversampling
  - Single-End Inputs
  - S/(N+D): 90dB
  - Dynamic Range, S/N: 100dB
  - Digital HPF for offset cancellation
  - Input PGA with +18dB gain & 0.5dB step
  - Input DATT with -72dB att
  - I/F format: MSB justified or I<sup>2</sup>S
- **24bit 2ch DAC**
  - 128x Oversampling
  - 24bit 8 times Digital Filter
    - Ripple: ±0.005dB, Attenuation: 75dB
  - SCF
  - Differential Outputs
  - S/(N+D): 94dB
  - Dynamic Range, S/N: 110dB
  - De-emphasis for 32kHz, 44.1kHz, 48kHz sampling
  - Output DATT with -72dB att
  - Soft Mute
  - I/F format: MSB justified, LSB justified or I<sup>2</sup>S
- **High Jitter Tolerance**
- **3-wire Serial Interface for Volume Control**
- **Master Clock**
  - X'tal Oscillating Circuit
  - 256fs/384fs/512fs/768fs/1024fs
- **Master Mode/Slave Mode**
- **5V operation**
- **3V Power Supply Pin for 3V I/F**
- **Small 28pin SSOP package**

■ Block Diagram



Block Diagram

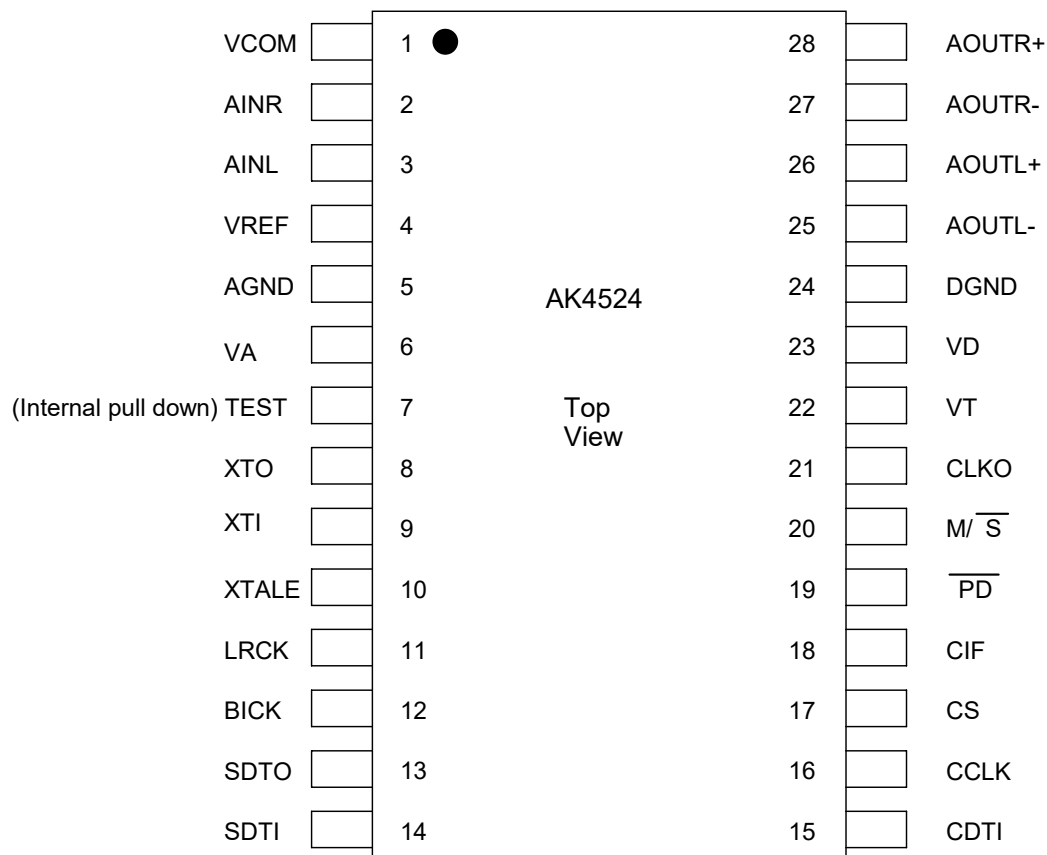
■ Ordering Guide

AK4524VM

-20 ~ +85°C

28pin SSOP (0.65mm pitch)

■ Pin Layout



| PIN/FUNCTION |                         |     |   |
|--------------|-------------------------|-----|---|
| No.          | Pin Name                | I/O | Function  |
| 1            | VCOM                    | O   | Common Voltage Output Pin, VA/2<br>Bias voltage of ADC inputs and DAC outputs.  |
| 2            | AINR                    | I   | Rch Analog Input Pin  |
| 3            | AINL                    | I   | Lch Analog Input Pin  |
| 4            | VREF                    | I   | Voltage Reference Input Pin, VA<br>Used as a voltage reference by ADC & DAC. VREF is connected externally to filtered VA. |
| 5            | AGND                    | -   | Analog Ground Pin   |
| 6            | VA                      | -   | Analog Power Supply Pin, 4.75 ~ 5.25V   |
| 7            | TEST                    | I   | Test Pin<br>(Internal pull-down pin)  |
| 8            | XTO                     | O   | X'tal Output Pin  |
| 9            | XTI                     | I   | X'tal/Master Clock Input Pin  |
| 10           | XTALE                   | I   | X'tal Osc Enable Pin<br>"H": Enable, "L": Disable   |
| 11           | LRCK                    | I/O | Input/Output Channel Clock Pin  |
| 12           | BICK                    | I/O | Audio Serial Data Clock Pin   |
| 13           | SDTO                    | O   | Audio Serial Data Output Pin  |
| 14           | SDTI                    | I   | Audio Serial Data Input Pin   |
| 15           | CDTI                    | I   | Control Data Input Pin  |
| 16           | CCLK                    | I   | Control Data Clock Pin  |
| 17           | CS                      | I   | Chip Select Pin   |
| 18           | CIF                     | I   | Control Data I/F Format Pin<br>"H": CS falling trigger, "L": CS rising trigger  |
| 19           | $\overline{\text{PD}}$  | I   | Power-Down Mode Pin<br>"H": Power up, "L": Power down, reset and initialize the control register.                         |
| 20           | $\overline{\text{M/S}}$ | I   | Master/Slave Mode Pin<br>"H": Master mode, "L": Slave mode  |
| 21           | CLKO                    | O   | Master Clock Output Pin   |
| 22           | VT                      | -   | Output Buffer Power Supply Pin, 2.7 ~ 5.25V   |
| 23           | VD                      | -   | Digital Power Supply Pin, 4.75 ~ 5.25V  |
| 24           | DGND                    | -   | Digital Ground Pin  |
| 25           | AOUTL-                  | O   | Lch Negative Analog Output Pin  |
| 26           | AOUTL+                  | O   | Lch Positive Analog Output Pin  |
| 27           | AOUTR-                  | O   | Rch Negative Analog Output Pin  |
| 28           | AOUTR+                  | O   | Rch Positive Analog Output Pin  |

Note: All input pins except pull-down pins should not be left floating.

|                                 |
|---------------------------------|
| <b>ABSOLUTE MAXIMUM RATINGS</b> |
|---------------------------------|

(AGND, DGND=0V; Note 1)

| Parameter                              |               | Symbol | min  | max    | Unit |
|--|---------------|--------|------|--------|------|
| Power Supplies:                        | Analog        | VA     | -0.3 | 6.0    | V    |
|  | Digital       | VD     | -0.3 | 6.0    | V    |
|  | Output Buffer | VT     | -0.3 | 6.0    | V    |
|  | VD-VA         | VDA    | -    | 0.3    | V    |
| Input Current, Any Pin Except Supplies |               | IIN    | -    | ±10    | mA   |
| Analog Input Voltage                   |               | VINA   | -0.3 | VA+0.3 | V    |
| Digital Input Voltage                  |               | VIND   | -0.3 | VA+0.3 | V    |
| Ambient Temperature (powered applied)  |               | Ta     | -20  | 85     | °C   |
| Storage Temperature                    |               | Tstg   | -65  | 150    | °C   |

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

|   |
|---|
| <b>RECOMMENDED OPERATING CONDITIONS</b> |
|---|

(AGND, DGND=0V; Note 1)

| Parameter                  |               | Symbol | min  | typ | max  | Unit |
|----------------------------|---------------|--------|------|-----|------|------|
| Power Supplies<br>(Note 2) | Analog        | VA     | 4.75 | 5.0 | 5.25 | V    |
|                            | Digital       | VD     | 4.75 | 5.0 | VA   | V    |
|                            | Output Buffer | VT     | 2.7  | 3.0 | VD   | V    |
| Voltage Reference          |               | VREF   | 3.0  | -   | VA   | V    |

Note: 1. All voltages with respect to ground.

2. VA and VD should be powered at the same time or VA should be powered earlier than VD.  
The power up sequence between VA and VT, or VD and VT is not critical.

\*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

| ANALOG CHARACTERISTICS   |                      |                        |     |     |     |        |
|--|----------------------|------------------------|-----|-----|-----|--------|
| (Ta=25°C; VA, VD, VT=5.0V; AGND=DGND=0V; VREF=VA; fs=44.1kHz; Signal Frequency=1kHz; 24bit Data; Measurement frequency = 10Hz ~ 20kHz at fs=44.1kHz, 10Hz ~ 40kHz at fs=96kHz; unless otherwise specified) |                      |                        |     |     |     |        |
| Parameter  |                      |                        | min | typ | max | Unit   |
| <b>Input PGA Characteristics:</b>  |                      |                        |     |     |     |        |
| Input Voltage  | (Note 3)             |                        | 2.7 | 2.9 | 3.1 | Vpp    |
| Input Resistance   |                      |                        | 5   | 10  | 15  | kΩ     |
| Step Size  |                      |                        | 0.2 | 0.5 | 0.8 | dB     |
| Gain Control Range   |                      |                        | 0   |     | 18  | dB     |
| <b>ADC Analog Input Characteristics: IPGA=0dB</b>  |                      |                        |     |     |     |        |
| Resolution   |                      |                        |     |     | 24  | Bits   |
| S/(N+D)  | (-0.5dBFS)           | fs=44.1kHz             | 84  | 90  |     | dB     |
|  |                      | fs=96kHz               | 80  | 88  |     | dB     |
| DR   | (-60dBFS)            | fs=44.1kHz, A-weighted | 94  | 100 |     | dB     |
|  |                      | fs=96kHz               | 88  | 96  |     | dB     |
| S/N  |                      | fs=44.1kHz, A-weighted | 94  | 100 |     | dB     |
|  |                      | fs=96kHz               | 88  | 96  |     | dB     |
| Interchannel Isolation   |                      |                        | 90  | 105 |     | dB     |
| Interchannel Gain Mismatch   |                      |                        |     | 0.2 | 0.5 | dB     |
| Gain Drift   |                      |                        |     | 20  | -   | ppm/°C |
| Power Supply Rejection   | (Note 4)             |                        |     | 50  | -   | dB     |
| <b>DAC Analog Output Characteristics:</b>  |                      |                        |     |     |     |        |
| Resolution   |                      |                        |     |     | 24  | Bits   |
| S/(N+D)  | (0dBFS)              | fs=44.1kHz             | 88  | 94  |     | dB     |
|  |                      | fs=96kHz               | 85  | 93  |     | dB     |
| DR   | (-60dBFS)            | fs=44.1kHz, A-weighted | 104 | 110 |     | dB     |
|  |                      | fs=96kHz               | 96  | 104 |     | dB     |
| S/N  |                      | fs=44.1kHz, A-weighted | 104 | 110 |     | dB     |
|  |                      | fs=96kHz               | 96  | 104 |     | dB     |
| Interchannel Isolation   |                      |                        | 100 | 110 |     | dB     |
| Interchannel Gain Mismatch   |                      |                        |     | 0.2 | 0.5 | dB     |
| Gain Drift   |                      |                        |     | 20  | -   | ppm/°C |
| Output Voltage   | (Note 5)             |                        | 5.0 | 5.4 | 5.8 | Vpp    |
| Load Resistance  | (In case of AC load) |                        | 1   |     |     | kΩ     |
| Output Current   | (In case of AC load) |                        |     |     | 1.5 | mA     |
| Load Capacitance   |                      |                        |     |     | 25  | pF     |

Note: 3. Full scale (0dB) of the input voltage at PGA=0dB.

This voltage is proportional to VREF.  $V_{in}=0.58 \times VREF$ .

4. PSR is applied to VA, VD, VT with 1kHz, 50mVpp. VREF pin is held a constant voltage.

5. Full scale (0dB) of the output voltage when summing the differential outputs, AOUT+/- by unity gain.

This voltage is proportional to VREF.  $V_{out}=1.08 \times VREF \times Gain$ .

| Parameter  | min | typ | max | Unit          |
|--|-----|-----|-----|---------------|
| <b>Power Supplies</b>  |     |     |     |               |
| Power Supply Current   |     |     |     |               |
| Normal Operation ( $\overline{\text{PD}} = \text{"H"}$ )         |     |     |     |               |
| VA   |     | 30  | 45  | mA            |
| VD+VT (fs=44.1kHz)   |     | 16  | 24  | mA            |
| (fs=96kHz)   |     | 24  | 36  | mA            |
| Power-down mode ( $\overline{\text{PD}} = \text{"L"}$ ) (Note 6) |     |     |     |               |
| VA   |     | 10  | 100 | $\mu\text{A}$ |
| VD+VT  |     | 10  | 100 | $\mu\text{A}$ |

Note: 6. XTAL="L" and all digital input pins are held VD or DGND.

| <b>FILTER CHARACTERISTICS</b>                                       |          |                   |       |             |               |  |
|---|----------|-------------------|-------|-------------|---------------|--|
| (Ta=25°C; VA, VD=4.75 ~ 5.25V; VT=2.7 ~ 5.25V; fs=44.1kHz; DEM=OFF) |          |                   |       |             |               |  |
| Parameter   | Symbol   | min               | typ   | max         | Unit          |  |
| <b>ADC Digital Filter (Decimation LPF):</b>                         |          |                   |       |             |               |  |
| Passband (Note 7)   | -0.005dB | PB                | 0     | 19.76       | kHz           |  |
|   | -0.02dB  |                   | -     | 20.02       | kHz           |  |
|   | -0.06dB  |                   | -     | 20.20       | kHz           |  |
|   | -6.0dB   |                   | -     | 22.05       | kHz           |  |
| Stopband  |          | SB                | 24.34 |             | kHz           |  |
| Passband Ripple   |          | PR                |       | $\pm 0.005$ | dB            |  |
| Stopband Attenuation  |          | SA                | 80    |             | dB            |  |
| Group Delay (Note 8)  |          | GD                |       | 31          | 1/fs          |  |
| Group Delay Distortion  |          | $\Delta\text{GD}$ |       | 0           | $\mu\text{s}$ |  |
| <b>ADC Digital Filter (HPF):</b>                                    |          |                   |       |             |               |  |
| Frequency Response (Note 7)   | -3dB     | FR                |       | 0.9         | Hz            |  |
|   | -0.5dB   |                   |       | 2.7         | Hz            |  |
|   | -0.1dB   |                   |       | 6.0         | Hz            |  |
| <b>DAC Digital Filter:</b>  |          |                   |       |             |               |  |
| Passband (Note 7)   | -0.01dB  | PB                | 0     | 20.0        | kHz           |  |
|   | -6.0dB   |                   | -     | 22.05       | kHz           |  |
| Stopband  |          | SB                | 24.1  |             | kHz           |  |
| Passband Ripple   |          | PR                |       | $\pm 0.005$ | dB            |  |
| Stopband Attenuation  |          | SA                | 75    |             | dB            |  |
| Group Delay (Note 8)  |          | GD                |       | 30          | 1/fs          |  |
| <b>DAC Digital Filter + SCF:</b>                                    |          |                   |       |             |               |  |
| Frequency Response:   |          | FR                |       |             |               |  |
| 0 ~ 20.0kHz   |          |                   |       | $\pm 0.2$   | dB            |  |
| ~ 40kHz (Note 9)  |          |                   |       | $\pm 0.3$   | dB            |  |

Note: 7. The passband and stopband frequencies scale with fs. For example, 20.02kHz at -0.02dB is 0.454 x fs.

The reference frequency of these responses is 1kHz.

8. The calculating delay time which occurred by digital filtering. This time is from the input of analog signal to setting the 24bit data of both channels to the output register for ADC.

For DAC, this time is from setting the 24bit data of both channels on input register to the output of analog signal.

9. fs=96kHz.

## DIGITAL CHARACTERISTICS

(Ta=25°C; VA, VD=4.75 ~ 5.25V; VT=2.7 ~ 5.25V)

| Parameter   | Symbol | min          | typ | Max | Unit |
|---|--------|--------------|-----|-----|------|
| High-Level Input Voltage                          | VIH    | 2.2          | -   | -   | V    |
| Low-Level Input Voltage                           | VIL    | -            | -   | 0.8 | V    |
| High-Level Output Voltage (Iout=-100μA) (Note 10) | VOH    | 2.7 / VT-0.5 | -   | -   | V    |
| Low-Level Output Voltage (Iout=100μA)             | VOL    | -            | -   | 0.5 | V    |
| Input Leakage Current                             | Iin    | -            | -   | ±10 | μA   |

Note: 10. Min value is lower voltage of 2.7V or VT-0.5V.

## SWITCHING CHARACTERISTICS

(Ta=25°C; VA, VD=4.75 ~ 5.25V; VT=2.7 ~ 5.25V; CL=20pF)

| Parameter   | Symbol           | min     | typ      | max    | Unit |
|---|------------------|---------|----------|--------|------|
| <b>Master Clock Timing</b>                        |                  |         |          |        |      |
| Crystal Resonator                                 | Frequency        | 11.2896 |          | 24.576 | MHz  |
| External Clock                                    | Frequency        | fCLK    | 8.192    | 49.152 | MHz  |
|   | Pulse Width Low  | tCLKL   | 0.4/fCLK |        | ns   |
|   | Pulse Width High | tCLKH   | 0.4/fCLK |        | ns   |
| <b>CLKO Output</b><br>(X'tal mode)                | Frequency        | fMCK    | 11.2896  | 24.576 | MHz  |
|   | Duty Cycle       | dMCK    | 35       | 65     | %    |
| <b>LRCK Frequency</b>                             |                  |         |          |        |      |
| Normal Speed Mode (DFS0="0", DFS1="0")            |                  | fsn     | 32       | 48     | kHz  |
| Double Speed Mode (DFS0="1", DFS1="0")            |                  | fsd     | 64       | 96     | kHz  |
| Quad Speed Mode (DFS0="0", DFS1="1")              |                  | fsq     | 128      | 192    | kHz  |
| Duty Cycle  | Slave mode       |         | 45       | 55     | %    |
|   | Master mode      |         | 50       |        | %    |
| <b>Audio Interface Timing</b>                     |                  |         |          |        |      |
| <b>Slave mode</b>                                 |                  |         |          |        |      |
| BICK Period                                       |                  | tBCK    | 81       |        | ns   |
| BICK Pulse Width Low                              |                  | tBCKL   | 33       |        | ns   |
| Pulse Width High                                  |                  | tBCKH   | 33       |        | ns   |
| LRCK Edge to BICK "↑" (Note 11)                   |                  | tLRB    | 20       |        | ns   |
| BICK "↑" to LRCK Edge (Note 11)                   |                  | tBLR    | 20       |        | ns   |
| LRCK to SDTO (MSB) (Except I <sup>2</sup> S mode) |                  | tLRS    |          | 40     | ns   |
| BICK "↓" to SDTO                                  |                  | tBSD    |          | 40     | ns   |
| SDTI Hold Time                                    |                  | tSDH    | 20       |        | ns   |
| SDTI Setup Time                                   |                  | tSDS    | 20       |        | ns   |
| <b>Master mode</b>                                |                  |         |          |        |      |
| BICK Frequency                                    |                  | fBCK    |          | 64fs   | Hz   |
| BICK Duty   |                  | dBCK    |          | 50     | %    |
| BICK "↓" to LRCK                                  |                  | tMBLR   | -20      | 20     | ns   |
| BICK "↓" to SDTO                                  |                  | tBSD    | -20      | 20     | ns   |
| SDTI Hold Time                                    |                  | tSDH    | 20       |        | ns   |
| SDTI Setup Time                                   |                  | tSDS    | 20       |        | ns   |

Note 11. BICK rising edge must not occur at the same time as LRCK edge.

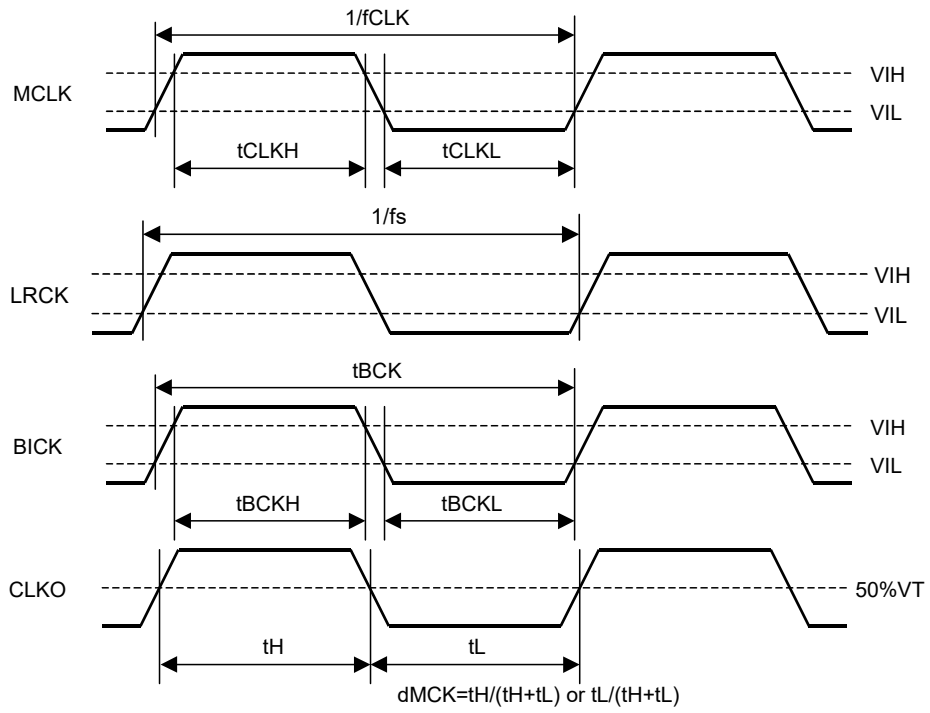


| Parameter                                    | Symbol | min | typ | max | Unit |
|--|--------|-----|-----|-----|------|
| <b>Control Interface Timing</b>              |        |     |     |     |      |
| <b>CIF="0"</b>                               |        |     |     |     |      |
| CCLK Period                                  | tCCK   | 200 |     |     | ns   |
| CCLK Pulse Width Low                         | tCCKL  | 80  |     |     | ns   |
| Pulse Width High                             | tCCKH  | 80  |     |     | ns   |
| CDTI Setup Time                              | tCDS   | 40  |     |     | ns   |
| CDTI Hold Time                               | tCDH   | 40  |     |     | ns   |
| CS "H" Time                                  | tCSW   | 150 |     |     | ns   |
| CS "L" Time                                  | tCSW   | 150 |     |     | ns   |
| CS "↑" to CCLK "↑"                           | tCSS   | 150 |     |     | ns   |
| CCLK "↑" to CS "↑"                           | tCSH   | 50  |     |     | ns   |
| <b>CIF="1"</b>                               |        |     |     |     |      |
| CCLK Period                                  | tCCK   | 200 |     |     | ns   |
| CCLK Pulse Width Low                         | tCCKL  | 80  |     |     | ns   |
| Pulse Width High                             | tCCKH  | 80  |     |     | ns   |
| CDTI Setup Time                              | tCDS   | 40  |     |     | ns   |
| CDTI Hold Time                               | tCDH   | 40  |     |     | ns   |
| CS "H" Time                                  | tCSW   | 150 |     |     | ns   |
| CS "L" Time                                  | tCSW   | 150 |     |     | ns   |
| CS "↓" to CCLK "↑"                           | tCSS   | 150 |     |     | ns   |
| CCLK "↑" to CS "↓"                           | tCSH   | 50  |     |     | ns   |
| <b>Reset Timing</b>                          |        |     |     |     |      |
| $\overline{\text{PD}}$ Pulse Width (Note 12) | tPD    | 150 |     |     | ns   |
| RSTAD "↑" to SDTO valid (Note 13)            | tPDV   |     | 516 |     | 1/fs |

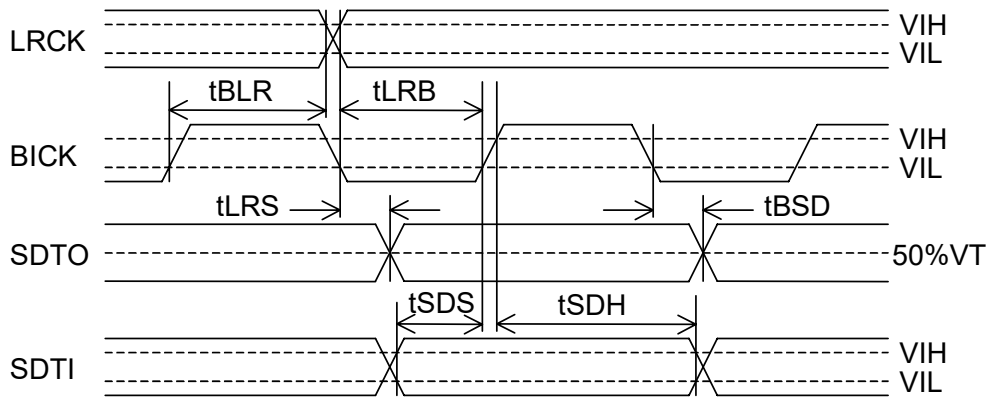
Note: 12. The AK4524 can be reset by bringing  $\overline{\text{PD}}$  "L".

13. These cycles are the number of LRCK rising from RSTAD bit.

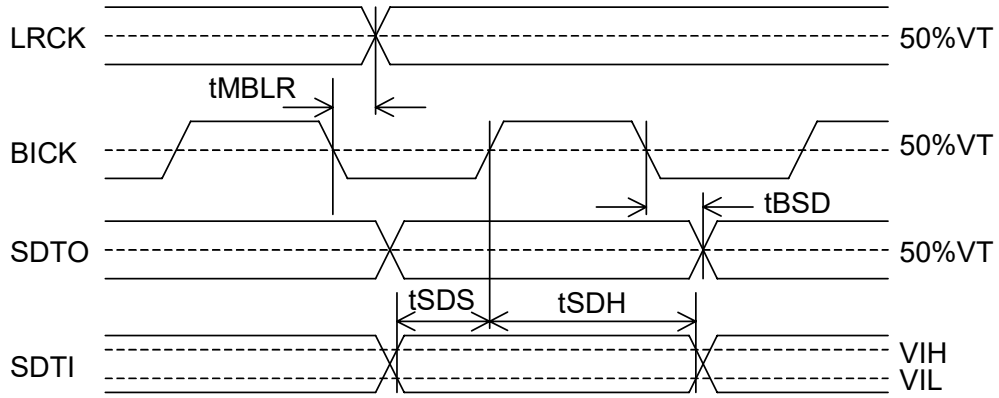
■ Timing Diagram



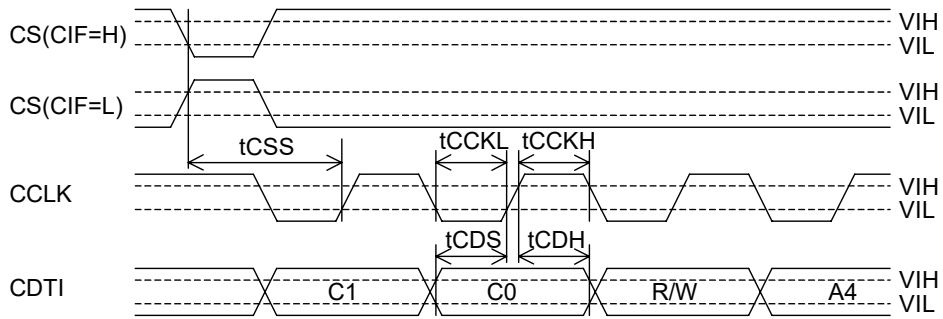
Clock Timing



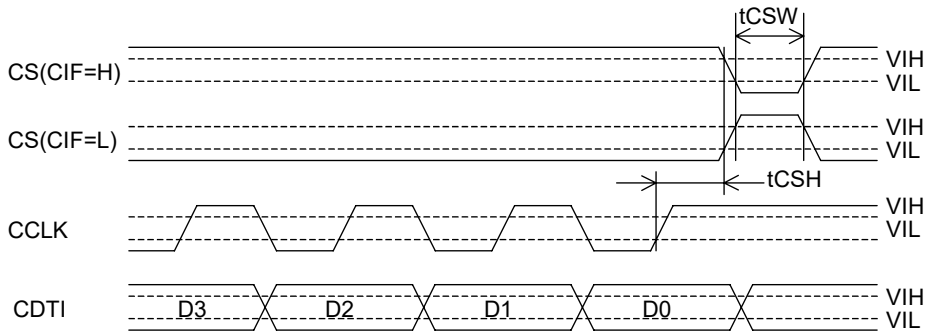
Audio Interface Timing (Slave mode)



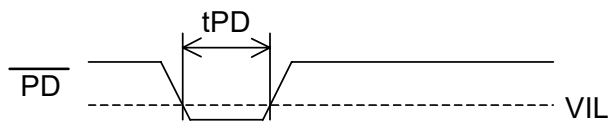
Audio Interface Timing (Master mode)



WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing

|                           |
|---------------------------|
| <b>OPERATION OVERVIEW</b> |
|---------------------------|

### ■ System Clock Input

The master clock (MCLK) can be either a crystal resonator placed across the XTI and XTO pin, or external clock input to the XTI pin with the XTO pin left floating. The master clock frequency can be selected by CMODE and CKS0-1 (Table 1). The sampling speed (normal speed mode, double speed mode or four times speed monitor mode) is selected by DFS0-1 (Table 2). The ADC is powered down during four times speed monitor mode. The frequency of the master clock output (CLKO) is the same as MCLK frequency and the output can be enabled or disabled by XTAL pin. When the CLKO output is not used externally, it should be disabled.

When using a crystal oscillator, external loading capacitors (between XTI/XTO and DGND) are required.

In slave mode, the LRCK clock input must be synchronized with MCLK, however the phase is not critical. Internal timing is synchronized to LRCK upon power-up. All external clocks must be present unless PD = "L" or all parts are powered down by control register, otherwise excessive current may result from abnormal operation of internal dynamic logic. In master mode, the clocks should be supplied by critical oscillation except for power down or the external clock (MCLK) should not be stopped.

| DFS1 | DFS0 | Sampling Rate              | Monitor mode      |
|------|------|----------------------------|-------------------|
| 0    | 0    | Normal speed               | -                 |
| 0    | 1    | Double speed               | -                 |
| 1    | 0    | 4 times speed (SDTO = "L") | Simple decimation |
| 1    | 1    | 4 times speed (SDTO = "L") | 2 tap filter      |

at reset

Table 1. Sampling Speed

| CMODE | CKS1 | CKS0 | MCLK                            |                                 |  |
|-------|------|------|---------------------------------|---------------------------------|--|
|       |      |      | Normal speed<br>(DFS1-0 = "00") | Double speed<br>(DFS1-0 = "01") | 4 times speed<br>(DFS1-0 = "10" or "11") |
| 0     | 0    | 0    | 256fs                           | N/A                             | N/A                                      |
| 0     | 0    | 1    | 512fs                           | 256fs                           | 128fs                                    |
| 0     | 1    | 0    | 1024fs                          | 512fs                           | 256fs                                    |
| 1     | 0    | 0    | 384fs                           | N/A                             | N/A                                      |
| 1     | 0    | 1    | 768fs                           | 384fs                           | 192fs                                    |

at reset

Table 2. Master Clock Frequency Select

|                    |            |           |                    |            |           |
|--------------------|------------|-----------|--------------------|------------|-----------|
| MCLK(Normal speed) | fs=44.1kHz | fs=48kHz  | MCLK(Double speed) | fs=88.2kHz | fs=96kHz  |
| 256fs              | 11.2896MHz | 12.288MHz | N/A                | N/A        | N/A       |
| 512fs              | 22.5792MHz | 24.576MHz | 256fs              | 22.5792MHz | 24.576MHz |
| 1024fs             | 45.1584MHz | 49.152MHz | 512fs              | 45.1584MHz | 49.152MHz |
| 384fs              | 16.9344MHz | 18.432MHz | N/A                | N/A        | N/A       |
| 768fs              | 33.8688MHz | 36.864MHz | 384fs              | 33.8688MHz | 36.864MHz |

|                     |             |           |
|---------------------|-------------|-----------|
| MCLK(4 times speed) | fs=176.4kHz | fs=192kHz |
| 128fs               | 22.5792MHz  | 24.576MHz |
| 256fs               | 45.1584MHz  | 49.152MHz |
| 192fs               | 33.8688MHz  | 36.864MHz |

Table 3. Master clock frequency

\* X'tal mode operates from 11.2896MHz to 24.576MHz.

\* The frequency over 24.576MHz supports only external clock mode.

■ Audio Serial Interface Format

Five serial modes selected by the DIF0 and DIF1 pins are supported as shown in Table 4. In all modes the serial data has MSB first, 2's compliment format. The SDTO is clocked out on the falling edge of BICK and the SDTI is latched on the rising edge. The interface supports both master mode and slave mode. In master mode, BICK and LRCK are outputs and the frequency of BICK is fixed to 64fs.

| Mode | DIF2 | DIF1 | DIF0 | SDTO                 | SDTI                 | LRCK | BICK   |
|------|------|------|------|----------------------|----------------------|------|--------|
| 0    | 0    | 0    | 0    | 24bit, MSB justified | 16bit, LSB justified | H/L  | ≥ 32fs |
| 1    | 0    | 0    | 1    | 24bit, MSB justified | 20bit, LSB justified | H/L  | ≥ 40fs |
| 2    | 0    | 1    | 0    | 24bit, MSB justified | 24bit, MSB justified | H/L  | ≥ 48fs |
| 3    | 0    | 1    | 1    | 24bit, IIS (I2S)     | 24bit, IIS (I2S)     | L/H  | ≥ 48fs |
| 4    | 1    | 0    | 0    | 24bit, MSB justified | 24bit, LSB justified | H/L  | ≥ 48fs |

at reset

Table 4. Audio data format

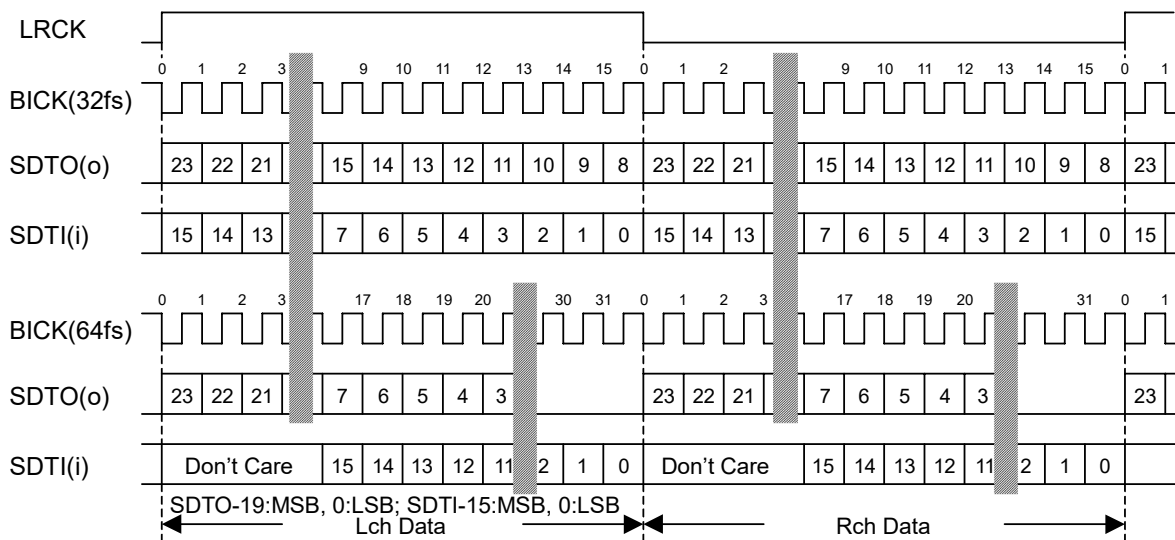


Figure 1. Mode 0 Timing

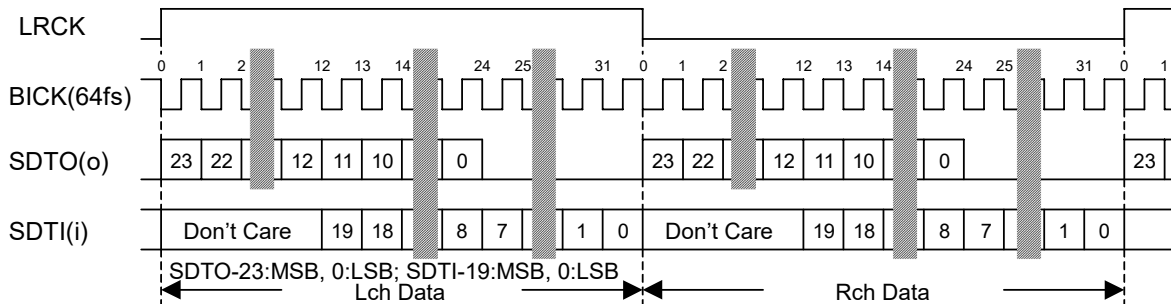


Figure 2. Mode 1 Timing

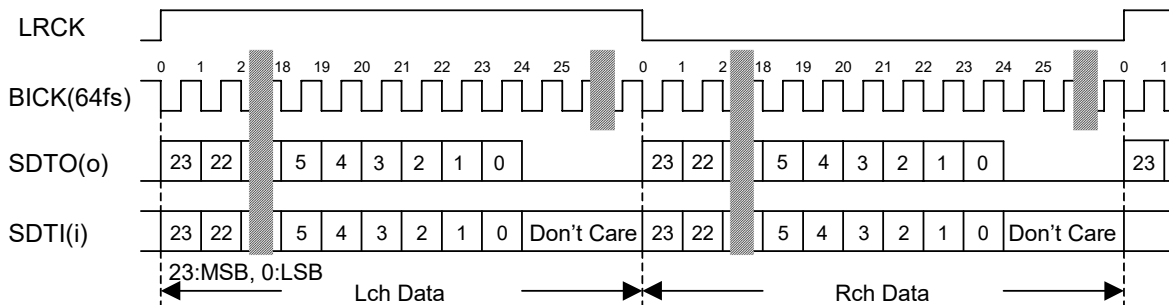


Figure 3. Mode 2 Timing

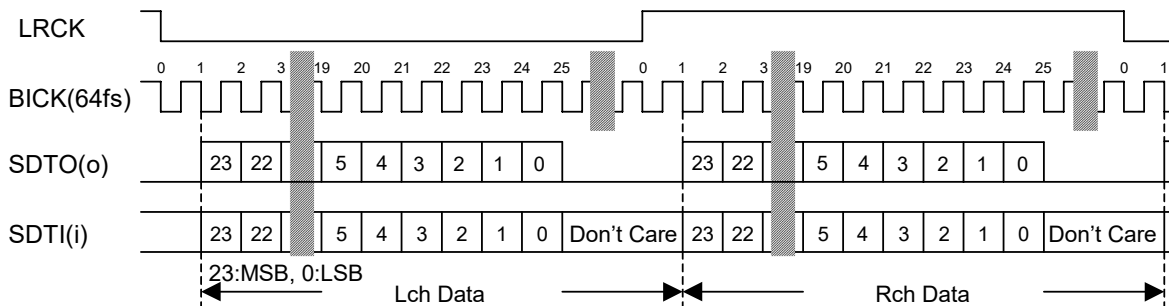


Figure 4. Mode 3 Timing

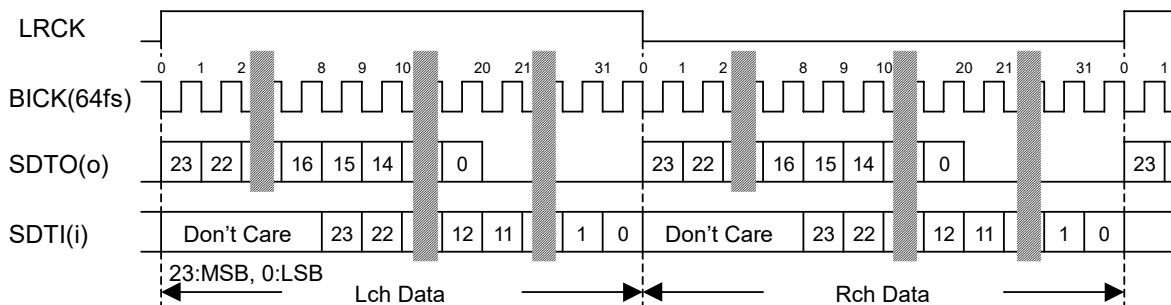


Figure 5. Mode 4 Timing

## ■ Input Volume

The AK4524 includes two channel independent analog volumes (IPGA) with 37 levels, 0.5dB step in front of ADC and digital volumes (IATT) with 128 levels (including MUTE) after ADC. The control data of both volumes are assigned in the same register address. When MSB of the register is “1”, the IPGA changes and the IATT changes at MSB “0”.

The IPGA is analog volumes and improves S/N compared with digital volume (Table 5). Level changes only occur during zero-crossings to minimize switching noise. Zero-crossing detection is performed channel independently. If there is no zero-crossings, then the level will change after a time-out. The time-out period ( $T_o$ ) scales with  $f_s$ . The periods of 256/ $f_s$ , 512/ $f_s$ , 1024/ $f_s$  and 2048/ $f_s$  are selectable by ZTM1-0 bits in normal speed mode. If new value is written to the IPGA register before IPGA changes by zero-crossing or time-out, the previous value becomes invalid. And then the timer (channel independent) for time-out is reset and the timer restarts for new IPGA value. Zero-crossing detection can be enabled by ZCEI in the control register.

The IATT is a pseudo-log volume linear-interpolated internally. When changing the level, the transition between ATT values has 8032 levels and is done by soft changes. Therefore, there is not any switching noise.

|                                 | Input Gain Setting |      |       |
|---------------------------------|--------------------|------|-------|
|                                 | 0dB                | +6dB | +18dB |
| $f_s=44.1\text{kHz}$ , A-weight | 100dB              | 98dB | 90dB  |

Table 5. IPGA+ADC S/N

| ZTM1 | ZTM0 | Normal speed | Double speed |
|------|------|--------------|--------------|
| 0    | 0    | 256          | 512          |
| 0    | 1    | 512          | 1024         |
| 1    | 0    | 1024         | 2048         |
| 1    | 1    | 2048         | 4096         |

at reset

Table 6. LRCK cycles for timeout period

## ■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancel. The cut-off frequency of the HPF is 0.9Hz at  $f_s=44.1\text{kHz}$  and also scales with sampling rate ( $f_s$ ).

## ■ Output Volume

The Ak4524 includes digital volumes (OATT) with 128 levels (including MUTE) which have the same architecture as IATT's in front of DAC. The OATT is a pseudo-log volume linear-interpolated internally. When changing the level, the transition between ATT values has 8032 levels and is done by soft changes. Therefore, there is not any switching noise.

### ■ De-emphasis Filter

The DAC includes the digital de-emphasis filter ( $t_c=50/15\mu s$ ) by IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz, 48kHz). This setting is done via contorl register. This filter is always OFF at double speed and four times speed modes.

| No | DEM1 | DEM0 | Mode    |
|----|------|------|---------|
| 0  | 0    | 0    | 44.1kHz |
| 1  | 0    | 1    | OFF     |
| 2  | 1    | 0    | 48kHz   |
| 3  | 1    | 1    | 32kHz   |

at reset

Table 7. De-emphasis control (DFS0=DFS1="0")

### ■ Soft Mute Operation

Soft mute operation is performed at digital domain. When SMUTE goes "H", the output signal is attenuated by  $-\infty$  during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.

Soft mute function is independent to output volume and cascade connected between both functions.

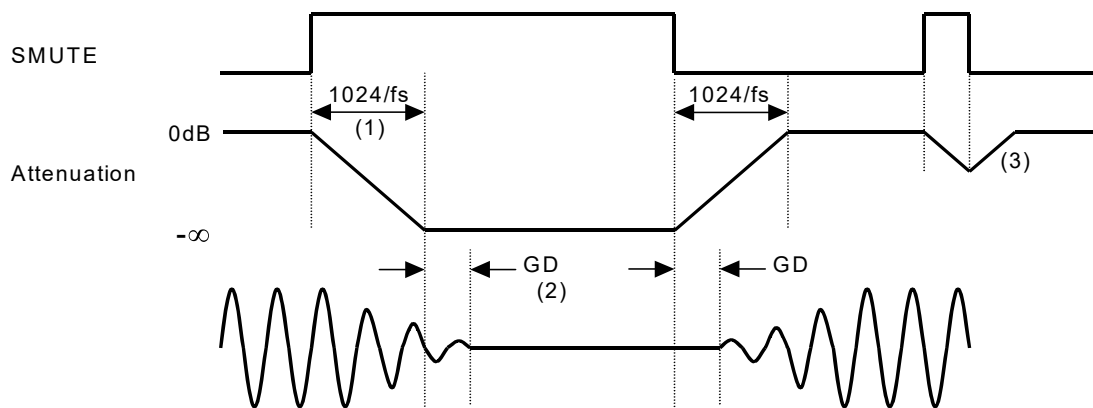


Figure 6. Soft Mute

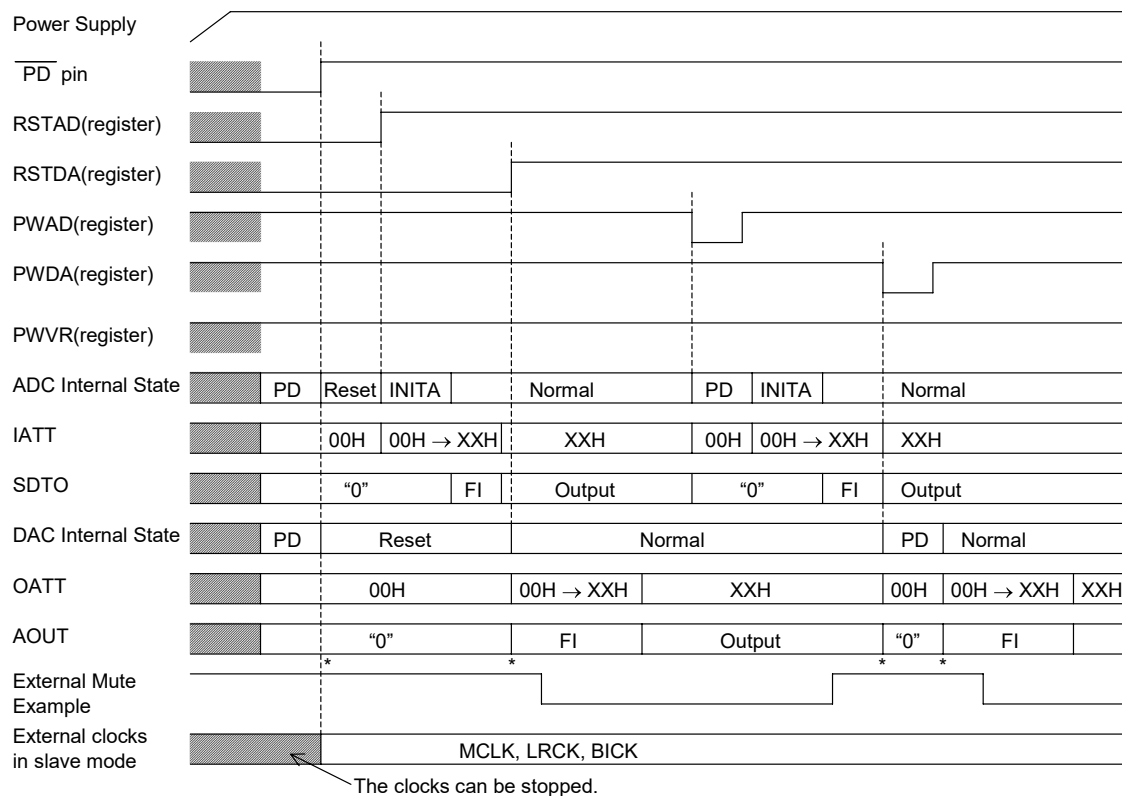
Notes:

- (1) The output signal is attenuated by  $-\infty$  during 1024 LRCK cycles ( $1024/f_s$ ).
- (2) Analog output corresponding to digital input has the group delay (GD).
- (3) If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.



■ Power Down & Reset

The ADC and DAC of AK4524 are placed in the power-down mode by bringing a power down pin,  $\overline{\text{PD}}$  “L” and each digital filter is also reset at the same time. The internal register values are initialized by  $\overline{\text{PD}}$  “L”. This reset should always be done after power-up. And then as both control registers of ADC and DAC go reset state (RSTAD=RSTDA=“0”), each register should be cancelled after doing the needed setting. In case of the ADC, an analog initialization cycle starts after exiting the power-down or reset state. Therefore, the output data, SDTO becomes available after 516 cycles of LRCK clock. This initialization cycle does not affect the DAC operation. Power down mode can be also controlled by the registers (PWAD, PWDA).



- INITA: Initializing period of ADC analog section (516/fs).
- PD: Power down state. The contents of all registers are hold.
- XXH: The current value in ATT register.
- FI: Fade in. After exiting power down and reset state, ATT value fades in.
- AOOUT: Some pop noise may occur at “\*”.

Figure 7. Reset & Power down sequence

### ■ Relationship between Clock Operation and Power-Down

XTALE pin controls the clock outputs. The operation in slave mode is shown Table 8. Table 9 shows the master mode operation. When a crystal oscillator is used, XTALE pin is set to “H”. XTALE pin should be “L” at external clock mode.

| Slave Mode     | XTALE=L  |  | XTALE=H   |   |
|----------------|--|--|---|---|
|                | $\overline{\text{PD}} = \text{H}$  | $\overline{\text{PD}} = \text{L}$  | $\overline{\text{PD}} = \text{H}$   | $\overline{\text{PD}} = \text{L}$   |
| XTAL mode      | Inhibit  | Inhibit  | Normal operation<br>XTAL = Oscillation<br>CLKO = Output<br>LRCK = Input<br>BICK = Input | Power down<br>XTAL = Oscillation<br>CLKO = Output<br>LRCK = Input<br>BICK = Input |
| EXT Clock mode | Normal operation<br>XTI = MCLK in<br>XTO = L<br>CLKO = L<br>LRCK = Input<br>BICK = Input | Shut off<br>XTI = MCLK in<br>XTO = L<br>CLKO = L<br>LRCK = Input<br>BICK = Input | Inhibit   | Inhibit   |

Table 8. Clock operation at slave mode ( $M/\overline{S} = \text{L}$ )

| Master Mode    | XTALE=L  |  | XTALE=H   |   |
|----------------|--|--|---|---|
|                | $\overline{\text{PD}} = \text{H}$  | $\overline{\text{PD}} = \text{L}$  | $\overline{\text{PD}} = \text{H}$   | $\overline{\text{PD}} = \text{L}$   |
| XTAL mode      | Inhibit  | Inhibit  | Normal operation<br>XTAL = Oscillation<br>CLKO = Output<br>LRCK = Output<br>BICK = Output | Power down<br>XTAL = Oscillation<br>CLKO = Output<br>LRCK = H<br>BICK = L |
| EXT Clock mode | Normal operation<br>XTI = MCLK in<br>XTO = L<br>CLKO = L<br>LRCK = Output<br>BICK = Output | Shut off<br>XTI = MCLK in<br>XTO = L<br>CLKO = L<br>LRCK = H<br>BICK = L | Inhibit   | Inhibit   |

Table 9. Clock operation at master mode ( $M/\overline{S} = \text{H}$ )

■ Serial Control Interface

The internal registers are written by the 3-wire  $\mu$ P interface pins: CS, CCLK, CDTI. The data on this interface consists of Chip address (2bits, C0/1) Read/Write (1bit), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Address and data is clocked in on the rising edge of CCLK. Data is latched after the 16th rising edge of CCLK, after a high-to-low transition of CS. The operation of the control serial port may be completely asynchronous with the audio sample rate. The maximum clock speed of the CCLK is 5MHz. The CS should be “H” or “L” if no access. The chip address is fixed to “10”. Writing is invalid for the access to the chip address except for “10”.  $\overline{PD}$  = “L” resets the registers to their default values.

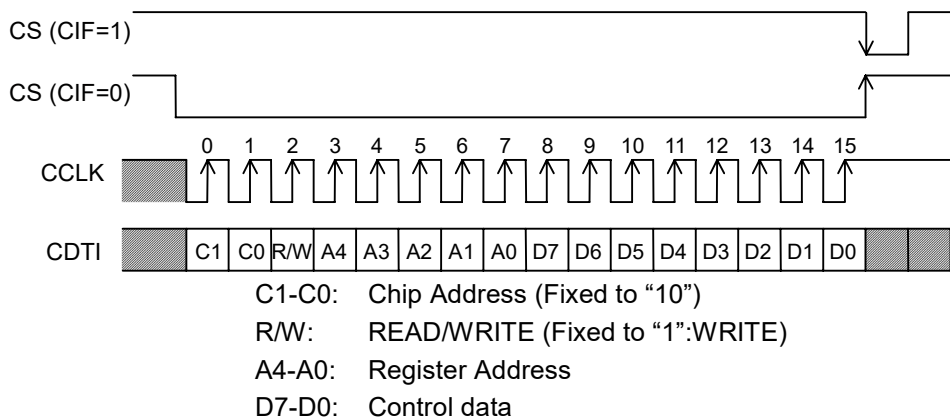


Figure 8. Control I/F Timing

\* READ command is not supported.

■ Register Map

| Addr | Register Name            | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|------|--------------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 00H  | Power Down Control       | 0     | 0     | 0     | 0     | 0     | PWVR  | PWAD  | PEDA  |
| 01H  | Reset Control            | 0     | 0     | 0     | 0     | 0     | 0     | RSTAD | RSTDA |
| 02H  | Clock and Format Control | DIF2  | DIF1  | DIF0  | CMODE | CKS1  | CKS0  | DFS1  | DFS0  |
| 03H  | Deem and Volume Control  | SMUTE | 0     | 0     | ZCEI  | ZTM1  | ZTM0  | DEM1  | DEM0  |
| 04H  | Lch IPGA Control         | IPGL7 | IPGL6 | IPGL5 | IPGL4 | IPGL3 | IPGL2 | IPGL1 | IPGL0 |
| 05H  | Rch IPGA Control         | IPGR7 | IPGR6 | IPGR5 | IPGR4 | IPGR3 | IPGR2 | IPGR1 | IPGR0 |
| 06H  | Lch ATT Control          | 0     | ATTL6 | ATTL5 | ATTL4 | ATTL3 | ATTL2 | ATTL1 | ATTL0 |
| 07H  | Rch ATT Control          | 0     | ATTR6 | ATTR5 | ATTR4 | ATTR3 | ATTR2 | ATTR1 | ATTR0 |

Note: For addresses from 08H to 1FH, data is not written.

$\overline{PD}$  = “L” resets the registers to their default values.

## ■ Control Register Setup Sequence

When  $\overline{\text{PD}}$  pin goes “L” to “H” upon power-up etc., the AK4524 should operate by the next sequence. In this case, all control registers are set to initial values and the AK4524 is in the reset state.

- (1) Set the clock mode and the audio data interface mode.
- (2) Cancel the reset state by setting RSTAD or RSTDA to “1”. Refer to Reset Control Register (01H).
- (3) ADC outputs and DAC outputs should be muted externally until cancelling each reset state. In master mode, there is a possibility the frequency and duty of LRCK and BICK outputs become an abnormal state.

The clock mode should be changed after setting RSTAD and RSTDA to “0”. At that time, ADC outputs and DAC outputs should be muted externally. In master mode, there is a possibility the frequency and duty of LRCK and BICK outputs become an abnormal state.

## ■ Register Definitions

| Addr | Register Name      | D7 | D6 | D5 | D4 | D3 | D2   | D1   | D0   |
|------|--------------------|----|----|----|----|----|------|------|------|
| 00H  | Power Down Control | 0  | 0  | 0  | 0  | 0  | PWVR | PWAD | PWDA |
|      | RESET              | 0  | 0  | 0  | 0  | 0  | 1    | 1    | 1    |

PWDA: DAC power down

0: Power down

1: Power up

Only DAC section is powered down by “0” and then the AOUTs go Hi-Z immediately. The OATTs also go “00H”. But the contents of all register are not initialized and enabled to write to the registers. After exiting the power down mode, the OATTs fade in the setting value of the control register (06H & 07H). The analog outputs should be muted externally as some pop noise may occur when entering to and exiting from this mode.

PWAD: ADC power down

0: Power down

1: Power up

Only ADC section is powered down by “0” and then the SDTO goes “L” immediately. The IPGAs also go “00H”. But the contents of all register are not initialized and enabled to write to the registers. After exiting the power down mode, the IPGAs fade in the setting value of the control register (04H & 05H). At that time, ADCs output “0” during first 516 LRCK cycles.

PWVR: Vref power down

0: Power down

1: Power up

All sections are powered down by “0” and then both ADC and DAC do not operate. The contents of all register are not initialized and enabled to write to the registers. When PWAD and PWDA go “0” and PWVR goes “1”, only VREF section can be powered up.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1    | D0    |
|------|---------------|----|----|----|----|----|----|-------|-------|
| 01H  | Reset Control | 0  | 0  | 0  | 0  | 0  | 0  | RSTAD | RSTDA |
|      | RESET         | 0  | 0  | 0  | 0  | 0  | 0  | 0     | 0     |

RSTDA: DAC reset

0: Reset

1: Normal Operation

The internal timing is reset by “0” and then the AOUTs go VCOM voltage immediately. The OATTs also go “00H”. But the contents of all register are not initialized and enabled to write to the registers. After exiting the power down mode, the OATTs fade in the setting value of the control register (06H & 07H). The analog outputs should be muted externally as some pop noise may occur when entering to and exiting from this mode.

RSTDA: ADC reset

0: Reset

1: Normal Operation

The internal timing is reset by “0” and then SDTO goes “L” immediately. The IPGAs also go “00H”. But the contents of all register are not initialized and enabled to write to the register. After exiting the power down mode, the IPGAs fade in the setting value of the control register (04H & 05H). At that time, ADCs output “0” during first 516 LRCK cycles.

| Addr | Register Name            | D7   | D6   | D5   | D4    | D3   | D2   | D1   | D0   |
|------|--------------------------|------|------|------|-------|------|------|------|------|
| 02H  | Clock and Format Control | DIF2 | DIF1 | DIF0 | CMODE | CKS1 | CKS0 | DFS1 | DFS0 |
|      | RESET                    | 0    | 1    | 0    | 0     | 0    | 0    | 0    | 0    |

DFS1-0: Sampling Speed Control (see Table 2)

Initial: Normal speed

CMODE, CKS1-0: Master Clock Frequency Select (see Table 1)

Initial: 256fs

DIF2-0: Audio data interface modes (see Table 4)

000: Mode 0

001: Mode 1

010: Mode 2

011: Mode 3

100: Mode 4

Initial: 24bit MSB justified for both ADC and DAC

| Addr | Register Name           | D7    | D6 | D5 | D4   | D3   | D2   | D1   | D0   |
|------|-------------------------|-------|----|----|------|------|------|------|------|
| 03H  | Deem and Volume Control | SMUTE | 0  | 0  | ZCEI | ZTM1 | ZTM0 | DEM1 | DEM0 |
|      | RESET                   | 0     | 0  | 0  | 1    | 1    | 0    | 0    | 1    |

DEM1-0: De-emphasis response (see Table 7)

00: 44.1kHz

01: OFF

10: 48kHz

11: 32kHz

Initial: OFF

ZTM1-0: Zero crossing time out period select (see Table 6)

Initial: 1024fs

ZCEI: ADC IPGA Zero crossing enable

0: Input PGA gain changes occur immediately

1: Input PGA gain changes occur only on zero-crossing or after timeout.

Initial: 1 (Enable)

SMUTE: DAC Input Soft Mute control

0: Normal operation

1: DAC outputs soft-muted

The soft mute is independent of the output ATT and performed digitally.

| Addr | Register Name    | D7    | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|------|------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 04H  | Lch IPGA Control | IPGL7 | IPGL6 | IPGL5 | IPGL4 | IPGL3 | IPGL2 | IPGL1 | IPGL0 |
| 05H  | Rch IPGA Control | IPGR7 | IPGR6 | IPGR5 | IPGR4 | IPGR3 | IPGR2 | IPGR1 | IPGR0 |
|      | RESET            | 0     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

IPGL/R7-0: ADC Input Gain Level

Refer to Table 10

Initial: 7FH (0dB)

Digital ATT with 128 levels operates when writing data of less than 7FH. This ATT is a linear ATT with 8032 levels internally and these levels are assigned to pseudo-log data with 128 levels. The transition between ATT values has 8032 levels and is done by soft changes. For example, when ATT changes from 127 to 126, the internal ATT value decreases from 8031 to 7775 one by one every fs cycles. It takes 8031 cycles (182ms@fs=44.1kHz) from 127 to 0 (Mute).

The IPGAs are set to "00H" when  $\overline{\text{PD}}$  pin goes "L". After returning to "H", the IPGAs fade in the initial value, "7FH" by 8031 cycles.

The IPGAs are set to "00H" when PWAD goes "0". After returning to "1", the IPGAs fade in the current value. But the ADCs output "0" during first 516 cycles.

The IPAGs are set to "00H" when RSTAD goes "0". After returning to "1", the IPGAs fade in the current value. But the ADCs output "0" during first 516 cycles.

| Data      | Internal (DATT) | Gain (dB) | Step width (dB) |  |
|-----------|-----------------|-----------|-----------------|--|
| 255 - 165 | -               | +18       | -               | <b>IPGA</b><br>Analog volume with 0.5dB step |
| 164       | -               | +18       | -               |  |
| 163       | -               | +17.5     | 0.5             |  |
| 162       | -               | +17       | 0.5             |  |
| :         | -               | :         | 0.5             |  |
| 130       | -               | +1.0      | 0.5             |  |
| 129       | -               | +0.5      | 0.5             |  |
| 128       | -               | 0         | 0.5             |  |
| 127       | 8031            | 0         | -               |  |
| 126       | 7775            | -0.28     | 0.28            |  |
| 125       | 7519            | -0.57     | 0.29            |  |
| :         | :               | :         | :               |  |
| 112       | 4191            | -5.65     | 0.51            |  |
| 111       | 3999            | -6.06     | 0.41            |  |
| 110       | 3871            | -6.34     | 0.28            |  |
| :         | :               | :         | :               |  |
| 96        | 2079            | -11.74    | 0.52            |  |
| 95        | 1983            | -12.15    | 0.41            |  |
| 94        | 1919            | -12.43    | 0.28            |  |
| :         | :               | :         | :               |  |
| 80        | 1023            | -17.90    | 0.53            |  |
| 79        | 975             | -18.32    | 0.42            |  |
| 78        | 943             | -18.61    | 0.29            |  |
| :         | :               | :         | :               |  |
| 64        | 495             | -24.20    | 0.54            |  |
| 63        | 471             | -24.64    | 0.43            |  |
| 62        | 455             | -24.94    | 0.30            |  |
| :         | :               | :         | :               |  |
| 48        | 231             | -30.82    | 0.58            |  |
| 47        | 219             | -31.29    | 0.46            |  |
| 46        | 211             | -31.61    | 0.32            |  |
| :         | :               | :         | :               |  |
| 32        | 99              | -38.18    | 0.67            |  |
| 31        | 93              | -38.73    | 0.54            |  |
| 30        | 89              | -39.11    | 0.38            |  |
| :         | :               | :         | :               |  |
| 16        | 33              | -47.73    | 0.99            |  |
| 15        | 30              | -48.55    | 0.83            |  |
| 14        | 28              | -49.15    | 0.60            |  |
| :         | :               | :         | :               |  |
| 5         | 10              | -58.10    | 1.58            |  |
| 4         | 8               | -60.03    | 1.94            |  |
| 3         | 6               | -62.53    | 2.50            |  |
| 2         | 4               | -66.05    | 3.52            |  |
| 1         | 2               | -72.07    | 6.02            |  |
| 0         | 0               | MUTE      |                 |  |

Table 10. IPGA code table

| Addr  | Register Name    | D7 | D6    | D5    | D4    | D3    | D2    | D1    | D0    |
|-------|------------------|----|-------|-------|-------|-------|-------|-------|-------|
| 06H   | Lch OATT Control | 0  | ATTL6 | ATTL5 | ATTL4 | ATTL3 | ATTL2 | ATTL1 | ATTL0 |
| 07H   | Rch OATT Control | 0  | ATTR6 | ATTR5 | ATTR4 | ATTR3 | ATTR2 | ATTR1 | ATTR0 |
| RESET |                  | 0  | 1     | 1     | 1     | 1     | 1     | 1     | 1     |

ATTL/R6-0: DAC ATT Level

Refer to Table 11

Initial: 7FH (0dB)

The AK4524 includes digital ATT with 128 levels equivalent to ADC's.

The OATTs are set to "00H" when  $\overline{\text{PD}}$  pin goes "L". After returning to "H", the OATTs fade in the initial value, "7FH" by 8031 cycles.

The OATTs are set to "00H" when PWDA goes "0". After returning to "1", the OATTs fade in the current value.

The OATTs are set to "00H" when RSTDA goes "0". After returning to "1", the OATTs fade in the current Value.

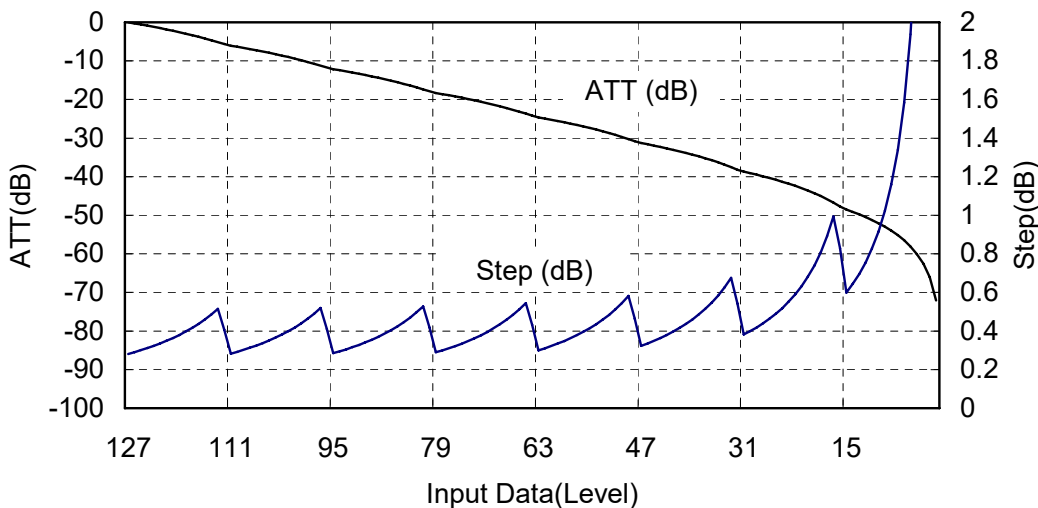


Figure 9. ATT characteristics

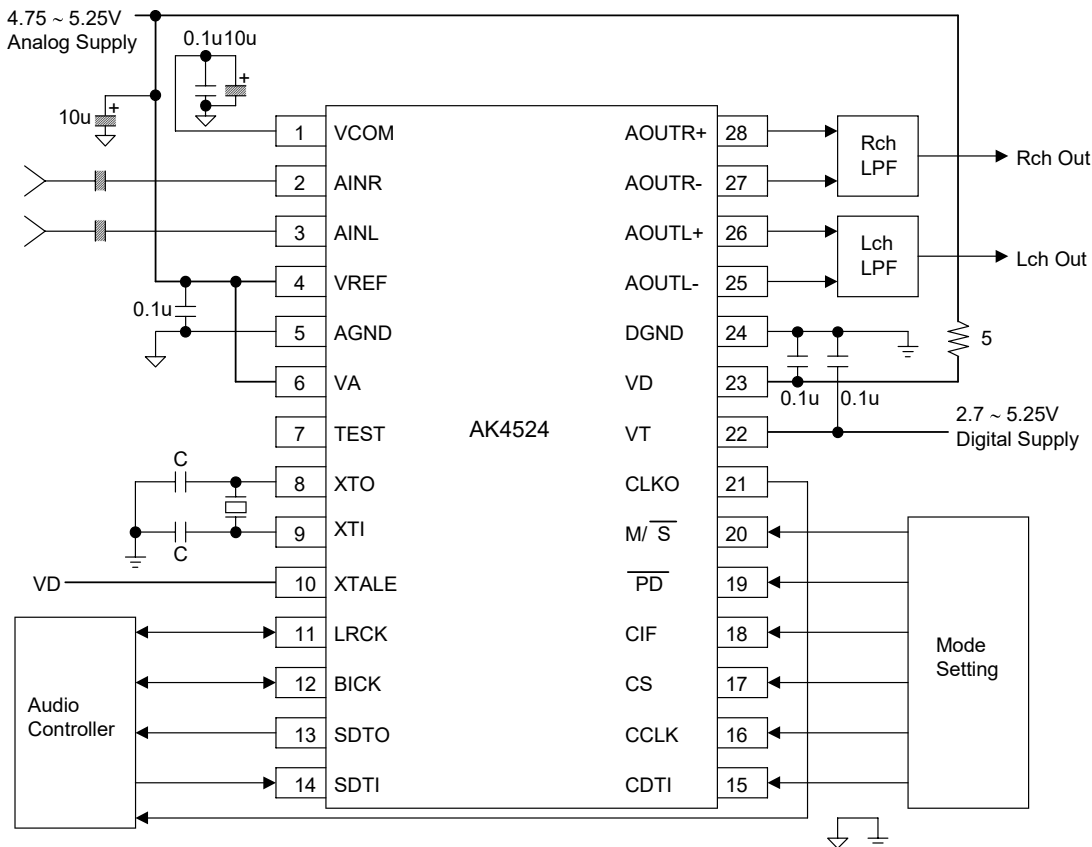


| Data | Internal (DATT) | Gain (dB) | Step width (dB) |   |
|------|-----------------|-----------|-----------------|---|
| 127  | 8031            | 0         | -               | <p style="text-align: center;"><b>OATT</b></p> <p>External 128 levels are converted to internal 8032 linear levels of DATT. Internal DATT soft-changes between DATAs.</p> <p><math>DATT=2^m \times (2 \times l + 33) - 33</math></p> <p>m: MSB 3-bits of data<br/>l: LSB 4-bits of data</p> |
| 126  | 7775            | -0.28     | 0.28            |   |
| 125  | 7519            | -0.57     | 0.29            |   |
| :    | :               | :         | :               |   |
| 112  | 4191            | -5.65     | 0.51            |   |
| 111  | 3999            | -6.06     | 0.41            |   |
| 110  | 3871            | -6.34     | 0.28            |   |
| :    | :               | :         | :               |   |
| 96   | 2079            | -11.74    | 0.52            |   |
| 95   | 1983            | -12.15    | 0.41            |   |
| 94   | 1919            | -12.43    | 0.28            |   |
| :    | :               | :         | :               |   |
| 80   | 1023            | -17.90    | 0.53            |   |
| 79   | 975             | -18.32    | 0.42            |   |
| 78   | 943             | -18.61    | 0.29            |   |
| :    | :               | :         | :               |   |
| 64   | 495             | -24.20    | 0.54            |   |
| 63   | 471             | -24.64    | 0.43            |   |
| 62   | 455             | -24.94    | 0.30            |   |
| :    | :               | :         | :               |   |
| 48   | 231             | -30.82    | 0.58            |   |
| 47   | 219             | -31.29    | 0.46            |   |
| 46   | 211             | -31.61    | 0.32            |   |
| :    | :               | :         | :               |   |
| 32   | 99              | -38.18    | 0.67            |   |
| 31   | 93              | -38.73    | 0.54            |   |
| 30   | 89              | -39.11    | 0.38            |   |
| :    | :               | :         | :               |   |
| 16   | 33              | -47.73    | 0.99            |   |
| 15   | 30              | -48.55    | 0.83            |   |
| 14   | 28              | -49.15    | 0.60            |   |
| :    | :               | :         | :               |   |
| 5    | 10              | -58.10    | 1.58            |   |
| 4    | 8               | -60.03    | 1.94            |   |
| 3    | 6               | -62.53    | 2.50            |   |
| 2    | 4               | -66.05    | 3.52            |   |
| 1    | 2               | -72.07    | 6.02            |   |
| 0    | 0               | MUTE      |                 |   |

Table 11. OATT code table

**SYSTEM DESIGN**

Figure 10 & Figure 11 show the system connection diagram. This is an example which the AK4524 operates at X'tal mode. In case of external clock mode, please refer to Figure 11. An evaluation board (AKD4524) is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



Notes:

- X'tal Oscillation circuit is specified from 11.2896MHz to 24.576MHz.
- AGND and DGND of AK4524 should be distributed separately from the ground of external controller etc.
- When AOUT+/- drives some capacitive load, some resistor should be added in series between AOUT+/- and capacitive load.
- All input pins except pull-down pin (TEST) should not be left floating.

Figure 10. Typical Connection Diagram (X'tal mode)

| X'tal Frequency                  | C    |
|----------------------------------|------|
| 11.2896MHz, 12.288MHz            | 33pF |
| 16.384MHz, 16.9344MHz, 18.432MHz | 15pF |
| 22.5792MHz, 24.576MHz            | 10pF |

Table 12. External capacitance example for X'tal  
(Please contact X'tal oscillator manufacturer)

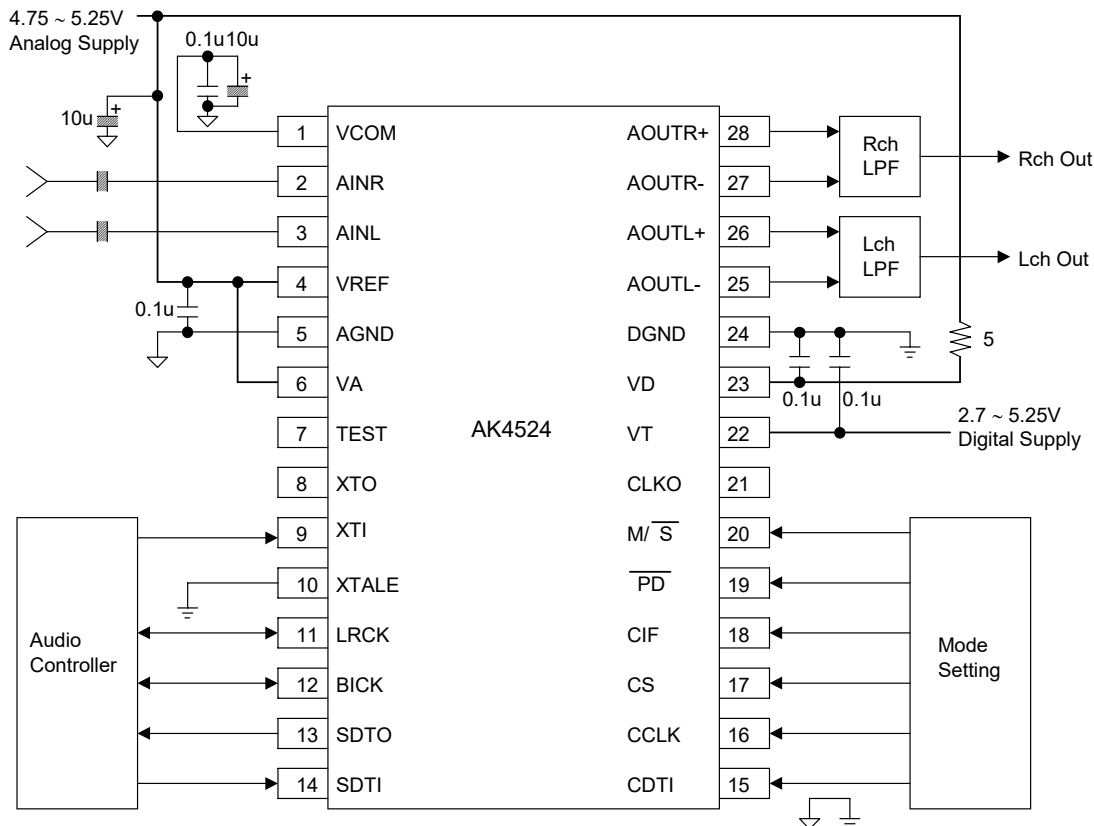


Figure 11. Typical Connection Diagram (EXT clock mode)

### 1. Grounding and Power Supply Decoupling

The AK4524 requires careful attention to power supply and grounding arrangements. VA and VD are usually supplied from analog supply in system. Alternatively if VA and VD are supplied separately, the power up sequence is taken care. VT is a power supply pin to interface with the external ICs and is supplied from digital supply in system. AGND and DGND of the AK4524 should be connected to analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4524 as possible, with the small value ceramic capacitor being the nearest.

### 2. Voltage Reference

The differential voltage between VREF and AGND sets the analog input/output range. VREF pin is normally connected to VA with a 0.1uF ceramic capacitor. VCOM is a signal ground of this chip. An electrolytic capacitor 10uF parallel with a 0.1uF ceramic capacitor attached to VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from the VREF and VCOM pins in order to avoid unwanted coupling into the AK4524.

### 3. Analog Inputs

The IPGA inputs are single-ended and the input resistance  $5k\Omega$  (min). The input signal range scales with the VREF voltage and nominally  $0.58 \times VREF$  Vpp centered in the internal common voltage (about VA/2). Usually the input signal is AC coupled with capacitor. The cut-off frequency is  $f_c = (1/2\pi RC)$ . The AK4524 can accept input voltages from AGND to VA. The ADC output data format is 2's complement. The output code is 7FFFFFFH(@24bit) for input above a positive full scale and 800000H(@24bit) for input below a negative full scale. The ideal code is 000000H(@24bit) with no input signal. The DC offset including ADC own DC offset removed by the internal HPF.

The AK4524 samples the analog inputs at 64fs. The digital filter rejects noise above the stopband except for multiples of 64fs. The AK4524 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

### 4. Analog Outputs

The analog outputs are full differential outputs and nominally  $0.54 \times VREF$  Vpp centered in the internal common voltage (about VA/2). The differential outputs are summed externally,  $V_{out} = (AOUT+) - (AOUT-)$  between AOUT+ and AOUT-. If the summing gain is 1, the output range is 5.4Vpp (typ@VREF=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFFH(@24bit) and a negative full scale for 800000H(@24bit). The ideal AOUT is 0V for 000000H(@24bit).

The internal switched-capacitor filter and the external LPF attenuate the noise generated by the delta-sigma modulator beyond the audio passband.

Differential outputs can eliminate any DC offset on analog outputs without using capacitors. Figure 12 to Figure 14 show the example of external op-amp circuit summing the differential outputs.

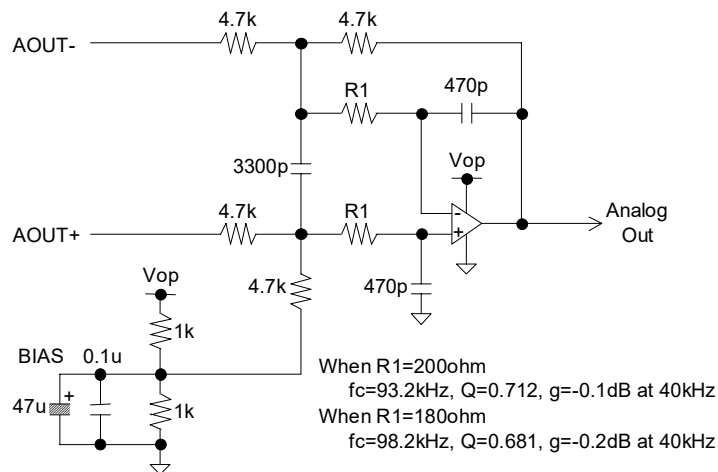


Figure 12. External 2nd order LPF Example (using single supply op-amp)

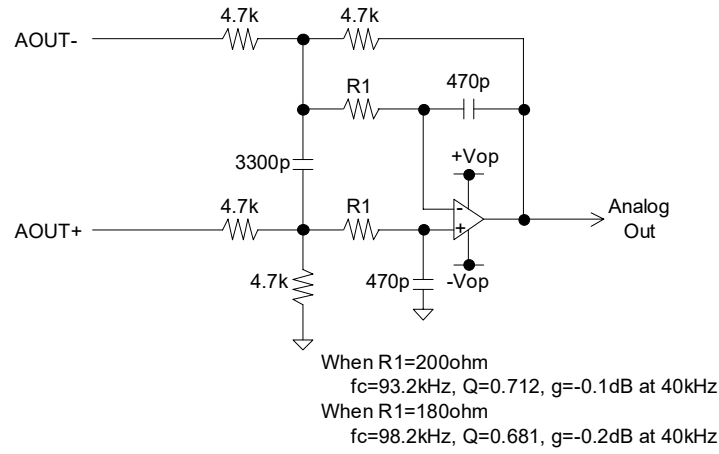


Figure 13. External 2nd order LPF Example (using dual supply op-amp)

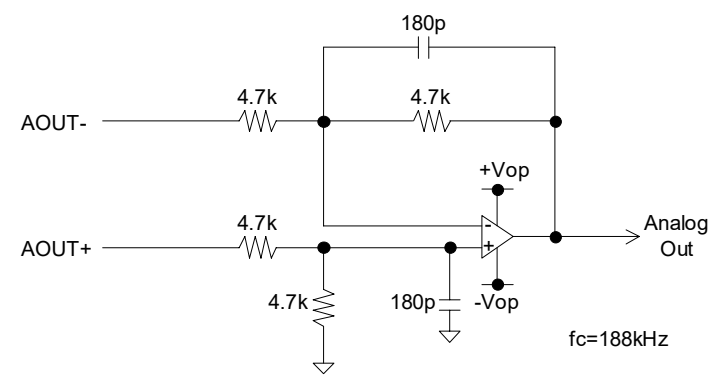


Figure 14. External low cost 1st order LPF Example (using dual supply op-amp)

■ Peripheral I/F Example

The digital inputs of the AK4524 are TTL inputs and can accept the signal of device with a nominal 3V supply. The digital output can interface with the peripheral device with a nominal 3V supply when the VT supply operates at a nominal 3V supply.

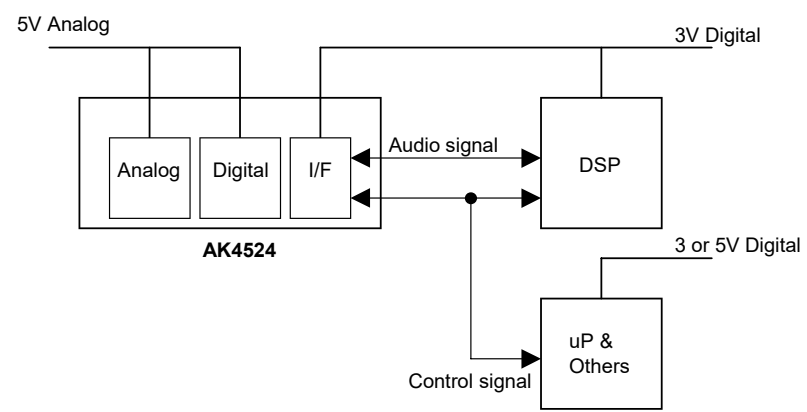
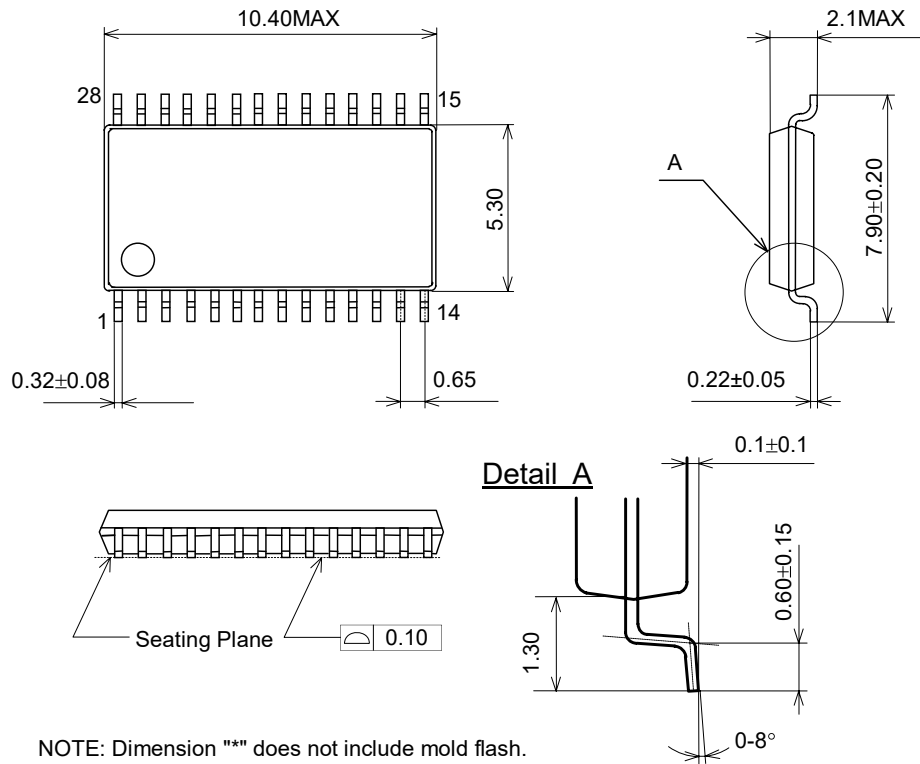


Figure 15. Power supply connection example

**PACKAGE**

28pin SSOP (Unit: mm)

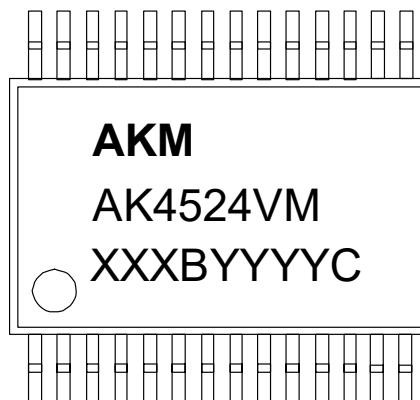


NOTE: Dimension "\*" does not include mold flash.

■ Package & Lead frame material

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder plate

|                |
|----------------|
| <b>MARKING</b> |
|----------------|



XXXXBYYYYC: Date code identifier

XXXXB: Lot number (X: Digit number, B: Alpha character)  
 YYYYYC: Assembly date (Y: Digit number, C: Alpha character)

|                         |
|-------------------------|
| <b>REVISION HISTORY</b> |
|-------------------------|

| Date (Y/M/D)                        | Revision                      | Reason                              | Page         | Contents  |
|-------------------------------------|-------------------------------|-------------------------------------|--------------|---|
| 98/12/05                            | 00                            | First Edition                       |              |   |
| 99/05/25                            | 01                            | Error Correction                    | 19, 24       | Addr:07H, D5: ATTL5 → ATTR5   |
|                                     |                               |                                     | 28           | 3. Analog Input, Line 2: Usually the signal input ~   |
|                                     |                               |                                     | 31           | “INPORTANT NOTICE” was added.   |
| 99/11/17                            | 02                            | Specification Change                | 3, 5         | Ambient Temperature: -10 ~ 70°C → -20 ~ 85°C  |
|                                     |                               | Error Correction                    | 10           | Timing Diagram, Clock Timing  |
|                                     |                               |                                     |              | MCLK Input Level: 1.5V → VIL, VIH   |
|                                     |                               |                                     |              | CLKO Output Level: VIH, VIL → 50%VT   |
|                                     |                               |                                     |              | Timing Diagram, Audio Interface Timing (Slave)  |
|                                     |                               | SDTO Output Level: VIH, VIL → 50%VT |              |   |
|                                     |                               | Description Change                  | 11           | Timing Diagram, Audio Interface Timing (Master)   |
| LRCK Output Level: VIH, VIL → 50%VT |                               |                                     |              |   |
| BICK Output Level: VIH, VIL → 50%VT |                               |                                     |              |   |
| SDTO Output Level: VIH, VIL → 50%VT |                               |                                     |              |   |
| 12, 13, 15                          | System Clock Table 1, 2, 3, 6 |                                     |              |   |
| 04/01/07                            | 03                            | Error Correction                    | 7            | FILTER CHARACTERISTICS<br>ADC Passband 22.20 → 20.20  |
| 12/01/12                            | 04                            | Specification Change                | 1, 3, 30, 31 | AK4524VF was deleted. (28pin VSOP)<br>AK4524VM was added. (28pin SSOP)<br>Ordering Guide was changed.<br>PACKAGE was changed.<br>MARKING was changed. |
| 13/03/08                            | 05                            | Error Correction                    | 31           | MARKING<br>Marking drawing was changed.   |

**IMPORTANT NOTICE**

0. Asahi Kasei Microdevices Corporation (“AKM”) reserves the right to make changes to the information contained in this document without notice. When you consider any use or application of AKM product stipulated in this document (“Product”), please make inquiries the sales office of AKM or authorized distributors as to current status of the Products.
1. All information included in this document are provided only to illustrate the operation and application examples of AKM Products. AKM neither makes warranties or representations with respect to the accuracy or completeness of the information contained in this document nor grants any license to any intellectual property rights or any other rights of AKM or any third party with respect to the information in this document. You are fully responsible for use of such information contained in this document in your product design or applications. **AKM ASSUMES NO LIABILITY FOR ANY LOSSES INCURRED BY YOU OR THIRD PARTIES ARISING FROM THE USE OF SUCH INFORMATION IN YOUR PRODUCT DESIGN OR APPLICATIONS.**
2. The Product is neither intended nor warranted for use in equipment or systems that require extraordinarily high levels of quality and/or reliability and/or a malfunction or failure of which may cause loss of human life, bodily injury, serious property damage or serious public impact, including but not limited to, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. Do not use Product for the above use unless specifically agreed by AKM in writing.
3. Though AKM works continually to improve the Product’s quality and reliability, you are responsible for complying with safety standards and for providing adequate designs and safeguards for your hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of the Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption.
4. Do not use or otherwise make available the Product or related technology or any information contained in this document for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). When exporting the Products or related technology or any information contained in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. The Products and related technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
5. Please contact AKM sales representative for details as to environmental matters such as the RoHS compatibility of the Product. Please use the Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. AKM assumes no liability for damages or losses occurring as a result of noncompliance with applicable laws and regulations.
6. Resale of the Product with provisions different from the statement and/or technical features set forth in this document shall immediately void any warranty granted by AKM for the Product and shall not create or extend in any manner whatsoever, any liability of AKM.
7. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of AKM.