ATP UHS-I microSDHC/microSDXC Memory Card Specification High Endurance S750 Series

Datasheet

Version 2.1

P/N

AF8GUD4A-EBAXM/ AF8GUD4A-EBAIM

AF16GUD4A-EBAXM/ AF16GUD4A-EBAIM

AF32GUD4A-EBAXM/ AF32GUD4A-EBAIM

AF64GUD4A-EBAXM/ AF64GUD4A-EBAIM

CONTENT

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Revision History

Date	Version	Changes compared to previous issue
Apr. 16th, 2019	1.0	- Official release of 1st Version with completely specification.
Jul. 25th, 2019	1.1	- Update Performance Information. - Update Voltage Information.
Jun. 14th, 2021	1.2	- Add alternative Solution
Jul. 04th, 2022	1.3	- Add UKCA certification into backside marking - Update TBW
Jul. 05th, 2022	2.1	- New solution release with LDPC controller High Endurance S750 series - Update main features (page 5) and Chapter 2 product features

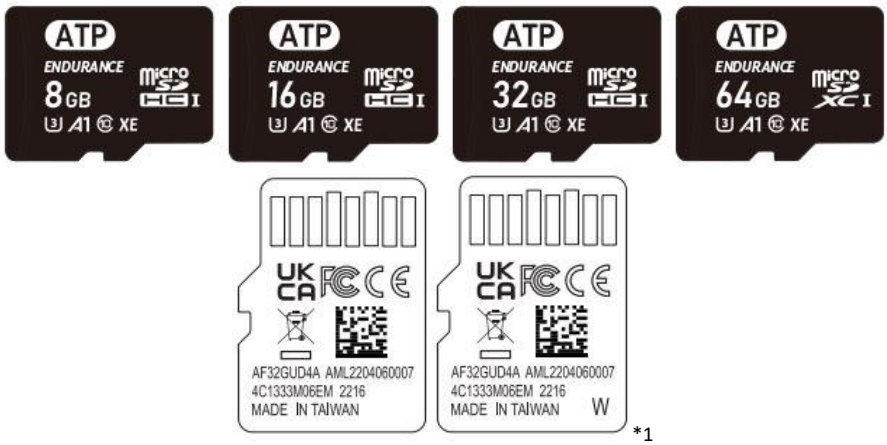
1.0 Product Specification

Main Features:

- Compliant with SD Specification version 6.10
- LDPC Controller
- SiP (System-In-Package) process
- Water proof, Dust proof and ESD Resistant
- High Endurance – Advanced Static/Dynamic Wear-Leveling
- High Endurance – 5K P/E cycles per block, low WAF
- Low Latency
- Data Integrity – Read retry & Auto-Read-Calibration (ARC)
- Data Integrity – Read Disturb Protector
- Data Integrity – Power failure protection
- Analysis method – SD Life monitor tool
- Analysis method – For SiP memory cards
- Non-CPRM support by default
- RoHS compliant
- CE & FCC & UKCA certification
- Controlled BOM
- Customized service: adjustable CID registers, firmware & setting and logo by projects

1.1 Product Image

Figure 1-1: ATP Product Image (For Reference)

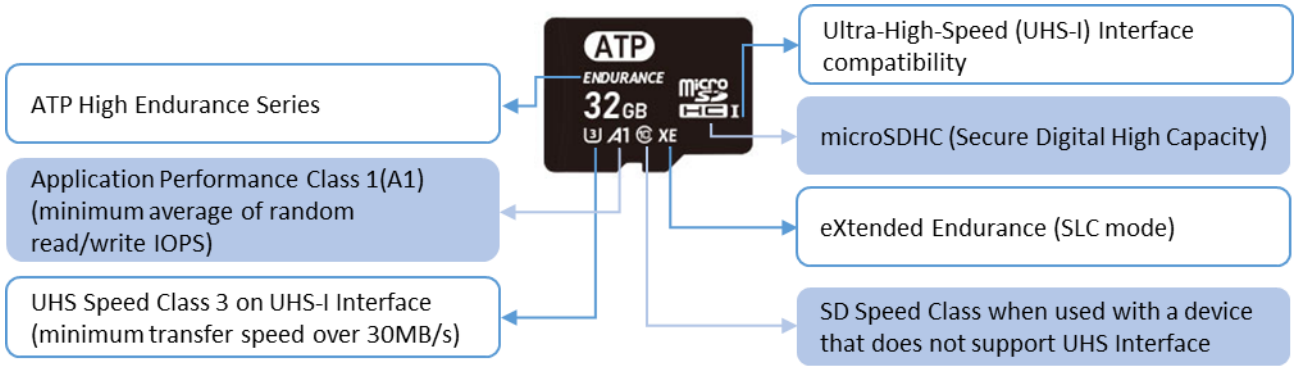


*1 W-marking represented W-Temp Series solution

1.2 Capacity

Table 1-2: Capacity Settings

ATP Part Number	Capacity
AF8GUD4A-EBAXM/ AF8GUD4A-EBAIM	8GB SDHC
AF16GUD4A-EBAXM/ AF16GUD4A-EBAIM	16GB SDHC
AF32GUD4A-EBAXM/ AF32GUD4A-EBAIM	32GB SDHC
AF64GUD4A-EBAXM/ AF64GUD4A-EBAIM	64GB SDXC



1.3 Environment Specifications

Table 1-3-1: Environment Specification

Type		Standard
Temperature	Operating	-25°C to 85°C -40°C to 85°C (W-Temp Solution)
	Non-Operating	-55°C to 90°C
Humidity	Operating	8% ~ 95% relative humidity , non-condensing
	Non-Operating	
Random Vibration Test	Non-Operating	10 ~ 2000Hz, 6Grms, 30min per axis
Bend Test	Non-Operating	10N to the center of the card, total 5 cycles
Torque Test	Non-Operating	0.15N-m or +/-2.5°
Salt Spray Test (MIL-STD-883G Method1009.8)	Non-Operating	35°C,Over 85% RH,3% Salt Concentration
Solar Radiation Test	Non-Operating	40°C ,Irradiation 1000W/m^2
UV Light Exposure Test (ISO 7816-1)	Non-Operating	254nm, 15Ws/cm^2
Drop Test	Non-Operating	150cm/Free fall, total 6 drops

1.4 Reliability

Table1-4: Reliability

Type	Meaurement	
Number of insertions	Up to 20,000 times	
TBW (Sequential Write)	8GB	436 Terabytes
	16GB	872 Terabytes
	32GB	1745 Terabytes
	64GB	3490 Terabytes
MTBF(@25°C)	>3,000,000 hours	

Note 1:
TBW (total bytes written) is an index of how many TB (Terabytes) can be used for written under product life time.
The endurance for flash cards can be predicted based on the usage conditions applied to the device, the internal NAND flash cycles, the write amplification factor, and the wear leveling efficiency of the flash devices. Above TBW is for reference only. Please contact ATP for TBW in real applications.
1 TeraBytes = 1000 GigaBytes (Disk storage)
Note 2:
MTBF highly depends on testing method. All ATP products are tested with Bellcore Method II (Combines Method I <Parts Count> predictions with laboratory data).

1.5 Electrical Characteristics – DC Characteristics

Power Consumption

Table 1-5-1: Product Power Consumption

Capacity	Operating Current (Typ.)	Operating Current (Max.)	Operating Mode
8GB	105mA	198mA	SDR104
16GB	113mA	238mA	SDR104
32GB	114mA	278mA	SDR104
64GB	118mA	366mA	SDR104

Note 1: Max. Allowed Power is defined as max. operating current 400mA at the max. voltage 3.6V. UHS-I card is up to 1.44W.
Note 2: Operation current might subject to host devices, applications, product configurations and operation modes.

Bus Operating Conditions for 3.3V Signaling

Table 1-5-2: DC Characteristics Under 3.3V Signaling

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage	VDD	2.7	3.6	V	
Output High Voltage	VOH	0.75x VDD	-	V	IOH=-2mA VDD min
Output Low Voltage	VOL	-	0.125 x VDD	V	IOL=-2mA VDD min
Input High Voltage	VIH	0.625x VDD	VDD + 0.3	V	
Input Low Voltage	VIL	Vss-0.3	0.25 x VDD	V	
Power Up Time			250	ms	From 0V to VDD min
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	

The current consumption is measured by averaging over 1 second.

- Before first command: Maximum 15 mA
- During initialization: Maximum 100 mA
- Operation in Default Speed Mode: Maximum 100 mA for SDSC and SDXC
  100 mA (XPC=0) or 150 mA (XPC=1) for SDXC
- Operation in High Speed Mode: Maximum 200 mA
- Operation in UHS-I Mode: Maximum 400 mA (UHS50,DDR50) or 800 mA (UHS104)

- Operation with other functions: Maximum 500 mA

Some functions can be added by CMD6 and SDIO (ex. McEX, ASSD and Combo Card). Host needs to select functions so that the total current of selected functions shall be up to 500mA. In case of UHS-I card, host should not select UHS-I mode and the other functions at the same time.

Bus Operating Conditions For 1.8V Signaling

Table 1-5-3 DC Characteristics Under 1.8V Signaling

Parameter	Symbol	Min	Max	Unit	Remark
Supply voltage	V_{DD}	2.7	3.6	V	
Regulator Voltage	V_{DDIO}	1.7	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.4	-	V	I_{OH}=-2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL}=-2mA
Input High Voltage	V_{IH}	1.27	2.0	V	
Input Low Voltage	V_{IL}	Vss-0.3	0.58	V	

1.6 Electrical Characteristics – Summary of Bus Speed Mode and Maximum Current

The maximum frequency and the maximum current are determined by CMD6.

Table 1-6-1 Bus Speed Modes

Bus Speed Mode*1	Max. Bus Speed [MB/s]	Max. Clock Frequency [MHz]	Signal Voltage [V]	Max. Power*2 [W]		
				SDSC*3	SDHC*4	SDXC*5
SDR104	104	208	1.8	-	2.88*6	2.88*6
SDR50	50	100	1.8	-	1.44	1.44
DDR50	50	50	1.8	-	1.44	1.44
SDR25	25	50	1.8	-	0.72	0.72
SDR12	12.5	25	1.8	-	0.36	0.36/0.54*7
High Speed	25	50	3.3	0.72	0.72	0.72
Default Speed	12.5	25	3.3	0.36	0.36	0.36/0.54*7

*1: The card supports a UHS-I mode shall support all lower UHS-I modes.
*2: Host may control power by the Power Limit function in CMD6.
*3: SDSC stands for SD Standard Capacity Memory Card and
*4: SDHC stands for SD High Capacity Memory Card.
*5: SDXC stands for SD Extended Capacity Memory Card.
*6: The actual maximum current may vary from the limit described in this table. It is limited by the Mechanical Addenda in the sections that define the thermal profile of the device and the connector profile.
*7: Host may select either maximum power by XPC in ACMD41.

1.7 Electrical Characteristics – AC Characteristics

High Speed Mode Bus Timing (3.3V Signaling)

Table 1-7-1: Bus Timing - Parameter Values (High Speed Mode)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{card} <= 10 pF(1 card)
Clock low time	t_{WL}	7	-	ns	C_{card} <= 10 pF(1 card)
Clock high time	t_{WH}	7	-	ns	C_{card} <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	3	ns	C_{card} <= 10 pF(1 card)
Clock fall time	t_{THL}	-	3	ns	C_{card} <= 10 pF(1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6	-	ns	C_{card} <= 10 pF(1 card)
Input hold time	t_{IH}	2	-	ns	C_{card} <= 10 pF(1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	C_L <= 40 pF (1 card)
Output Hold time	t_{OH}	2.5	-	ns	C_L <= 15 pF (1 card)
Total System capacitance for each line[1]	C_L	-	40	pF	1 card

Notes: In order to satisfy severe timing, host shall drive only one card.

Default Bus Timing (3.3V Signaling)

Table 1-7-2: Bus Timing - Parameter Values (Default)

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
ClockfrequencyDataTransferMode	f_{PP}	0	25	MHz	C_{card} <= 10 pF(1 card)
Clock frequency Identification Mode	f_{OD}	0[1]/100	400	KHz	C_{card} <= 10 pF(1 card)
Clock low time	t_{WL}	10	-	ns	C_{card} <= 10 pF(1 card)
Clock high time	t_{WH}	10	-	ns	C_{card} <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	10	ns	C_{card} <= 10 pF(1 card)

Clock fall time	t_{THL}	-	10	ns	C_{card} <= 10 pF(1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5	-	ns	C_{card} <= 10 pF(1 card)
Input hold time	t_{IH}	5	-	ns	C_{card} <= 10 pF(1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	14	ns	C_L <= 40 pF(1 card)
Output Delay time during Identification Mode	t_{ODLY}	-	50	ns	C_L <= 40 pF(1 card)

Notes: 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required (refer to SDA Chapter 4.4 Clock Control).

High Speed Mode Bus Timing (1.8V Signaling) For SDR50 Mode

Table 1-7-3: Bus Timing - Parameter Values (SDR50 mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input SDCK					
Clock frequency Data Transfer Mode	f_{PP}	0	100	MHz	C_L <= 10 pF(1 card)
Clock low time	t_{WL}	3	-	ns	C_L <= 10 pF(1 card)
Clock high time	t_{WH}	3	-	ns	C_L <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	2	ns	C_L <= 10 pF(1 card)
Clock fall time	t_{THL}	-	2	ns	C_L <= 10 pF(1 card)
Inputs DAT (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	3	-	ns	C_L <= 10 pF(1 card)
Input hold time	t_{IH}	0.8	-	ns	C_L <= 15 pF(1 card)
Outputs DAT (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	7.5	ns	C_L <= 30 pF(1 card)
Output Hold time	t_{OH}	1.5	-	ns	C_L <= 15 pF(1 card)

High Speed Mode Bus Timing (1.8V Signaling) For SDR104 Mode

Table 1-7-4: Bus Timing - Parameter Values (SDR104 mode)

Parameter	Symbol	Min	Max	Unit	Remark
Input SDCK					
Clock frequency Data Transfer Mode	f_{PP}	0	208	MHz	C_L <= 10 pF(1 card)
Clock low time	t_{WL}	1.5	-	ns	C_L <= 10 pF(1 card)
Clock high time	t_{WH}	1.5	-	ns	C_L <= 10 pF(1 card)
Clock rise time	t_{TLH}	-	0.96	ns	C_L <= 10 pF(1 card)

Clock fall time	t_{THL}	-	0.96	ns	C_L <= 10 pF(1 card)
Inputs DAT (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	1.4	-	ns	C_L<= 10 pF(1 card)
Input hold time	t_{IH}	0.8	-	ns	C_L<= 5 pF(1 card)
Outputs DAT (referenced to CLK rising edge)					
Card Output Phase	t_{OP}	0	2	UI	C_L <= 15 pF(1 card)

SD Dual Data Rate (DDR50) Mode Timing

Table 1-7-5: Bus Timings – Parameters Values (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Remark
CMD Inputs and Output (referenced to CLK rising edge)					
CMD Input set-up time	t_{ISU}	3	-	ns	C_L<= 10 pF(1 card)
CMD Input hold time	t_{IH}	0.8	-	ns	C_L <= 10 pF(1 card)
CMD Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	C_L<= 30 pF(1 card)
CMD Output Hold time	t_{OH}	1.5		ns	C_L <= 15 pF(1 card)
DAT Inputs and Output (referenced to CLK rising and falling edge)					
DAT Input set-up time	t_{ISU2x}	3	-	ns	C_L<= 10 pF(1 card)
DAT Input hold time	t_{IH2x}	0.8	-	ns	C_L <= 10 pF(1 card)
DAT Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7	ns	C_L<= 25 pF(1 card)
DAT Output Hold time	t_{OH2x}	1.5		ns	C_L <= 15 pF(1 card)

1.8 Electrical Characteristics – Bus Signal Line Load

The total capacitance CL of each line of the SD bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CCARD of each card connected to this line:

CL = CHOST + CBUS + N*CCARD

N is the number of connected cards.

Table 1-8-1: Bus Signal Line Load

Parameter	Symbol	Min	Max.	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	Kohm	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Card capacitance for each signal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	f_{PP} <= 20 MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	Kohm	May be used for card detection
Capacity Connected to Power Line	C_C		5	uF	To prevent inrush current

1.9 IOPS

Table 1-9-1: TestMetrix IOPS at 4K Random Read/Write

Capacity	Minimum Random Read (IOPS)	Minimum Random Write (IOPS)	Minimum sustained Sequential Write (MBytes/sec)
8GB	2930	1645	36.0
16GB	2916	911	36.1
32GB	3021	1379	36.1
64GB	2912	1128	36.1

Note 1: Tested by TestMetrix VTE-4100

Note 2: Application Performace Class 1 (A1): Minimum Random Read 1500IOPS, Minimum Random Write 500IOPS, Minimum Sustained Sequential Write 10Mbytes/sec.

Note 3: The performance may vary depending on the configuration, firmware, setting, application and test environment

1.10 Sequential Maximum Read/Write Performance

Table 1-10-1: SDR104 Speed Mode

Capacity	Seq. Read (MB/s)	Seq. Write (MB/s)	Random 4K Read (MB/s)	Random 4K Write (MB/s)
8GB	99.00	55.58	7.96	4.14
16GB	95.01	76.13	8.18	4.23
32GB	98.98	81.16	7.95	3.97
64GB	99.00	82.41	7.90	3.12

Note 1: SDR104: One of UHS modes with single data rate. Up to 104MB/s at 208MHz

Note 2: Tested by CrystalDiskMark 5.0.2 with 100MB file size.

Note 3:The performance may vary depending on the configuration, firmware, setting, application and test environment

1.11 Write/Erase Endurance

Table 1-11-1: Data Retention

Endurance Used	Corresponding Data Retention
≦10% P/E cycles	10 years @ 40 oC use condition
＞10%~100% P/E cycles	1 year @ 40 oC use condition

Note 1: Data retention refers to the ability of a memory bit to retain its data state over a period of time after the data is written in NAND Flash regardless of whether the part is powered on or powered off.
A data retention failure is when there is at least 1 bit of data that cannot be read or is read incorrectly.

Note 2: NAND Flash suppliers refer to JEDEC JESD47 & JESD22 for Data Retention testing. Assuming <10% of maximum P/E cycles and UBER<1E-14 at minimum required ECC.

1.12 Extra Features

Table 1-12-1: Extra Features

Type	Measurement
Water Proof	IEC 60529 Edition 2.1: 2001-02—IPX7, below 1000mm water, 30min
Dust Proof	IEC 60529 Edition 2.1: 2001-02—IP6X
ESD Resistant	IEC 61000-4-2: contact pad +/- 4KV, non-contact pad (Coupling plane discharge) +/- 8KV, non-contact pad (Air discharge) +/- 15KV
RoHS Compliant	Yes

1.13 Certificates

Mark/Approval	Documentation
CE	The CE marking (also known as CE mark) is a mandatory conformance mark on many products placed on the single market in the European Economic Area (EEA). The CE marking certifies that a product has met EU consumer safety, health or environmental requirements. CE stands for Conformité Européenne, "European conformity" in French
FC	FCC Part 15 Class B was used for Evolution of United States (US) Emission Standards for Commercial Electronic Products, The United States (US) covers all types of unintentional radiators under Subparts B of FCC 47 CFR Part 2 and 15, usually called just FCC Part 15
UKCA	The UKCA (UK Conformity Assessed) marking is a new UK product marking that is used for goods being placed on the market in Great Britain (England, Wales and Scotland). UKCA marking was specified in the original 'EU Exit' UK Statutory Instruments, and defined in UK Statutory Instrument 2019 No. 696, and amendments.
China RoHS	China RoHS is a Chinese government regulation to control certain materials, including lead. All items shipped to China now have to be marked as to whether the items contained in the box are compliant or non-compliant. Environment Friendly Use Period (EFUP) is the period of time before any of the RoHS substances are likely to leak out, causing possible harm to health and the environment.

2.0 Product Features

2.1 Ultra-High-Speed Type I (UHS-I) Card

UHS-I provides up to 104MB/sec performance on 4-bit SD bus with the single end driver interface. Card form factor is the same and existing connector can be used.

UHS-I Card Operation Modes

- DS - Default Speed up to 25MHz 3.3V signaling
- HS - High Speed up to 50MHz 3.3V signaling
- SDR12 - SDR up to 25MHz 1.8V signaling
- SDR25 - SDR up to 50MHz 1.8V signaling
- SDR50 - SDR up to 100MHz 1.8V signaling
- SDR104 - SDR up to 208MHz 1.8V signaling
- DDR50 - DDR up to 50MHz 1.8V signaling

Note: Timing in 1.8V signaling is different from that of 3.3V signaling.

2.2 UHS-I Card Types

UHS-I supports two card Types: UHS50 and UHS104

UHS-I is not applied to SDSC card but can be applied to SDHC and SDXC card.

Figure 4-2-1 and Figure 4-2-2 show UHS-I supported modes. DDR50 is mandatory for microSD form factor and optional for Standard size SD form factor

Figure 2-2-1 UHS-I Card Type Modes of Operation versus Frequency Range

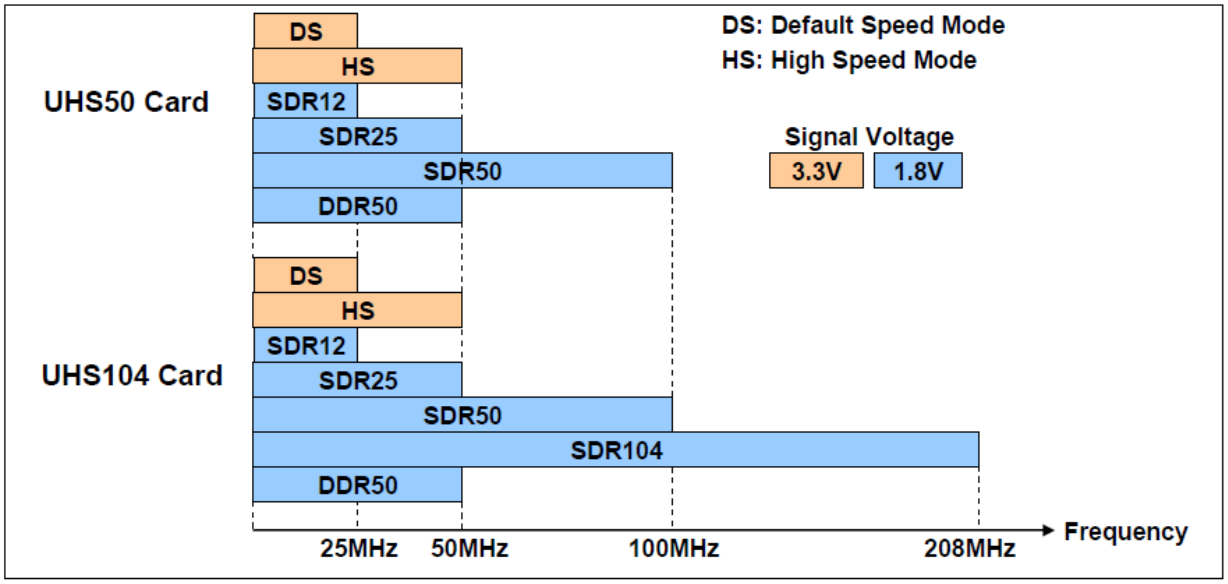
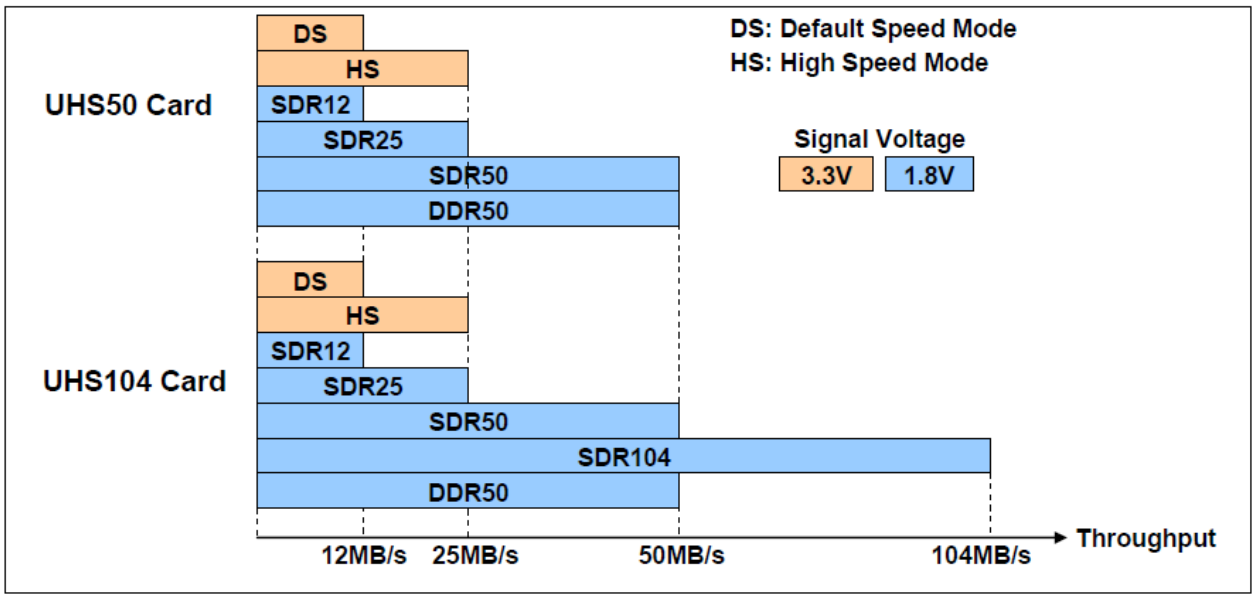


Figure 2-2-2 UHS-I Card Type Modes of Operation versus Throughout



2.3 Host and Card Combination

Table 4-3 shows usable UHS performance depends on the combination of host and card. UHS-I for removable card is presumed that one card is connected to a SD bus. Maximum performance of up to 104MB/s is possible only if host supports SDR104 mode and card is UHS104 Card (supports SDR104 mode). If card is a UHS50 Card or if host doesn't support SDR104 mode, performance is limited to 50MB/s (SDR104 mode cannot be used). Host may use DDR50 mode with UHS50 Card and UHS104 Card in microSD form factors.
Host types:
SDR-FD – SDR signaling, fixed-delay (can't use tuning)
SDR-VD – SDR signaling, variable-delay (can use tuning)
DDR – DDR signaling

Table 2-3 host and card combination

Host type / Card type	HOST-SDR-FD (SDR, fixed-delay)	HOST-SDR-VD (SDR, variable-delay)	HOST-DDR (DDR)
UHS50 card microSD	SDR50 ≤ 100MHz	SDR50 ≤ 100MHz + tuning	DDR50 ≤ 50MHz
UHS104 card microSD	SDR50 ≤ 100MHz	SDR104 ≤ 208MHz + tuning	DDR50 ≤ 50MHz
UHS50 card Full-size SD	SDR50 ≤ 100MHz	SDR50 ≤ 100MHz + tuning	Optional
UHS104 card Full-size SD	SDR50 ≤ 100MHz	SDR104 ≤ 208MHz + tuning	Optional

Host can choose one of UHS-I modes by CMD6 Function Group 1. Each UHS-I mode is specified by the

maximum frequency, sampling edges (rising-only or both) and maximum current consumption for compatibility with existing cards. Host can choose one of UHS-I mode depending on capability of generating SDCLK frequency and capacity of power supply host supported.

CMD19 can be executed in transfer state of 1.8V signaling mode while the card is unlocked. The other case, CMD19 is treated as illegal command

2.4 Bus Speed Mode Selection Sequence

Figure 2-4 Command sequence to use UHS-I page

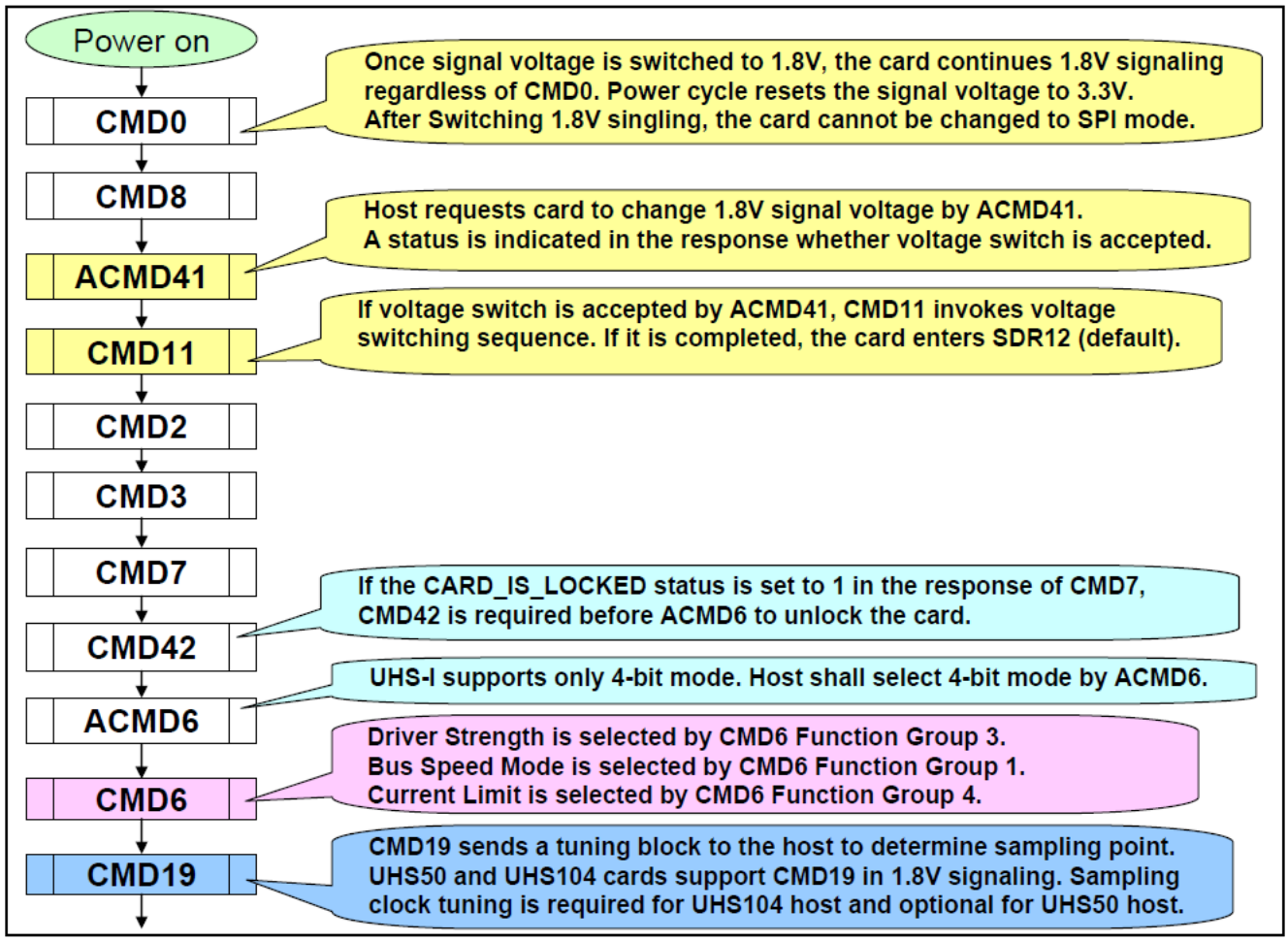


Figure 3-4 shows command sequence to use a UHS-I. After power cycle, card is in 3.3V signaling mode. The first CMD0 selects the bus mode; SD mode. 1.8V signaling mode can be entered only in SD mode. Once the card enters 1.8V signaling mode, the card cannot be switched to 3.3V signaling without power cycle. If the card receives CMD0, card returns to Idle state but still work with SDR12 timing. UHS-I is provided in SD mode but not in SPI mode.

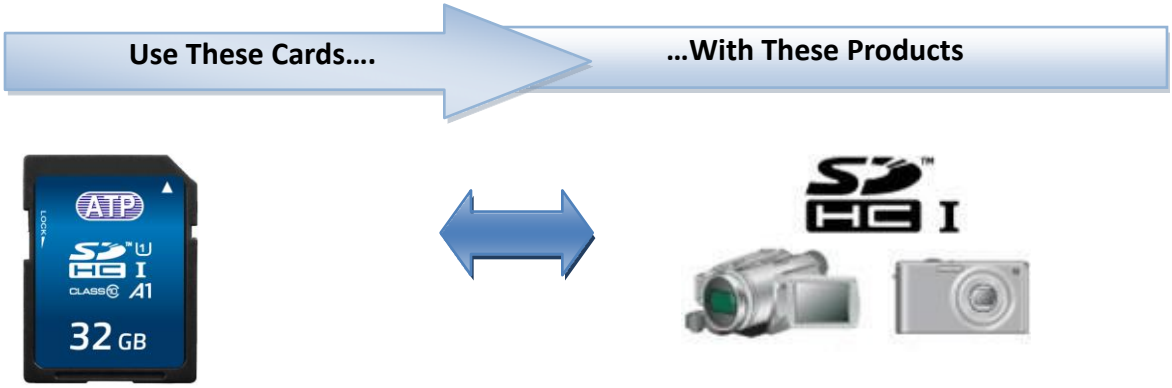
As higher bus speed requires low level signaling, UHS-I adopts 1.8V signaling level for SDR50, DDR50 and SDR104 modes. Still card is supplied with 3.3V by the host and 1.8V signaling level for SDCLK, CMD and DAT[3:0] lines is converted from 3.3V power line. To avoid voltage mismatch between host and card, signaling level is changed by voltage switch sequence at the initialization. The host and card communicate using ACMD41 whether host and card support 1.8V signaling mode. Support of 1.8V signaling both host and card means UHS-I can be used. CMD11 invokes the voltage switch sequence. The card enters UHS-I mode and card input and output timings are changed (SDR12 in default) when the voltage switch sequence is completed successfully. (Refer to Section 6.6.4 for more detail.)

Only 4-bit bus mode is supported in UHS-I except CMD42. If the card is locked, host needs to unlock the card by CMD42 in 1-bit mode and then needs to issue ACMD6 to change 4-bit bus mode. Operating in 1-bit mode is not assured.
Host can choose suitable output driver strength by CMD6 Function Group 3.

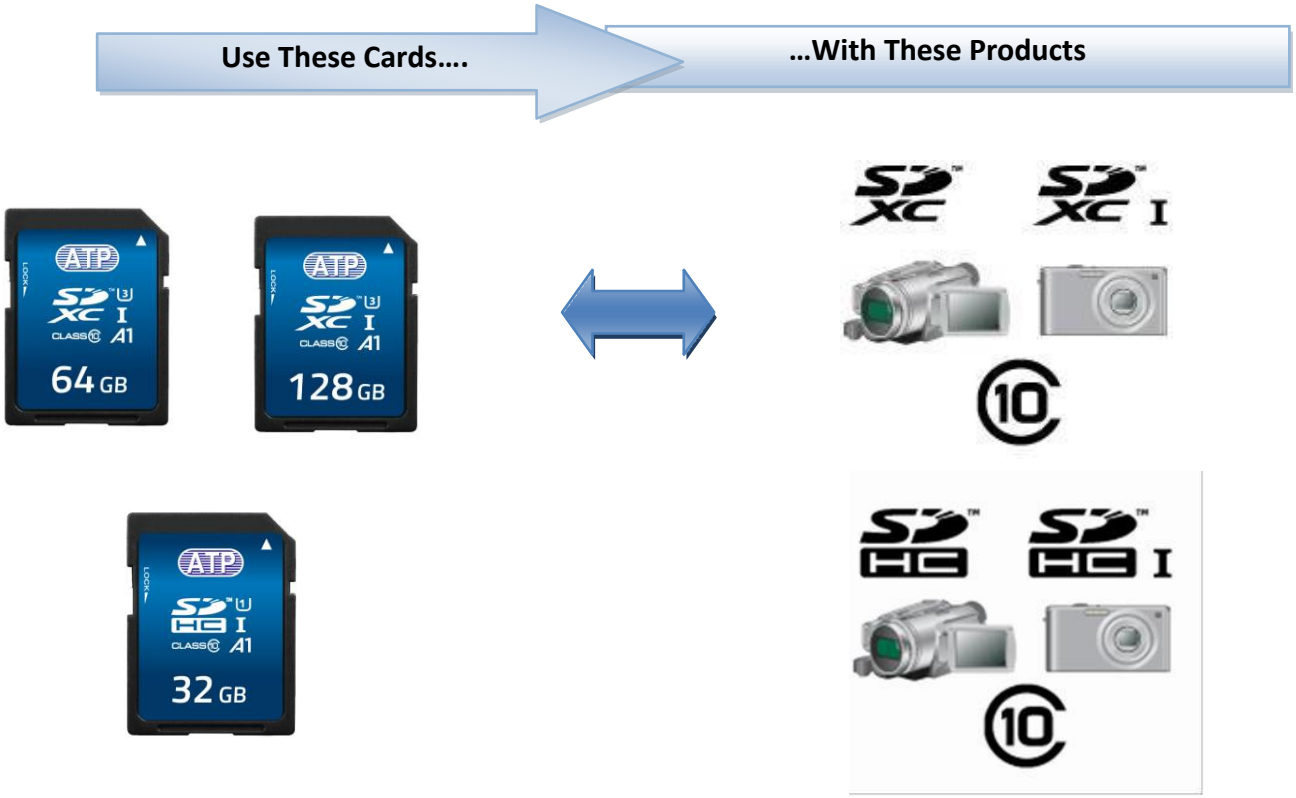
2.5 Host Device Compatibility

Before choosing a card for your devices, it is important that you understand how to use your memory card to its greatest ability. Speed Class and UHS Speed Class are two different speed indication symbols for different devices. However, a UHS-I memory card may also indicate a Speed Class. The UHS-I SDHC/XC card can still apply on non-UHS (high speed) devices. Nonetheless, the Ultra- High-Speed SDHC/XC card can reach its best performance along with UHS-I devices.

UHS Speed Class Compatibility



Speed Class Compatibility



2.6 High Endurance

- **TLC NAND Flash with 5K P/E cycles per block.** ATP high-endurance memory cards built with 5K P/E cycles triple-level-cell (TLC) NAND flash have 1.6 times higher P/E cycles per block than normal 3K P/E cycles multi-level-cell (MLC) NAND flash.
- **Advanced Wear Leveling.** This evenly distributes erase counts to each block to extend the lifetime of the storage device. ATP high-endurance memory cards have a delta of no more than 128 erase counts per block, showing the effectivity of the Advanced Wear Leveling mechanism.
- **Write Amplification Factor (WAF)**. A high WAF negatively impacts the memory card's endurance. ATP's high-endurance memory cards have a WAF of just close to 1[1], according to a test by 128KB sequential write with the IOMeter 2.0 tool on Windows 10.

[1]Results may vary depending on test conditions and environment.

2.7 Low Latency

Users expect their systems to be ready with fast response. Taking the drive recorder as an example — after power on, the bootup time depends on the embedded memory, yet the time required to be ready for recording and succeeding programming depends on the external/removable storage, such as SD/microSD cards.

Normal cards may take 7 to 12 seconds to be ready, yet ATP S650 cards' response time is less than 1 second. While recording 16 MB data sequentially, ATP S650 cards take less than 0.1 second compared with consumer-rated cards that may take around 0.2 seconds, thereby cutting 50% of the writing time and enabling high-speed backup without data loss.

2.8 Data Integrity - Read Retry and Auto Read Calibration (ARC)

Reference voltage is applied on the NAND flash to identify the state of cells and read out data correctly. However, the voltage distributions are dynamic and may change when flash wears out at high/low temperatures, thus affecting data retention. When the distributions shift, the optimal reference voltage is required to recover from bit errors and read the correct information (data).

When the distribution shifts, ATP SD cards activate **READ RETRY**, a scale of voltage calibration method, to find a new reference voltage. If the read still fails for bit errors beyond the ECC correction threshold, the firmware (FW) will select the next consecutive read retry option and repeat READ RETRY operations. If the voltage adjustment scale between READ RETRY levels become too large, a subtle and more precise voltage adjustment, **AUTO READ CALIBRATION (ARC)** will be applied.

2.9 Data Integrity - Read Disturb Protector

Read Disturb Protector aims to prevent read disturbance and data corruption by monitoring error bits and read counts in every operation before reaching or going over the preset threshold[1]. If the error bits are within the threshold, ATP FW will find the reference voltage to recover the errors by activating Read Retry and ARC. Nonetheless, if the error bits are above threshold, the data will still be recovered and moved to another healthy block. Simultaneously, the original block will be marked as a bad block due to its high risk.

If the read counts are reaching threshold, to prevent from read disturb, we will also move data to another healthy block, and the original block will be refreshed for reuse.

[1]ECC threshold may vary depending on FW & BOM configuration

2.10 Data Integrity - Power Failure Protection

1. Back-up FW mechanism

Important system tables consist of FW/ISP code, flash translation layer (FTL) info table, and boot table, which are stored in the NAND flash (SLC mode system blocks) and will be loaded to the controller SRAM during SD card initialization. If the FW/ISP code and boot tables are corrupted, the memory cards cannot be initialized successfully. If the FTL info table is corrupted, the memory card can be initialized but the data may be missing.

Though the SLC mode blocks are robust, to avoid the crash of main system tables, back-up tables are stored in another system block. Thus, the SD card can be initialized, and the data can be accessed from either the main system tables or back-up system tables.

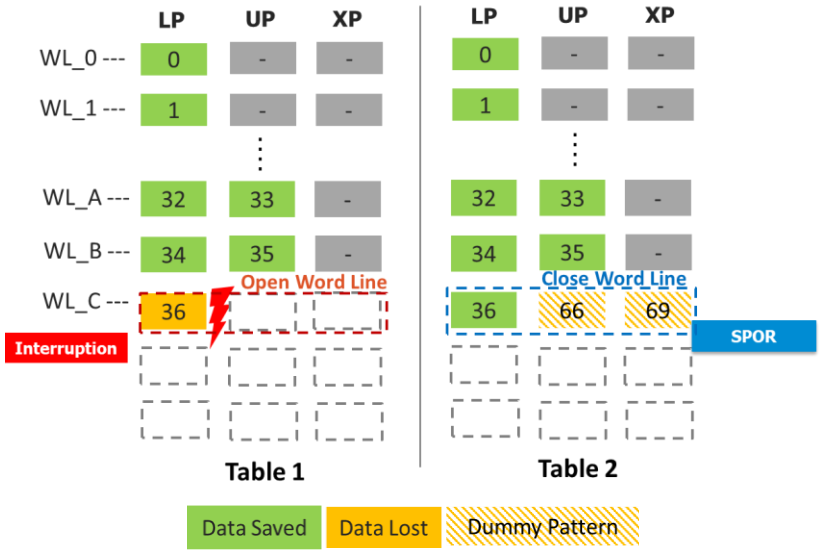
2. ATP Sudden-Power-Off-Recovery (SPOR) FW mechanism

The basic unit of a memory chip is a cell, and the cells are arranged in a row called a word line (WL). There are paired pages (lower page, upper page, and extra page) that share the same word line in TLC architecture. When the programming in the same WL is not completed (open WL), this may lead to data corruption.

To save as much data as possible, ATP Sudden Power-Off Recovery (SPOR) firmware will fill in the remaining cells of the same WL (close WL) with a dummy pattern.

Taking Figure 2-10-1 below as an example, ATP SPOR firmware mechanism completes the programming operation on page 36 by filling in paired pages 66 and 69 in the same WL with a dummy pattern. This can guarantee that the whole operation is completed and the data in page 36 is saved.

Figure 2-10-1 ATP SPOR firmware mechanism



2.11 Analysis Method - SD Life Monitor tool

To get detailed reports on the health status of the SD/microSD card, the SD Life Monitor tool can be applied for product development.

- On Windows, the ATP SD Life monitor tool provides health status reports and card identification information. Furthermore, with additional “Workload Inspection” pie chart, users can quickly check the write operation and file size by the host systems.

  The table below shows the file size ranges categorized from 512 bytes (normally for file system update) to 128 KB (max. transfer data size each time via card reader).

  To ensure the lowest WAF to prolong the life cycle (endurance) of the memory cards, users can refer to Tables 2-11-1 and 2-11-2 in evaluating the host’s data size range in relation to the storage density.

  Considering the NAND flash page size and FW algorithm, the tables provide recommendations for the host devices’ program data based on the multiples of minimum data transfer size.

Table 2-11-1 Workload with Data Size

Data Size Written by Host	Data Size Range	Remarks
512 bytes	0 to 512 bytes	File system
4K bytes	> 512 bytes to 4K bytes	Random small file size
16K bytes	> 4K bytes to 16K bytes	Random small file size
32K bytes	> 16K bytes to 32K bytes	Random/sequential file size
64K bytes	> 32K bytes to 64K bytes	Sequential file size
128K bytes	> 64K bytes to 128K bytes	Sequential file size
Others	> 128K bytes	Max. transfer file size / time by card reader

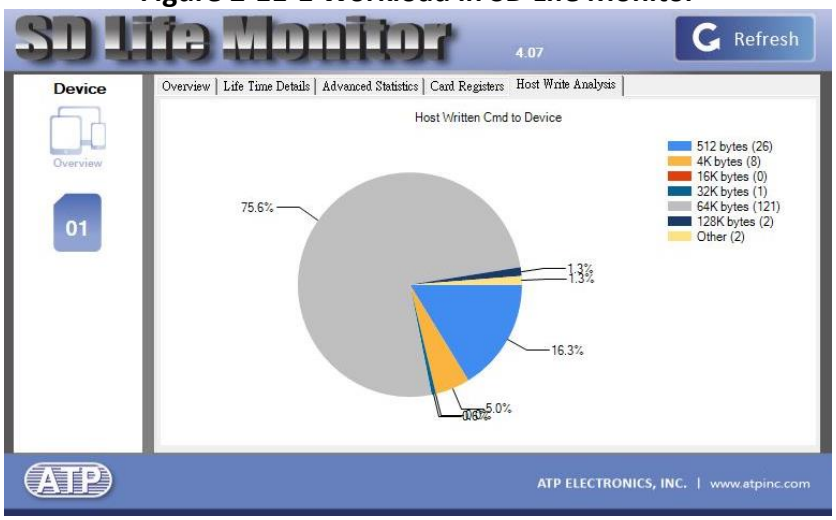
Table 2-11-2 Relation of Density and Min. Data Size

Density of SD/microSD Cards	Min. Data (file) Size
32 GB	32 KB
64 GB	64 KB
128 GB	128 KB
256 GB	256 KB

NOTE: The minimum data (file size) may vary depending on configuration.

Taking Figure 2-11-1 as an example, majority of the file sizes written by the host device is 64KB (121 times). According to Table 2-11-2, using 32 GB and 64 GB memory cards will gain the lowest WAF and ideally, the optimal endurance.

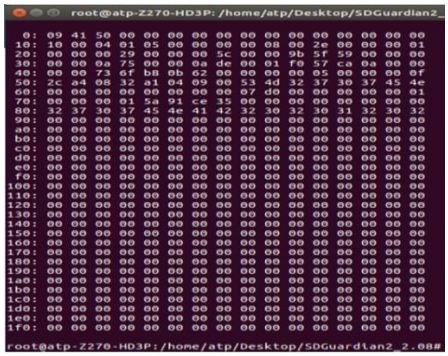
Figure 2-11-1 Workload in SD Life Monitor



- On Linux, customers can install the ATP SD Guardian tool (user friendly) or refer to the ATP CMD56 guidelines (directly issue SD vendor CMD for software integration).

Figure 2-11-2 ATP SD Monitor Tool in Linux

Command 56



ATP SD Guardian

2.12 Advanced Card Analysis for SiP (System-In-Package) Memory Cards

Memory cards are IP67/IP57-certified and manufactured using System-in-Package (SiP) wafer/die process, making it difficult to do component analysis compared to SMT (surface- mount technology) process. ATP's uniquely designed substrate and debug tool make this mission "possible."

1. ATP-Developed Hardware Design - Substrate with reserved testing pin is available for future component analysis.
2. Solder Mask Removal by Laser – Precise and efficient method to remove solder mask so as to reach the reserved testing pins on the substrate.
3. ATP's Own Customized Debug Tool - This is connected to the HW reserved testing pin and then linked to the SW analysis system.

For more information, please link to YouTube: ATP Mission Impossible Video

3.0 Product Overview

3.1 Block Diagram

Figure 3-1-1: SD Card Function Block Diagram

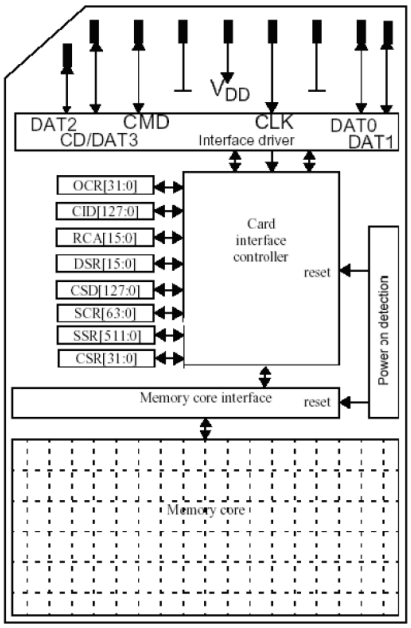


Table 3-1-2: Pad Assignment

Pin #	SD Interface		
	Name	Type[1]	Description
1	CD/DAT3[2]	I/O/PP[3]	Card Detect /Data Line (Bit 3)
2	CMD	PP	Command/ Response
3	V_{SS1}	S	Supply Voltage Ground
4	V_{DD}	S	Supply Voltage
5	CLK	I	Clock
6	V_{SS2}	S	Supply Voltage Ground
7	DAT0	I/O/PP	Data Line (Bit 0)
8	DAT1[4]	I/O/PP	Data Line (Bit 1)
9	DAT2[5]	I/O/PP	Data Line (Bit 2)

Notes：

1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;

2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.

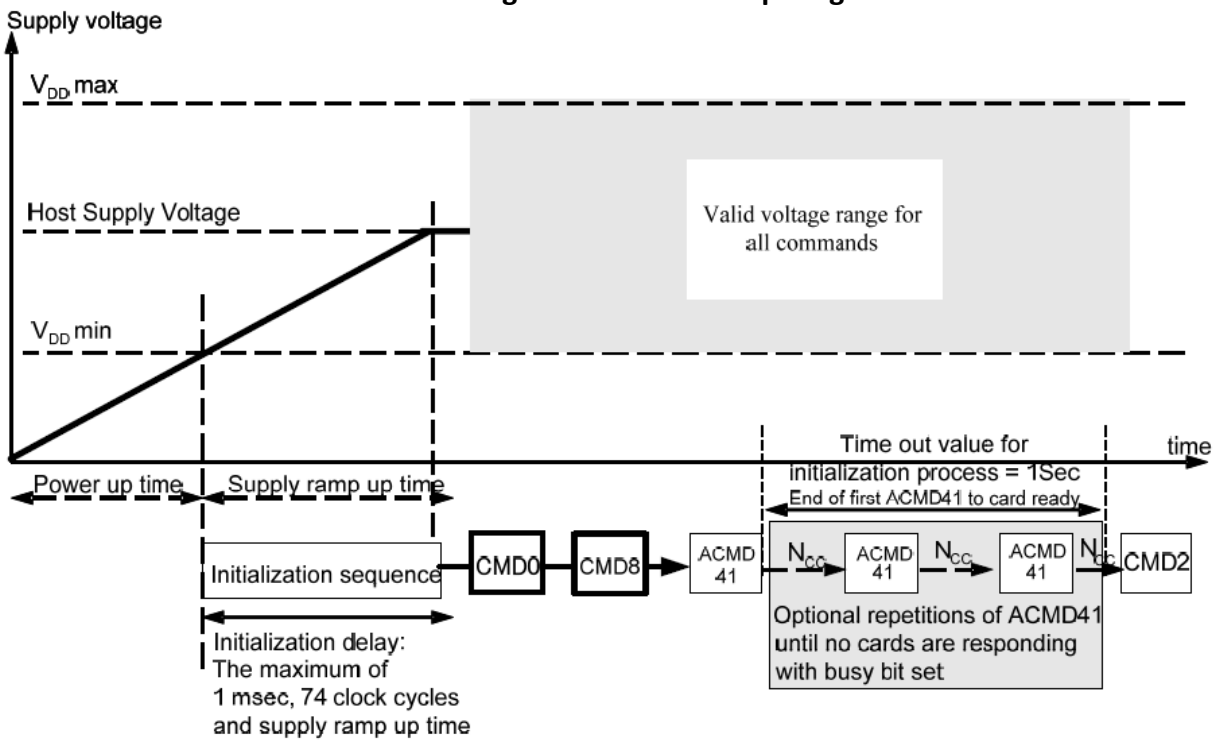
3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command

4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).

5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

3.2 Power Up

Figure 3-2-1 Power-Up Diagram



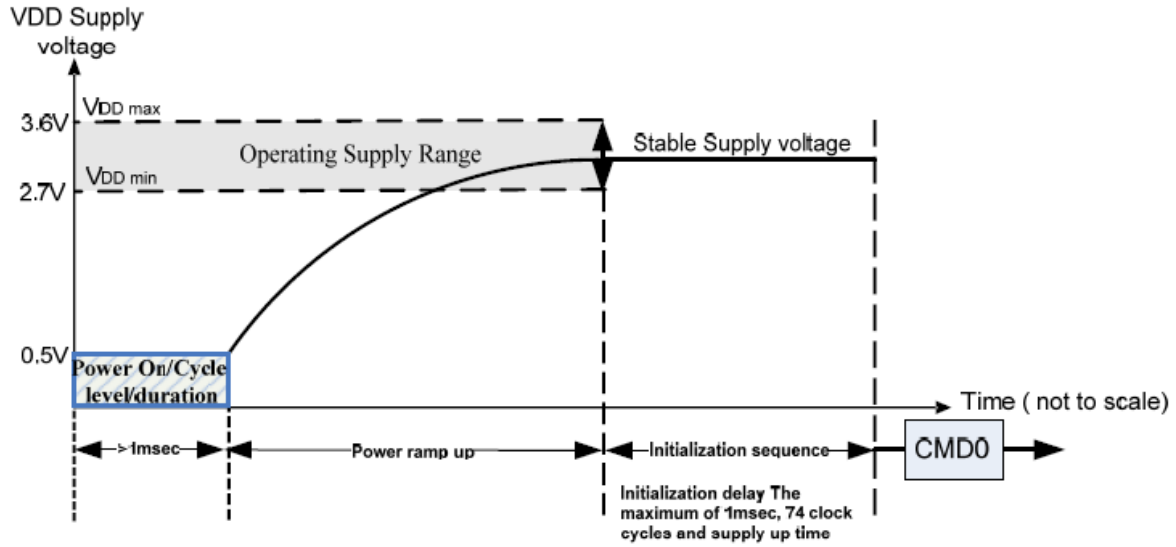
'Power up time' is defined as voltage rising time from 0 volt to VDD min (refer to 6.6) and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.
'Supply ramp up time' provides the time that the power is built up to the operating level (Host Supply Voltage) and the time to wait until the SD card can accept the first command,

- The host shall supply power to the card so that the voltage is reached to Vdd_min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high.
- After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the idle state. In case of SD host, CMD0 is not necessary.
- CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 or later host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.
- ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. In case the host system connectsmultiple cards, the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

3.3 Power Up Time

Reset level is not described in Physical Layer Specification Version 2.00. Change of Figure 2-3-1 is applied.
Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.

Figure 3-3-1 Change of Figure for power up



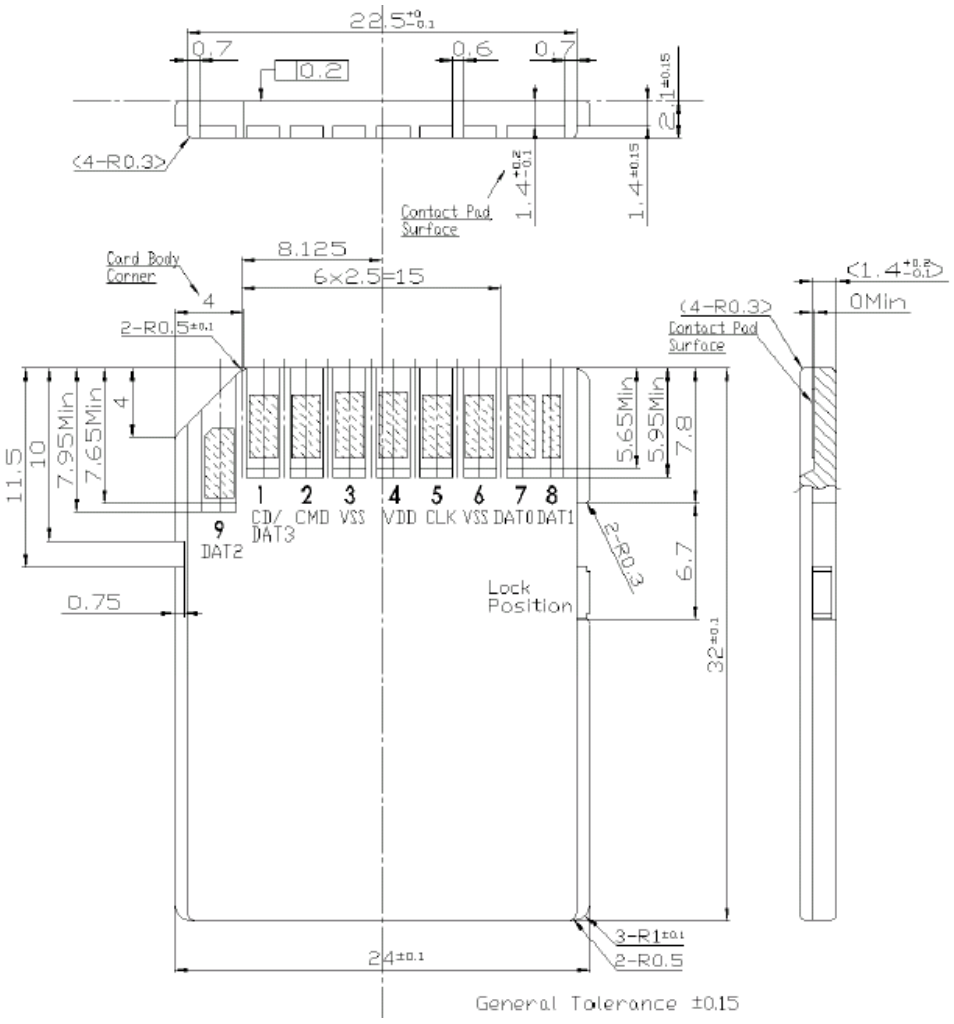
4.0 Mechanical Dimension

4.1 Physical Dimension (Units in mm)

Type	Measurement
Length	32.0mm +/- 0.10mm
Width	24.0mm +/- 0.10mm
Thickness	2.1mm +/- 0.15mm
Weight	2.0g Max.

4.2 Mechanical Form Factor (Units in mm)

Table 4.2: Physical Form Factor



5.0 Card Registers

Six registers are defined within the card interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. To enable future extension, the card shall return 0 in the reserved bits of the registers.

Register	SD 2.x	SD 3.0x
Operation Condition Register (OCR)	V	V
Card Identification Register (CID)	V	V
Driver Stage Register (DSR)	NA	NA
Relative Card Address Register (RCA)	V	V
Card Specific Data Register (CSD)	V	V
SD Card Configuration Register (SCR)	V	V

5.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit. The OCR register shall be implemented by the cards.
The 32-bit operation conditions register stores the VDD voltage profile of the card. Bit 7 of OCR is newly defined for Dual Voltage Card and set to 0 in default. If a Dual Voltage Card does not receive CMD8, OCR bit 7 in the response indicates 0, and the Dual Voltage Card which received CMD8, sets this bit to1. Additionally, this register includes 2 more status information bits.
Bit 31 - Card power up status bit, this status bit is set if the card power up procedure has been finished.
Bit 30 - Card Capacity Status bit, 0 indicates that the card is SDSC. 1 indicates that the card is SDHC or SDXC. The Card Capacity Status bit is valid after the card power up procedure is completed and the card power up status bit is set to 1. The Host shall read this status bit to identify SDSC Card or SDHC/SDXC Card.

The OCR register shall be implemented by the cards.

Table5-1: OCR Register Definition

OCR bit position	OCR Fields Definition
0-3	reserved
4	reserved
5	reserved
6	reserved
7	Reserved for Low Voltage Range
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24[3]	Switching to 1.8V Accepted (S18A)
25-29	reserved
30	Card Capacity Status (CCS)[1]
31	Card power up status bit (busy)[2]

VDD Voltage Window

1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.
3) Only UHS-I card supports this bit.

The supported voltage range is coded as shown in Table5-1. A voltage range is not supported if the corresponding bit value is set to LOW. As long as the card is busy, the corresponding bit (31) is set to LOW.

5.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Table 5-2: The CID fields

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

- **MID**

An 8 bit binary number identifies the card manufacturer. The MID number is controlled, defined and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

- **OID**

A 2-characters ASCII string characters that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

Note: SD-3C, LLC licenses companies that wish to manufacture and/or sell SD Memory Cards, including but not limited to flash memory, ROM, OTP, RAM, and SDIO Combo Cards. SD-3C, LLC is a limited liability company established by Panasonic Corporation, SanDisk Corporation and Toshiba Corporation.

- **PNM**

The product name is a string, 5-characters ASCII characters long.

- **PRV**

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an “n.m” revision number. The “n” is the most significant nibble and “m” is the least significant nibble. As an example, the PRV binary value field for product revision “6.2” will be: 0110 0010

- **PSN**

The Serial Number is 32 bits of binary number.

- **MDT**

The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m). The “m” field [11:8] is the month code. 1 = January.

The “y” field [19:12] is the year code. 0 = 2000. As an example, the binary value of the Date field for production date “April 2001” will be: 00000001 0100.

- **CRC**

CRC7 checksum (7 bits). This is the checksum of the CID contents.

5.3 CSD Register

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be hanged by CMD27. The type of the entries in the table below is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

Table 5-3-1 shows Definition of the CSD Version 2.0 for High Capacity SD Memory Card and Extended Capacity SD Memory Card.

The following sections describe the CSD fields and the relevant data types for SDHC and SFXC Cards.

CSD Version 2.0 is applied to SDHC and SDXC Cards. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R= readable, W(1)= writable once, W= multiple writable.

Table 5-3-1: The CSD Register fields (CSD Version 2.0)

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000b	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
max. data transfer rate	(TRAN_SPEED)	8	32h, 5Ah, 0Bh or 2Bh	R	[103:96]
card command classes	CCC	12	01x110110101b	R	[95:84]
max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE_BLK_MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000b	R	[75:70]
device size	C_SIZE	22	xxxxxxh	R	[69:48]
reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
write protect group enable	(WP_GRP_ENABLE)	1	0	R	[31:31]
reserved		2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE_FORMAT_GRP)	1	0	R	[15:15]
copy flag	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
not used, always'1'	-	1	1	-	[0:0]

• **CSD_STRUCTURE**

Field structures of the CSD register are different depend on the Physical Layer Specification Version and Card Capacity. The CSD_STRUCTURE field in the CSD register indicates its structure version. Table 5-3-2 shows the version number of the related CSD structure.

Table 5-3-2: CSD register structure

CSD_STRUCTURE	CSD structure version	Valid for SD Card Physical Specification Version
0	CSD version 1.0	Standard Capacity
1	CSD version 2.0	High Capacity and Extended Capacity
2-3	reserved	

- **TAAC**

This field is fixed to 0Eh, which indicates 1 ms. The host should not use TAAC, NSAC, and R2W_FACTOR to calculate timeout and should uses fixed timeout values for read and write operations (See 4.6.2).

- **NSAC**

This field is fixed to 00h. NSAC should not be used to calculate time-out values.

- **TRAN_SPEED**

TRAN_SPEED is variable depends on bus speed mode of SD Interface. Definition of this field is same as in CSD Version1.0 in case of Default and High Speed mode. This field shall be set to 0Bh (100Mbit/sec) in both SDR50 and DDR50 mode and shall be set to 2Bh (200Mbit/sec) in SDR104 mode. When CMD0 is received, this field is reset to 32h. UHS-II mode is not related to this field.

- **CCC**

Definition of this field is same as in CSD Version1.0.

- **READ_BL_LEN**

This field is fixed to 9h, which indicates READ_BL_LEN=512 Byte.

- **READ_BL_PARTIAL**

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

- **WRITE_BLK_MISALIGN**

This field is fixed to 0, which indicates that write access crossing physical block boundaries is always disabled in SDHC and SDXC Cards.

- **READ_BLK_MISALIGN**

This field is fixed to 0, which indicates that read access crossing physical block boundaries is always disabled in SDHC and SDXC Cards.

- **DSR_IMP**

Definition of this field is same as in CSD Version1.0.

- **C_SIZE**

This field is expanded to 22 bits and can indicate up to 2 TBytes (It is the same as the maximum memory space specified by a 32-bit block address.)
This parameter is used to calculate the user data area capacity in the SD memory card (not include the protected area). The user data area capacity is calculated from C_SIZE as follows:

memory capacity = (C_SIZE+1) * 512K byte
The Minimum user area size of SDHC Card is 4,211,712 sectors (2GB + 8.5MB).
The Minimum value of C_SIZE for SDHC in CSD Version 2.0 is 001010h (4112).
The maximum user area size of SDHC Card is (32GB - 80MB)
The maximum value of C_SIZE for SDHC in CSD Version 2.0 is 00FF5Fh (65375).
The Minimum user area size of SDXC Card is 67,108,864 sectors (32GB).
The Minimum value of C_SIZE for SDXC in CSD Version 2.0 is 00FFFFh (65535).

- **ERASE_BLK_EN**

This field is fixed to 1, which means the host can erase one or multiple units of 512 bytes.

- **SECTOR_SIZE**

This field is fixed to 7Fh, which indicates 64 KBytes. This value is not related to erase operation. SDHC and SDXC Cards indicate memory boundary by AU size and this field should not be used.

- **WP_GRP_SIZE**

This field is fixed to 00h. SDHC and SDXC Cards do not support write protected groups.

- **WP_GRP_ENABLE**

This field is fixed to 0. SDHC and SDXC Cards do not support write protected groups.

- **R2W_FACTOR**

This field is fixed to 2h, which indicates 4 multiples. Write timeout can be calculated by multiplying the read access time and R2W_FACTOR. However, the host should not use this factor and should use 250 ms for write timeout

- **WRITE_BL_LEN**

This field is fixed to 9h, which indicates WRITE_BL_LEN=512 Byte.

- **WRITE_BL_PARTIAL**

This field is fixed to 0, which indicates partial block read is inhibited and only unit of block access is allowed.

- **FILE_FORMAT_GRP**

This field is set to 0. Host should not use this field.

- **COPY**

Definition of this field is same as in CSD Version1.0.

- **PERM_WRITE_PROTECT**

Definition of this field is same as in CSD Version1.0.

- **TMP_WRITE_PROTECT**

Definition of this field is same as in CSD Version1.0.

- **FILE_FORMAT**

This field is set to 0. Host should not use this field.

- **CRC**

Definition of this field is same as in CSD Version1.0.

5.4 RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

5.5 DSR Register (Optional)

The 16-bit driver stage register is described in detail in Chapter 6.5. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of cards). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

5.6 SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD Memory Card's special features that were configured into the given card. The size of SCR register is 64 bits. This register shall be set in the factory by the SD Memory Card manufacturer.

The following table describes the SCR register content.

Table 5-6-1: The SCR Fields

Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Memory Card - Spec. Version	SD_SPEC	4	R	[59:56]
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
CPRM Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
Spec. Version 3.00 or higher	SD_SPEC3	1	R	[47]
Extended Security Support	EX_ SECURITY	4	R	[46:43]
Reserved		9	R	[42:34]
Command Support bits	CMD_SUPPORT	2	R	[33:32]
reserved for manufacturer usage	-	32	R	[31:0]

Table 5-6-2: SCR Register Structure Version

SCR_STRUCTURE	SCR structure version	SD Physical Layer Specification Version
0	SCR version 1.0	Version 1.01-3.01
1-15	reserved	

5.7 SSR Register

SD Status; information about the card proprietary features (See 6.5)

5.8 CSR Register

Card Status; information about the card status

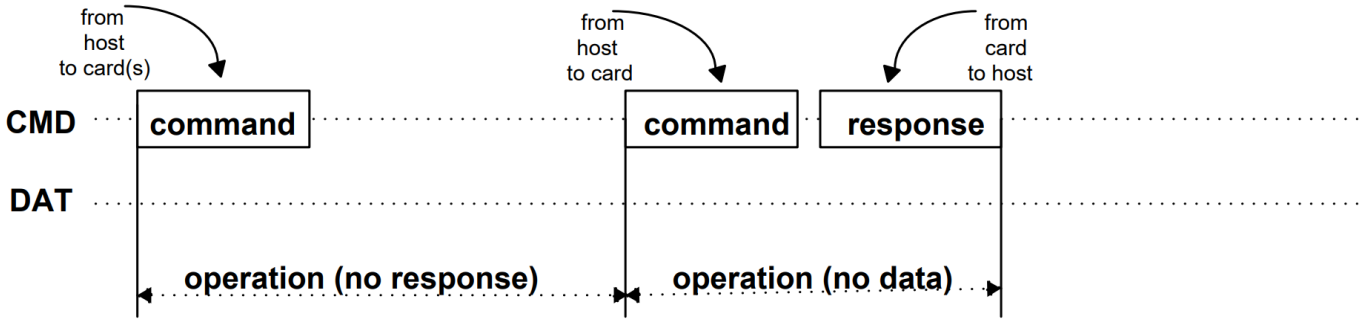
6.0 SD Card Functional Description

6.1 SD BUS Protocol

Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

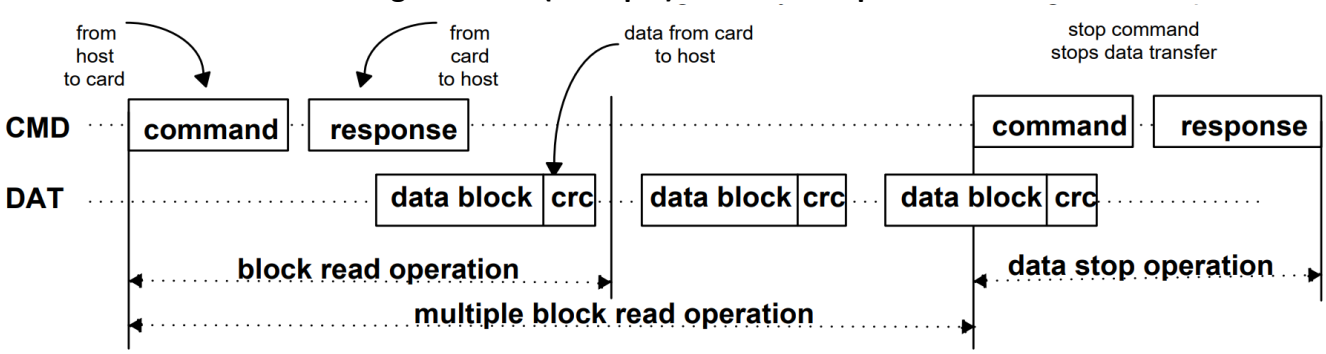
Figure 6-1-1: "no response" And "no data" Operations



Card addressing is implemented using a session address, assigned to the card during the initialization phase. The basic transaction on the SD bus is the command/response transaction (refer to Figure 6-1-1). This type of bus transactions transfers their information directly within the command or response structure. In addition, some operations have a data token.

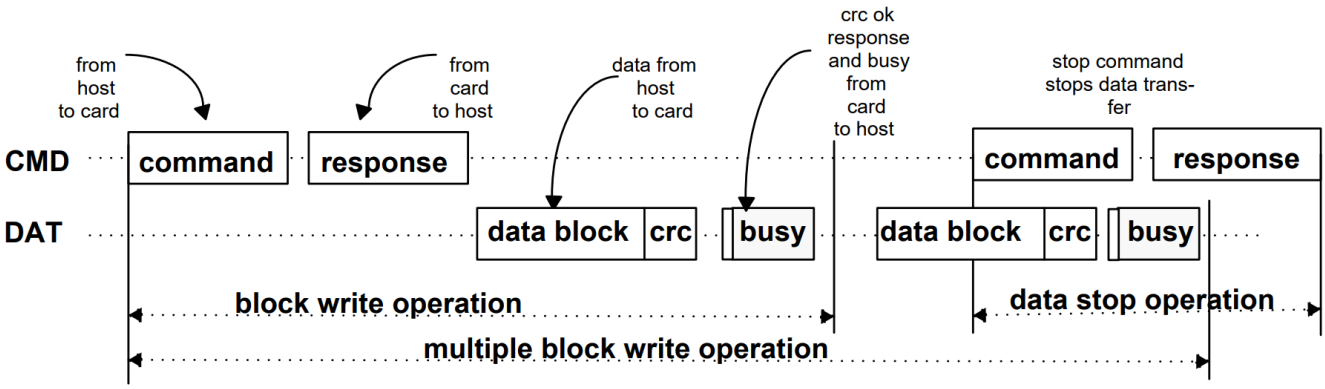
Data transfers to/from the SD Memory Card are done in blocks. Data blocks always were succeeded by CRC bits. Single and multiple block operations are defined. Note that the Multiple Block operation mode is better for faster write operation. A multiple block transmission is terminated when a stop command follows on the CMD line. Data transfer can be configured by the host to use single or multiple data lines.

Figure 6-1-2: (Multiple) Block Read Operation



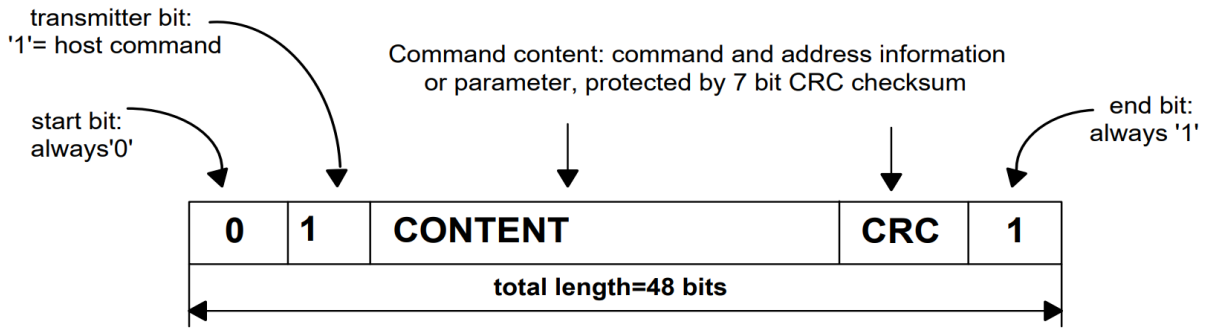
The block write operation uses a simple busy signaling of the write operation duration on the DAT0 data line (see Figure 6-1-3) regardless of the number of data lines used for transferring the data.

Figure 6-1-3: (Multiple) Block Write Operation



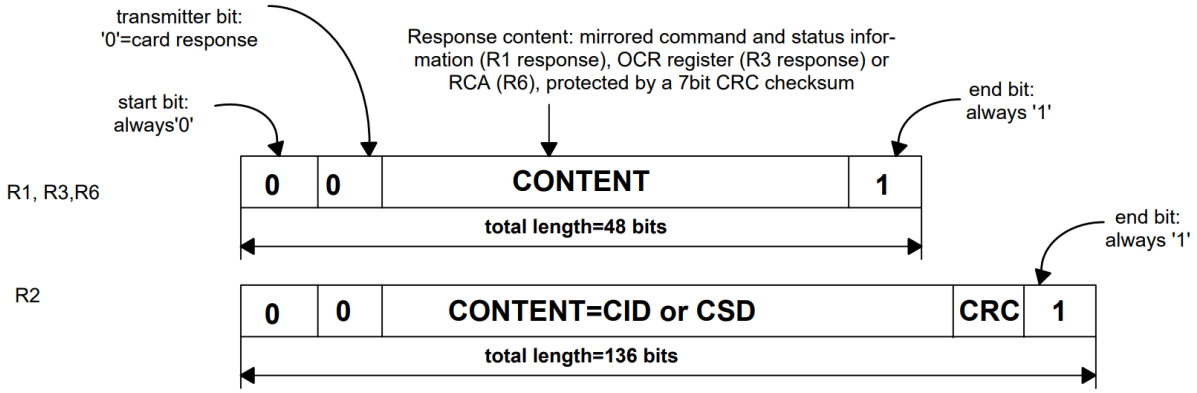
Command tokens have the following coding scheme:

Figure 6-1-4: Command Token Format



Each command token is preceded by a start bit (0) and succeeded by an end bit (1). The total length is 48 bits. Each token is protected by CRC bits so that transmission errors can be detected and the operation may be repeated. Response tokens have one of four coding schemes, depending on their content. The token length is either 48 or 136 bits. The CRC protection algorithm for block data is a 16-bit CCITT polynomial.

Figure 6-1-5: Response Token Format

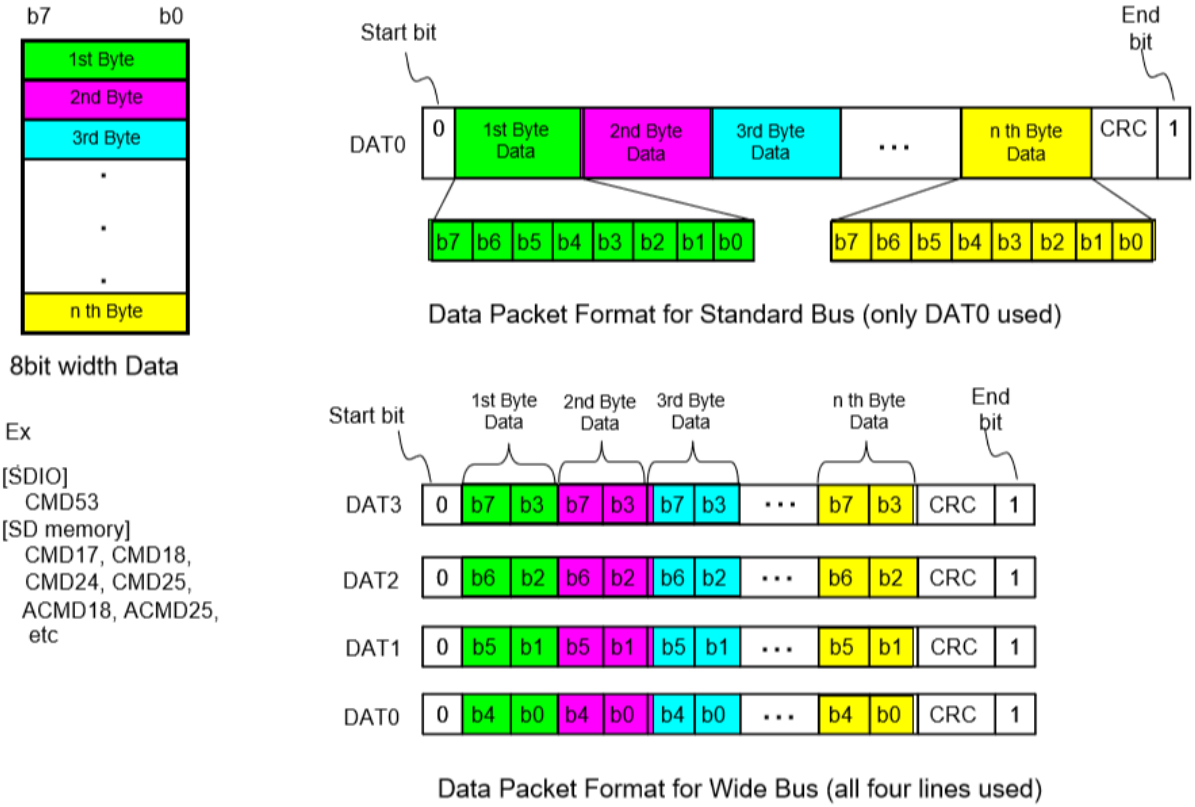


In the CMD line the Most Significant Bit (MSB) bit is transmitted first the Least Significant Bit (LSB) bit is the last. When the wide bus option is used, the data is transferred 4 bits at a time. Start and end bits, as well as the CRC bits, are transmitted for every one of the DAT lines. CRC bits are calculated and checked for every DAT line individually. The CRC status response and Busy indication will be sent by the card to the host on DAT0 only (DAT1-DAT3 during that period are don't care).

There are two types of Data packet format for the SD card.

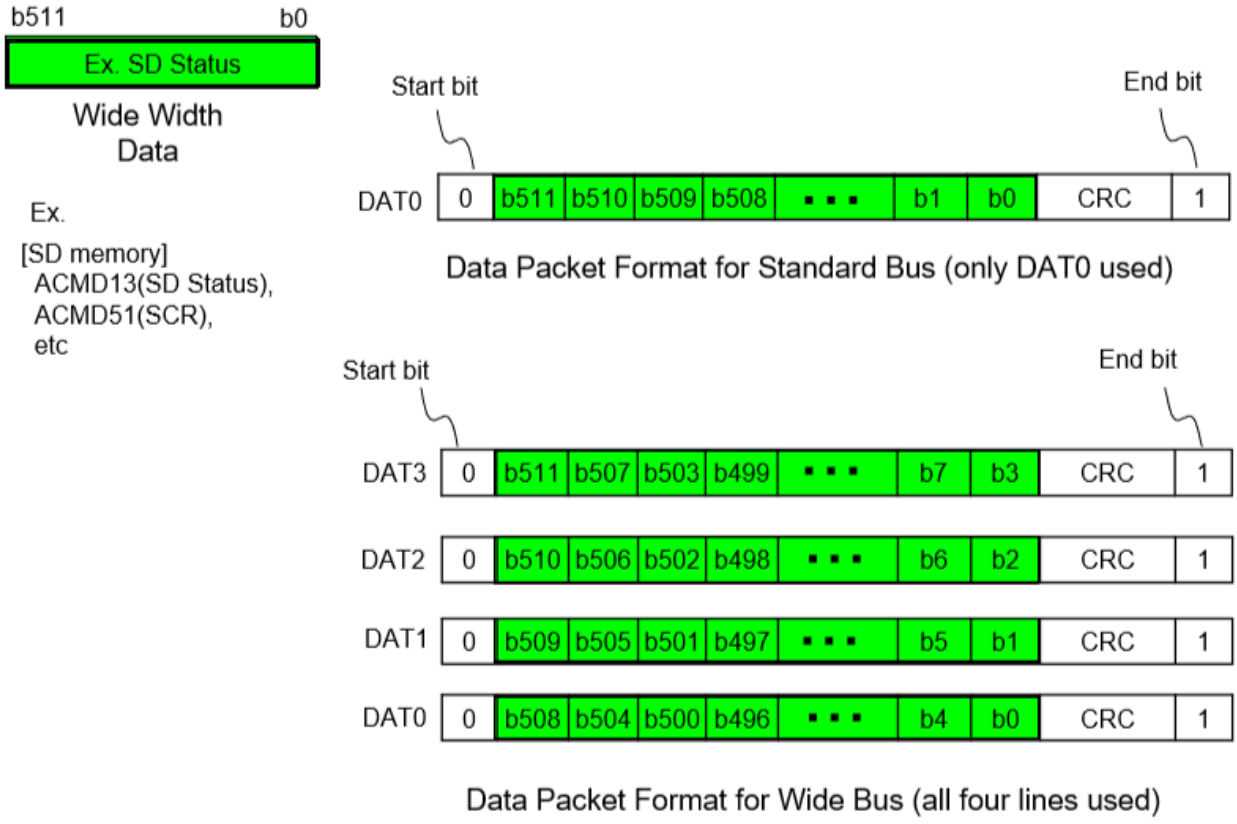
(1) Usual data (8 bit width) The usual data (8 bit width) are sent in LSB (Least Significant Byte) first, MSB (Most Significant Byte) last manner. But in the individual byte it is MSB (Most Significant Bit) first, LSB (Least Significant Bit) last.

Figure 6-1-6: Data packet format - Usual data



(2)Wide width data (SD Memory Register) The wide width data is shifted from MSB bit.

Figure 6-1-7: Data packet format - Wide width data



6.2 Command

6.2.1 Command Types and Format

All communication between host and cards is controlled by the host (master). The host sends commands of two types: broadcast and addressed (point-to-point) commands.

Broadcast commands

Broadcast commands are intended for all cards. Some of these commands require a response.

Addressed (point-to-point) commands

The addressed commands are sent to the addressed card and cause a response from this card.

Command Format

All commands have a fixed code length of 48 bits, needing a transmission time of 2.4 µs @ 20 MHz

Table 6-2-1: Command Format

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'1'	x	x	x	'1'
Description	Start bit	Transmission bit	Command index	Argument	CRC7	End bit

A command always starts with a start bit (always ‘0’), followed by the bit indicating the direction of transmission (host = ‘1’). The next 6 bits indicate the index of the command, this value being interpreted as a binary coded number (between 0 and 63). Some commands need an argument (e.g. an address), which is coded by 32 bits. A value denoted by ‘x’ in the table above indicates this variable is dependent on the command. All commands are protected by a CRC. Every command codeword is terminated by the end bit (always ‘1’). All commands and their arguments are listed in Table 6-2-1.

6.2.2 Command Classes

The command set of the SD Memory Card system is divided into several classes (See Table 6-2-2). Each class supports a set of card functionalities.

Class 0, 2, 4, 5 and 8 are mandatory supported by ATP SD Cards. Class 7 except CMD40 is mandatory for SDHC and SDXC. The other classes are optional. The supported Card Command Classes (CCC) are coded as a parameter in the card specific data (CSD) register of each card, providing the host with information on how to access the card.

If different types of commands are assigned to a Command Class (Class 7, Class 8 and Class 11), which command supported can be determined by referring command support information in SCR register.

Table 6-2-2: Card Command Classes (CCCs)

Card Command Class (CCC)	0	1	2	3	4	5	6	7	8	9	10	11
	basic	Command Queue	block read	reserved	block write	erase	write protec-tion	lock card	application specific	I/O mode	switch	extension
CMD0	+											
CMD2	+											
CMD3	+											
CMD4	+											
CMD5										+		
CMD6											+	
CMD7	+											
CMD8	+											
CMD9	+											
CMD10	+											
CMD11	+											
CMD12	+											
CMD13	+											
CMD15	+											
CMD16			+		+			+				
CMD17			+									
CMD18			+									
CMD19			+									
CMD20			+		+							
CMD21												+
CMD23			+		+							
CMD24					+							
CMD25					+							
CMD27					+							
CMD28							+					
CMD29							+					
CMD30							+					
CMD32						+						
CMD33						+						
CMD34-37											+	
CMD38						+						
CMD40								+				
CMD42								+				
CMD43-47		+										
CMD48												+
CMD49												+
CMD50											+	
CMD52										+		
CMD53										+		

Card Command Class (CCC)	0	1	2	3	4	5	6	7	8	9	10	11
	basic	Command Queue	block read	reserved	block write	erase	write protec-tion	lock card	application specific	I/O mode	switch	extension
CMD55									+			
CMD56									+			
CMD57											+	
CMD58												+
CMD59												+
ACMD6									+			
ACMD13									+			
ACMD14									+			
ACMD15									+			
ACMD16									+			
ACMD22									+			
ACMD23									+			
ACMD28									+			
ACMD41									+			
ACMD42									+			
ACMD51									+			

6.2.3 Detailed CommandDescription

The following tables define in detail all SD Memory Card bus commands.

Table 6-2-31: Basic commands (class 0)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD0	bc	[31:0] stuff bits	-	GO_IDLE_STATE	Resets all cards to idle state
CMD1	reserved				
CMD2	bcr	[31:0] stuff bits	R2	ALL_SEND_CID	Asks any card to send the CID numbers on the CMD line (any card that is connected to the host will respond)
CMD3	bcr	[31:0] stuff bits	R6	SEND_RELATIVE_ ADDR	Ask the card to publish a new relative address (RCA)
CMD4	bc	[31:16] DSR [15:0] stuff bits	-	SET_DSR	Programs the DSR of all cards
CMD5	reserved for I/O cards (refer to "SDIO Card Specification")				
CMD7	ac	[31:16] RCA [15:0] stuff bits	R1b (only from the selecte d card)	SELECT/DESELECT_ CARD	Command toggles a card between the stand-by and transfer states or between the programming and disconnect states. In both cases, the card is selected by its own relative address and gets deselected by any other address; address 0 deselects all. In the case that the RCA equals 0, then the host may do one of the following: - Use other RCA number to perform card de-selection. - Re-send CMD3 to change its RCA number to other than 0 and then use CMD7 with RCA=0 for card de-selection.
CMD8	bcr	[31:12]reserved bits [11:8]supply voltage(VHS) [7:0]check pattern	R7	SEND_IF_COND	Sends SD Memory Card interface condition, which includes host supply voltage information and asks the card whether card supports voltage. Reserved bits shall be set to '0'.
CMD9	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CSD	Addressed card sends its card-specific data (CSD) on the CMD line.
CMD10	ac	[31:16] RCA [15:0] stuff bits	R2	SEND_CID	Addressed card sends its card identification (CID) on CMD the line.
CMD11	ac	[31:0] reserved bits (all 0)	R1	VOLTAGE_SWITCH	Switch to 1.8V bus signaling level.
CMD12	ac	[31:0] stuff bits	R1b	STOP_ TRANSMISSION	Forces the card to stop transmission

CMD INDEX	type	argument	resp	abbreviation	command description
CMD13	ac	[31:16] RCA [15] Send Task Status Register [14:0] stuff bits	R1	SEND_STATUS/SEND_TASK_STATUS	CQ not enabled: [15] = '0' or '1', Addressed card sends its status register CQ enabled: [15]='0', Addressed card sends its status register. [15]='1', Addressed card sends task status register.
CMD14	Reserved				
CMD15	ac	[31:16] RCA [15:0] reserved bits	-	GO_INACTIVE_STATE	Sends an addressed card into the *Inactive State*. This command is used when the host explicitly wants to deactivate a card. Reserved bits shall be set to '0'.

CMD INDEX	type	argument	resp	abbreviation	command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	In the case of a Standard Capacity SD Memory Card, this command sets the block length (in bytes) for all following block commands (read, write, lock). Default block length is fixed to 512 Bytes. Set length is valid for memory access commands only if partial block read operation are allowed in CSD. In the case of SDHC and SDXC Cards, block length set by CMD16 command does not affect memory read and write commands. Always 512 Bytes fixed block length is used. This command is effective for LOCK_UNLOCK command. In both cases, if block length is set larger than 512Bytes, the card sets the BLOCK_LEN_ERROR bit. In DDR50 mode, data is sampled on both edges of the clock. Therefore, block length shall always be even.
CMD17	adtc	[31:0] data address[2]	R1	READ_SINGLE_ BLOCK	In the case of a Standard Capacity SD Memory Card, this command, this command reads a block of the size selected by the SET_BLOCKLEN command. [1] In case of SDHC and SDXC Cards, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command.

Table 6-2-32: Block oriented read commands (class 2)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD18	adtc	[31:0] data address[2]	R1	READ_MULTIPLE_ BLOCK	Continuously transfers data blocks from card to host until interrupted by a STOP_TRANSMISSION command. Block length is specified the same as READ_SINGLE_BLOCK command.
CMD19	adtc	[31:0] reserved bits (all 0)	R1	SEND_TUNING_ BLOCK	64 bytes tuning pattern is sent for SDR50 and SDR104.
CMD20	ac	[31:28]Speed Class Control [27:0]See command description	R1b	SPEED_CLASS_CON TROL	Speed Class control command. [27:0] Speed Class - 4.13.2.8 [27:0] UHS Speed Grade - See section 4.13.2.8 [27:0] Video Speed Class - See section 4.13.4.7
CMD22	reserved				
CMD23	ac	[31:0] Block Count	R1	SET_BLOCK_COUNT	Specify block count for CMD18 and CMD25.

1) The data transferred shall not cross a physical block boundary unless READ_BLK_MISALIGN is set in theCSD.
2) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 Bytes unit).

Table 6-2-33: Block oriented write commands (class 4)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	See description in Table 4-24
CMD20	ac	[31:28]Speed Class Control [27:0]See command description	R1b	SPEED_CLASS_CONTROL	Speed Class control command. [27:0] Speed Class - 4.13.2.8 [27:0] UHS Speed Grade - See Section 4.13.2.8 [27:0] Video Speed Class - See Section 4.13.4.7
CMD23	ac	[31:0] Block Count	R1	SET_BLOCK_COUNT	Specify block count for CMD18 and CMD25.
CMD24	adtc	[31:0] data address[2]	R1	WRITE_BLOCK	In case of SDSC Card, block length is set by the SET_BLOCKLEN command[1]. In case of SDHC and SDXC Cards, block length is fixed 512 Bytes regardless of the SET_BLOCKLEN command.
CMD25	adtc	[31:0] data address[2]	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows. Block length is specified the same as WRITE_BLOCK command.
CMD26	Reserved For Manufacturer				
CMD27	adtc	[31:0] stuff bits	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.

1) The data transferred shall not cross a physical block boundary unless WRITE_BLK_MISALIGN is set in the CSD. In the case that write partial blocks is not supported, then the block length=default block length (given in CSD).
2) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 bytes unit).

Table 6-2-34: Block oriented write protection commands (class 6)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD28	ac	[31:0] data address[2]	R1b	SET_WRITE_PROT	If the card has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE). SDHC and SDXC Cards do not support this command.
CMD29	ac	[31:0] data address[2]	R1b	CLR_WRITE_PROT	If the card provides write protection features, this command clears the write protection bit of the addressed group. SDHC and SDXC Cards do not support this command.
CMD30	adtc	[31:0] write protect data address[2]	R1	SEND_WRITE_ PROT	If the card provides write protection features, this command asks the card to send the status of the write protection bits.[1] SDHC and SDXC Cards do not support this command.
CMD31	Reserved				

1) 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data line. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last groups are outside the valid range, then the corresponding write protection bits shall be set to 0.
2) Data address is in byte units in a Standard Capacity SD Memory Card.

Table 6-2-35: Erase commands (class 5)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD32	ac	[31:0] data address[1]	R1	ERASE_WR_BLK_ START	Sets the address of the first write block to be erased.
CMD33	ac	[31:0] data address[1]	R1	ERASE_WR_BLK_END	Sets the address of the last write block of the continuous range to be erased.
CMD38	ac	[31:0] Erase Function	R1b	ERASE	Erase Function 00000001h = Discard 00000002h = FULE Others = Erase
CMD39	Reserved				
CMD41	Reserved				

1) SDSC Card (CCS=0) uses byte unit address and SDHC and SDXC Cards (CCS=1) use block unit address (512 bytes unit).
2) CMD40 is moved to Class 7.

Table 6-2-36: Lock card (class 7)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	See description in Table 4-24
CMD40	adtc	Defined by DPS Spec.	R1	Defined by DPS Spec.	Single block read type. Available even if card is locked.
CMD42	adtc	[31:0] Reserved bits (Set all 0)	R1	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command. Reserved bits in the argument and in Lock Card Data Structure shall be set to 0.
CMD51	reserved				

Table 6-2-37: Application specific commands (class 8)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD55	ac	[31:16] RCA [15:0] stuff bits	R1	APP_CMD	Indicates to the card that the next command is an application specific command rather than a standard command
CMD56	adtc	[31:1] stuff bits. [0]: RD/WR	R1	GEN_CMD	Used either to transfer a data block to the card or to get a data block from the card for general purpose/application specific commands. In case of a SDSC Card, block length is set by the SET_BLOCK_LEN command. In case of SDHC and SDXC Cards, block length is fixed to 512 bytes. The host sets RD/WR=1 for reading data from the card and sets to 0 for writing data to the card.
CMD60-63	reserved for manufacturer				

All the application-specific commands (given in Table 6-2-9) are supported if Class 8 is allowed (mandatory in SD Memory Card).

Table 6-2-38: I/O mode commands (class 9)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD52-54	Commands for SDIO (refer to "SDIO Card Specification")				

All future reserved commands shall have a codeword length of 48 bits, as well as their responses (if there are any).

The following table describes all the application specific commands supported/reserved by the SD Card. All the following ACMDs shall be preceded with APP_CMD command (CMD55).

Table 6-2-39: Application Specific Commands used/reserved by SDCard

ACMD INDEX	type	argument	resp	abbreviation	command description
ACMD1-5	Reserved				
ACMD6	ac	[31:2] stuff bits [1:0]bus width	R1	SET_BUS_WIDTH	Defines the data bus width ('00'=1bit or '10'=4 bits bus) to be used for data transfer. The allowed data bus widths are given in SCR register.
ACMD7-12	Reserved				
ACMD13	adtc	[31:0] stuff bits	R1	SD_STATUS	Send the SD Status. The status fields are given in Table 4-44.
ACMD14-16	Reserved for DPS Specification				
ACMD17	Reserved				
ACMD18	Reserved for SD security applications[1]				
ACMD19-21	Reserved				
ACMD22	adtc	[31:0] stuff bits	R1	SEND_NUM_WR_ BLOCKS	Send the number of the written (with-out errors) write blocks. Responds with 32bit+CRC data block. If WRITE_BL_PARTIAL='0', the unit of ACMD22 is always 512 byte. If WRITE_BL_PARTIAL='1', the unit of ACMD22 is a block length which was used when the write command was executed.
ACMD23	ac	[31:23] stuff bits [22:0]Number of blocks	R1	SET_WR_BLK_ ERASE_COUNT	Set the number of write blocks to be pre-erased before writing (to be used for faster Multiple Block WR com-mand). "1"=default (one wr block)[2].
ACMD24	Reserved				
ACMD25	Reserved for SD security applications[1]				
ACMD26	Reserved for SD security applications[1]				
ACMD27	Shall not use this command				
ACMD28	Reserved for DPS Specification				
ACMD29	Reserved				
ACMD30-35	Reserved for Security Specification				
ACMD36-37	Reserved				
ACMD38	Reserved for SD security applications[1]				
ACMD39-40	Reserved				

1) Refer to the "Part3 Security Specification" for a detailed explanation about the SD Security Features
2) Command STOP_TRAN (CMD12) shall be used to stop the transmission in Write Multiple Block whether or not the pre erase (ACMD23) feature is used.

Table 6-2-310: Switch function commands (class 10)

CMD INDEX	type	argument	resp	abbreviation	command description
CMD6	adtc	[31] Mode 0:Check function 1:Switch function [30:24] reserved (All '0') [23:20] reserved for function group 6 (0h or Fh) [19:16] reserved for function group 5 (0h or Fh) [15:12] function group 4 for Power Limit [11:8] function group 3 for Drive Strength [7:4] function group 2 for Command System [3:0] function group 1 for Access Mode	R1	SWITCH_FUNC	Checks switch-able function (mode 0) and switch card function (mode 1). See Section 4.3.10.
CMD34 CMD35	Reserved for each command system set by switch function command (CMD6). Detailed definition is referred to each command system specification.				

CMD INDEX	type	argument	resp	abbreviation	command description
CMD36 CMD37					
CMD50 CMD57					

6.3 Card State Transition Table

Table 6-3 defines the card state transitions in dependency of the received command. State name in the table is the next state after the command is executed. "-" indicated that the command is treated as illegal command. In addition, whether a command is executable depends on command class (CCC).

Table 6-3: Card state transition table

Commands	Current State									
	idle	ready	ident	stby	tran	data	rcv	prg	dis	ina
"Operation Complete"	-	-	-	-	-	tran	-	tran	stby	-
class 0										
CMD0	idle	idle	idle	idle	idle	idle	idle	idle	idle	-
CMD2	-	ident	-	-	-	-	-	-	-	-
CMD3	-	-	stby	stby	-	-	-	-	-	-
CMD4	-	-	-	stby	-	-	-	-	-	-
CMD7, card is addressed	-	-	-	tran	-	-	-	-	prg	-
CMD7, card is not addressed	-	-	-	stby	stby	stby	-	dis	-	-
CMD8	idle	-	-	-	-	-	-	-	-	-
CMD9	-	-	-	stby	-	-	-	-	-	-
CMD10	-	-	-	stby	-	-	-	-	-	-
CMD11	-	ready	-	-	-	-	-	-	-	-
CMD12	-	-	-	-	-	tran	prg	-	-	-
CMD13	-	-	-	stby	tran	data	rcv	prg	dis	-
CMD15	-	-	-	ina	ina	ina	ina	ina	ina	-
class 2										
CMD16	-	-	-	-	tran	-	-	-	-	-
CMD17	-	-	-	-	data	-	-	-	-	-
CMD18	-	-	-	-	data	-	-	-	-	-
CMD19	-	-	-	-	data	-	-	-	-	-
CMD20	-	-	-	-	prg	-	-	-	-	-
CMD23	-	-	-	-	tran	-	-	-	-	-
class 4										
CMD16	-	-	-	-	tran	-	-	-	-	-
CMD20	-	-	-	-	prg	-	-	-	-	-
CMD23	-	-	-	-	tran	-	-	-	-	-
CMD24	-	-	-	-	rcv	-	-	-	-	-
CMD25	-	-	-	-	rcv	-	-	-	-	-
CMD27	-	-	-	-	rcv	-	-	-	-	-
class 6										
CMD28	-	-	-	-	prg	-	-	-	-	-
CMD29	-	-	-	-	prg	-	-	-	-	-
CMD30	-	-	-	-	data	-	-	-	-	-
class 5										
CMD32	-	-	-	-	tran	-	-	-	-	-
CMD33	-	-	-	-	tran	-	-	-	-	-
CMD38	-	-	-	-	prg	-	-	-	-	-
class 7										

Commands	Current State									
	idle	ready	ident	stby	tran	data	rcv	prg	dis	ina
CMD40	-	-	-	-	data	-	-	-	-	-
CMD42	-	-	-	-	rcv	-	-	-	-	-
class 8										
CMD55	idle	-	-	stby	tran	data	rcv	prg	dis	-
CMD56; RD/WR = 0	-	-	-	-	rcv	-	-	-	-	-
CMD56; RD/WR = 1	-	-	-	-	data	-	-	-	-	-
ACMD6	-	-	-	-	tran	-	-	-	-	-
ACMD13	-	-	-	-	data	-	-	-	-	-
ACMD14-16	Refer to DPS Specification									
ACMD22	-	-	-	-	data	-	-	-	-	-
ACMD23	-	-	-	-	tran	-	-	-	-	-
ACMD28	Refer to DPS Specification									
ACMD18,25,26,38, 43,44,45,46,47,48,49	Refer to "Part3 Security Specification" for information about the SD Security Features									
ACMD41, OCR check is OK and card is not busy	ready	-	-	-	-	-	-	-	-	-
ACMD41, OCR check is OK and card is busy[2]	idle	-	-	-	-	-	-	-	-	-
ACMD41, OCR check fails	ina	-	-	-	-	-	-	-	-	-
ACMD41, query mode	idle	-	-	-	-	-	-	-	-	-
ACMD42	-	-	-	-	tran	-	-	-	-	-
ACMD51	-	-	-	-	data	-	-	-	-	-
class 9										
CMD52-CMD54	Refer to "SDIO Card Specification"									
class 10[1]										
CMD6	-	-	-	-	data	-	-	-	-	-
CMD34-37,50,57	Refer to each command system specification									
class 11										
CMD21	Refer to DPS Specification									
CMD48	-	-	-	-	data	-	-	-	-	-
CMD49	-	-	-	-	rcv	-	-	-	-	-
CMD58	-	-	-	-	data	-	-	-	-	-
CMD59	-	-	-	-	rcv	-	-	-	-	-
CMD41	reserved									
CMD60...CMD63	reserved for manufacturer									
class 1										
CMD43-CMD47	Illegal command in Non CQ mode. Refer to Table 4-75 for Card state transition in CQ mode									

Note (1): Class 10 commands were defined in Version 1.10.
Note (2): Card returns busy in case of following. - Card executes internal initialization process
- When HCS in the argument is set to 0 to SDHC or SDXC Card.

6.4 Responses

All responses are sent via the command line CMD. The response transmission always starts with the left bit of the bit string corresponding to the response codeword. The code length depends on the response type.
A response always starts with a start bit (always 0), followed by the bit indicating the direction of transmission (card = 0). A value denoted by 'x' in the tables below indicates a variable entry. All responses except the type R3 (see below) are protected by a CRC. Every command codeword is terminated by the end bit (always 1).
There are five types of responses for the SD Memory Card. The SDIO Card supports additional response types named R4 and R5. Refer to SDIO Card Spec for detailed information on the SDIO commands and responses. Their formats are defined as follows:

6.4.1 R1 (Normal Response Command)

Code length is 48 bits. The bits 45:40 indicate the index of the command to be responded to, this value being interpreted as a binary coded number (between 0 and 63). The status of the card is coded in 32 bits. Note that if a data transfer to the card is involved, then a busy signal may appear on the data line after the transmission of each block of data. The host shall check for busy after data block transmission.

Table 6-4-1 Response R1

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	x	x	x	'1'
Description	start bit	transmission bit	command index	card status	CRC7	end bit

6.4.2 R1b

R1b is identical to R1 with an optional busy signal transmitted on the data line. The card may become busy after receiving these commands based on its state prior to the command reception. The Host shall check for busy at the response.

6.4.3 R2 (CID, CSD register)

Code length is 136 bits. The contents of the CID register are sent as a response to the commands CMD2 and CMD10. The contents of the CSD register are sent as a response to CMD9. Only the bits [127...1] of the CID and CSD are transferred, the reserved bit [0] of these registers is replaced by the end bit of the response.

Table 6-4-3: Response R2

Bit position	135	134	[133:128]	[127:1]	0
Width (bits)	1	1	6	127	1
Value	'0'	'0'	'111111'	x	'1'
Description	start bit	transmission bit	reserved	CID or CSD register incl. internal CRC7	end bit

6.4.4 R3 (OCR Register)

Code length is 48 bits. The contents of the OCR register are sent as a response to ACMD41

Table 6-4-4: Response R3

Bit position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	x	'1111111'	'1'
Description	start bit	transmission bit	reserved	OCR register	reserved	end bit

6.4.5 R6 (Published RCA response)

Code length is 48 bit. The bits 45:40 indicate the index of the command to be responded to - in that case, it will be '000011' (together with bit 5 in the status bits it means = CMD3). The 16 MSB bits of the argument field are used for the Published RCA number.

Table 6-4-5: Response R6

Bit position	47	46	[45:40]	[39:8] Argument field		[7:1]	0
Width (bits)	1	1	6	16	16	7	1
Value	'0'	'0'	x	x	x	x	'1'
Description	start bit	transmission bit	command index ('000011')	New published RCA [31:16] of the card	[15:0] card status bits: 23,22,19,12:0 (see Table 4-36)	CRC7	end bit

6.4.6 R7 (Card interface condition)

Code length is 48 bits. The card support voltage information is sent by the response of CMD8. Bits 19- 16 indicate the voltage range that the card supports. The card that accepted the supplied voltage returns R7 response. In the response, the card echoes back both the voltage range and check pattern set in the argument.

Table 6-4-61: Response R7

Bit position	47	46	[45:40]	[39:20]	[19:16]	[15:8]	[7:1]	0
Width (bits)	1	1	6	20	4	8	7	1
Value	'0'	'0'	'001000'	'00000h'	x	x	x	'1'
Description	Start bit	Transmission bit	Command index	Reserved bits	Voltage accepted	Echo-back of check pattern	CRC7	End bit

Table 6-4-62 shows the format of 'voltage accepted' in R7

Voltage accepted	Value Definition
0000b	Not Defined
0001b	2.7-3.6V
0010b	Reserved for Low Voltage Range
0100b	Reserved
1000b	Reserved
Others	Not Defined

6.5 SD Card Status

The SD Memory Card supports three card status fields as follows:

- 'Card Status': Error and state information of a executed command, indicated in the response.
- 'SD Status': Extended status field of 512bits that supports special features of the SD Memory Card and future Application Specific features.
- 'Task Status'. Status information of queued tasks in CQ mode, indicated in the response. CMD13 R1 indicates either Card Status or Task Status by selecting b[15] of CMD13 argument. R1 of the other commands indicates only Card Status.

6.5.1 Card Status

The response format R1 contains a 32-bit field named card status as a response to CMD13 with argument b[15]='0'. This field is intended to transmit the card's status information (which may be stored in a local status register) to the host. If not specified otherwise, the status entries are always related to the previous issued command. Table 6-5-11 defines the different entries of the status. Unused reserved bits shall be set to 0. The type and clear condition fields in the table are abbreviated as follows:

Type:

E: Error bit. S:
Status bit.
R: Detected and set for the actual command response.
X: Detected and set during command execution. The host can get the status by issuing a command with R1 response.

Clear Condition:

A: According to the card current state.
B: Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).
C: Clear by read.

Table 6-5-11: Card status

Bits	Identifier	Type	Value	Description	Clear Condition
31	OUT_OF_RANGE	E R X	'0'= no error '1'= error	The command's argument was out of the allowed range for this card.	C
30	ADDRESS_ERROR	E R X	'0'= no error '1'= error	A misaligned address which did not match the block length was used in the command.	C
29	BLOCK_LEN_ERROR	E R X	'0'= no error '1'= error	The transferred block length is not allowed for this card, or the number of transferred bytes does not match the block length.	C
28	ERASE_SEQ_ERROR	E R	'0'= no error '1'= error	An error in the sequence of erase commands occurred.	C
27	ERASE_PARAM	E R X	'0'= no error '1'= error	An invalid selection of write-blocks for erase occurred.	C
26	WP_VIOLATION	E R X	'0'= not protected '1'= protected	Set when the host attempts to write to a protected block or to the temporary or permanent write protected card.	C
25	CARD_IS_LOCKED	S X	'0' = card unlocked '1' = card locked	When set, signals that the card is locked by the host	A
24	LOCK_UNLOCK_FAILED	E R X	'0' = no error '1' = error	Set when a sequence or password error has been detected in lock/unlock card command.	C
23	COM_CRC_ERROR	E R	'0'= no error '1'= error	The CRC check of the previous command failed.	B
22	ILLEGAL_COMMAND	E R	'0'= no error '1'= error	Command not legal for the card state	B
21	CARD_ECC_FAILED	E R X	'0'= success '1'= failure	Card internal ECC was applied but failed to correct the data.	C
20	CC_ERROR	E R X	'0'= no error '1'= error	Internal card controller error	C
19	ERROR	E R X	'0'= no error '1'= error	A general or an unknown error occurred during the operation.	C
18	reserved				
17	reserved for DEFERRED_RESPONSE (Refer to eSD Addendum)				
16	CSD_OVERWRITE	E R X	'0'= no error '1'= error	Can be either one of the following errors: - The read only section of the CSD does not match the card content. - An attempt to reverse the copy (set as original) or permanent WP (unprotected) bits was made.	C
15	WP_ERASE_SKIP	E R X	'0'= not protected '1'= protected	"Set when only partial address space was erased due to existing write protected blocks or the temporary or permanent write protected card was erased.	C

Bits	Identifier	Type	Value	Description	Clear Condition
14	CARD_ECC_DISABLED	S X	'0'= enabled '1'= disabled	The command has been executed without using the internal ECC.	A
13	ERASE_RESET	S R	'0'= cleared '1'= set	An erase sequence was cleared before executing because an out of erase sequence command was received	C
12:9	CURRENT_STATE	S X	0 = idle 1 = ready 2 = ident 3 = stby 4 = tran 5 = data 6 = rcv 7 = prg 8 = dis 9-14 = reserved 15 = reserved for I/O mode	The state of the card when receiving the command. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as a binary coded number between 0 and 15.	B
8	READY_FOR_DATA	S X	'0'= not ready '1'= ready	Corresponds to buffer empty signaling on the bus	A
7	reserved				
6	FX_EVENT	SX	'0'= No event '1'= Event invoked	Extension Functions may set this bit to get host to deal with events.	A
5	APP_CMD	S R	'0' = Disabled '1' = Enabled	The card will expect ACMD, or an indication that the command has been interpreted as ACMD	C
4	reserved for SD I/O Card				
3	AKE_SEQ_ERROR (SD Memory Card app. spec.)	E R	'0' = no error '1' = error	Error in the sequence of the authentication process	C
2	reserved for application specific commands				
1, 0	reserved for manufacturer test mode				

For each command responded by R1 response, following table defines the affected bits in the status field. An 'x' means the error/status bit may be set in the response to the respective command.

Table 6-5-12: Card status field / command - cross reference

CMD Number	Response Format Card Status Bit Number																					
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12:9	8	6	5
3[1]									x	x			x							x			
6[2]	x						x		x	x	x	x	x							x		x	
7					x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
11							x		x	x			x							x			
12	x	x				x	x		x	x	x	x	x					x		x		x	

CMD Number	Response Format Card Status Bit Number																						
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12:9	8	6	5
13	x	x			x	x	x	x	x	x	x	x	x			x	x	x		x	x	x	
16			x		x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
17	x	x			x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
18	x	x			x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
19	x	x			x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
20	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
23	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
24	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
25	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
26					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
27					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
28	x				x	x	x	x	x	x	x	x	x			x	x	x	x	x			
29	x				x	x	x	x	x	x	x	x	x			x	x	x	x	x			
30	x				x	x	x	x	x	x	x	x	x			x	x	x	x	x			
32	x			x	x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
33	x			x	x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
38	x			x	x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
40	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
42					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	
43						x	x		x	x		x	x					x	x	x		x	
44						x	x		x	x		x						x	x	x		x	
45						x	x		x	x		x						x	x	x		x	
46	x					x	x		x	x	x	x	x					x	x	x		x	
47	x					x	x		x	x		x	x					x	x	x	x	x	
48	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
49	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
55					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	x
56					x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	x
58	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
59	x	x	x		x	x	x	x	x	x	x	x	x			x	x	x	x	x	x	x	
ACMD6	x				x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	x
ACMD13					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	x
ACMD22					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	x
ACMD23					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	x
ACMD42					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	x
ACMD51					x	x	x	x	x	x	x	x	x			x	x	x	x	x		x	x

(1) The response to CMD3 is R6 that includes only bits 23, 22, 19 and 12:9 out of the Card Status
(2) This command was defined in version 1.10
(3) Bit 06 will be set in R1 (R1b) response after entering "tran" state.

6.5.2 SD Status

The SD Status contains status bits that are related to the SD Memory Card proprierary features and may be used for future application-specific usage. The size of the SD Status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with a 16-bit CRC. The SD Status is sent to the host over the DAT bus as a response to ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in '*tran_state*' (card is selected). SD Status structure is described in bellow. Unused reserved bits shall be set to 0.
The same abbreviation for 'type' and 'clear condition' were used as for the Card Status above.

Table 6-5-21: SD Card Status

Bits	Identifier	Type	Value	Description	Clear Condi - tion
511: 510	DAT_BUS_WIDTH	S R	'00'= 1 (default) '01'= reserved '10'= 4 bit width '11'= reserved	Shows the currently defined data bus width that was defined by SET_BUS_WIDTH command	A
509	SECURED_MODE	S R	'0'= Not in the Mode '1'= In Secured Mode	Shows if the card is in the secured mode of operation or not.	A
508:502	Reserved for Security Functions				
501:496	Reserved				
495: 480	SD_CARD_TYPE	SR	'00xxh'= SD Memory Cards as defined by this document ('x'=don't care). The following cards are currently defined: '0000h'= Regular SD RD/WR Card. '0001h'= SD ROM Card '0002h'=OTP	In the future, the 8 LSBs will be used to define different variations of an SD Memory Card (Each bit will define different SD Types).	A
479: 448	SIZE_OF_PROTECTED_AREA	SR	Size of protected area	The actual area = (SIZE_OF_PROTECTED_AREA) * MULT * BLOCK_LEN.	A
447: 440	SPEED_CLASS	SR	Speed Class of the card (See below)	(See below)	A
439: 432	PERFORMANCE_MOVE	SR	Performance of move indicated by 1 [MB/s] step. (See below)	(See below)	A
431: 428	AU_SIZE	SR	Size of AU (See below)	(See below)	A
427:	reserved				
424					

423:408	ERASE_SIZE	SR	Number of AUs to be erased at a time	(See below)	A
407:402	ERASE_TIMEOUT	SR	Timeout value for erasing areas specified by UNIT_OF_ERASE_AU	(See below)	A
401:400	ERASE_OFFSET	SR	Fixed offset value added to erase time.	(See below)	A
399:396	UHS_SPEED_GRADE	S R	Speed Grade for UHS mode	(See below)	A
395:392	UHS_AU_SIZE	S R	Size of AU for UHS mode	(See below)	A
391:384	VIDEO_SPEED_CLASS	S R	Video Speed Class value of the card	(See below)	A
383:378	reserved				
377:368	VSC_AU_SIZE	S R	AU size in MB for Video Speed Class	(See below)	A
367:346	SUS_ADDR	S R	Suspension Address	(See below)	A
345:340	reserved				
339:336	APP_PERF_CLASS	S R	Application Performance Class Value of the card	(See below)	A
335:328	PERFORMANCE_ENHANCE	S R	Support for Performance Enhancement functionalities	(See below)	A
327:314	reserved				
313	DISCARD_SUPPORT	S R	‘0’ Not Supported ‘1’ Supported	Discard Support	A
312	FULE_SUPPORT	S R	‘0’ Not Supported ‘1’ Supported	Full User Area Logical Erase Support	A
311:0	reserved for manufacturer				

SIZE_OF_PROTECTED_AREA

Setting this field differs between Standard and High Capacity Cards.
In the case of a Standard Capacity Card, the capacity of protected area is calculated as follows:
Protected Area = SIZE_OF_PROTECTED_AREA_* MULT * BLOCK_LEN. SIZE_OF_PROTECTED_AREA is specified by the unit in MULT*BLOCK_LEN.
In the case of a High Capacity Card, the capacity of protected area is specified in this field:
Protected Area = SIZE_OF_PROTECTED_AREA
SIZE_OF_PROTECTED_AREA is specified by the unit in byte.

SPEED_CLASS

This 8-bit field indicates the Speed Class. Classes lower than indicated by this field are also effective. For example, Class 10 is indicated, host should consider Class 2 to 6 is also effective.

Table 6-5-22: Speed Class Code Field

SPEED_CLASS	Value Definition
00h	Class 0
01h	Class 2
02h	Class 4
03h	Class 6
04h	Class 10
05h – FFh	Reserved

Application Note: If a Class value indicated in SD Status (including reserved value) is larger than that of host supported, the host should read as any Class can be used with the card

PERFORMANCE_MOVE

This 8-bit field indicates Pm and the value can be set by 1 [MB/sec] step. If the card does not move used RUs, Pm should be considered as infinity. Setting to FFh means infinity. The minimum value of Pm is defined by in Table 6-5-23. Pm is defined for Class 2 to 6 in Default Speed Mode. When host uses Class 10, Pm indicated in SD Status shall be ignored and treated as 0.

Table 6-5-23: Performance Move Field

PERFORMANCE_MOVE	Value Definition
00h	Sequential Write
01h	1 [MB/sec]
02h	2 [MB/sec]
.....	.....
FEh	254 [MB/sec]
FFh	Infinity

AU_SIZE

This 4-bit field indicates AU Size and the value can be selected in power of 2 from 16 KB.

Table 6-5-24: AU_SIZE Field

AU_SIZE	Value Definition
0h	Not Defined
1h	16 KB
2h	32 KB
3h	64 KB
4h	128 KB
5h	256 KB
6h	512 KB
7h	1 MB
8h	2 MB
9h	4 MB
Ah	8 MB
Bh	12 MB
Ch	16 MB
Dh	24 MB
Eh	32 MB
Fh	64 MB

The maximum AU size, depends on the card capacity, is defined in Table 6-5-25. The card can set any AU size specified in Table 6-5-24 that is less than or equal to the maximum AU size. The card should set smaller AU size as much as possible.

Table 6-5-25: Maximum AU size

Capacity	up to 64MB	up to 256MB	up to 512MB	up to 32GB	up to 2TB
Maximum AU Size	512 KB	1 MB	2 MB	4 MB	64 MB

Application Notes: The host should determine host buffer size based on total busy time of 4MB and the card supported class. The host can treat multiple AUs combined as one unit.

ERASE_SIZE

This 16-bit field indicates N_{ERASE}. When N_{ERASE} numbers of AUs are erased, the timeout value is specified by ERASE_TIMEOUT (Refer to ERASE_TIMEOUT). The host should determine proper number of AUs to be erased in one operation so that the host can indicate progress of erase operation. If this field is set to 0, the erase timeout calculation is not supported.

Table 6-5-26: Erase Size Field

ERASE_SIZE	Value Definition
0000h	Erase Time-out Calculation is not supported.
0001h	1 AU
0002	2 AU
0003	3 AU
.....	.....
FFFFh	65535 AU

ERASE_TIMEOUT

This 6-bit field indicates the T_{ERASE} and the value indicates erase timeout from offset when multiple AUs are erased as specified by ERASE_SIZE. The range of ERASE_TIMEOUT can be defined as up to 63 seconds and the card manufacturer can choose any combination of ERASE_SIZE and ERASE_TIMEOUT depending on the implementation. Once ERASE_TIMEOUT is determined, it determines the ERASE_SIZE. If ERASE_SIZE field is set to 0, this field shall be set to 0.

Table 6-5-27: Erase Timeout Field

ERASE_TIMEOUT	Value Definition
00	Erase Time-out Calculation is not supported.
01	1 [sec]
02	2 [sec]
03	3 [sec]
.....	.....
63	63 [sec]

ERASE_OFFSET

This 2-bit field indicates the T_{OFFSET} and one of four values can be selected. The erase offset adjusts the line by moving in parallel on the upper side. This field is meaningless if ERASE_SIZE and ERASE_TIMEOUT fields are set to 0.

Table 6-5-28: Erase Offset Field

ERASE_OFFSET	Value Definition
0h	0 [sec]
1h	1 [sec]
2h	2 [sec]
3h	3 [sec]

UHS_SPEED_GRADE

This 4-bit field indicates the UHS mode Speed Grade. Reserved values are for future speed grades larger than the highest defined value. Host shall treat reserved values (undefined) as highest grade defined.

Table 6-5-29: UHS_SPEED_GRADE Field

UHS_SPEED_GRADE	Value Definition
0h	Less than 10MB/sec
1h	10MB/sec and above
2h	Reserved
3h	30MB/sec and above
4h – Fh	Reserved

UHS_AU_SIZE

This 4-bit field indicates AU Size for UHS Speed Grade of UHS-I and UHS-II cards. Card should set smaller

value as much as possible. Host shall refer to UHS_AU_SIZE instead of AU_SIZE when the card is operating as UHS Speed Grade in UHS-I or UHS-II bus speed modes.

Table 6-5-30: UHS_AU_SIZE Field

UHS_SPEED_GRADE	Value Definition
0h	Not Defined
1h – 6h	Not Used
7h	1 MB
8h	2 MB
9h	4 MB
Ah	8 MB
Bh	12 MB
Ch	16 MB
Dh	24 MB
Eh	32 MB
Fh	64 MB

VIDEO_SPEED_CLASS

Table 6-5-31 defines an 8-bit field that indicates the Video Speed Class supported by the card. The Video Speed Class defined in the table shall be equal or less than the minimum write performance of the card in Video Speed Class (e.g., Video Speed Class 6 supports at least 6MB/s). Any Video Speed Class lower than the specified Video Speed Class value shall also be supported (e.g., if the value in this field is 1Eh, then Video Speed Class 10 and Video Speed Class 6 are supported).

Table 6-5-31: VIDEO_SPEED_CLASS Field

VIDEO_SPEED_CLASS	Value Definition
0(=00h)	Video Speed Class 0 (Video Speed Class is not supported)
6(=06h)	Video Speed Class 6
10(=0Ah)	Video Speed Class 10
30(=1Eh)	Video Speed Class 30
60(=3Ch)	Video Speed Class 60
90(=5Ah)	Video Speed Class 90
Others	Reserved

VSC_AU_SIZE

Table 6-5-32 defines a 10-bit field that indicates the AU Size for Video Speed Class recording. It is recommended that cards report the smallest value if multiple values are valid. This field shall be set to one of the specified AU sizes described in Table 6-5-33 or zero (e.g., if VSC_AU_SIZE is 480MB, 1E0h (=480) is set in this field). Note that the other values which are not specified in Table 6-5-33 are reserved. Since these reserved values may be assigned by SDA in future, card manufacturers shall not use these reserved values until SDA defines those in future versions of specification.

And SU size is also determined by this field, because a unique SU size is bound for each AU size. For example, if VSC_AU_SIZE is set as 160MB, SU size is 8MB as shown in Table 6-5-33.

SDHC cards shall have a minimum of 40 AU blocks (e.g., for a 4GB card, AU sizes over 96MB do not result in 40 AUs). SDXC cards shall have a minimum of 80 AU blocks.

Table 6-5-32: VSC_AU_SIZE Field

VSC_AU_SIZE	Value Definition
0	Video Speed Class is not supported
1 to 1023(=3FFh)	AU Size for Video Speed Class of the card in unit of[MB]

Table 6-5-33: Valid AU Size and SU Size

VSC_AU_SIZE	AU Size	SU Size
008h	8 MB	8 MB
010h	16 MB	8 MB
015h	21 MB	7 MB
018h	24 MB	8 MB
01Bh	27 MB	9 MB
01Ch	28 MB	7 MB
01Eh	30 MB	10 MB
020h	32 MB	8 MB
024h	36 MB	9 MB
028h	40 MB	8 MB
02Ah	42 MB	7 MB
02Dh	45 MB	9 MB
030h	48 MB	8 MB
036h	54 MB	9 MB
038h	56 MB	8 MB
03Ch	60 MB	10 MB
040h	64 MB	8 MB
048h	72 MB	8 MB
050h	80 MB	8 MB
060h	96 MB	8 MB
070h	112 MB	8 MB
078h	120 MB	8 MB
080h	128 MB	8 MB
090h	144 MB	8 MB
0A0h	160 MB	8 MB
0C0h	192 MB	8 MB
0D8h	216 MB	8 MB
0E0h	224 MB	8 MB
0F0h	240 MB	8 MB
100h	256 MB	8 MB
120h	288 MB	8 MB
140h	320 MB	8 MB
180h	384 MB	8 MB
1B0h	432 MB	8 MB
1C0h	448 MB	8 MB

1E0h	480 MB	8 MB
200h	512 MB	8 MB

SUS_ADDR

Table 6-5-34 defines a 22-bit field that indicates a valid suspension address in 512KB units. If this field is set to zero, then this card does not have a valid suspension address. If this field is non-zero, then a valid suspension address is reported by this field.

Table 6-5-34: SUS_ADDR Field

SUS_ADDR	Value Definition
0	No valid suspension address
Non-zero	Valid suspension address in 512KB units

A valid suspension address is set by the CMD20 "Suspend AU" command.
The suspension address is cleared by any of these events:
a) the host issues a CMD20 "Set Free AU" command;
b) the host writes to any location within the suspended AU; and
c) the host erases any location within the suspended AU.

APP_PERF_CLASS

Table 6-5-35 defines a 4-bit field that indicates the Application Performance Class supported by the card. The Application Performance Class defined in the table shall be equal or less than the average random performance of the card.

Table 6-5-35: APP_PERF_CLASS Field

APP_PERF_CLASS	Value Definition
0h	Application Performance Class is not supported
1h	A1, Application Performance Class 1
2h	A2, Application Performance Class 2
3h - Fh	Reserved

Application Notes:
For any APP_PERF_CLASS indicated by the card, it is assumed that the lower classes are supported as well. Then Application Performance supported Hosts should assume that higher APP_PERF_CLASS levels may be set in the future. For example, A1 host should interpret APP_PERF_CLASS; not only 1h but also higher value indicates support of Application Class 1.

PERFORMANCE_ENHANCE

Table 6-5-36 defines a 8-bit field that indicates the performance enhancement functionalities supported by the card.

Table 6-5-36: PERFORMANCE_ENHANCE Field

PERFORMANCE_ENHANCE	Description
SD_STATUS b[335:331]	Command Queue Support. Refer to Table 6-5-37
SD_STATUS b[330]	Support for Cache 0 : Not Supported 1: Supported
SD_STATUS b[329]	Support for Host-initiated maintenance 0 : Not Supported 1: Supported
SD_STATUS b[328]	Support for Card-initiated maintenance 0 : Not Supported 1: Supported

SD Status b[335:331], as in Table 6-5-37, indicates the command queue support and the depth required to meet Application Performance Class 2

Table 6-5-37: Command Queue Support Field

Command Queue Support	Value Definition
0h	Command Queue is not supported
1h	Command Queue supported, with queue depth 2
2h	Command Queue supported, with queue depth 3
….	
1Fh	Command Queue supported, with queue depth 32

6.6 Card Identification Mode and Data Transfer Mode

Two operation modes are defined for the SD Card system:

Card identificationmode

The host will be in card identification mode after reset and while it is looking for new cards on the bus. Cards will be in this mode after reset until the SEND_RCA command (CMD3) is received.

Data transfermode

Cards will enter data transfer mode after their RCA is first published. The host will enter data transfer mode after identifying all the cards on the bus.

The following table shows the dependencies between operation modes and card states. Each state in the SD Card state diagram is associated with one operation mode:

Table 6-6: Overview of Card States vs. Operation modes

Card state	Operation mode
Inactive State	inactive
Idle State	card identification mode
Ready State	
Identification State	
Stand-by State	data transfer mode
Transfer State	
Sending-data State	
Receive-data State	
Programming State	
Disconnect State	

6.6.1 Card IdentificationMode

While in card identification mode the host resets all the cards that are in card identification mode, validates operation voltage range, identifies cards and asks them to publish Relative Card Address (RCA). This operation is done to each card separately on its own CMD line. All data communication in the Card Identification Mode uses the command line (CMD) only.
During the card identification process, the card shall operate in the SD clock frequency of the identification clock rate f_{OD}.

Card Reset

In SD mode, The command GO_IDLE_STATE (CMD0) is the software reset command and sets each card into Idle State regardless of the current card state. Cards in Inactive State are not affected by this command. After power-on by the host, all cards are in Idle State, including the cards that have been in Inactive State before.
After power-on or CMD0, all cards' CMD lines are in input mode, waiting for start bit of the next command.
The cards are initialized with a default relative card address (RCA=0x0000) and with a default driver strength with 400KHz clock frequency. In case of 3.3V signaling, default driver strength is specified by the Driver Stage Register (DSR) if supported and selected highest driving current capability. In case of 1.8V signaling, default driver strength is specified by type B driver.

Operating Condition Validation

At the start of communication between the host and the card, the host may not know the card supported voltage and the card may not know whether it supports the current supplied voltage. The host issues a reset command (CMD0) with a specified voltage while assuming it may be supported by the card. To verify the voltage, a following new command (CMD8) is defined in the Physical Layer Specification Version 2.00.

SEND_IF_COND (CMD8) is used to verify SD Memory Card interface operating condition. The card

checks the validity of operating condition by analyzing the argument of CMD8 and the host checks the validity by analyzing the response of CMD8. The supplied voltage is indicated by VHS filed in the argument. The card assumes the voltage specified in VHS as the current supplied voltage. Only 1-bit of VHS shall be set to 1 at any given time. Both CRC and check pattern are used for the host to check validity of communication between the host and the card.

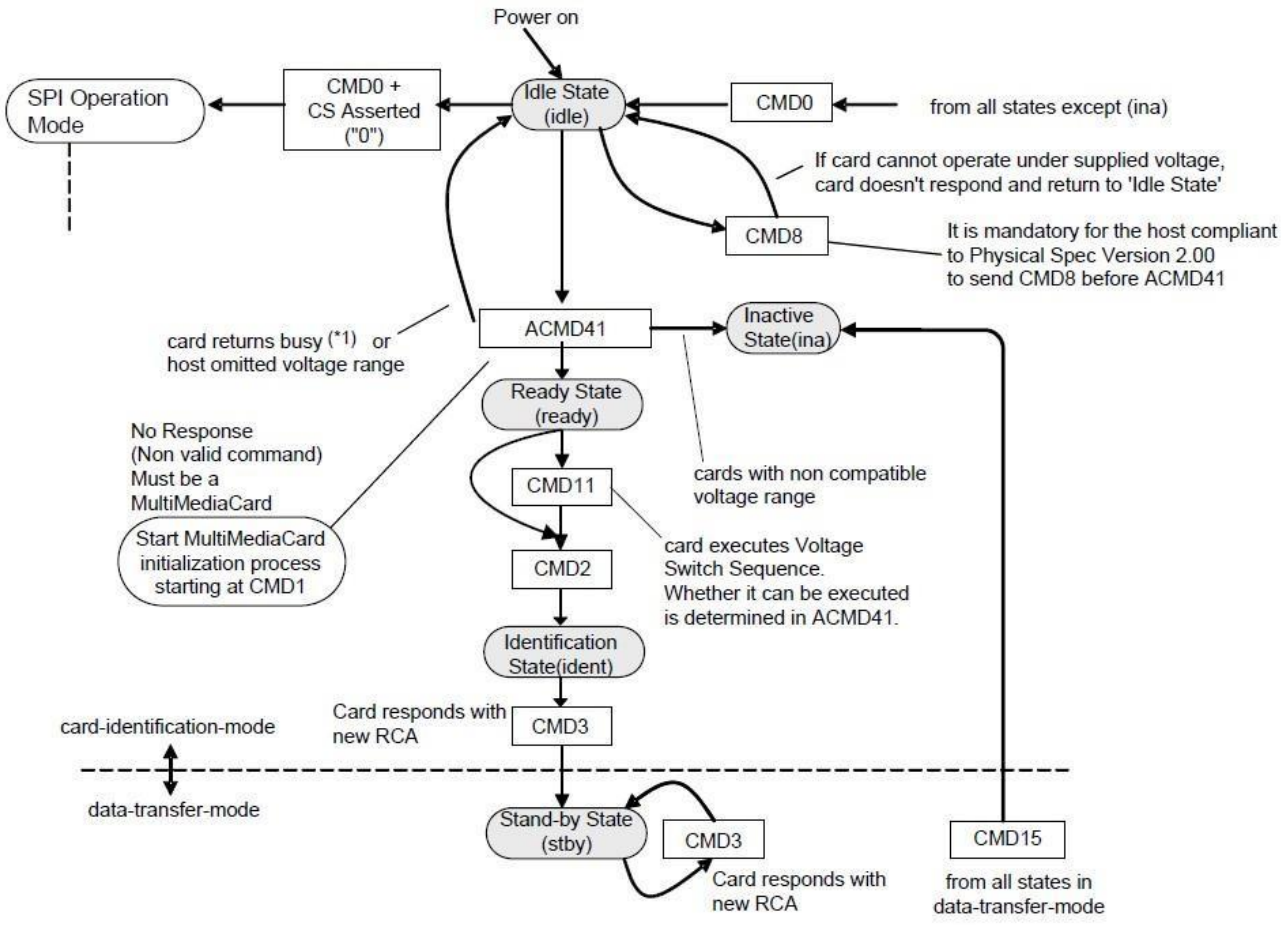
If the card can operate on the supplied voltage, the response echoes back the supply voltage and the check pattern that were set in the command argument.

If the card cannot operate on the supplied voltage, it returns no response and stays in idle state. It is mandatory to issue CMD8 prior to first ACMD41 to initialize SDHC or SDXC Card.Receipt of CMD8 makes the cards realize that the host supports the Physical Layer Version 2.00 or later and the card can enable new functions.

SD_SEND_OP_COND (ACMD41) is designed to provide SD Memory Card hosts with a mechanism to identify and reject cards which do not match the VDD range desired by the host. This is accomplished by the host sending the required VDD voltage window as the operand of this command.
Cards which cannot perform data transfer in the specified range shall discard themselves from further bus operations and go into Inactive State. The levels in the OCR register shall be defined accordingly
Note that ACMD41 is application specific command; therefore APP_CMD (CMD55) shall always precede ACMD41. The RCA to be used for CMD55 in idle_state shall be the card's default RCA = 0x0000.
After the host issues a reset command (CMD0) to reset the card, the host shall issue CMD8 prior to ACMD41 to re-initialize the SD Memory card

By setting the OCR to zero in the argument of ACMD41, the host can query each card and determine the common voltage range before sending out-of-range cards into the Inactive State (query mode). This query should be used if the host is able to select a common voltage range or if a notification to the application of non usable cards in the stack is desired. The card does not start initialization and ignores HCS in the argument if ACMD41 is issued as a query. Afterwards, the host may choose a voltage for operation and reissue ACMD41 with this condition, sending incompatible cards into the Inactive State.
During the initialization procedure, the host is not allowed to change the operating voltage range.

Figure 6-6-1: SD Memory Card State Diagram (Card Identification Mode)



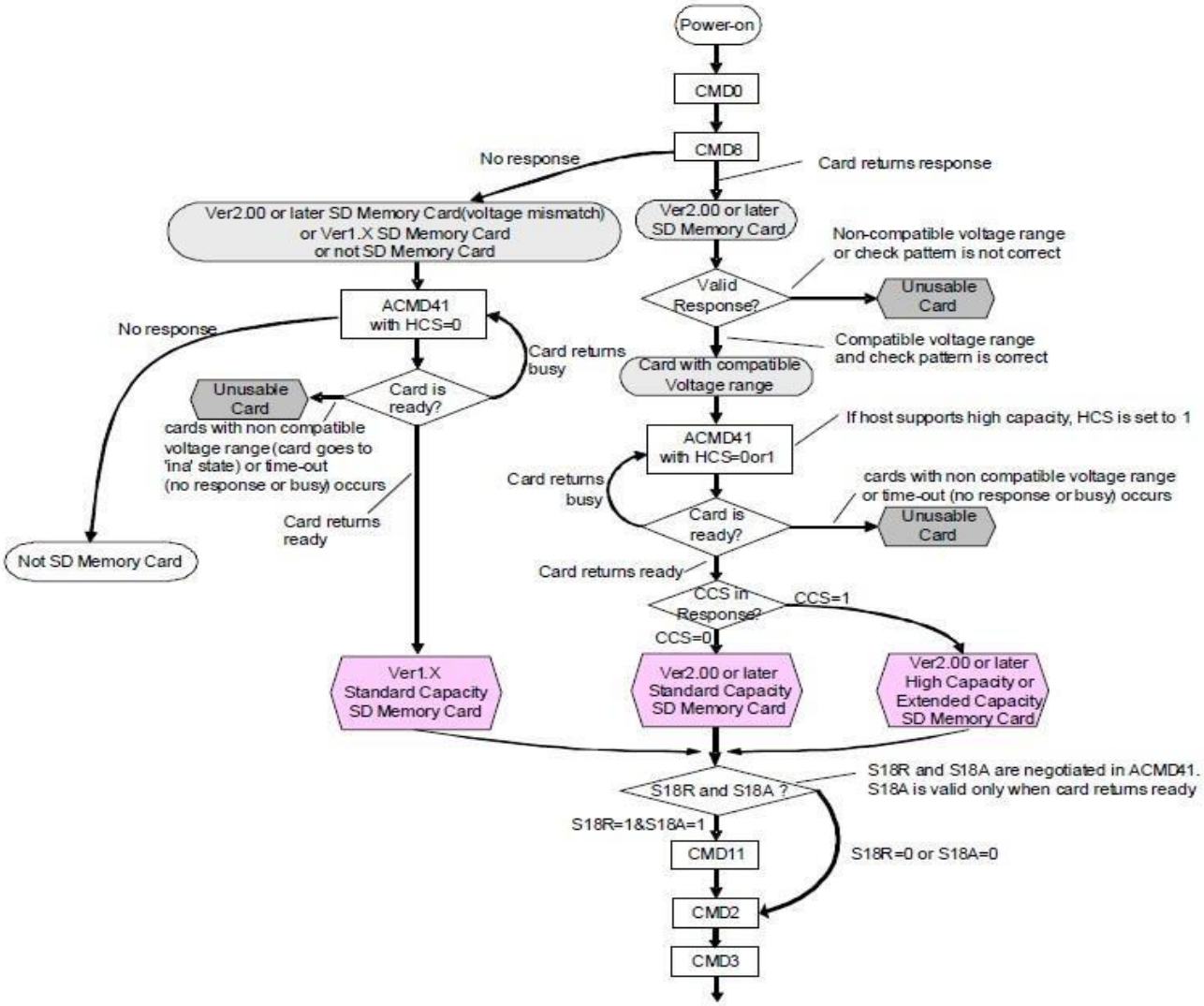
(*1) Note: Card returns busy when
- Card executes internal initialization process
- Card is High or Extended capacity SD Memory Card and host doesn't support High or Extended capacity
  This means that CMD8 is mandatory to initialize High capacity SD Memory Card

6.6.2 Card Initialization and Identification Process

After the bus is activated the host starts card initialization and identification process.
The initialization process starts with SD_SEND_OP_COND (ACMD41) by setting its operational conditions and the HCS bit in the OCR. The HCS (Host Capacity Support) bit set to 1 indicates that the host supports SDHC or SDXC Card. The HCS (Host Capacity Support) bit set to 0 indicates that the host supports neither SDHC nor SDXC Card.
Receiving of CMD8 expands the ACMD41 function; HCS in the argument and CCS (Card Capacity Status) in the response. HCS is ignored by cards, which didn't respond to CMD8. However the host should set HCS to 0 if the card returns no response to CMD8. Standard Capacity SD Memory Card ignores HCS. If HCS is set to 0, SDHC and SDXC Cards never return ready status (keep busy bit to 0).
The busy bit in the OCR is used by the card to inform the host whether initialization of ACMD41 is completed. Setting the busy bit to 0 indicates that the card is still initializing. Setting the busy bit to 1 indicates completion of initialization. Card initialization shall be completed within 1 second from the first ACMD41. The host repeatedly issues ACMD41 for at least 1 second or until the busy bit are set to 1. The card checks the operational conditions and the HCS bit in the OCR only at the first ACMD41 with setting voltage window in the argument. While repeating ACMD41, the host shall not issue another command except CMD0.
If the card responds to CMD8, the response of ACMD41 includes the CCS field information. CCS is valid when the card returns ready (the busy bit is set to 1). CCS=0 means that the card is SDSC.
CCS=1 means that the card is SDHC or SDXC.
The host performs the same initialization sequence to all of the new cards in the system. Incompatible cards are sent into Inactive State. The host then issues the command ALL_SEND_CID (CMD2), to each card to get its unique card identification (CID) number. Card that is unidentified (i.e. which is in Ready State) sends its CID number as the response (on the CMD line). After the CID was sent by the card it goes into Identification State. Thereafter, the host issues CMD3 (SEND_RELATIVE_ADDR) asks the card to publish a new relative card address (RCA), which is shorter than CID and which is used to address the card in the future data transfer mode. Once the RCA is received the card state changes to the Stand-by State. At this point, if the host wants to assign another RCA number, it can ask the card to publish a new number by sending another CMD3 command to the card. The last published RCA is the actual RCA number of the card.
The host repeats the identification process, i.e. the cycles with CMD2 and CMD3 for each card in the system.
Initialization of SDXC is identical to SDHC. User area capacity of SDXC card is specified by C_SIZE and it shall be more than or equal to 32GB. Figure 6-2-2 shows Card Initialization and Identification for SD I/F.

Application Notes:
The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

Figure 6-6-2: Card Initialization and Identification Flow (SD mod



6.6.3 Initialization Command (ACMD41)

Followings are general rules of the argument of ACMD41:
(1) If the voltage window field (bit 23-0) in the argument is set to zero, it is called "inquiry CMD41" that does not start initialization and is use for getting OCR. The inquiry ACMD41 shall ignore the other field (bit 31-24) in the argument.
(2) If the voltage window field (bit 23-0) in the argument is set to non-zero at the first time, it is called "first ACMD41" that starts initialization. The other field (bit 31-24) in the argument is effective.
(3) The argument of following ACMD41 shall be the same as that of the first ACMD41.

Figure 6-6-31 shows argument format and Figure 6-6-32 shows response format. Two new fields are added to the argument of ACMD41.
If a SDXC Card is initialized with XPC=0, the card is operating at up to 0.36W (100mA at 3.6V on VDD1) in Default Speed or SDR12, and if the card does not support Speed Class, Class 0 is indicated in SD Status. If a SDXC Card is initialized with XPC=1, the card is operating at up to 0.54W (150mA at 3.6V on VDD1) in Default Speed or SDR12, and the card supports Speed Class. Re-initialization is required to change XPC selection.
UHS-I supported host sets S18R=1 in the argument of ACMD41 to request the card to switch 1.8V signaling level. UHS-I supports card respond with S18A=1 in the response of ACMD41 (if in 3.3V signaling mode) and then host can issue voltage switch command. Once voltage switch is performed, UHS-I card indicates S18A=0 to keep current signal voltage.

(1) Argument of ACMD41

Figure 6-6-31: Argument of ACMD41

47	46	45-40	39	38	37	36	35-33	32	31-16	15-08	07-01	00
S	D	Index	Busy 31	HCS 30	(FB) 29	XPC 28	Reserved 27-25	S18R 24	OCR 23-08	Reserved 07-00	CRC7	E
0	1	101001	0	x	0	x	000	x	xxxxh	0000000	xxxxxxx	1
1	1	6	1	1	1	1	3	1	16	8	7	1

Host Capacity Support
0b: SDSC Only Host
1b: SDHC or SDXC Supported

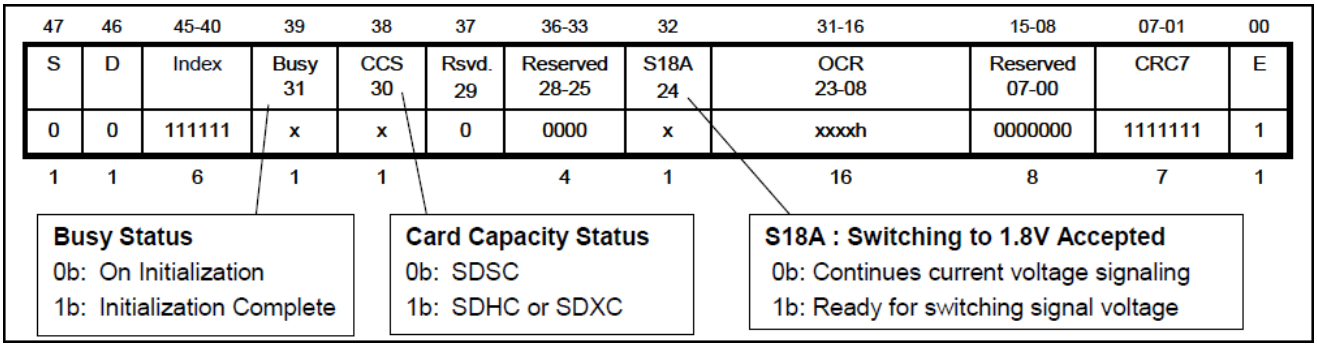
SDXC Power Control
0b: Power Saving
1b: Maximum Performance

S18R : Switching to 1.8V Request
0b: Use current signal voltage
1b: Switch to 1.8V signal voltage

Note: Fast Boot (Bit 29) is reserved for eSD

(2) Response of ACMD41 (R3)

Figure 6-6-32: Response of ACMD



CCS (Bit 30) and S18A (Bit 24) are valid when Busy (Bit 31) is set to 1.

6.6.4 Bus Signal Voltage Switch Sequence

Figure 6-6-41 shows sequence of commands to perform voltage switch and Figure 6-6-42 shows initialization flow chart for UHS-I hosts. Red and yellow boxes are new procedure to initialize UHS-I card.

Figure 6-6-41 : ACMD41 Timing Followed by Voltage Switch Sequence

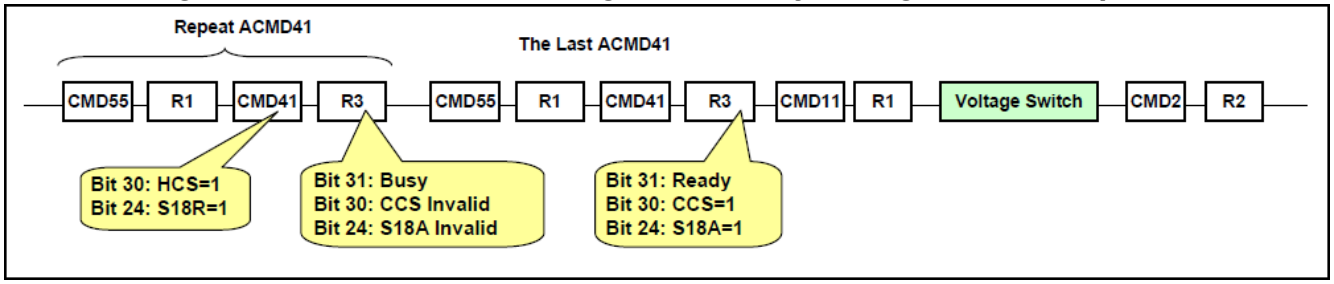
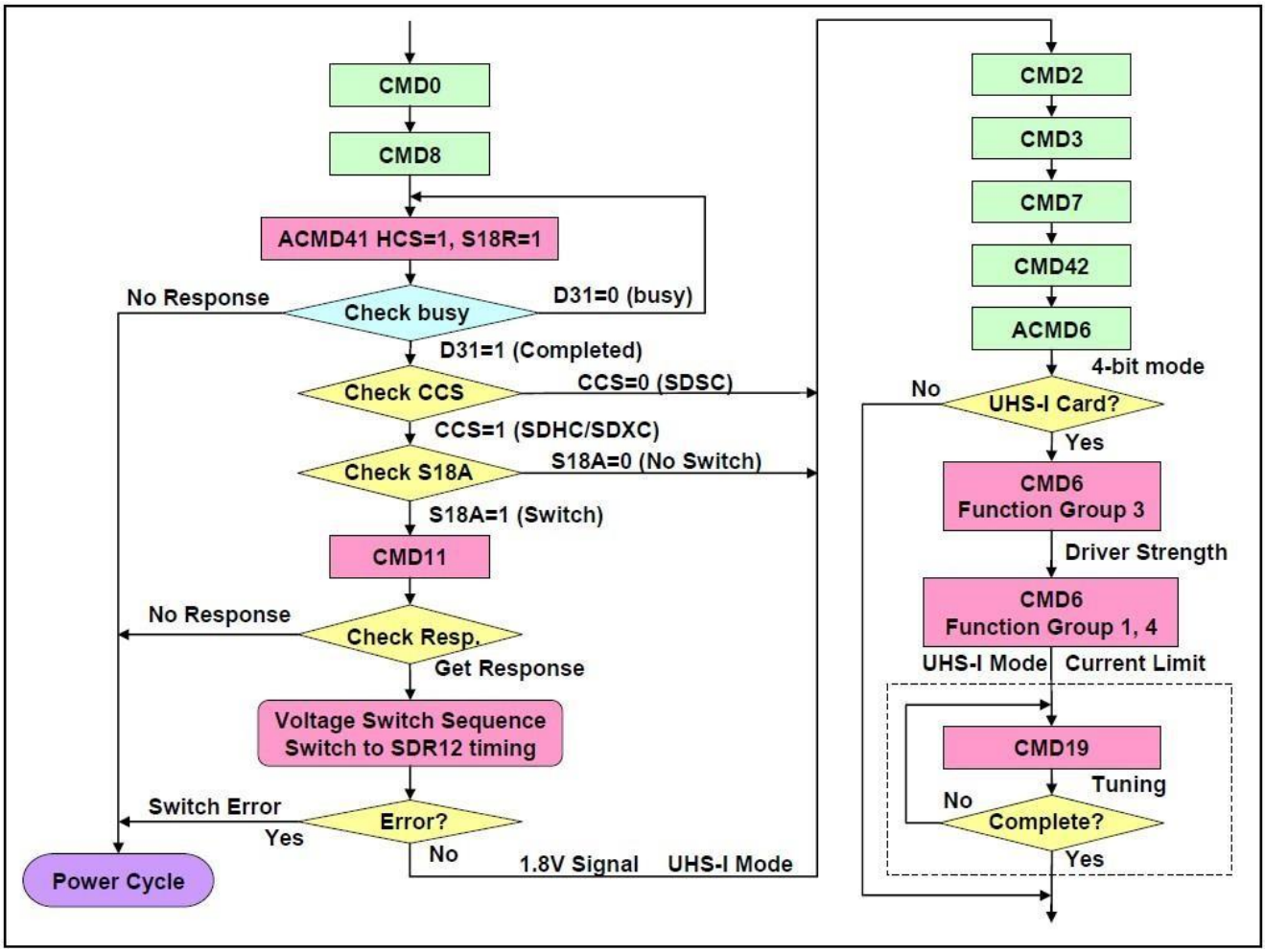


Figure 6-6-42: UHS-I Host Initialization Flow Chart



When signaling level is 3.3V, host repeats to issue ACMD41 with HCS=1 and S18R=1 until the response indicates ready. The argument (HCS and S18R) of the first ACMD41 is effective but the all following ACMD41 should be issued with the same argument. If Bit 31 indicates ready, host needs to check CCS and S18A. The card indicates S18A=0, which means that voltage switch is not allowed and the host needs to use current signaling level. S18A=1 means that voltage switch is allowed and host issues CMD11 to invoke voltage switch sequence. By receiving CMD11, the card returns R1 response and start voltage switch sequence. No response of CMD11 means that S18A was 0 and therefore host should not have sent CMD11. Completion of voltage switch sequence is checked by high level of DAT[3:0]. Any bit of DAT[3:0] can be checked depends on ability of the host.

When entering tran state, CARD_IS_LOCKED status in the R1 response should be checked (it is indicated in the response of CMD7). If the card is locked, CMD42 is required to unlock the card. If the card is unlocked, CMD42 can be skipped. In case of UHS-I card, appropriate driver strength is selected by CMD6 Function Group 3 and one of UHSI modes is selected by CMD6 Function Group 1. In SDR50 and SDR104 modes, if tuning of sampling point is required, CMD19 is repeatedly issued until tuning is completed.

6.6.5 Timing to Switch Signal Voltage

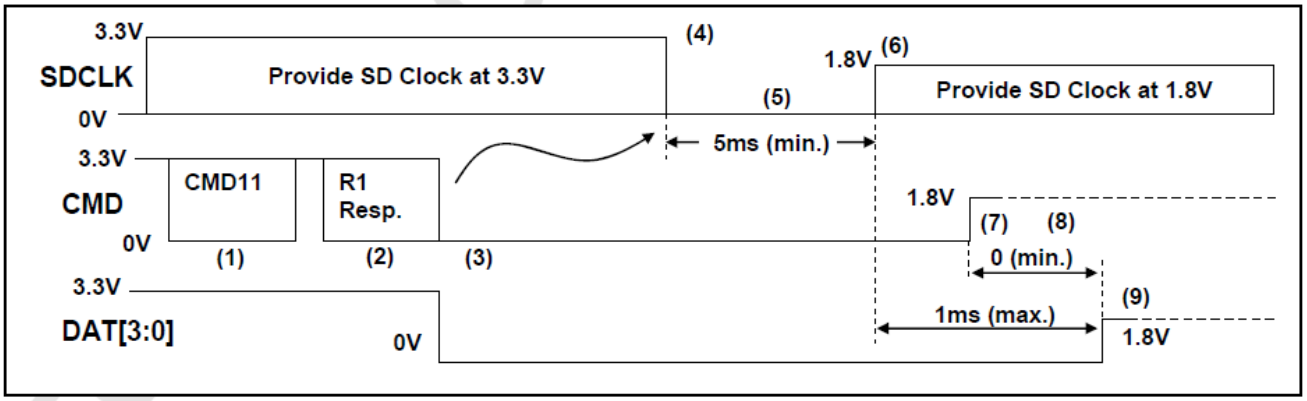
Clock frequency range shall be 100 KHz-400 KHz during initialization sequence. Table 6-6-51 shows command (S18R) – response (S18A) combinations to switch signal voltage in ACMD41. S18A is defined in the command argument and indicates signal voltage switch acceptance by the card (voltage is not switched here). If signaling level is already 1.8V, S18R is ignored and signal voltage switch sequence is not started. S18A=0 means that current signaling level is maintained. Refer to Section 6.6.4 about new fields defined in ACMD41.

Table 6-6-51: S18R and S18A Combinations

Current Signaling Level	S18R	S18A	Comment
3.3V	0	0	1.8V signaling is not requested
	1	0	The card does not support 1.8V signaling
	1	1	Start signal voltage switch sequence
1.8V	X	0	Already switched to 1.8V

To change signaling level at the same time between host card, signal voltage switch sequence is invoked by CMD11 as shown in Figure 6-6-52. CMD11 is issued only when S18A=1 in the response of ACMD41.

Figure 6-6-52: Signal Voltage Switch Sequence



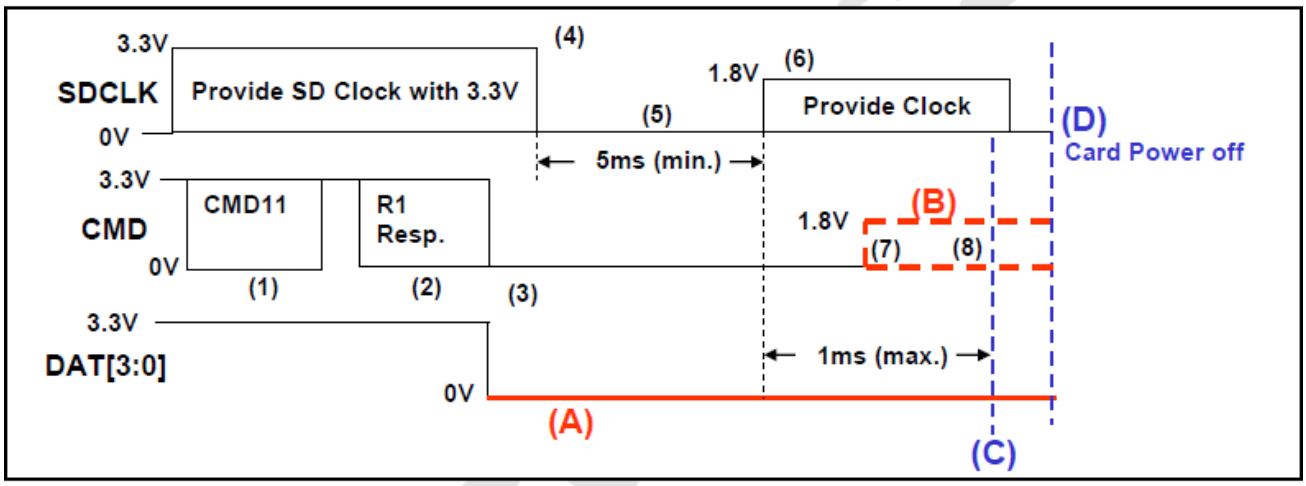
(1) The Host starts the voltage switch protocol by issuing CMD11.
(2) The card returns an R1 response.
(3) The card drives CMD and DAT[3:0] to low at the next clock of the end bit for R1 response after completing the R1 response and holds the signals low until the card drives CMD high to 1.8V in step (7) and DAT[3:0] high in step (9).
(4) After receiving the R1 response, the host stops SDCLK cycling by holding SDCLK low. The host shall hold SDCLK low for at least 5ms. The timing for the host to begin holding SDCLK low is not specified. Note that after issuing CMD11, the host is not driving CMD and DAT[3:0] until completion of voltage switching sequence. The host may monitor any one of the CMD signal or the DAT[3:0] signals. If the host does not detect a low signal level on monitored signal, the host should abort the voltage switch sequence and cycle power to the card. 1.8V output of voltage regulator in card shall be stable within 5ms. Host keeps SDCLK low at least 5ms. This means that 5ms is the maximum for the card and the minimum for the host.
(5) After detecting SDCLK low, the card shall begin switching voltage regulator to a 1.8V supply. The card's 1.8V voltage regulator shall be stable within 5ms of SDCLK going low. Note that this protocol ensures that all SD signals are held low before the card switches to the 1.8V supply.
(6) The host shall restart SDCLK transitions with1.8V signaling after at least 5ms from holding SDCLK low and the 1.8V host regulator being stable.
(7) Within 1ms from detecting SDCLK transition, the card shall: (a) drive CMD to 1.8V for at least one SDCLK period, and then (b) stop driving CMD (tri-state).
(8) The card may test for host pull-up level of 1.8V through checking the CMD line.
(9) Within 1ms from detecting SDCLK transition, the card shall: (a) drive all DAT[3:0] to 1.8V for at least one SDCLK cycle, and then (b) stop driving DAT[3:0] (tri-states). Host checks whether at least one of DAT[3:0] is high after 1ms from restarting SDCLK transitions to confirm completion of voltage switch sequence.

3.3V SD clock is provided before (4) and 1.8V SD clock is provided from (6), and its frequency range is 100KHz-400KHz. Stopping clock is allowed only in the period (5) during voltage switching sequence. After the sequence is completed, the host and the card start communication in SDR12 timing.

6.6.6 Timing of Voltage Switch Error Detection

Figure 6-6-6 shows the timing when an error occurs during signal voltage switch sequence.

Figure 6-6-6: Error Indication Timing



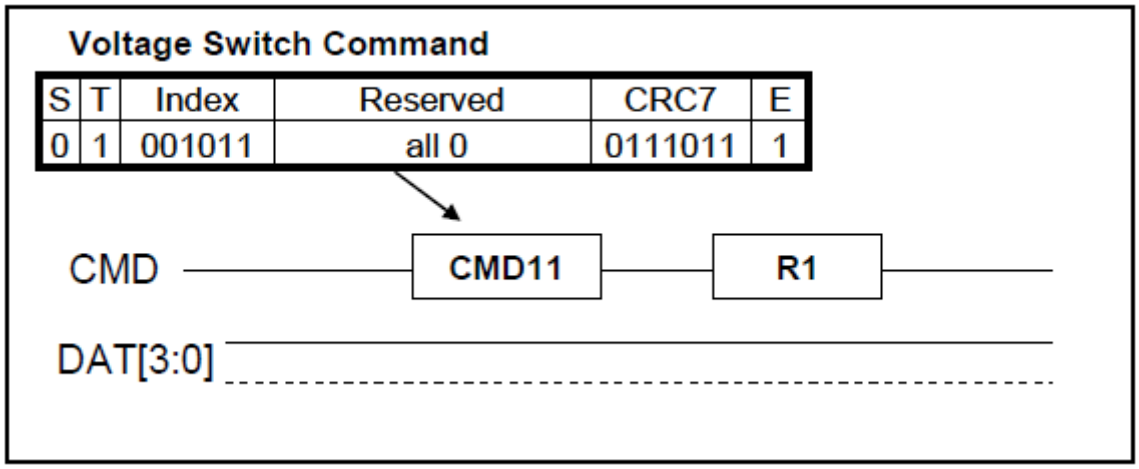
(A) If the card detects voltage error at any point in (5)-(8), the card keeps driving DAT[3:0] to low until card power off.
(B) CMD may be low or tri-state.
(C) The host checks whether DAT[3:0] is high after 1ms from starting to provide SDCLK.
(D) If DAT[3:0] is low, the host drives SDCLK to low and then stops supplying the card power.

The card shall check voltages of own regulator output and host signals to be less than 2.5V. Error occurrences are indicated by (A) and (B). Card checks voltage level either SDCLK or CMD between step (6) and step (8).

6.6.7 Voltage Switch Command

Figure 6-6-7 shows Voltage Switch Command (CMD11) definition. CMD11 can be executed in ready state and doesn't change the state. Even if the card is locked, CMD11 can be executed. Returning R1 type response means the card starts voltage switch sequence. If the host detects no response, power cycle should be executed.
There are four cases that the card indicates no response to CMD11.
(1) The card does not support voltage switch.
(2) The card supports voltage switch but ACMD41 is received with S18R=0.
(3) The card receives CMD11 not in ready state.
(4) Signaling level is already switched to 1.8V.
For all above cases, CMD11 is treated as an illegal command.

Figure 6-6-7 : Voltage Switch Command

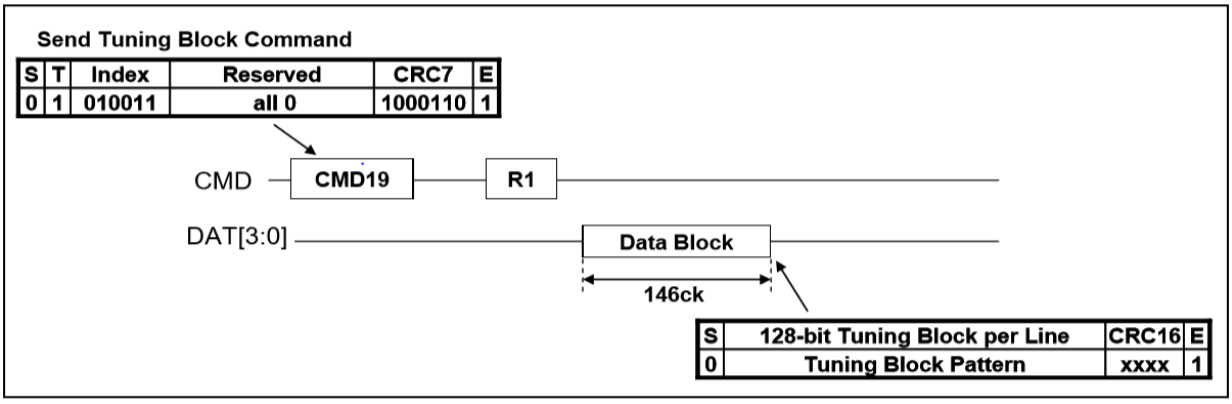


6.6.8 Tuning Command

A known data block ("Tuning block") can be used to tune sampling point for tuning required hosts. The tuning capability of sampling point is mandatory for HOST-SDR-VD and optional for HOST-SDR-FD. This procedure gives the system optimal timing for each specific host and card combination and compensates for static delays in the timing budget including process, voltage and different PCB loads and skews.
CMD19 is defined for Send Tuning Block Command. R1 type response is defined. CMD19 can be executed in transfer state of 1.8V signaling mode while the card is unlocked. The other case, CMD19 is treated as illegal command. Data block, carried by DAT[3:0], contains a pattern for tuning sampling position to receive data on the CMD and DAT[3:0] line. The block length of CMD19 is fixed and CMD16 is not required

The tuning command (CMD19) follows the timing of the single block read command as described in Figure 6-6-81.

Figure 6-6-81: Send Tuning Block Command



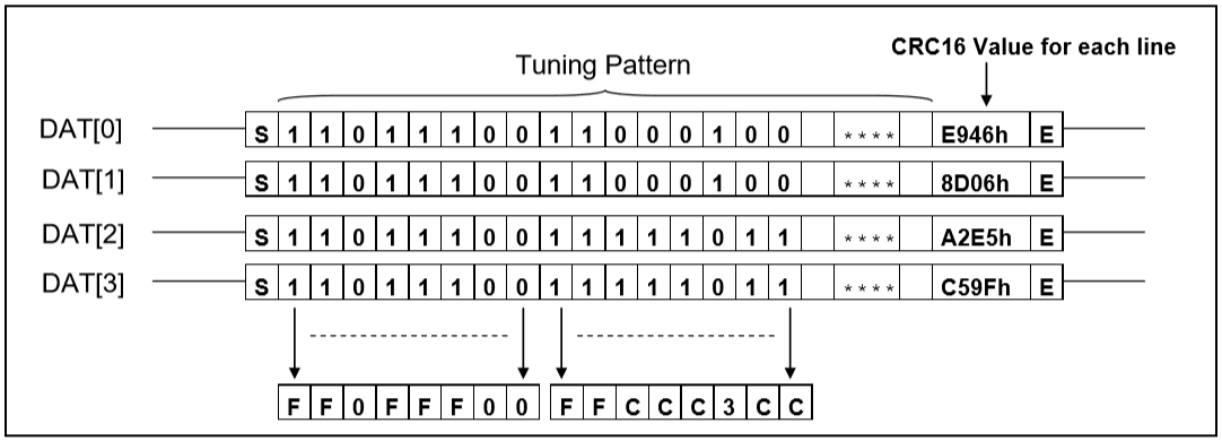
This sequence is defined as multiple, consecutive executions of CMD19 that are sent from the host and responded by the card, without any other command mixed between them.
The card shall complete a sequence of 40 times CMD19 executions in no more than 150ms. The tuning process is normally shorter than 40 executions of CMD19, and therefore should be shorter than 150 ms.
The sequence period definition does not include any host processing time. If host needs time to process CMD19 between executions, the sequence may be longer by this amount of time.
The tuning block is defined as a regular block, containing 64 bytes of a known predefined data. DAT[3:0] outputs 4-bit data in Figure 6-6-82 every SDCLK from left to right and up to down.

Table 6-6-8: Tuning Block Pattern

FF0FFF00	FFCCC3CC	C33CCCFF	FEFFFEEF
FFDFFFDD	FFFBFFFB	BFFF7FFF	77F7BDEF
FFF0FFF0	0FFCCC3C	CC33CCCF	FFEFFFEE
FFFDFFFD	DFFFBFFF	BBFFF7FF	F77F7BDE

The tuning block is defined as a regular block, containing 64 bytes of a known predefined data. DAT[3:0] outputs 4-bit data in Figure 6-6-82 every SDCLK from left to right and up to down.

Figure 6-6-82: Tuning Block on DAT[3:0]



How to output the pattern to DAT[3:0] is illustrated in Figure 4-11 (only the first 8 bytes are indicated). The fixed CRC16 value for each line is also indicated in the figure.

The following 3 cases are designed into the tuning block:
(1) Positive pulse to all 4 DAT lines simultaneously simulating maximum power & ground bounce effects – usually gives the maximum overshoot / undershoot.
(2) Positive pulse to 2 DAT lines and, at the same time, negative pulse to the other 2 DAT lines

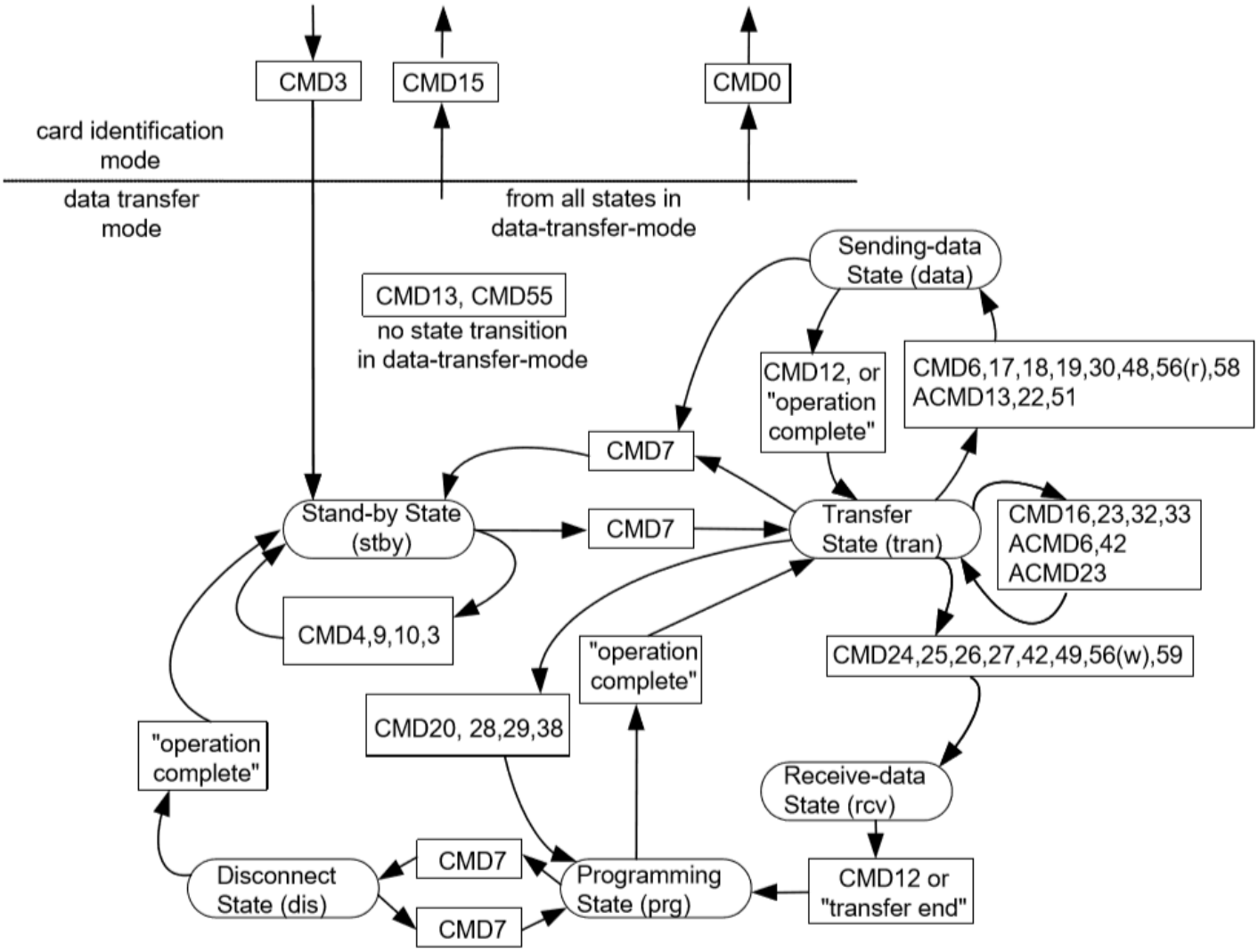
Simulating combination of ground bounce and impedance mismatch – usually gives maximum Tpd.
(3) Positive pulse to 1 DAT line, while the other 3 DAT lines are quiet Simulating impedance mismatch effects – usually gives minimum Tpd.

The tuning block purpose is to create a "special" signal integrity cases on the bus. This causes the maximum: noise, deterministic jitter, ISI and timing errors. Therefore, the purpose is to create the worst case "eye diagram" that the system should experience in a specific host and card combination.

6.6.9 Data Transfer Mode

Until the end of Card Identification Mode the host shall remain at fOD frequency because some cards may have operating frequency restrictions during the card identification mode. In Data Transfer Mode the host may operate the card in fPP frequency range. The host issues SEND_CSD (CMD9) to obtain the Card Specific Data (CSD register), e.g. block length, card storage capacity, etc.
The broadcast command SET_DSR (CMD4) configures the driver stages of all identified cards. It programs their DSR registers corresponding to the application bus layout (length) and the number of cards on the bus and the data transfer frequency. The clock rate is also switched from fOD to fPP at that point. SET_DSR command is an option for the card and the host.
CMD7 is used to select one card and put it into the Transfer State. Only one card can be in the Transfer State at a given time. If a previously selected card is in the Transfer State its connection with the host is released and it will move back to the Stand-by State. When CMD7 is issued with the reserved relative card address "0x0000", all cards are put back to Stand-by State (Note that it is the responsibility of the Host to reserve the RCA=0 for card de-selection - refer to CMD7.

Figure 6-6-9: SD Memory Card State Diagram (data transfer mode)



This may be used before identifying new cards without resetting other already registered cards. Cards which already have an RCA do not respond to identification commands (ACMD41, CMD2) in this state. Important Note: The card de-selection is done if certain card gets CMD7 with un-matched RCA. That happens automatically if selection is done to another card and the CMD lines are common. So, in SD Memory Card system it will be the responsibility of the host either to work with common CMD line (after initialization is done) - in that case the card de-selection will be done automatically or if the CMD lines are separate then the host shall be aware to the necessity to de-select cards.
All data communication in the Data Transfer Mode is point-to point between the host and the selected card (using addressed commands). All addressed commands get acknowledged by a response on the CMD line.

6.7 Write Protect Management

Three write protect methods are supported in the SD Memory Card as follows:
- Mechanical write protect switch (Host responsibility only)
- Card internal write protect (Card's responsibility)
- Password protection card lock operation.

6.7.1 Mechanical Write Protect Switch

A mechanical sliding tablet on the side of the card (refer to the Part 1 Standard Size SD Card Mechanical Addendum) will be used by the user to indicate that a given card is write protected or not. If the sliding tablet is positioned in such a way that the window is open it means that the card is write protected. If the window is close the card is not write-protected.
A proper, matched, switch on the socket side will indicate to the host that the card is write-protected or not. It is the responsibility of the host to protect the card. The position of the write protect switch is unknown to the internal circuitry of the card.

6.7.2 Card's Internal Write Protection (Optional)

Card data may be protected against either erase or write. The entire card may be permanently write-protected by the manufacturer or content provider by setting the permanent or temporary write protect bits in the CSD. For cards which support write protection of groups of sectors by setting the WP_GRP_ENABLE bit in the CSD, portions of the data may be protected (in units of WP_GRP_SIZE sectors as specified in the CSD), and the write protection may be changed by the application. The SET_WRITE_PROT command sets the write protection of the addressed write-protect group and the CLR_WRITE_PROT command clears the write protection of the addressed write-protect group.
The SEND_WIRTE_PROT command is similar to a single block read command. The card shall send a data block containing 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits. The address field in the write protect commands is a group address in byte units. The card will ignore all LSB’s below the group size.
The Password Card Lock protection is described in the following section.
Note that SDHC and SDXC Cards do not support Write Protection and do not respond to write-protection commands (CMD28, CMD29 and CMD30)

6.7.3 Card Lock/Unlock Operation

The password protection feature enables the host to lock a card while providing a password, which later will be used for unlocking the card. The password and its size are kept in a 128-bit PWD and 8-bit PWD_LEN registers, respectively. Optionally, Force Erase Password can be stored in additional 128-bit FEP and 8-bit FEP_LEN registers shall be present in case Card Ownership Protection (COP) is supported by the card. These registers are non-volatile so that a power cycle will not erase them. Locked cards respond to (and execute) all commands in the "basic" command class (class 0), ACMD41, CMD16 and

"lock card" command class. Thus, the host is allowed to reset, initialize, select, query for status, etc., but not to access data on the card. If the password was previously set (the value of PWD_LEN is not 0), the card will be locked automatically after power on. Similar to the existing CSD register write commands, the lock/unlock command is available in "transfer state" only. This means that it does not include an address argument and the card shall be selected before using it. The card lock/unlock command has the structure and bus transaction type of a regular single block write command. The transferred data block includes all the required information of the command (password setting mode, PWD itself, card lock/unlock etc.). Content protection is managed by PWD. Physical Card Ownership is managed with COP feature.

Card Ownership Protection

Card Ownership Protection (COP) prevents re-use of COP Card without knowing the protection password PWD. Once Force Erase Password (FEP) is set, it disables “Force Erase” operation, and “Clear PWD” operations. Alternatively, “FEP Force Erase” can be used. As this behavior is different from the Physical Specification Version 5.00 or earlier, COP Unlock is required to operate the card after power up when FEP=set, to ensure only the hosts familiar with COP operations can use such a card.

Application Note:

Card Ownership Protection is addressing specific user needs and applications. It is not recommended for support on host devices that are not designed for specific applications that know how to make use of this feature. It is recommended to support this feature only in cards specially designed to work with those designated hosts.

Special Terms for Lock/Unlock

The following terms and notations are introduced in this section:

- COP: Card Ownership Protection
  - COP feature: set of additional functions to support Card Ownership Protection
  - COP bit: bit4 of CMD42 argument that indicates COP-specific functions vs. PWD functions
- COP Card / Non-COP Card
  - COP Card is a card that supports COP features
  - Non-COP Card is another expression of Type 1, 2 Cards that does not support COP feature
- PWD: Card Lock Password
  - PWD indicates a register to hold a password to lock the card
  - "PWD=0" indicates that PWD is not set and PWD_LEN is set to 0
  - "PWD=set" indicates that a password is set to PWD and the password length is set to PWD_LEN
- FEP: Force Erase Password
  - "FEP" indicates a register to hold a password to protect Force Erase
  - "FEP=0" indicates that FEP is not set and FEP_LEN is set to 0
  - "FEP=set" indicates that a password is set to FEP and the password length is set to FEP_LEN
- Force Erase: is the function of CMD42[08h] (with no password) to erase PWD, PWD_LEN and all memory area. This function is disabled when FEP=set
- FEP Force Erase: is the function of CMD42[18h] (with FEP) to erase PWD, PWD_LEN and all memory

area. This function is disabled when FEP=0

- COP Unlock
  - command CMD42 with argument 1Fh (notated as CMD42[1Fh]) that is required to access COP feature functions. Also, if FEP=set, after power on reset or reset COP Unlock is required to enable any other CMD42 functions.
- COP Locked state
  - state of the card after power on reset or reset, when any other argument to CMD42 is not accessible till COP Unlock is performed. Also, the card shall behave as locked card to any other commands.
- Clean COP Card - COP Card with no FEP/PWD set
- Locked COP Card – COP Card with PWD set
- PWD functions - COP Card CMD42 functions
- COP functions - COP Card CMD42 functions

Card Behavior

Figure 6-7-31 shows simplified behavior of Non-COP Card. After power on, card is "PWD Locked" if PWD=set or "PWD Unlocked" if PWD=0. Force Erase allows to reset the PWD, while erasing all the User area data. CMD42[1Fh] is not defined and Non-COP Card returns LOCK_UNLOCK_FAILED error in R1.

Figure 6-7-31 : Simplified Non-COP Card State Diagram

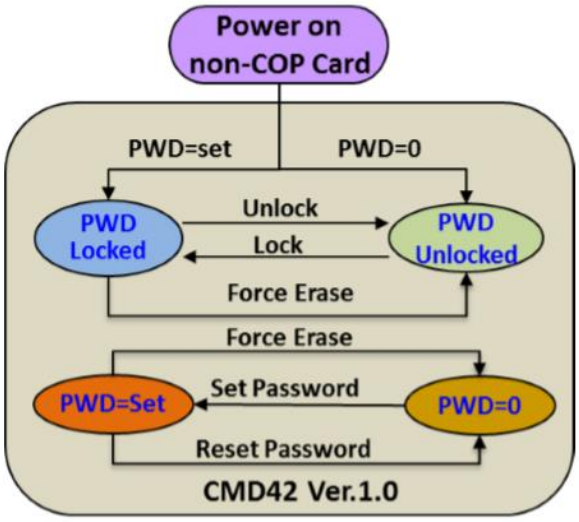


Figure 6-7-32 shows simplified behavior of a COP Card. After power on reset or reset, COP Card starts in CMD42 Ver.1.0 Compatible mode:

- If FEP=0, CMD42 functions are compatible with CMD42 Ver.1.0, except the support of additional argument 1Fh (COP Unlock).
- If FEP=1, COP Card is in COP Locked state to prevent access by Non-COP Hosts. COP Card does not

execute any CMD42 function and indicates CARD_IS_LOCKED status and LOCK_UNLOCK_FAILED error except CMD42[1Fh]. On receiving CMD42[1Fh] COP Card moves to CMD42 Ver.2.0 mode.

In CMD42 Ver.2.0 mode, "FEP Locked" is disabled and CMD42 functions are extended with functions accessible with COP bit set to '1'. There are three additional features to Ver.1.0:

(1) FEP Management

FEP is managed by Reset FEP, Set FEP and Replace FEP functions.

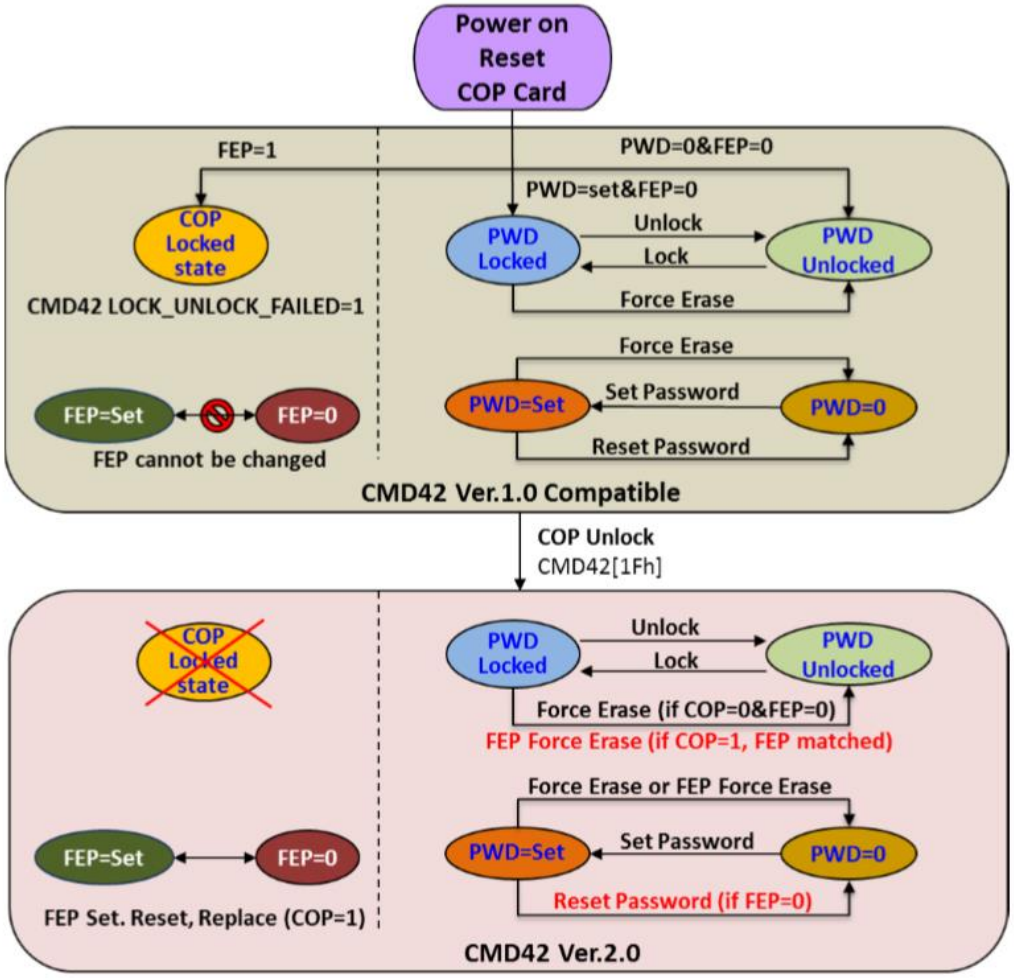
(2) Force Erase

There are 2 types of Force Erase operation supported based on FEP state: "Force Erase" (CMD42[08h] with no password) to erase PWD, PWD_LEN and all memory area can be executed as long as FEP=0. It is disabled if FEP=set. "FEP Force Erase" (CMD42[18h] with password) to erase PWD, PWD_LEN and all memory area which if executed if the password matches FEP. It is enabled if FEP=set and disabled if FEP=0.

(3) Reset PWD inhibit

Once PWD is set, PWD can be replaced, but PWD cannot be reset during FEP=set.

Figure 6-7-32 : Simplified COP Card State Diagram



Lock Card Data Structure

Table 6-7-3 describes the structure of the command data block. Note that the host compliant to the Physical Specification Version 5.10 or later shall set reserved bits (Bit7-5) to 0 when issuing CMD42.

Table 6-7-3: Lock Card Data Structure

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Reserved (shall be set to 0)			COP	ERASE	LOCK_ UNLOCK	CLR_ PWD	SET_ PWD
1	PWDS_LEN							
2	Password data							
...								
PWDS_LEN + 1								

- **COP:** When set to 1, indicates Card Ownership Protection feature operations
- **ERASE:** 1 Defines Forced Erase Operation. In byte 0, bit 3 will be set to 1 (all other bits shall be 0). All other bytes of this command will be ignored by the card.
- **LOCK/UNLOCK:** 1 = Locks the card. 0 = Unlock the card (note that it is valid to set this bit together with SET_PWD but it is not allowed to set it together with CLR_PWD).
- **CLR_PWD:** 1 = Clears PWD.
- **SET_PWD:** 1 = Set new password to PWD
- **PWDS_LEN:** Defines the following password(s) length (in bytes). In case of a password change, this field includes the total password lengths of old and new passwords. The password length is up to 16 bytes. In case of a password change, the total length of the old password and the new password can be up to 32 bytes.
- **Password data:** In case of setting a new password, it contains the new password. In case of a password change, it contains the old password followed by the new password.

The data block size shall be defined by the host before it sends the card lock/unlock command. The block length shall be set to greater than or equal to the required data structure of the lock/unlock command. In the following explanation, changing block size by CMD16 is not a mandatory requirement for the lock/unlock command. If preset block length is larger than length of required data structure, dummy data shall be sent by the host for unused data area of the block.
Since block length shall always be even in DDR50 mode, the block length for CMD42 shall always be rounded up to an even size. If CMD16 is used prior to CMD42 to set the block length, it shall always specify an even length.

Command Sequences Common to COP/Non-COP Cards

The following paragraphs define the various lock/unlock command sequences common to COP/NonCOP Cards (items relevant to COP Cards only are marked by square brackets []):

Setting PWD:

- Select a card (CMD7), if not previously selected.

- Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bits password size (in bytes), and the number of bytes of the new password. In the case that a password replacement is done, then the block size shall consider that both passwords-the old and the new one-are sent with the command.
- Send the Card Lock/Unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode (SET_PWD), the length (PWDS_LEN) and the password itself. In the case that a password replacement is done, then the length value (PWDS_LEN) shall include both passwords (the old and the new one) and the password data field shall include the old password (currently used) followed by the new password. Note that the card shall handle the calculation of the new password length internally by subtracting the old password length from PWDS_LEN field.
- [In CMD42 ver.2.0 mode, COP Card can execute this command when COP bit=0.]
- In the case that the sent old password is not correct (not equal in size and content), then the LOCK_UNLOCK_FAILED error bit will be set in the status register and the old password does not change. In the case that the sent old password is correct (equal in size and content), then the given new password and its size will be saved in the PWD and PWD_LEN registers, respectively.

Note that the password length register (PWD_LEN) indicates if a password is currently set. When it equals 0, there is no password set. If the value of PWD_LEN is not equal to zero, the card will lock itself after power up. COP Card shall also lock itself after CMD0. Non-COP Card lock status after CMD0 is up to implementation. It is possible to lock the card immediately in the current power session by setting the LOCK/UNLOCK bit (while setting the password) or sending an additional command for card lock.

Reseting PWD:

- Select a card (CMD7), if not previously selected.
- Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.
- Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode CLR_PWD, the length (PWDS_LEN), and the password itself. If the PWD and PWD_LEN content match the sent password and its size, then the content of the PWD register is cleared and PWD_LEN is set to 0. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.
- [In CMD42 ver.2.0 mode, COP Card can execute this command when COP bit=0.]
- [If FEP is set, PWD and PWD_LEN registers shall not be affected, and the LOCK_UNLOCK_FAILED error bit shall be set in the status register.]
- [Resetting PWD shall not affect FEP and FEP_LEN registers.]

Locking PWD Unlocked Card:

- Select a card (CMD7), if not previously selected.
- Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.
- Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode LOCK, the length (PWDS_LEN) and the password itself.
- [In CMD42 ver.2.0 mode, COP Card can execute this command when COP bit=0.]

In PWD Unlocked state, if the PWD content is equal to the sent password, then the card will be PWD locked and the card-locked status bit will be set in the status register. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.
Note that it is possible to set the password and to lock the card in the same sequence. In such a case, the host shall perform all the required steps for setting the password (as described above) including the bit LOCK set while the new password command is sent. If the password was previously set (PWD_LEN is not 0), then the card will be PWD locked automatically after power on reset.
An attempt to lock a locked card or to lock a card that does not have a password will fail and the LOCK_UNLOCK_FAILED error bit will be set in the status register, unless it was done during a password definition or change operations.

Unlocking PWD Locked Card:

- Select a card (CMD7), if not previously selected.
- [If FEP=set, after power on reset or reset with CMD0, COP Unlock is required (refer to Unlocking COP locked state sequence in Section 4.3.7.1.6)]
- Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password PWD.
- Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode UNLOCK, the length (PWDS_LEN) and the password itself.
- [In CMD42 ver.2.0 mode, COP Card can execute this command when COP bit=0.]

If the PWD content is equal to the sent password, then the card will be unlocked and the card-locked status bit will be cleared in the status register. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit will be set in the status register.
Note that unlocking is done only for the current power session. As long as the PWD [or FEP] is not cleared, the card will be locked automatically on the next power up. Only if PWD=0 [and FEP=0], the card shall be unlocked after power on and CMD0.
An attempt to unlock an unlocked card will fail and LOCK_UNLOCK_FAILED error bit will be set in the status register, unless it was done during PWD definition or change operation.

COP specific Command Sequences

The following paragraphs define the various lock/unlock command sequences applicable to COP Cards only:

Enabling Card Ownership Protection (COP) Function Set:
If FEP=0, after power on reset or reset COP Card shall not execute any COP function of CMD42 other than COP Unlock and shall interpret it as PWD function, unless it was done after COP functions are unlocked after the power on reset or reset by the sequence below:

- Select a card (CMD7), if not previously selected.
- Define the block length (CMD16) to 1 byte (8-bit card lock/unlock command). Send the card lock/unlock command with the appropriate data block of one byte on the data line including the 16 bit CRC. The data block shall have COP, ERASE, LOCK_UNLOCK, CLR_PWD, SET_PWD bits set to 1.

If COP Unlock was accepted, then the card shall go to CMD42 ver.2.0 mode. While FEP=0, the only COP function supported is set FEP. “Set PWD” command shall require COP bit to be set to 0.
Before receiving COP Unlock, COP Card is CMD42 Ver.1.0 Compatible mode and CMD42 with COP bit=1 is ignored (except COP Unlock).
Note: For the card not supporting COP, the LOCK_UNLOCK_FAILED error bit shall be set in the status register and the COP enabling request is rejected.

Setting Force Erase Password (FEP):

- Unlock COP function set.
- Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bits password size (in bytes), and the number of bytes of the new password. In the case that a password replacement is done, then the block size shall consider that both passwords-the old and the new one-are sent with the command.
- Send the Card Lock/Unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode (SET_PWD and COP), the length (PWDS_LEN) and the password itself. In the case that a password replacement is done, then the length value (PWDS_LEN) shall include both passwords (the old and the new one) and the password data field shall include the old password (currently used FEP) followed by the new password. Note that the card shall handle the calculation of the new password length internally by subtracting the old password length from PWDS_LEN field.
- In the case that the sent old password is incorrect (not equal in size and content), then the LOCK_UNLOCK_FAILED error bit shall be set in the status register and the old password does not change. In the case that the sent old password is correct (equal in size and content), then the given new password and its size shall be saved in the FEP and FEP_LEN registers, respectively.
- Setting FEP automatically disables “Force Erase” and “Reset PWD” (CLR_PWD) operations. No power cycle is required.

Note that the password length register (FEP_LEN) indicates if a FEP is currently set. When it equals 0, there is no password set. Setting FEP is not affecting current card LOCK/UNLOCK state.

Unlocking COP Locked State:

If FEP=1, after power on reset or reset with CMD0, COP Card shall be in locked state and shall fail any other CMD42 parameter and LOCK_UNLOCK_FAILED error bit shall be set in the status register, unless it was done after COP function set is unlocked after the power on reset or reset by the sequence below:
Select a card (CMD7), if not previously selected.
Define the block length (CMD16) to 1 byte (8-bit card lock/unlock command). Send the card lock/unlock command with the appropriate data block of one byte on the data line including the 16 bit CRC. The data block shall have COP, ERASE, LOCK_UNLOCK, CLR_PWD, SET_PWD bits set to 1. This command does not require any password to be included in data block.

If COP Unlock was accepted, then COP Card shall go to CMD42 ver.2.0 mode and processing of other CMD42 operations shall be enabled by the card. PWD commands shall require COP bit to be set to 0.
Note: For the card not supporting COP, the LOCK_UNLOCK_FAILED error bit shall be set in the status register and the COP enabling request is rejected.

Resetting FEP:

- Unlock COP function set, if not unlocked already.
- Define the block length (CMD16), given by the 8-bit card lock/unlock mode, the 8-bit password size (in bytes), and the number of bytes of the currently used password.
- Send the card lock/unlock command with the appropriate data block size on the data line including the 16-bit CRC. The data block shall indicate the mode (CLR_PWD and COP), the length (PWDS_LEN), and the password itself. If the FEP and FEP_LEN content match the sent password and its size, then the content of the FEP register is cleared and FEP_LEN is set to 0. If the password is not correct, then the LOCK_UNLOCK_FAILED error bit shall be set in the status register.
- If resetting FEP fails, FEP and FEP_LEN registers are maintained, and the LOCK_UNLOCK_FAILED error bit shall be set in the status register.
- Resetting FEP shall not affect current card LOCK/UNLOCK state.
- Resetting FEP shall not affect PWD and PWD_LEN registers.
- Clearing FEP enables “Force Erase” and “Reset PWD” operations.
- Clearing FEP disables “FEP Force Erase” and other COP operations.

Card Ownership Protection Flowcharts

Figure 6-7-33 presents COP protection setup sequence (left) and FEP Force Erase sequence (right).
Figure 6-7-34 presents Lock/Unlock operations sequence on COP Card with FEP set

Figure 6-7-33 : COP Card Protection Setup (left) and FEP Force Erase (right) Sequences

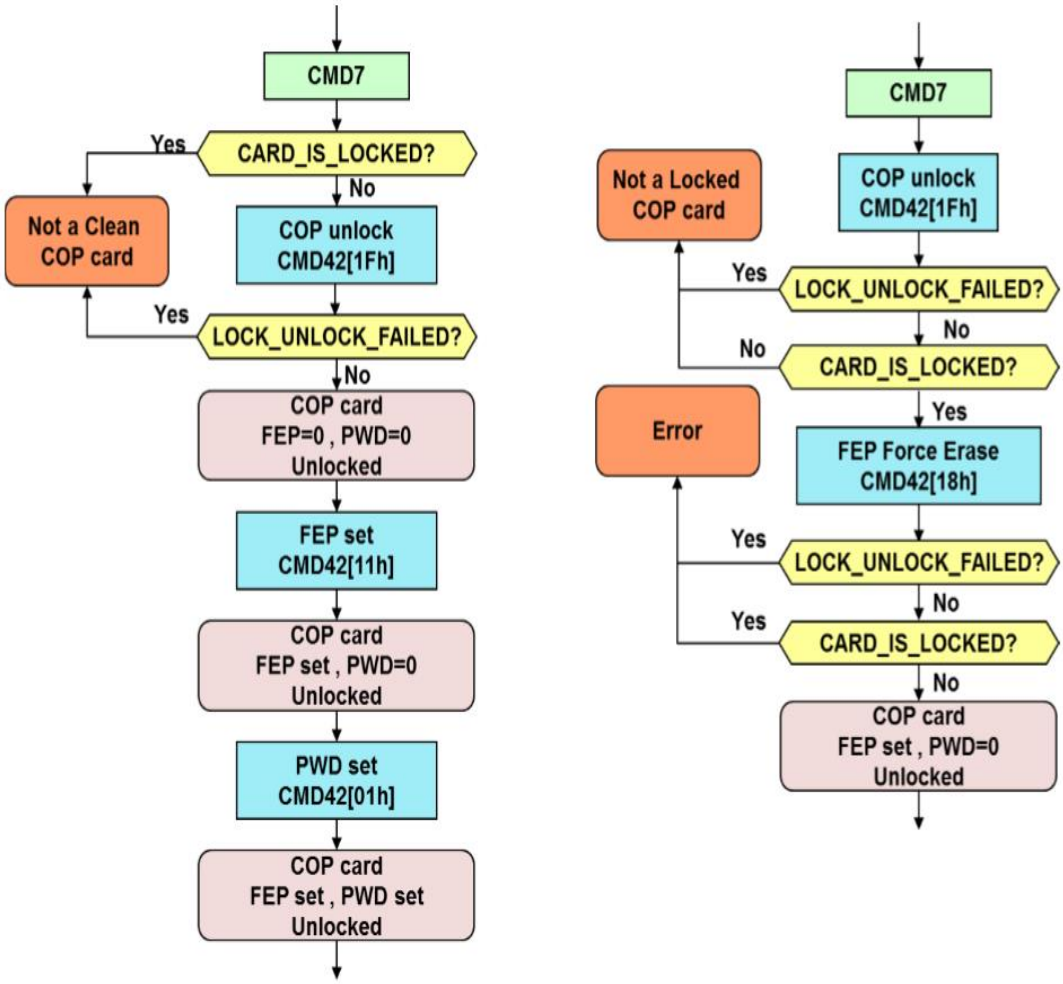
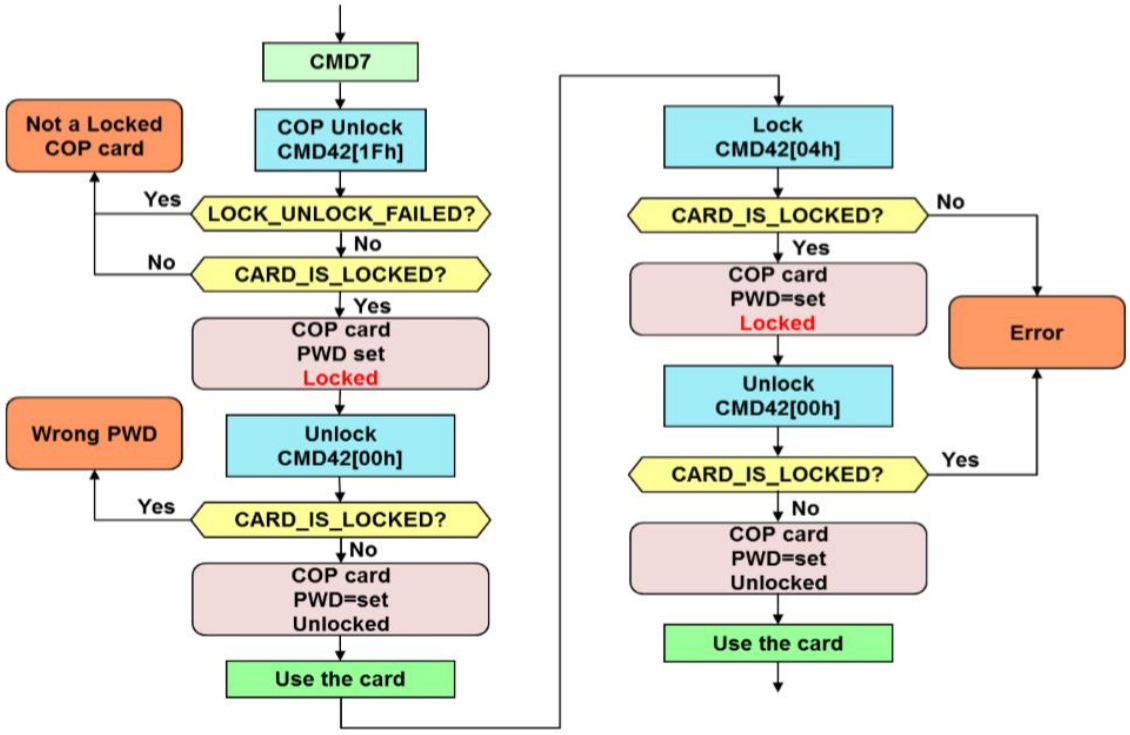


Figure 6-7-34 : COP Card Unlock/Lock Sequence



6.7.4 Parameter and the Result of CMD42

The block length shall be greater than or equal to the required data structure of CMD42; otherwise, the result of CMD42 is undefined and the card may be in the unexpected locked state. Table 6-7-41 clarifies the behavior of CMD42 for Non-COP Cards. Table 6-7-42 clarifies the behavior of PWD commands for COP Card. Table 6-7-43 clarifies the behavior of COP specific functions for COP Card. The reserved bits in the parameter (bit7-5 for COP Card and bit 7-4 for Non-COP Card) of CMD42 shall be don't care. In the case that CMD42 requires the password, it is assumed that the old password and the new password are set correctly; otherwise the card indicates an error regardless of Table 6-7-41, Table 6-7-42 and Table 6-7-43. If the password length is 0 or greater than 128 bits, the card indicates an error. If errors occur during execution of CMD42, the LOCK_UNLOCK_FAILED (Bit24 of Card Status) shall be set to 1 regardless of Table 6-7-41, Table 6-7-42 and Table 6-7-43. The CARD_IS_LOCKED (Bit25 of Card Status) in the response of CMD42 shall be the same as Current Card State in Table 6-7-41, Table 6-7-42 and Table 6-7-43. In the field of Card Status, 0 to 1 means the card changes to Locked and 1 to 0 means the card changes to Unlocked after execution of CMD42. It can be seen in the response of CMD13 after the CMD42. The LOCK_UNLOCK_FAILED (Bit24 of Card Status) as the result of CMD42 can be seen in the response of either CMD42 or the following CMD13.

Table 6-7-41: CMD42 Ver.1.0 Mode (Non-COP Card) Lock Unlock Function

CMD42 Parameter in the data
Bit3: ERASE
Bit2: LOCK_UNLOCK
Bit1: CLR_PWD
Bit0: SET_PWD

Related bits in the Card Status
Bit25: CARD_IS_LOCKED
Bit24: LOCK_UNLOCK_FAILED

CMD42 Parameter				Current Card State	PWD_LEN and PWD	Result of the Function	Card Status	
Bit3	Bit2	Bit1	Bit0				Bit25	Bit24
After Power On					Exist	The card is locked	1	0
					Cleared	The card is unlocked	0	0
1	0	0	0	Locked	Exist	Force Erase	Table 4-8	
1	0	0	0	Unlocked	Exist	Error	0	1
1	0	0	0	Unlocked	Cleared	Error	0	1
0	1	0	0	Locked	Exist	Error	1	1
0	1	0	0	Unlocked	Exist	Lock the card	0 to 1	0
0	1	0	0	Unlocked	Cleared	Error	0	1
0	1	0	1	Locked	Exist	Replace password and the card is still locked	1	0
0	1	0	1	Unlocked	Exist	Replace password and the card is locked	0 to 1	0
0	1	0	1	Unlocked	Cleared	Set Password and lock the card	0 to 1	0
0	0	1	0	Locked	Exist	Clear PWD_LEN and PWD and the card is unlocked	1 to 0	0
0	0	1	0	Unlocked	Exist	Clear PWD_LEN and PWD	0	0
0	0	1	0	Unlocked	Cleared	Error (Note *4 Refer to Table 4-10)	0	1
0	0	0	1	Locked	Exist	Replace password and the card is unlocked	1 to 0	0
0	0	0	1	Unlocked	Exist	Replace password and the card is unlocked	0	0
0	0	0	1	Unlocked	Cleared	Set password and the card is still unlocked	0	0
0	0	0	0	Locked	Exist	Unlock the card	1 to 0	0
0	0	0	0	Unlocked	Exist	Error	0	1
0	0	0	0	Unlocked	Cleared	Error	0	1
Other combinations				Don't care	Don't care	Error (Note *1 Refer to Table 4-10)	0 or 1	1

Table 6-7-42: CMD42 Ver.1.0 Mode (Non-COP Card) Lock Unlock Function

CMD42 Parameter in the data
Bit4: COP
Bit3: ERASE
Bit2: LOCK_UNLOCK
Bit1: CLR_PWD
Bit0: SET_PWD

Related bits in the Card Status
Bit25: CARD_IS_LOCKED
Bit24: LOCK_UNLOCK_FAILED

CMD42 Parameter					Current Card State	PWD	Result of the Function	Card Status	
Bit4	Bit3	Bit2	Bit1	Bit0				Bit25	Bit24
After Power On or Reset						Exist	The card is locked	1	0
						Cleared	The card is unlocked	0	0
						Don't care	The card is locked (If FEP is set (4))	1	0
X(2)	1	0	0	0	Locked	Exist	Force Erase (1)	Table 4-8	
X(2)	1	0	0	0	Unlocked	Exist	Error	0	1
X(2)	1	0	0	0	Unlocked	Cleared	Error	0	1
X(2)	0	1	0	0	Locked	Exist	Error	1	1
X(2)	0	1	0	0	Unlocked	Exist	Lock the card	0 to 1	0
X(2)	0	1	0	0	Unlocked	Cleared	Error	0	1
X(2)	0	1	0	1	Locked	Exist	Replace PWD and the card is still locked	1	0
X(2)	0	1	0	1	Unlocked	Exist	Replace PWD and the card is locked	0 to 1	0
X(2)	0	1	0	1	Unlocked	Cleared	Set PWD and lock the card	0 to 1	0
X(2)	0	0	1	0	Locked	Exist	Clear PWD_LEN and PWD and the card is unlocked (1)	1 to 0	0
X(2)	0	0	1	0	Unlocked	Exist	Clear PWD_LEN and PWD (1)	0	0
X(2)	0	0	1	0	Unlocked	Cleared	Error	0	1
X(3)	0	0	0	1	Locked	Exist	Replace PWD and the card is unlocked	1 to 0	0
X(3)	0	0	0	1	Unlocked	Exist	Replace PWD and the card is unlocked	0	0
X(3)	0	0	0	1	Unlocked	Cleared	Set PWD and the card is still unlocked	0	0
X(2)	0	0	0	0	Locked	Exist	Unlock the card	1 to 0	0
X(2)	0	0	0	0	Unlocked	Exist	Error	0	1
X(2)	0	0	0	0	Unlocked	Cleared	Error	0	1

Notes:
(1) - Disabled as long as FEP=set
(2) - Bit4 can be set to either 0 or 1 as long as FEP=0. Bit4 shall be set to 0 as long as FEP=set. Functions that shall be accepted with Bit4=1 are defined by Table 6-7-43.
(3) - Bit4 shall be set to 0 after CMD42[1Fh].
(4) - If FEP=set, all CMD42 functions are blocked before receiving CMD42[1Fh].
(5) - COP Unlock (CMD42[1Fh]) enables CMD42 COP function set. No FEP is required
(6) - CMD42[1Fh] followed by CMD42[11h]+FEP sequence is used to set FEP
Application Note:
To replace password, the host should consider following cases. When PWD_LEN and password data exist, the card assumes old and new passwords are set in the data structure. When PWD_LEN and PWD are cleared, the card assumes only new password is set in the data structure. In this case, the host shall not set old password in the data structure; otherwise, unexpected password is set.

Table 6-7-43: CMD42 Ver.1.0 Mode (Non-COP Card) Lock Unlock Function

CMD42 Parameter					Current Card State	PWD	FEP	Result of the Function	Card Status	
Bit4	Bit3	Bit2	Bit1	Bit0					Bit25	Bit24
1	1	0	0	0	Locked	Exist	Exist	Protected Force Erase (with proper FEP)(5)	1 to 0	0
1	1	0	0	0	Locked	Cleared	Exist	Error	1	1
1	1	0	0	0	Unlocked	Don't care	Exist	Error	0	1
1	0	0	1	0	Locked	Exist	Exist	Clear FEP and the card is still locked(5)	1	0
1	0	0	1	0	Unlocked	Don't care	Exist	Clear FEP and the card is still unlocked(5)	0	0
1	0	0	0	1	Locked	Exist	Don't care	Set/Replace FEP and card is still locked	1	0
1	0	0	0	1	Unlocked	Don't care	Don't care	Set/Replace FEP and the card is still unlocked	0	0
1	1	1	1	1	Unlocked	Don't care	Cleared	Enable Ver.2.0 function set	0	0
1	1	1	1	1	Locked	Exist	Cleared	Enable Ver.2.0 function set	1	0
1	1	1	1	1	Locked(1)	Cleared	Exist	(COP unlock)Enable other CMD42 functions card is unlocked (1)(3)	1 to 0	0
1	1	1	1	1	Locked(1)	Exist	Exist	(COP unlock)Enable other CMD42 functions card is PWD locked (1)(3)(4)	1	0
1	1	1	1	1	Locked(2)	Exist	Exist	Card is still locked (2)(4)	1	1
1	1	1	1	1	Unlocked	Don't care	Exist	Card is still unlocked	0	1

Notes:
(1) - 1st time after Power On Reset or Reset
(2) - 2nd time or more after Power On Reset or Reset
(3) - "COP Unlock" – CMD42[1Fh] with no FEP is required to access any other CMD42 commands after power on reset or reset, when FEP=set
(4) - If PWD is set, Unlock with PWD - CMD42[00h] is required to unlock the card after "Unlock COP"
(5) - Disabled as long as FEP=0
(6) - Commands not covered by Table 6-7-42 and Table 6-7-43 shall return LOCK_UNLOCK_ERROR with no change to card state.
Application Note: To replace password, the host should consider following cases. When FEP_LEN and password data exist, the card assumes old and new passwords are set in the data structure. When FEP_LEN and FEP are cleared, the card assumes only new password is set in the data structure.

Commands Accepted for Locked Card

The locked card shall accept commands listed below and return response with setting CARD_IS_LOCKED.

1) Basic class (0)
2) Lock card class (7)
3) CMD16
4) ACMD41
5) ACMD42

All other commands including security commands are treated as illegal commands.

Note: CMD11 (Class 0) and CMD40 (Class 7) are new commands accepted in the locked card state. CMD40 is reserved for Security Specification.

Application Note: After power on or reset, the host can recognize the card lock/unlock state by the CARD_IS_LOCKED in the response of CMD7 or CMD1

6.8 Error Handling

To correct defects in the memory field inside card the card include error correction codes in the payload data (ECC). This correction is intended to correct static errors. Additionally two methods of detecting errors generated during the data transfer (dynamic errors) via a cyclic redundancy check (CRC) are implemented

6.8.1 Error Correction Code (ECC)

The ATP SD Card is free of static errors. All errors are covered inside the card; even errors occurring during the lifetime of the card are covered for the user. The only effect which may be notified by the end user is, that the overall memory capacity may be reduced by small number of blocks. All flash handling is done on card, so that no external error correction is needed.

6.8.2 Cyclic Redundancy Check (CRC)

The CRC is intended for protecting SD Card commands, responses and data transfer against transmission errors on the SD Card bus. One CRC is generated for every command and checked for every response on the CMD line. For data blocks one CRC per transferred block is generated. The CRC is generated and checked as described in the following.

CRC7

The CRC7 check is used for all commands, for all responses except type R3, and for the CSD and CID registers. The CRC7 is a 7-bit value and is computed as follows:
generator polynomial: G(x) = x7 + x3 + 1.
M(x) = (first bit) * xn + (second bit) * xn-1 +...+ (last bit) * x0 CRC[6...0]
= Remainder [(M(x) * x7) / G(x)]
The first bit is the most left bit of the corresponding bit string (of the command, response, CID or CSD). The degree n of the polynomial is the number of CRC protected bits decreased by one. The number of bits to be protected is 40 for commands and responses (n = 39), and 120 for the CSD and CID (n = 119).

CRC16

In case of one DAT line usage (as in MultiMediaCard) than the CRC16 is used for payload protection in block transfer mode. The CRC check sum is a 16-bit value and is computed as follows:
generator polynomial G(x) = x16 +x12 +x5 +1
M(x) = (first bit) * xn + (second bit)* xn-1 +...+ (last bit) * x0 CRC[15...0] = Remainder [(M(x) * x16) / G(x)]
The first bit is the first data bit of the corresponding block. The degree n of the polynomial denotes the number of bits of the data block decreased by one (e.g. n = 4095 for a block length of 512 bytes). The generator polynomial G(x) is a standard CCITT polynomial. The code has a minimal distance d=4 and is used for a payload length of up to 2048 Bytes (n <= 16383). The same CRC16 method is used in single DAT line mode and in wide bus mode. In wide bus mode, the CRC16 is done on each line separately.

6.8.3 CRC and Illegal Command

All commands are protected by CRC (cyclic redundancy check) bits. If the addressed card's CRC check fails, the card does not respond and the command is not executed. The card does not change its state, and COM_CRC_ERROR bit is set in the status register.
Similarly, if an illegal command has been received, the card will not change its state, will not response and will set the ILLEGAL_COMMAND error bit in the status register. Only the non-erroneous state branches are shown in the state diagrams contains a complete state transition description.
There are different kinds of illegal commands:
Commands which belong to classes not supported by the card (e.g. write commands in read only cards).
Commands not allowed in the current state (e.g. CMD2 in Transfer State).
Commands which are not defined (e.g. CMD5).

6.8.4 Read, Write and Erase Time-out

The times after which a time-out condition for read operations occurs are (card independent) either 100 times longer than the typical access times for these operations given below or 100ms (the lower of them).
The times after which a time-out condition for Write/Erase operations occurs are (card independent) either 100 times longer than the typical program times for these operations given below or 250ms (the lower of them).
A card shall complete the command within this time period, or give up and return an error message. If the host does not get any response with the given time out it should assume the card is not going to respond anymore and try to recover (e.g. reset the card, power cycle, reject, etc.).
The typical access and program times are defined as follows:

Read

For a Standard Capacity SD Memory Card, the times after which a timeout condition for read operations occurs are (card independent) either 100 times longer than the typical access times for these operations given below or 100 ms (the lower of the two). The read access time is defined as the sum of the two times given by the CSD parameters TAAC and NSAC. In the case of a single read operation, these card parameters define the typical delay between the end bit of the read command and the start bit of the data block. In the case of a multiple-read operation, they also define the typical delay between the end bit of a data block and the start bit of next data block. A High Capacity SD Memory Card and Extended Capacity SD Memory Card indicate TAAC and NSAC as fixed values. The host should use 100 ms timeout (minimum) for single and multiple read operations rather than using TAAC and NSAC.

Write

For a Standard Capacity SD Memory Card, the times after which a timeout condition for write operations occurs are (card independent) either 100 times longer than the typical program times for these operations given below or 250 ms (the lower of the two). The R2W_FACTOR field in the CSD is used to calculate the typical block program time obtained by multiplying the read access time by this factor. It applies to all write commands (e.g. SET(CLR)_WRITE_PROTECT, PROGRAM_CSD and the block write commands). High Capacity SD Memory Card and Extended Capacity SD Memory Card indicate R2W_FACTOR as a fixed value.
In case of High Capacity SD Memory Card, maximum length of busy is defined as 250ms for all write operation.
While the card should try to maintain that busy indication of write operation does not exceed 250ms in the case of SDXC card, if the card is not possible to maintain operations with 250ms busy, the card can indicate write busy up to 500ms including single and multiple block write in the following scenarios:

a) The last busy in any write operation up to 500ms including single and multiple block write.
b) When multiple block write is stopped by CMD12, the busy from the response of CMD12 is up to 500ms.
c) When multiple block write is stopped by CMD23, the busy after the last data block is up to 500ms
d) Busy indication at block gap in multiple block write is up to 250ms except a following case. When the card executes consecutive two blocks write (2*512Bytes) and it spans across the physical block boundary, the busy after the each block can be indicated up to 500ms.

Especially regardless of the above definition, a speed class writing mode specified by CMD20 shall keep write busy up to 250ms in any case until the end of speed class write is indicated.

There are two types of busies in a multiple block write operation.

(1) Write busy at block gap (without CMD12) is maximum 250ms
(2) Write busy after CMD12 is maximum 250ms (500ms for SDXC)

If CMD12 is issued during a multiple block write operation's busy period, the host timeout counter is reset and the 250ms (500ms for SDXC) timeout period is measured from the response of CMD12.

Erase

If the card supports parameters for erase timeout calculation in the SD Status, the host should use them to determine erase timeout. If the card does not support these parameters, erase timeout can be estimated by block write delay.
The duration of an erase command can be estimated by the number of write blocks (WRITE_BL) to be erased multiplied by 250 ms.

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