AFE840x System Evaluation Kit and GC Studio Reference

User's Guide

Literature Number: SLWU034A
May 2006–Revised November 2008

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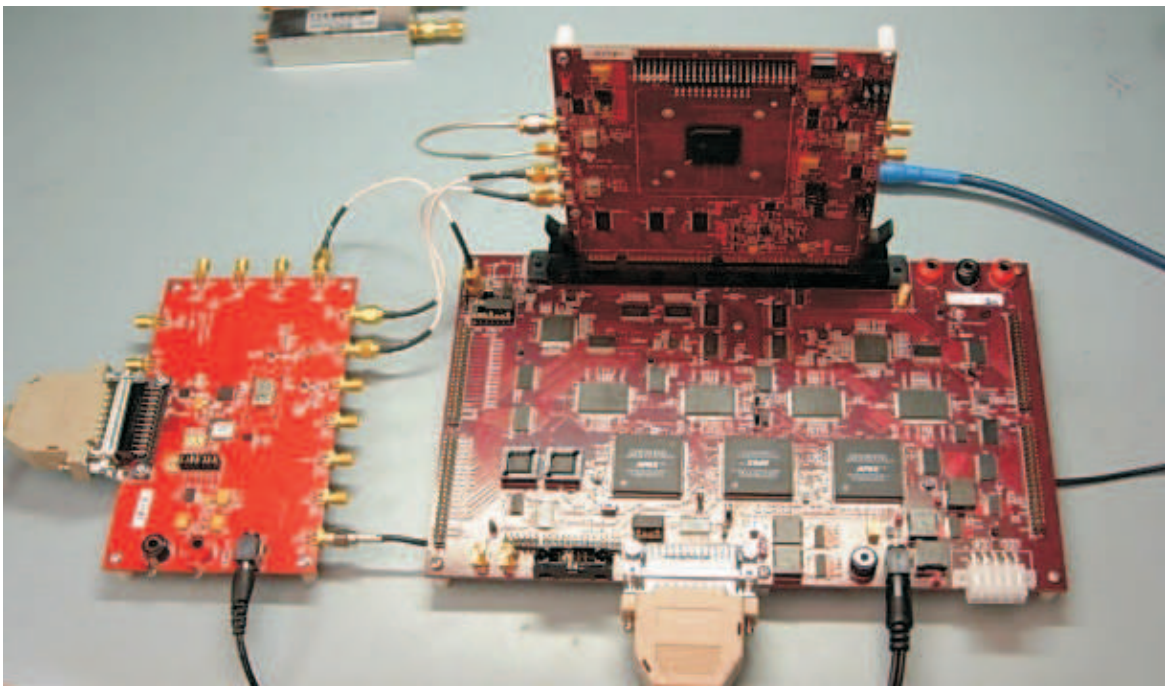
AFE840x System Evaluation Kit (SEK) Overview

The AFE840x is a multichannel communications signal processor that provides analog-to-digital conversion and digital downconversion optimized for cellular base transceiver systems. The AFE8405 and AFE8406 both support UMTS, CDMA-1X and TD-SCDMA air-interface cellular standards.

The AFE8405 provides up to 8 UMTS digital downconverter channels (DDC), 16 CDMA DDCs, or 16 TD-SCDMA DDCs. The DDC channels are independent and operate simultaneously. The AFE8405 has two input ports: one is hardwired to an internal 14-bit analog-to-digital converter and the other is a 16-bit digital input. Each DDC channel can be programmed to accept data from any one of the two input ports.

The AFE8406 provides up to 8 UMTS digital downconverter channels (DDC), 16 CDMA DDCs, or 16 TD-SCDMA DDCs. The DDC channels are independent and operate simultaneously. The AFE8406 has four input ports: two are hardwired to internal 14-bit analog-to-digital converters and two are 16-bit digital inputs. Each DDC channel can be programmed to accept data from any one of the four input ports.

The AFE8405 and AFE8406 SEK's are a set of hardware and software tools designed to ease the AFE840x evaluation. This guide provides a step-by-step description on how to set up the AFE840x system solution.



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1.1 AFE840x System Evaluation Kit

The AFE840x system evaluation kit includes the items shown in Figure 1-1:

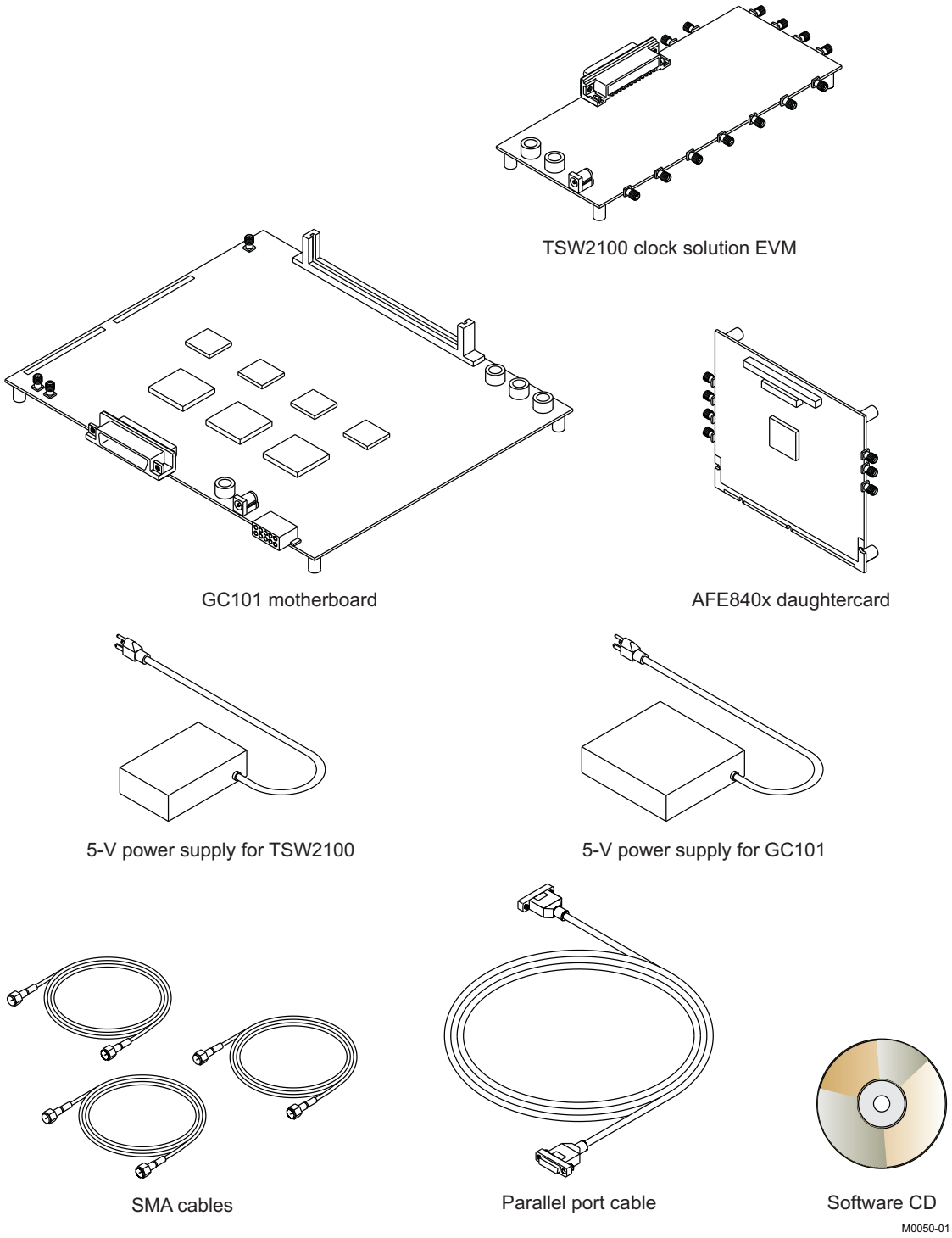


Figure 1-1. Kit Contents

The CD includes two software packages that must be installed before connecting the hardware:

- TSW2100 SPI software – used to configure the TSW2100
- GC Studio software – used to configure the GC101 and AFE8406 as well as to analyze the results

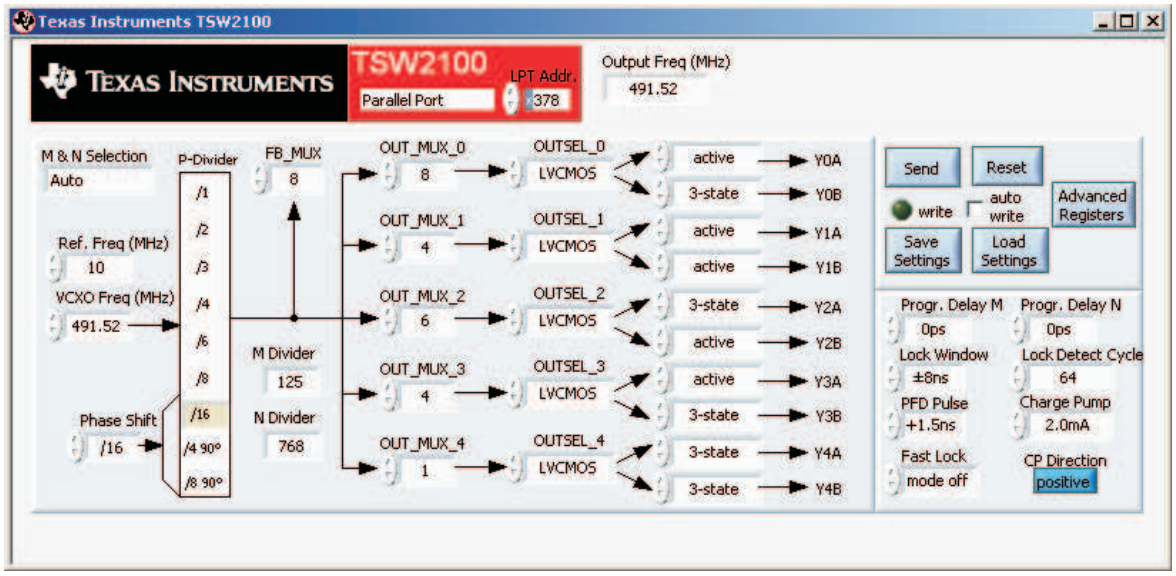
Installing the Software

All necessary software to operate the serial interface is provided on the included CD. This section describes in detail how to install the required software packages.

2.1 TSW2100 SPI Software Installation

The TSW2100 SPI is a GUI-based software that allows full control and programmability of the CDCM7005 (core device of the TSW2100). Load the software as follows:

1. Insert the CD into the computer to be used to operate the serial interface.
2. Open the TSW2100_Installvxpx folder, where vxpx is the software version.
3. Double-click on the file called setup.exe.
4. The installation wizard opens. Follow the on-screen instructions.
5. After the installation is complete, you can access the program from the programs list on the Start menu.
6. On starting the program, the following screen should be present:



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For more information on the various parameters shown on the GUI, see the CDCM7005 product page: http://focus.ti.com/docs/prod/folders/print/cdcm7005.html.

2.2 GC Studio Software Installation

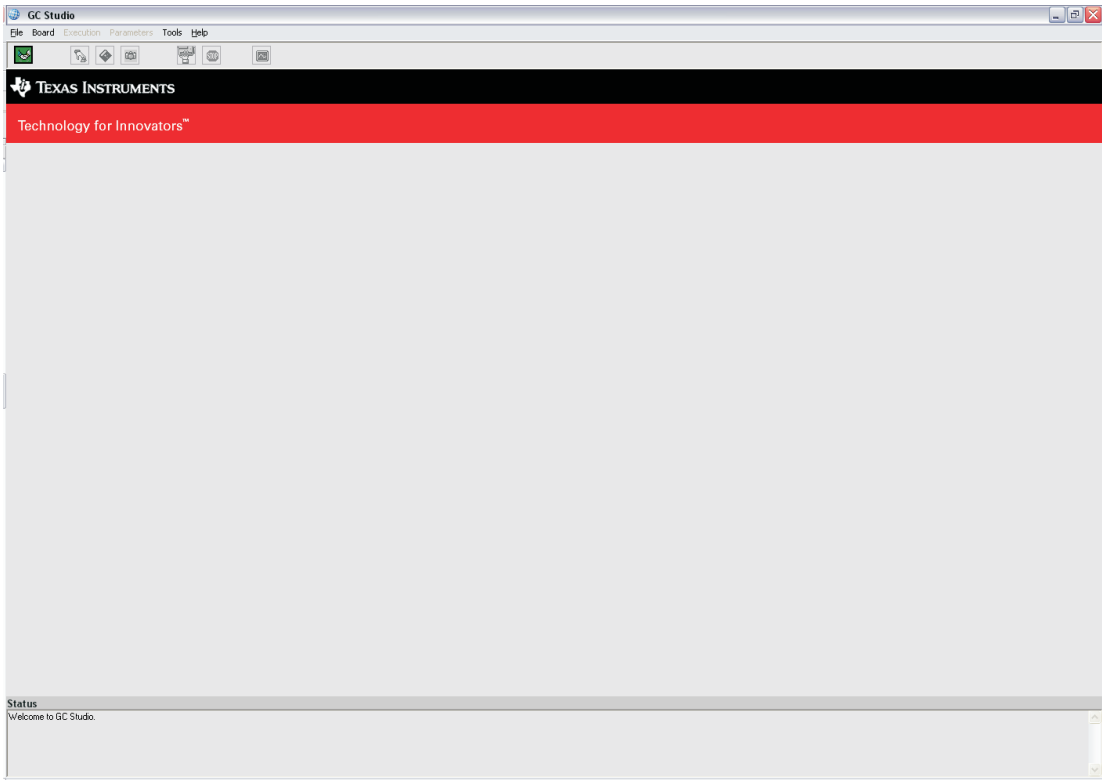
The GC Studio software program, along with the GC101 motherboard, provides a framework to evaluate the AFE840x. The primary uses of the GC101 EVM are to program the AFE840x, to provide a stream of stimulus information, and to capture the response information for processing by the computer. The GC Studio software controls the GC101 EVM, provides a stimulus image, and retrieves and processes the response image. Several GC Studio projects for the AFE8405 and AFE8406 are included in the installation. These projects can be used as the starting point for creating new experiments.

The minimum requirements to install GC Studio are:

- Host computer (PC) with BIOS supporting ECP mode for LPT1, running Windows™ 98 SP 2, Windows ME, Windows 2000 SP 1, Windows XP™ Home or Windows XP Professional
- Administrator group privileges

The steps to install GC Studio are as follows:

1. Insert the CD into the computer to be used to operate the serial interface.
2. Double-click the file called GCStudio_Setup_xx_xx_xxxxxx.exe, where xx_xx_xxxx corresponds to the GC Studio version number.
3. The installation wizard opens. Follow the on-screen instructions. This loads the main GC Studio software.
4. After the installation is complete, you can access the program from the programs list on the Start menu.
5. To start the program, click on the Windows menu sequence **Start - All Programs - GC Studio - GC Studio**. On starting the program, the following screen should be present:



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Setting up the System

3.1 Hardware Setup

The GC101 and AFE840x daughtercard require three clocks when used for operation with an analog input signal. The clocks are described in Table 3-1.

Table 3-1. Clock Requirements

BOARD	CONNECTOR	DESCRIPTION
AFE840x daughtercard	CLKP (J6)	AFE840x ADC clock. On the AFE840x daughtercard, this signal is converted to a differential signal and routed to AFE840x balls CLK(M/P)(A/B). It must be a low-jitter clock for optimal performance.
AFE840x daughtercard	CLKM (J5)	AFE840x digital clock. Routed to AFE840x ball RXCLK.
GC101 motherboard	EXT CLK (J1)	Digital clock input for GC101. Digital source and capture rate.

When the AFE840x FIFO is enabled (recommended), an arbitrary skew between the AFE840x ADC clock and the AFE840x digital clock can be used. The skew between the AFE840x digital clock and the GC101 EXT CLK is important, and the optimum setting depends on the clock frequency. Note that the frequency of the two digital clocks must be the same frequency and locked.

The TSW2100 EVM provides a platform for providing multiple clock sources without any other equipment. In particular, several outputs have an amplifier and filter circuit that can provide a low-jitter clock for the AFE840x ADC clocks. The TSW2100 default configuration has a 491.52-MHz VCXO, which allows for output frequencies of 491.52/N MHz, where N = 2, 3, 4, 6, 8, or 16. See the *TSW2100 EVM User's Guide* (SLWU026) for more information. The default board has three filter clock paths at 122.88 MHz, 81.92 MHz, and 61.44 MHz (N = 4, 6, and 8, respectively).

Alternatively, the TSW2100 VCXO can be bypassed so that an input signal with arbitrary frequency can be used. In this mode, the TSW2100 can still be used as a multiple-output buffer and clock divider.

In the default configuration, the TSW2100 can generate a filtered ADC clock at 61.44 MHz and two digital clocks for the AFE840x daughtercard and GC101 at 122.88 MHz. This is a common configuration for WCDMA applications. With this configuration, the TSW2100 EVM and GC101/AFE840x cards are connected as described in the following steps and in Figure 3-1.

1. Plug the AFE840x daughtercard into the GC101 EVM.
2. Connect the TSW2100 to the GC101/AFE840x system using the included SMA cables, as indicated in Table 3-2.
3. Connect the external analog input signal(s) to AIN and/or BIN (AFE8406 only) on the AFE840x daughtercard.
4. For synchronization, an external 10-MHz reference can be plugged into the TSW2100 J2 SMA connector. If this is the case, ensure there is a jumper on J14 between pins 11 and 12. If using the onboard reference, then the jumper must be between pins 10 and 11.
5. Ensure the remaining jumpers for the TSW2100 are installed as follows: W2 pins 2-3, J14 pins 2-3, 5-6, 8-9, 10-11, 14-15, 17-18, 20-21, 26-27, and 29-30. Verify that the jumpers on the AFE840x are set as indicated in Table 3-3.

Table 3-2. SMA Cable Connections

TSW2100 SMA Connector	GC101/AFE8406 SMA Connector
J3 (Y1A)	AFE840x J5 (CLKM)
J4 (Y1B)	GC101 J1 (EXTCLK)
J12 (Y0A)	AFE840x J6 (CLKP)

Table 3-3. Default Jumper Settings

Jumper		Connect Pins
Rev. F Boards	All Other Boards	
W2	J7	2–3
W3	J8	1–2
W4	J9	1–2
W5	W27	1–2
W6	J23	Open
W7	W14	1–2
W8	W25	1–2
W9	J17	3–4, 5–6 for AFE8406; 3-4 for the AFE8405
W10	W15	1–2
W11	W26	1–2
W12	J11	1–2
W13	J12	2–3
SJP1	JP1	2–3
SJP2	JP2	2–3
SJP3	JP3	2–3
SJP4	JP4	2–3
N/A	W13	1–2

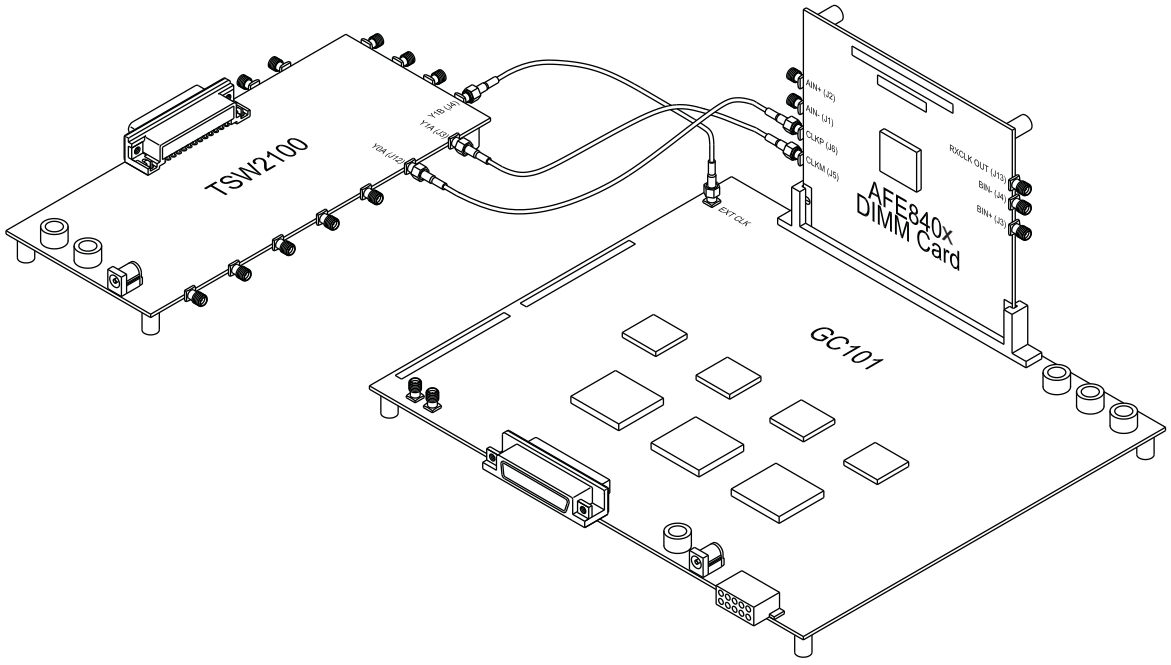

Figure 3-1. System Setup

A typical setup with external 10-MHz reference is shown in Figure 3-2.

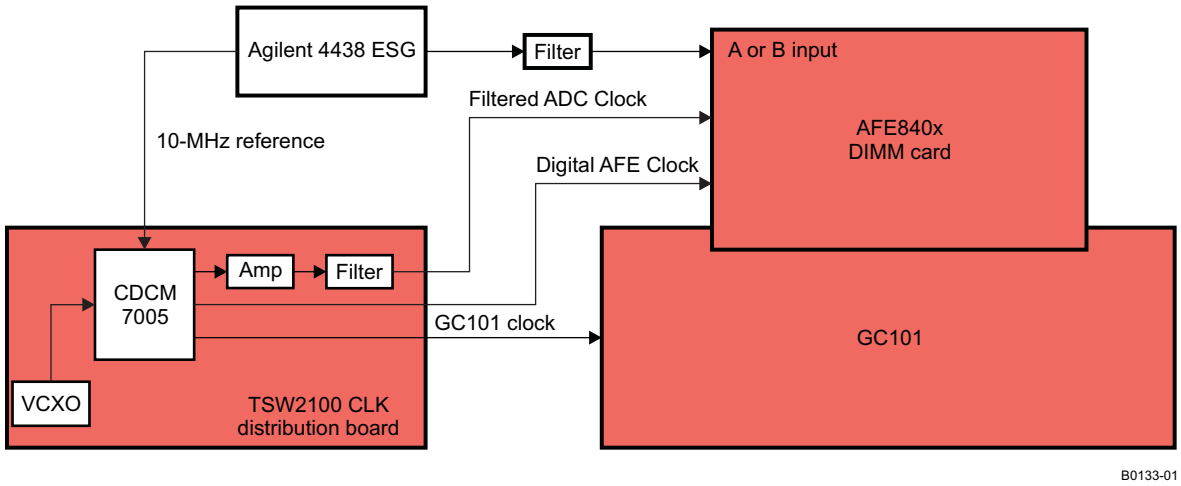

Figure 3-2. Typical Setup

The following steps are required to set up the TSW2100:

1. If using a USB interface, plug the provided USB-to-parallel port adapter board into J10 of the TSW2100 EVM. Connect one end of the supplied USB interface cable to a PC USB port and the other end of the cable into J1 of the adpater board. If using a parallel port interface, plug one end of the provided parallel-port cable into J10 on the EVM and the other end to the PC parallel port.
2. Provide 5 V to J15 by using the power supply provided. LED D1 should light, indicating that the reference input is present. LED D3 should light, indicating that the VCXO input is present. If LED D1 does not light, ensure that a jumper is on J14 between pins 10 and 11 if using the onboard reference. The jumper should be between pins 11 and 12 if using the external reference.
3. Open the TSW2100 SPI software.
4. The default settings assume that the base address for the parallel port is hexadecimal 378. If this is not the case, the base address should be changed to match your computer configuration. If using the USB adapter board, go to the red GUI window that displays *Parallel Port* located at the top of the TSW2100 GUI. Click on this box and select the *USB* option.
5. Click the *Load Setting* button (Figure 3-3). This opens up a window asking for an *.reg7005 configuration file. Load the file TSW2100_491p52VCXO_61p44Filter.reg7005, located on the provided CD.
6. Click the *Send* button (Figure 3-3). LED D2 should light, indicating that the clock outputs are synchronized with the reference input. The EVM is now ready to clock the AFE840x and GC101 boards.

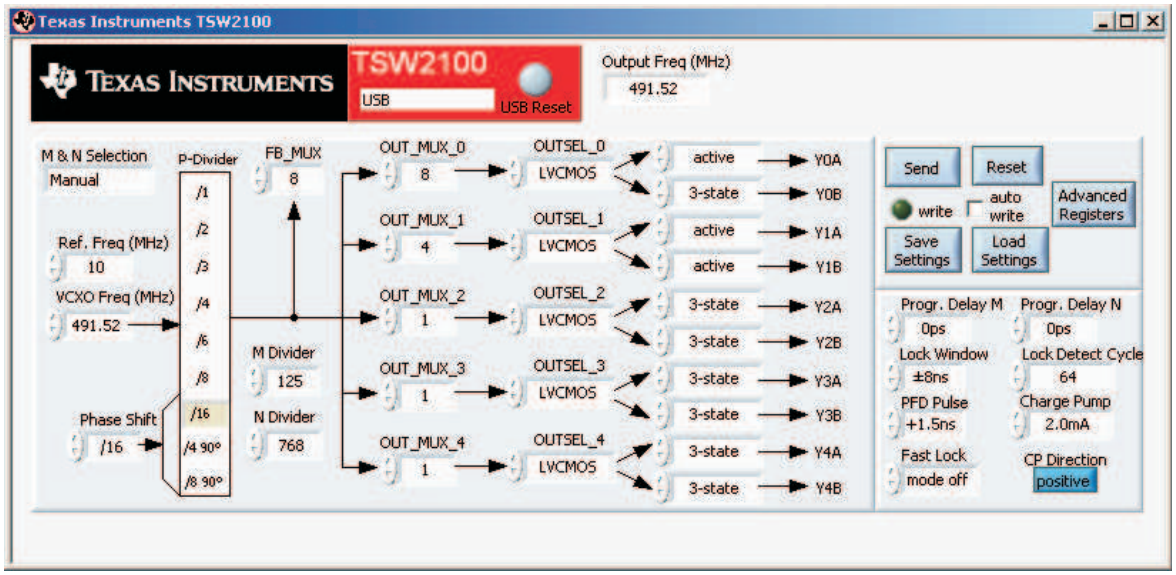

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Figure 3-3. TSW2100 SPI Software Screen

3.2 Loading and Running a GC Studio Project

The simplest way to use GC Studio with the AFE840x is to open an existing project and to modify it according to the application-specific requirements. These projects are loaded during the installation of GC Studio at **My Documents - My GC Studio Projects - AFE8405 and AFE8406**. The following example projects, along with the corresponding TSW2100 setup files, are included in the Experiments directory:

3.2.1 ADC Experiments: AFE840x_TESTBUS_EX Directory

In this project, the AFE840x test bus is used to obtain the internal analog-to-digital converter outputs with a sampling rate of 61.44 Msps and 81.92 Msps. The ADC outputs are decimated by a factor of 32.

3.2.2 UMTS Experiment: AFE840x_UMTS_EX Directory

In this project, a UMTS signal with IF frequency of 15.36 MHz, either from analog input or file, is downconverted. The ADC rate is 61.44 Msps. The NCO mixes the input down to baseband. The mixer baseband output is upsampled 2× (zero-stuffed) to 122.88 Msps. The zero-stuffed output is decimated 8× by the CIC filter, then decimated 2× by a 32-tap CFIR, with final symbol shaping provided by a 64-tap PFIR. Serial output of the recovered UMTS signal (7.68 Msps) is captured from output port A0 and graphed spectrally.

3.2.3 CDMA2000 Experiment: AFE840x_CDMA2k_EX Directory

In this project, a two-carrier CDMA2000 signal with IF frequency of 8.6432 MHz, either from analog input or file, is downconverted. The ADC rate is 78.6432 Msps. The NCO mixes the carriers down to baseband. The mixer outputs are decimated 16× by the CIC filter, then decimated 2× by a 32-tap CFIR, with final symbol shaping provided by a 64-tap PFIR. Serial outputs of the recovered CDMA2000 signals (2.4576 Msps) are captured from output ports A0 and B0 and graphed spectrally.

3.2.4 DDC AGC Experiment: AFE840x_AGC_EX Directory

This project demonstrates the adaptation of the DDC AGC. The AFE8406 built-in self-test circuit is used to output a constant which, when multiplied by the NCO, generates a sinusoid signal at the input to the AGC block. Both the PFIR and CFIR have the maximum positive value (131071) programmed into the corresponding tap0 to allow signal values to pass through the FIRs without being disturbed. In CDMA

mode, two signals are present in the interleaved data stream (A and B). To demonstrate the effectiveness of the AGC on both streams, the A and B paths have different AGC gain values. The AGC operation causes the two signals converge to the same amplitude, one from a lower value (requiring amplification) and one from a higher value (requiring attenuation). Adjusting the agc_gaina_lsb/msb (GAIN_FOR_A) and agc_gainb_lsb/msb (GAIN_FOR_B) values adjusts the amount of change. The rate of change is controlled by the following parameters: agc_dabv, agc_dblw, agc_dsat, and agc_dzro.

3.2.5 ADC Experiment: AFE840x_ADC_EX Directory

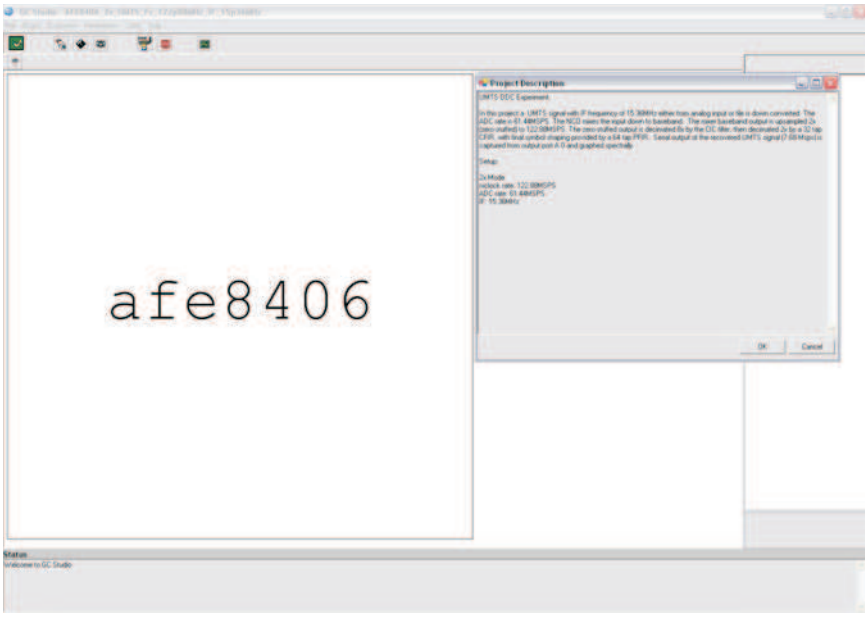
In this project, an input IF of 70.1 MHz, provided from an external source, is sent to the internal analog-to-digital converter outputs with a sampling rate of 61.44 Msps. The ADC outputs are decimated 8× by the CIC filter, then decimated 2× by a 32-tap CFIR, with final symbol shaping provided by a 64-tap PFIR.

3.2.6 Parallel Port Output Experiment: AFE840x_Parallel_Output_EX Directory

In this project, the ADC is bypassed and a digital test pattern is brought in through the C digital-input port. The zero-stuffed output is decimated 8× by the CIC filter, then decimated 2× by a 32-tap CFIR, with final symbol shaping provided by a 64-tap PFIR.

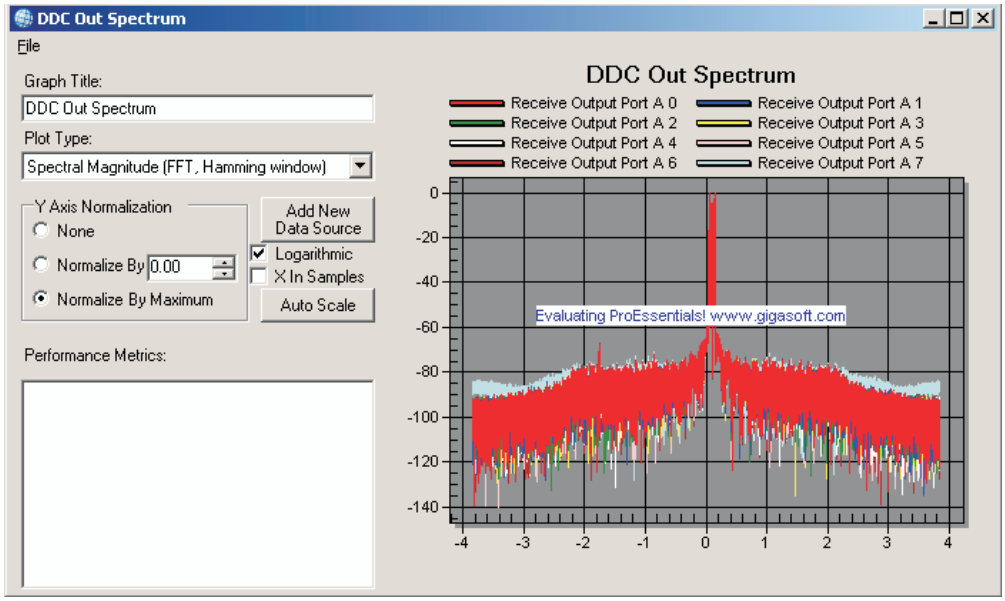
To load and run an existing GC Studio project, perform the following steps:

- Connect the parallel-port cable to the port connector on the GC101.
- Provide power to the GC101 using the power supply provided.
- Open the GC Studio program from the Start menu. This opens the main GC Studio window.
- Select Open Project… from the File menu. From the CD, go to the AFE8405 experiments directory. Under the directory called *AFE8405_Parallel_Output_EX*, select the project called *afe8405_cicd8_cfird2_pfird1_umts_parinCsel.gcproj*. This loads the experiment into GC Studio. This experiment will work with either the AFE8405EVM or the AFE8406EVM.
- In the same directory, load the TSW2100 with the file called *tsw2100_rxclk_gc101_122p88_adc61p44.reg7005*.

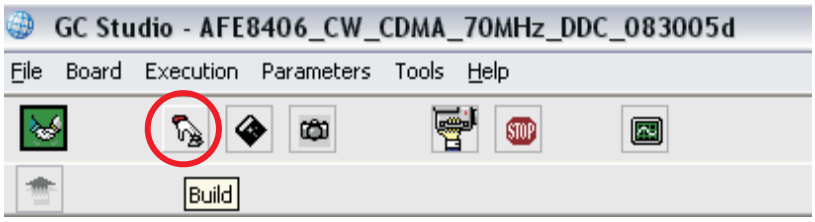


C005

- Click on the Build button. This instructs GC Studio to build the experiment, load it into the GC101 and AFE840x, and capture one frame of data.
- After the experiment is complete, the captured data should look as shown.

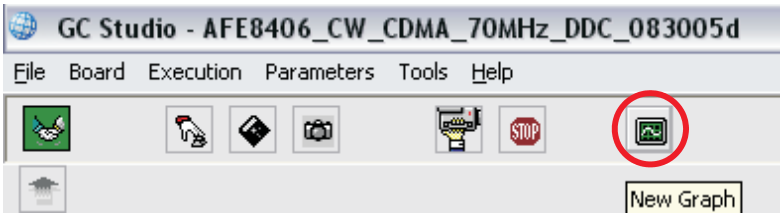


C052



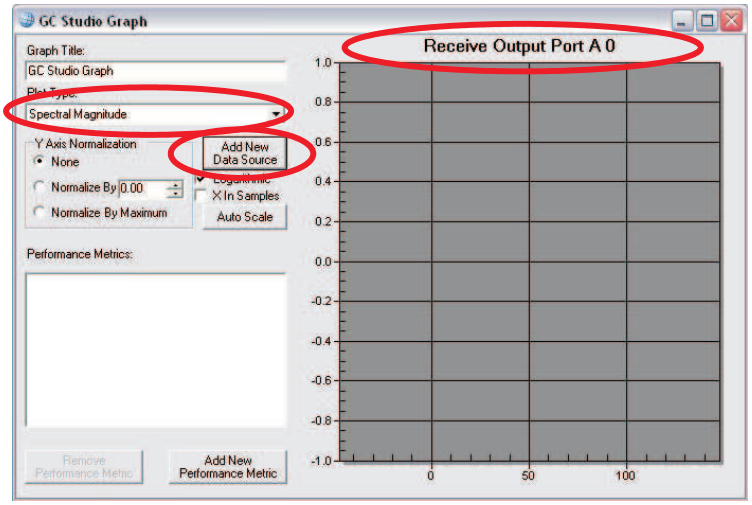
C006

- Each of the example projects comes with a set of predefined plots. New plots can be added by clicking on the New Graph button on the top toolbar.



C007

- This example lists the steps to add the spectral plot of output port A0: On the graph window click on Plot Type and choose Spectral Magnitude. Also, put a checkmark on the Logarithmic box. Click on Add New Data Source to add Receive Output Port A 0 to the graph.



C008

- After adding the new data source, the FFT plot of output port A 0 is displayed on the right side of the screen.

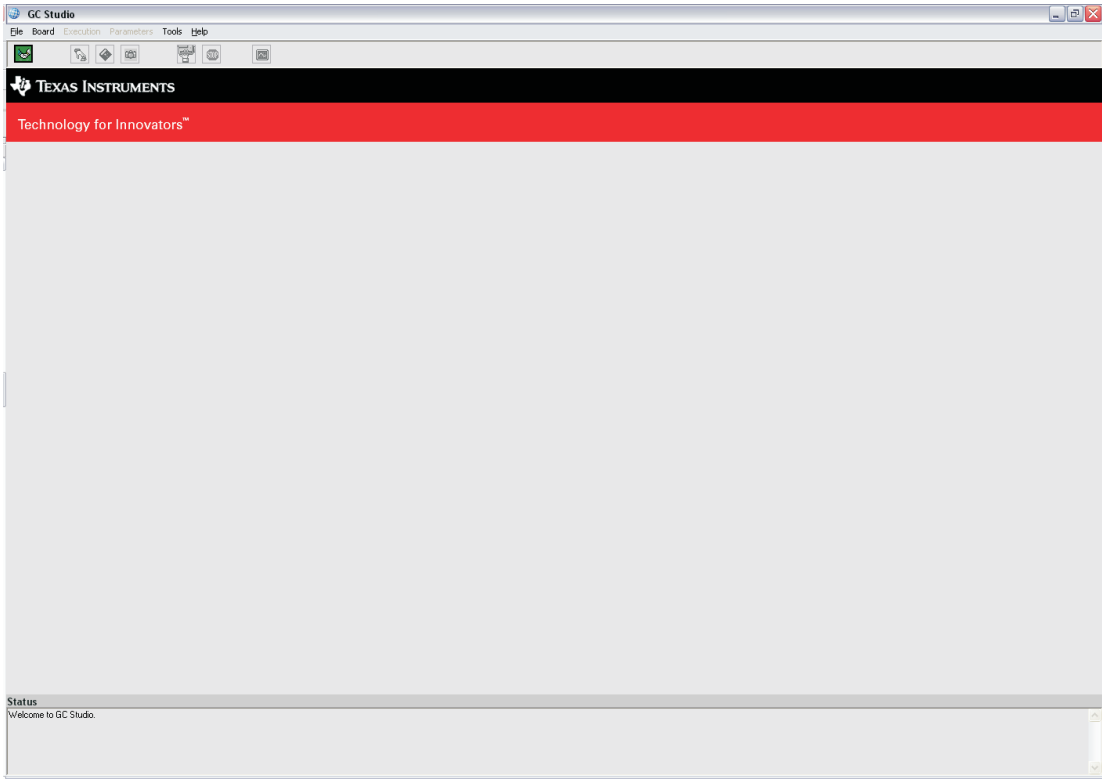
3.3 Creating a New GC Studio Project

The following example describes how to generate a new GC Studio project from scratch. In this project, an AFE8406 is configured to process a UMTS signal. The same example can be performed with an AFE8405EVM. The AFE8406 configuration details are as follows:

- A single, real UMTS carrier is applied to the AFE8406 rxin_c and rxin_d digital inputs with a simulated sample rate of 61.44 Msps and an IF frequency of 15.36 MHz.
- The RXCLK to the AFE840x is 122.88 MHz.
- Receive FIFOs are enabled.
- Receive AGC is bypassed.
- Receive channel 0 is configured to process the signal.
- The mixer/NCO shifts the 15.36-MHz IF to dc.
- The dc-centered signal is zero-stuffed to increase the rate from 61.44 Msps to 122.88 Msps. This is required, as the CIC uses only full-rate RXCLK input signals.
- The CIC filter is programmed to decimate by 8. The output sample rate at the CIC output is 15.36 Msps.
- The CFIR filter compensates for the droop in the CIC filter and provides some low-pass filtering. It is configured as a 32-tap filter, which is the maximum length that can be computed with RXCLK at 122.88 MHz and the CFIR output rate of 7.68 Msps.
- The 64-tap PFIR provides final symbol shaping and filtering.
- Channel AGC is configured as fixed unity gain.
- Baseband data is transmitted and captured using the serial interface at the full RXCLK rate.

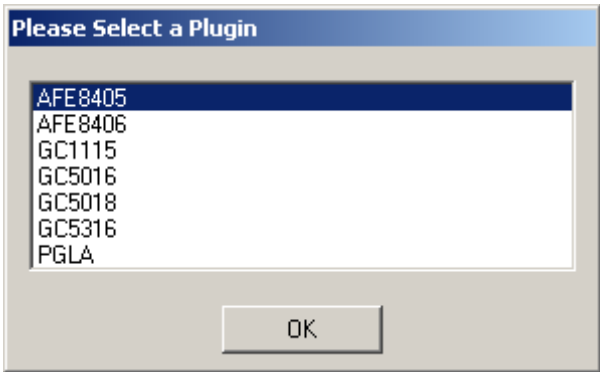
To generate the project, follow these steps:

1. Start GC Studio.



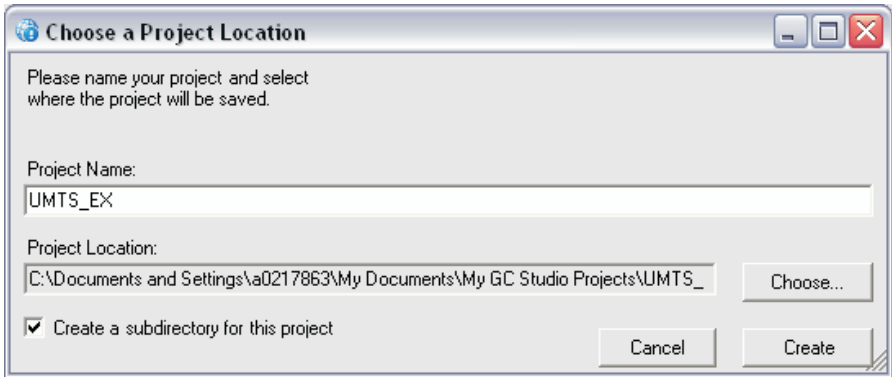
C003

2. Select AFE8406 for the plug-in and click OK.



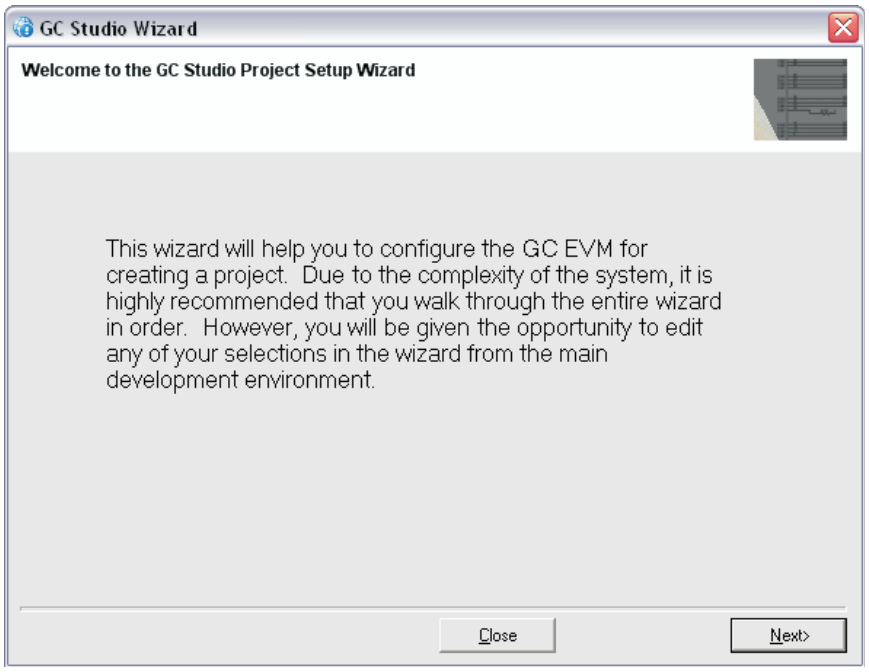
C010

3. Select New Project from the File menu and choose a name for the new project. Click create.



C009

4. Click Next> on the Welcome to the GC Studio Project Setup Wizard window.



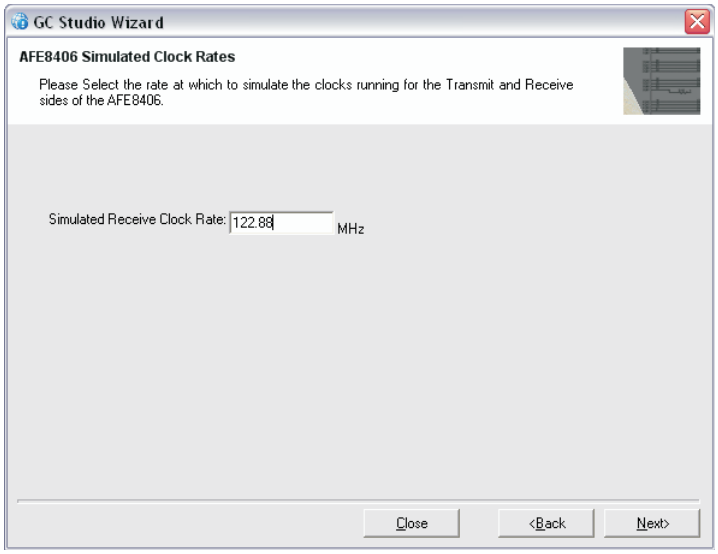
C011

5. Configure the AFE8406 I/O mode. In this example, ensure the ADC clock rate is set to 1/2 and that the Rx Sync Offsets and Lengths satisfy the requirements described in Section 4.2. Click Next>.


GC Studio Wizard
AFE8406 I/O Mode Selection
This determines what ports from the AFE8406 are available to bring back to the PC. Please choose both an input and an output mode
Output Mode
DDC Outputs
SyncOut+
rx_sync_out_6
Sp5
interrupt
Sp6
rx_sync_out_0
OutClk
rxclk_out
ADC Clock Rate
1/2
Rx Sync A Offset (From beginning of memory)
305000
Rx Sync A Length
100
Rx Sync B Offset (From beginning of memory)
305000
Rx Sync B Length
100
Enable 1.5V Regulator
Close
<Back
Next>

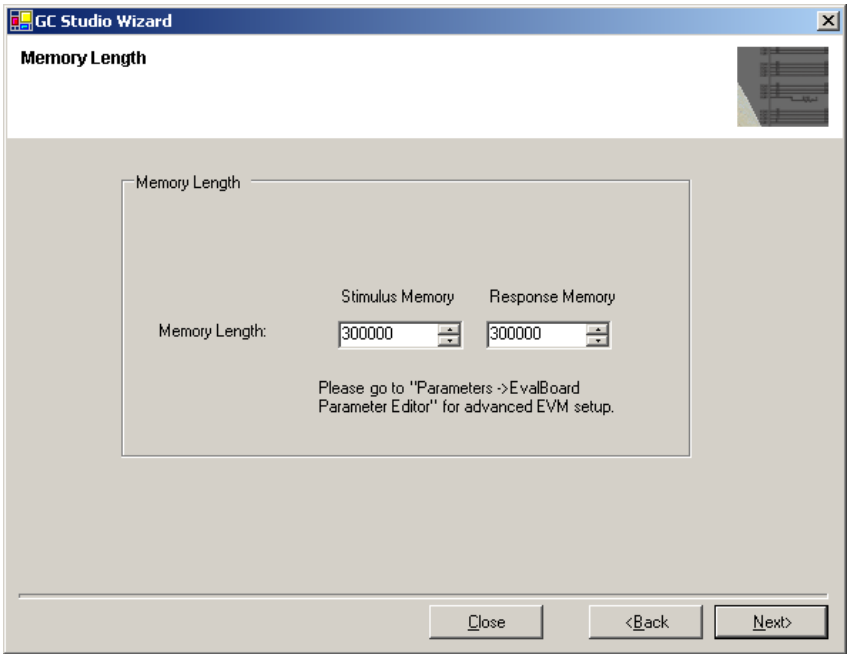
C013

6. Set the simulated clock rate to 122.88 MHz and click Next>.



C014

7. Click Next> on Channel Copying.
8. Set the desired Stimulus and Response Memory length. Click Next>.



C053

9. Enter a description for the project. Click Next>.

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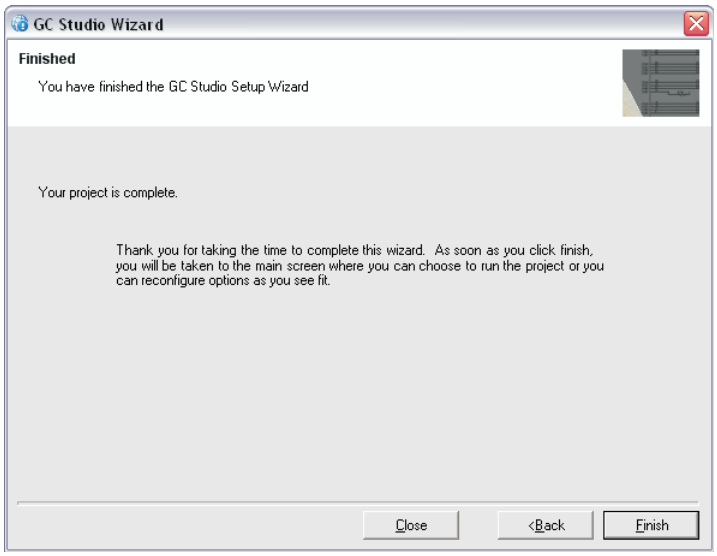
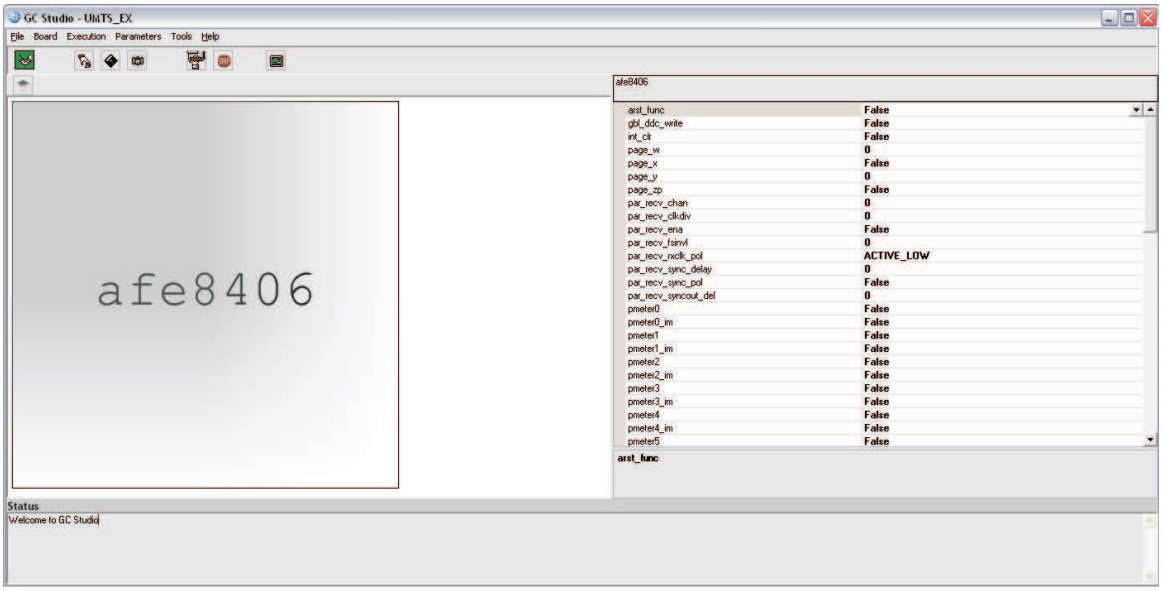
10. Click Finish to exit the GC Studio Wizard.



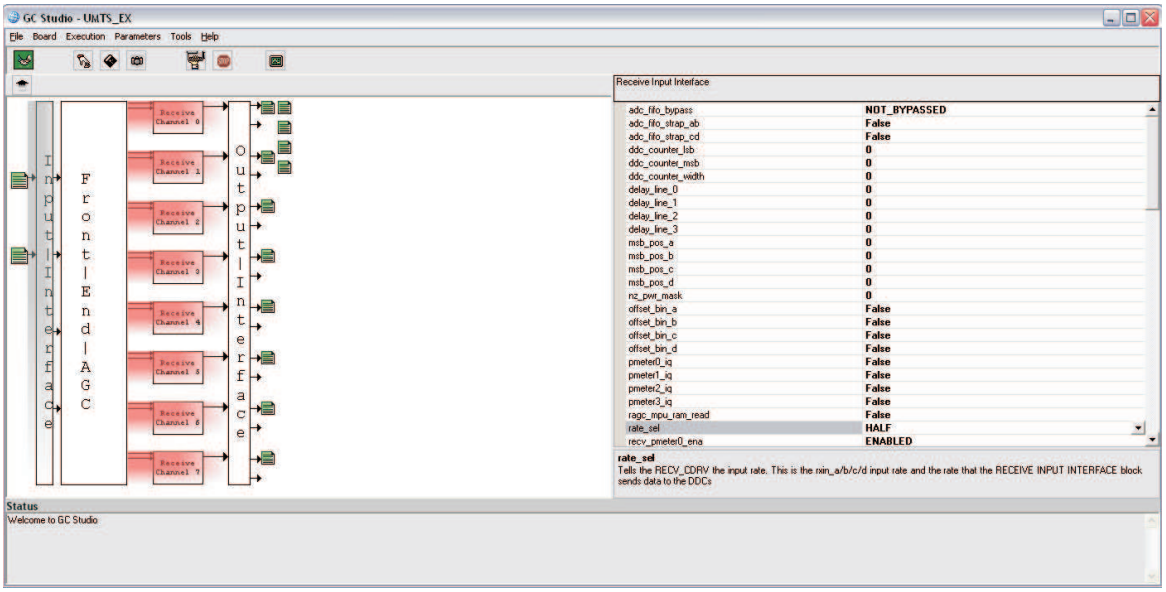
C017

11. Click on the large AFE8406 box on the left side of the GUI to display the global control registers.



C018

12. Double-click on the AFE8406 block to *push down* one level into the AFE8406. Click on the Input Interface block to display and edit the receive input interface registers. Set rate_sel to HALF; this configures the AFE8406 for input samples at 1/2 the RXCLK rate. Set adc_fifo_bypass to NOT BYPASSED to enable the rxin_a/b/c/d input FIFO circuits.



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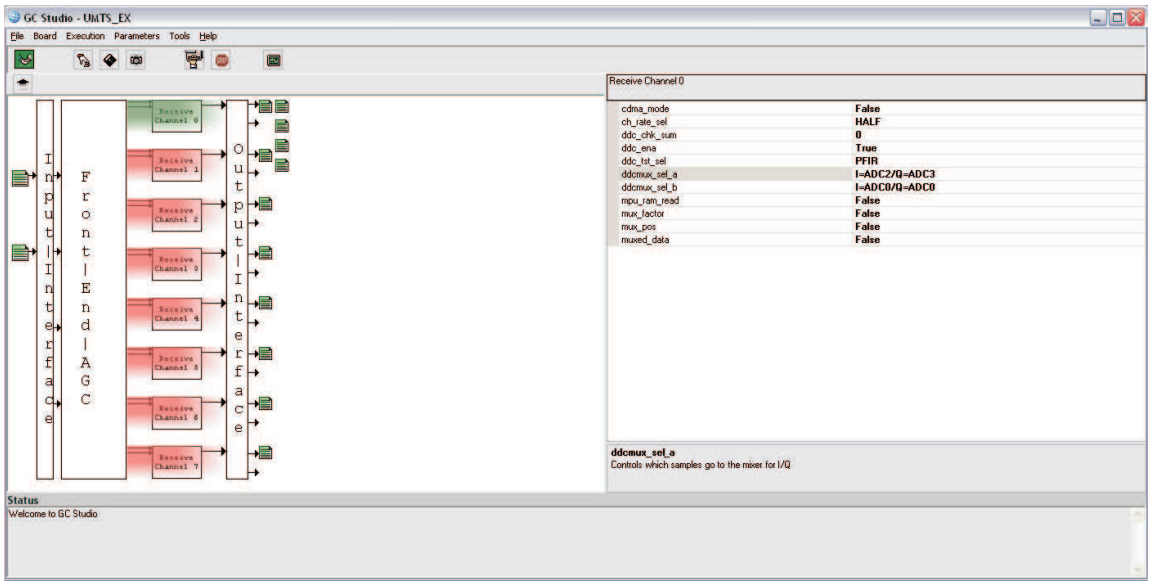
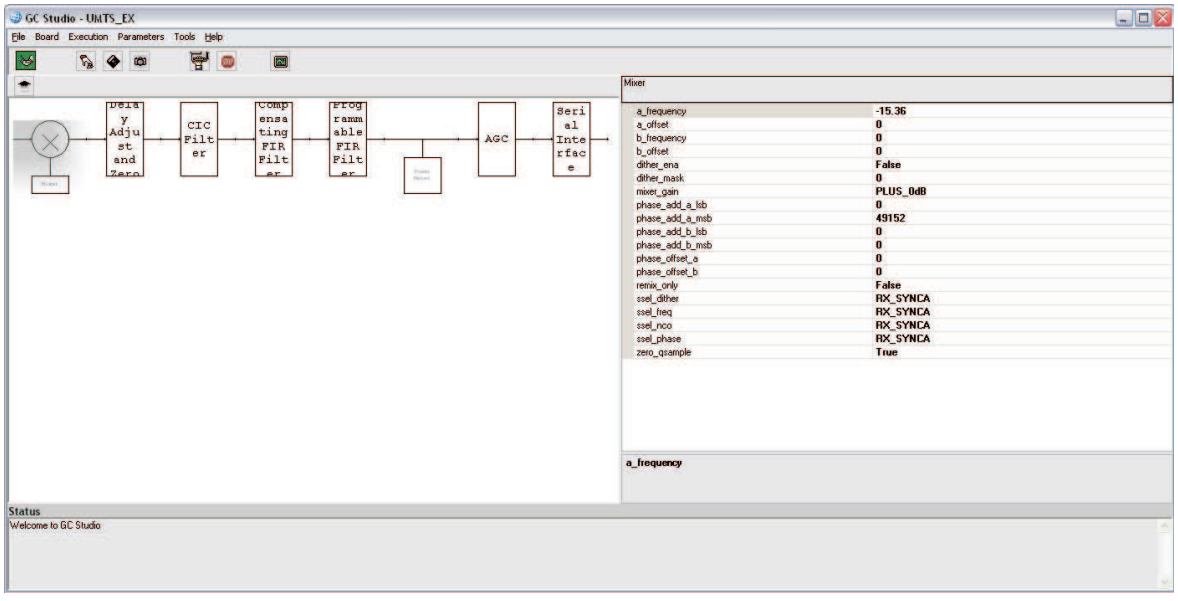
13. Click on the upper Receive Channel 0 block. Set ddc_ena to True. The topmost receive channel will change to green because it has been enabled. Set ddcmux_sel_a to I = ADC2/Q = ADC3; this selects the AFE8406 digital rxin_c and rxin_d input ports as the I and Q data sources. If the UMTS signal is to be provided externally, set ddcmux_sel_a to I = ADC0/Q = ADC0.



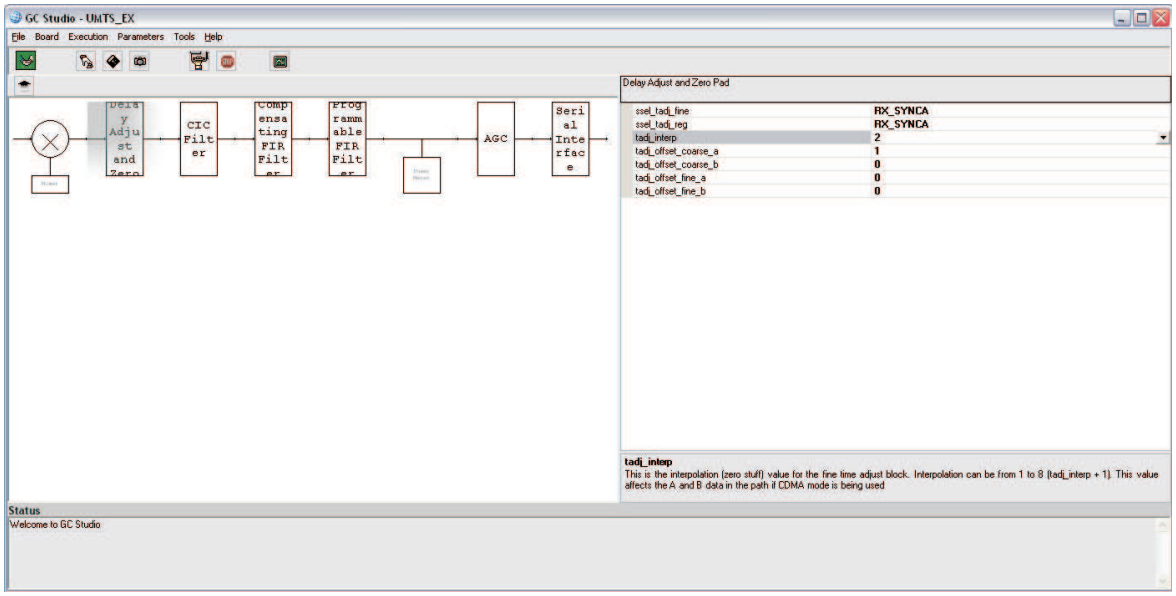
C020

14. Double-click on the Receive Channel 0 block to push down into this channel. The block diagram now shows the subblocks in the receive channel, and the registers to configure it. Select the mixer/NCO block (leftmost block). Set a_frequency to –15.36 (MHz). The b_frequency setting is not used when the channel is in UMTS mode. *GC Studio calculates the required values for the phase_add registers and updates the values after the experiment is run.* Set zero_qsample to True. Verify the settings match those shown in the following panel.



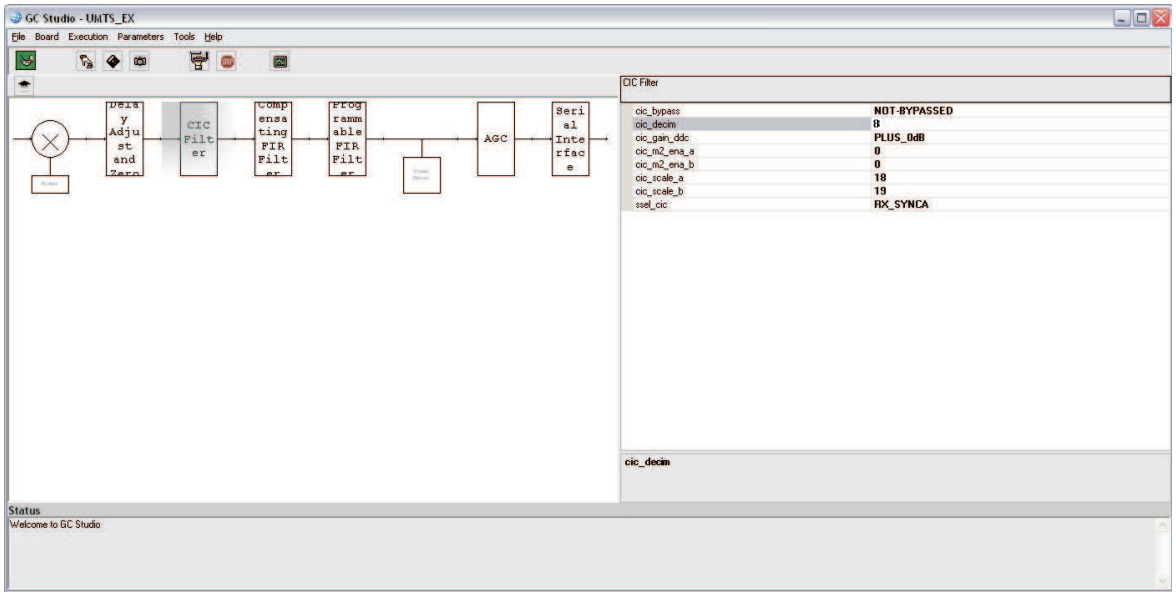
C021

15. Select the Delay Adjust and Zero Stuff block. Because the input sample rate is set to 1/2 the RXCLK rate, this block is automatically configured by GC Studio to interpolation by 2, inserting a zero sample between each actual sample before being applied to the CIC filter. This moves the 61.44-Msps input signal stream to the 122.88-Msps RXCLK rate. The tadj_offset_coarse and tadj_offset_fine settings allow the user to adjust the delay between various receive channels if desired.



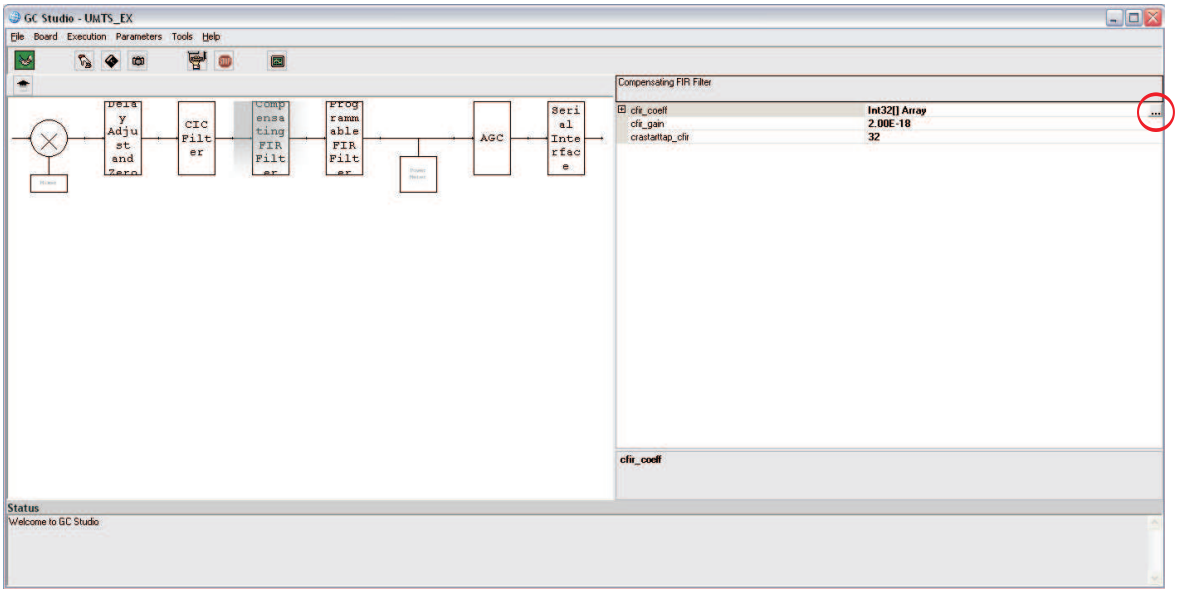
C022

16. Click on the CIC filter block and set the registers as shown in the following panel. The decimation in the CIC is set to 8, resulting in a 15.36-Msps CIC output rate.



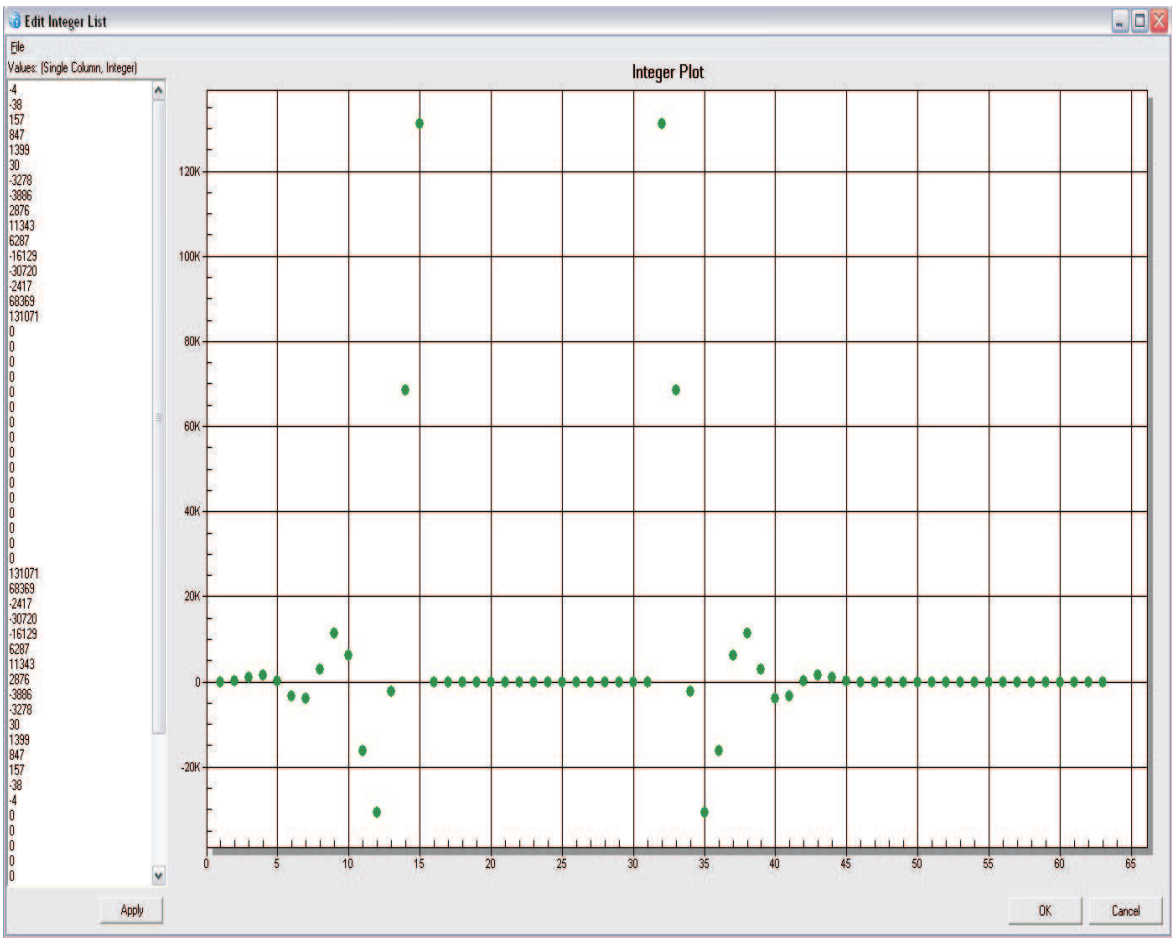
C023

17. Select the CFIR block, set cfir_gain to 2.00E-18, and set cra_starttap_cfir to 32 taps. Next, select the cfir_coeff register setting by clicking on it, and then click on the browse button, circled in red on the preceding panel, to open the Edit Filter window and fill in the CFIR filter tap weights.



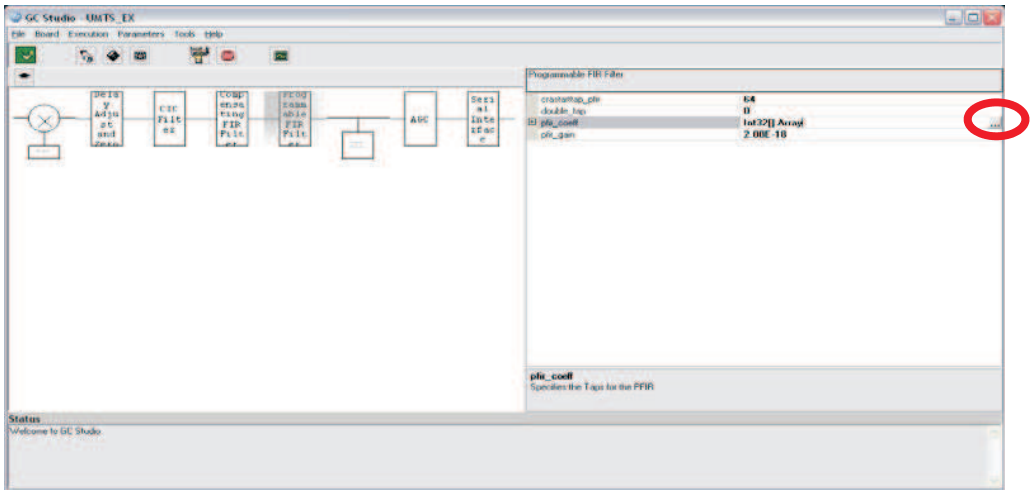
C024

18. The CFIR tap weights are entered as shown. Note that the first 20 taps are entered as the first 20 entries, and then 12 lines are skipped before entering the second 20. This is due to the AFE8406 coefficient RAM being split into two blocks of 32 words. See the AFE8406 data sheet (SLWS168) for more details, if necessary. For this example, the CFIR tap weights are:



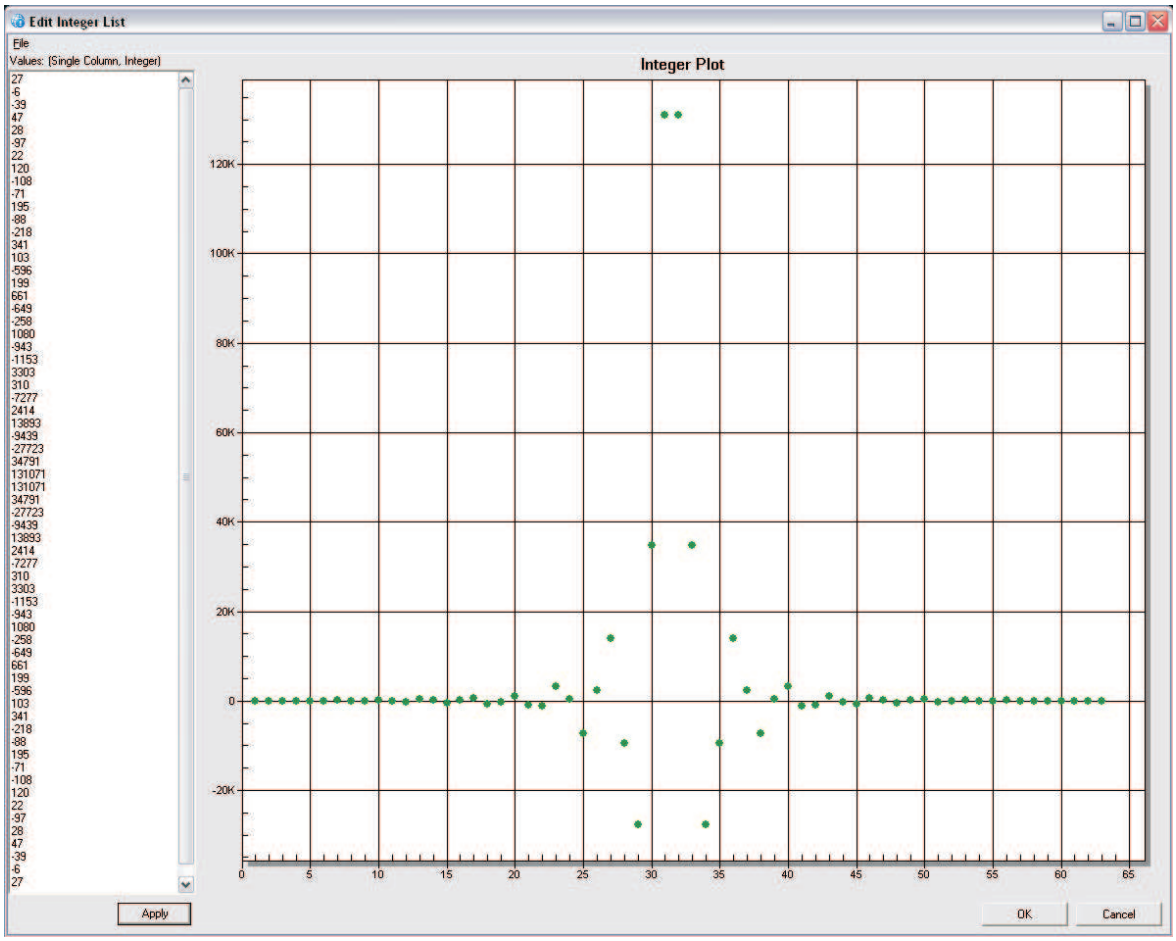
C025

19. Select the PFIR block, set pfir_gain to 2.00E-18, and set crastarttap_pfir to 64. Select the pfir_coeff register, and again select the browse button.



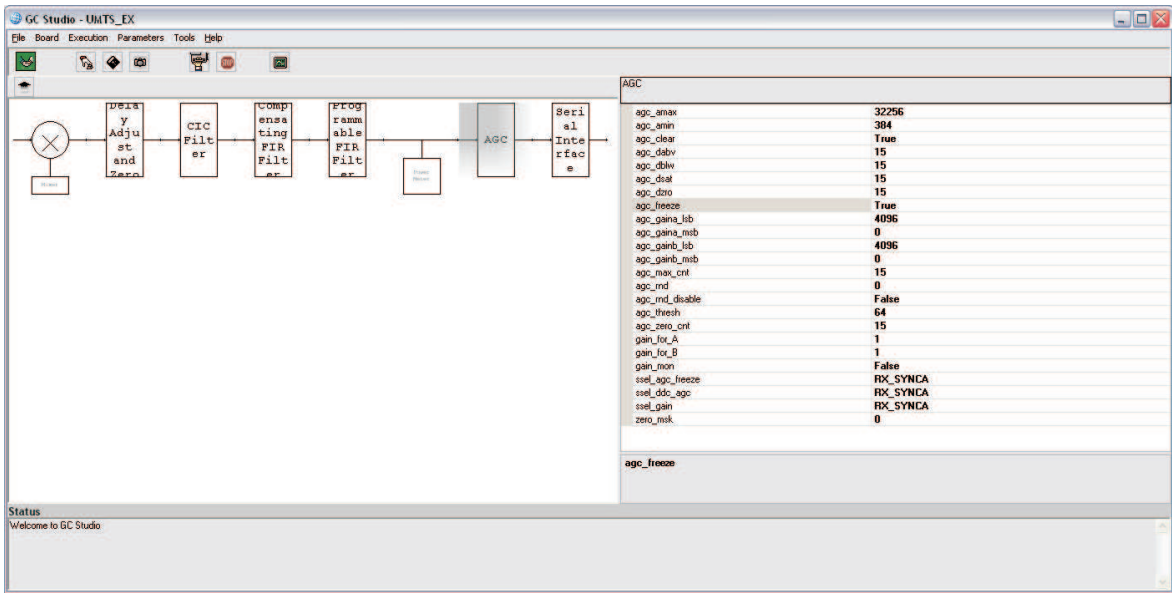
C026

20. The PFIR tap weights are entered as shown. For the 64-tap PFIR in this example, all coefficients are used. For this example, the PFIR tap weights are:



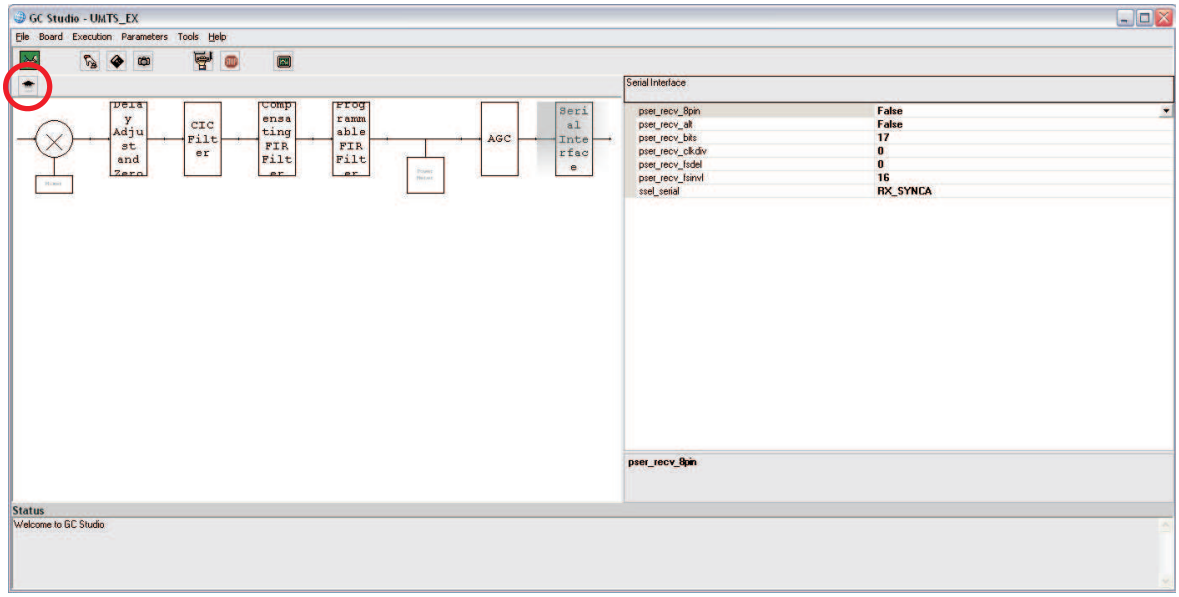
C027

21. Select the AGC block and set the registers as shown in the following panel. The gain_for_A value is set to unity, and the agc_freeze and agc_clear are both set to True for this example. This puts the AGC in unity fixed-gain mode. GC Studio calculates the required values for the agc_gain registers and updates the values after the experiment is run.



C028

22. Select the Serial Interface block and set the parameters as indicated.



C029

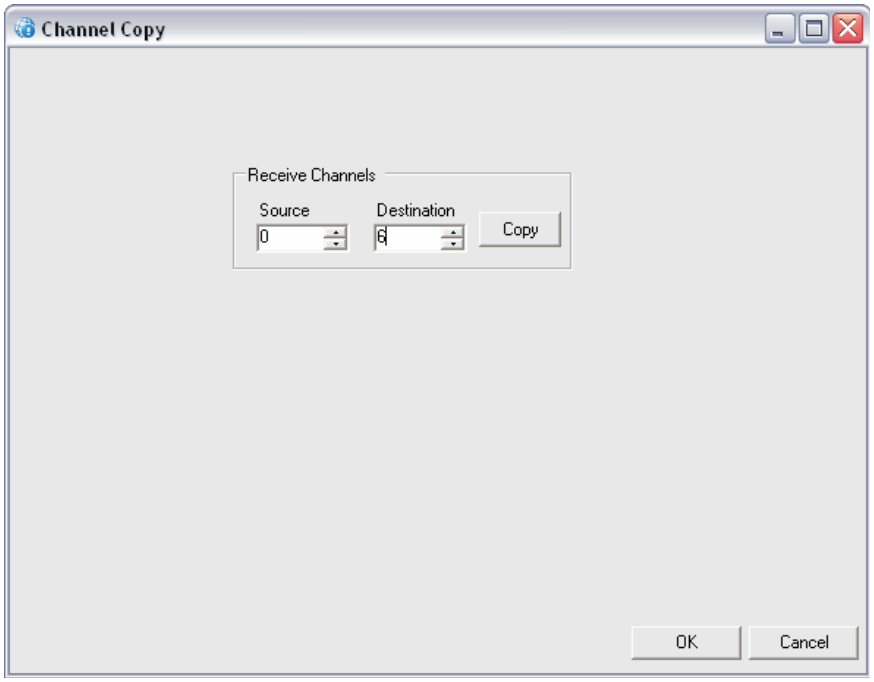
23. After verifying the values for the serial interface, click the arrow circled in red in the preceding panel to pop up one level in the AFE8406 hierarchy.

    Through the preceding steps, receive channel 0 has now been configured as follows:

    - UMTS input signal at 61.44 Msps with a 15.36-MHz IF
    - Mixer/NCO block shifts the signal to dc.
    - Zero-stuff block interpolates by 2, moving the 61.44-Msps signal to 122.88 Msps.
    - CIC block decimates by 8, to 15.36 Msps.
    - 32-tap CFIR compensates for the CIC droop, filters and decimates the signal to 7.68 Msps.
    - 64-tap PFIR filters the signal.
    - Channel AGC is set to a fixed gain of 1.
    - Serial interface is used to output the baseband signal.

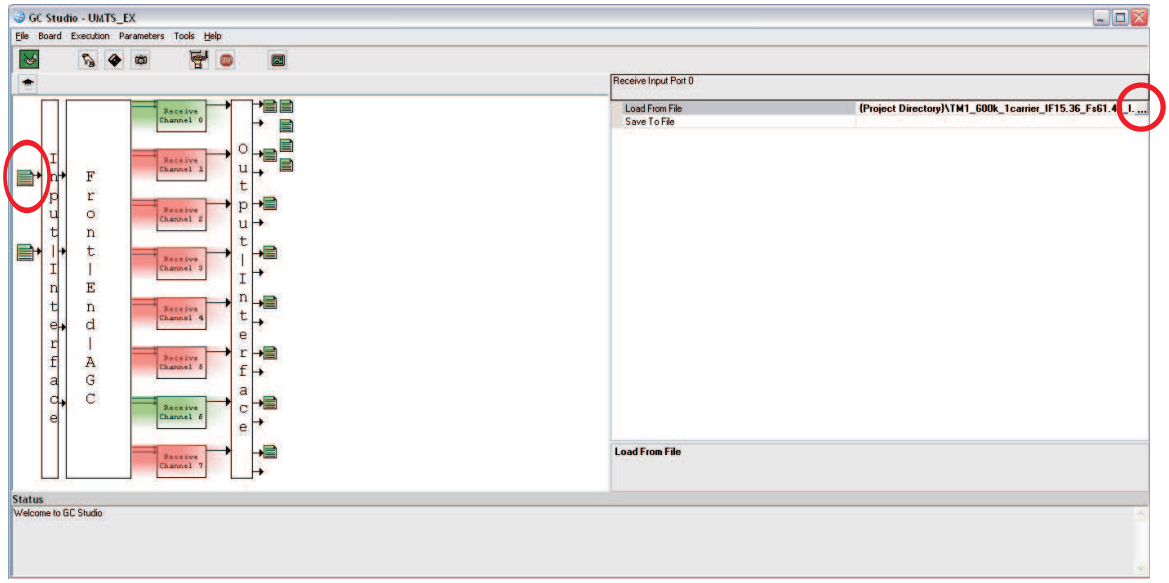
    The AFE8406 daughtercard configuration uses rx_sync_out_6 as the strobe that indicates when the serial output data starts each transfer. In the following step, the receive channel-0 configuration is copied to receive channel 6 so the strobe is present in the captured GC101 data.

24. Select AFE8406 Channel Copy from the Parameters menu to bring up the Channel Copy panel. With channel 0 selected as the source and channel 6 selected as the destination, click Copy, and then click OK. The block diagram should now show both channels 0 and 6 active (green).



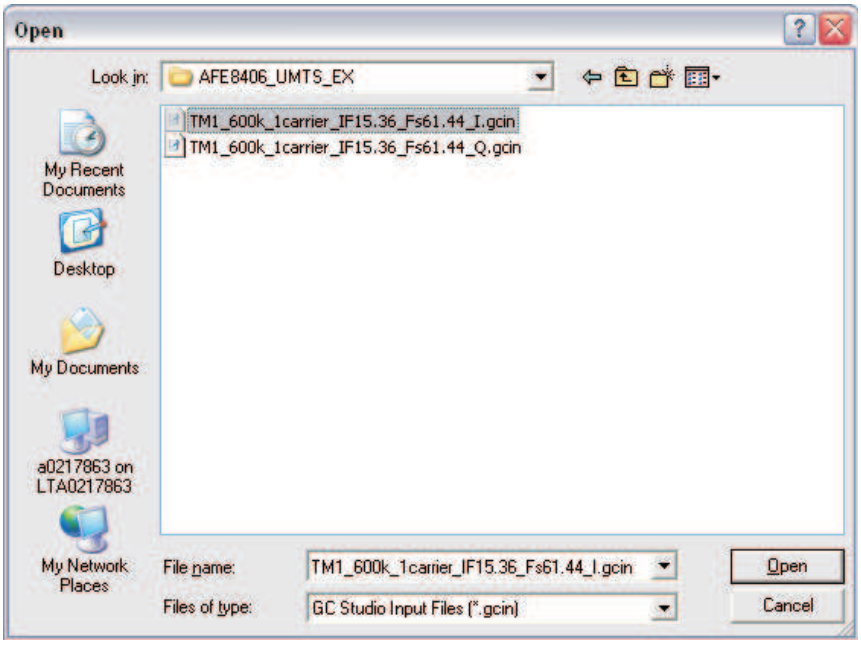
C030

25. In this example, the input data presented to the AFE8406 comes from data files. Two input file icons can be seen in the block diagram to the left of the Input Interface block. The upper file icon is connected to the AFE8406 digital rxin_c input port, and the lower icon is connected to the digital rxin_d input port. Click on the top icon to show the Receive Input Port 0 menu. Following this, click on the browse button to bring up the Open file window.



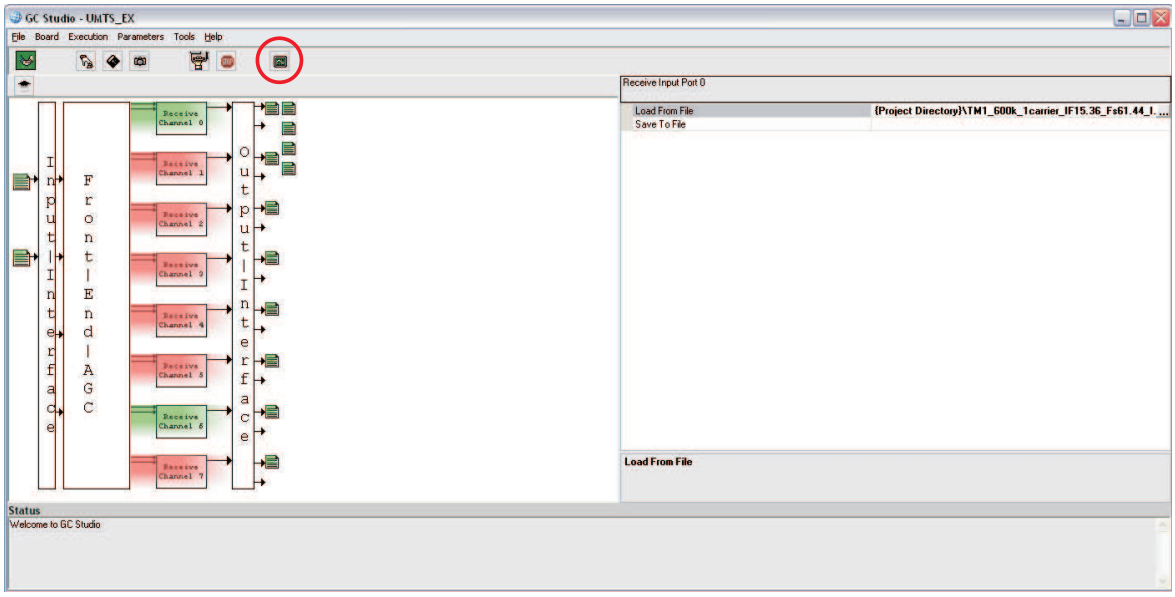
C031

26. Navigate to the AFE8406_UMTS_EX folder and select TM1_600k_1carrier_IF15.36_Fs61.44_I.gcin. Repeat for the lower input file icon, selecting in this case the TM1_600k_1carrier_IF15.36_Fs61.44_Q.gcin file.



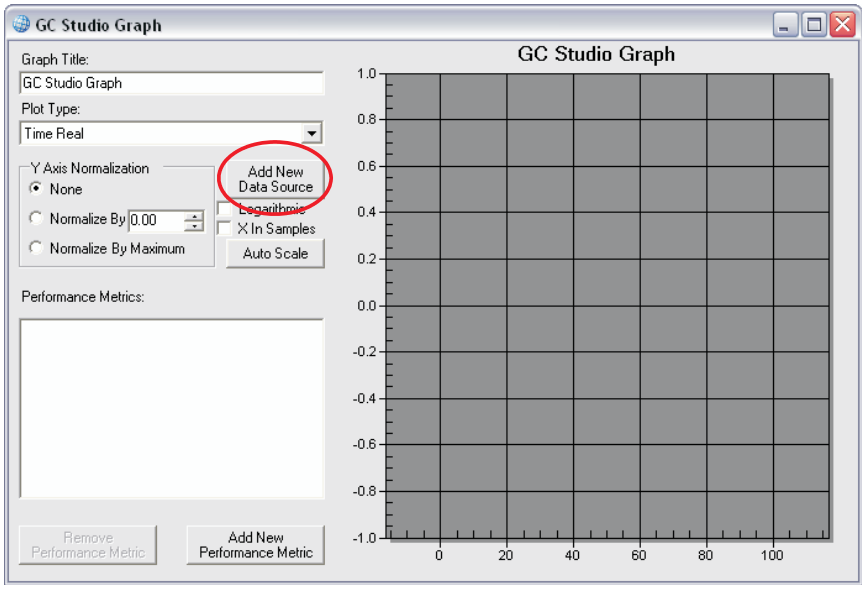
C032

27. Click on the graph button, circled in red, to open the graph panel.

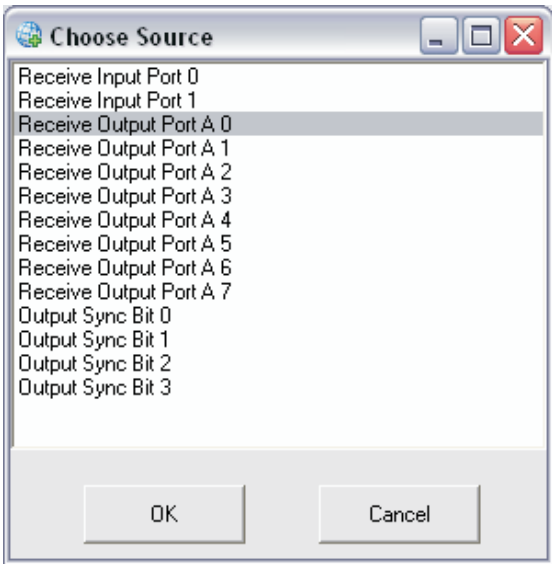


C033

28. Click the Add New Data Source button and select Receive Output Port A 0.

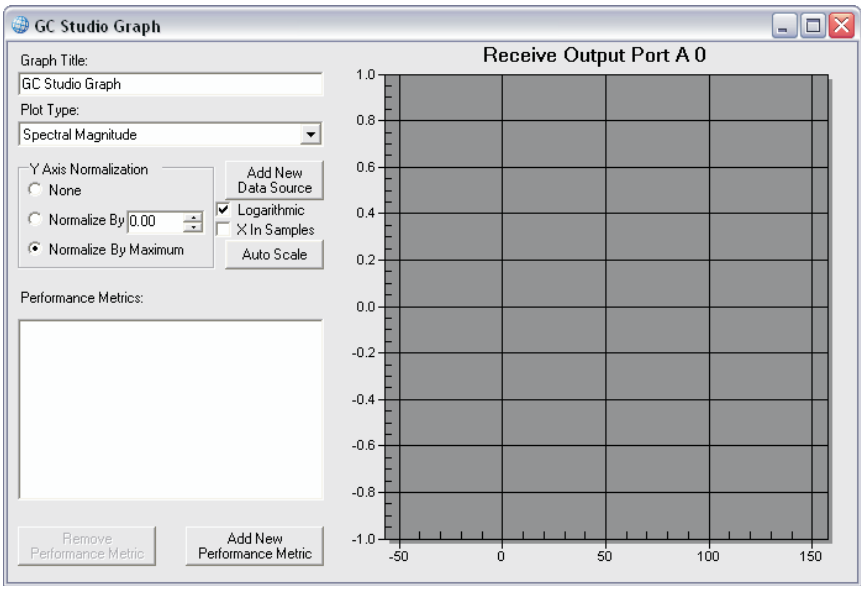


C034



C035

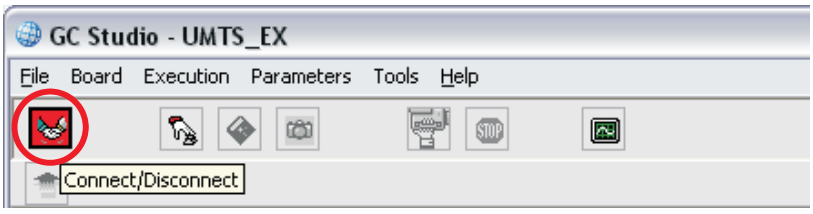
29. In the graph panel, set the Plot Type to Spectral Magnitude, check the Logarithmic check box, and select Normalize by Maximum.



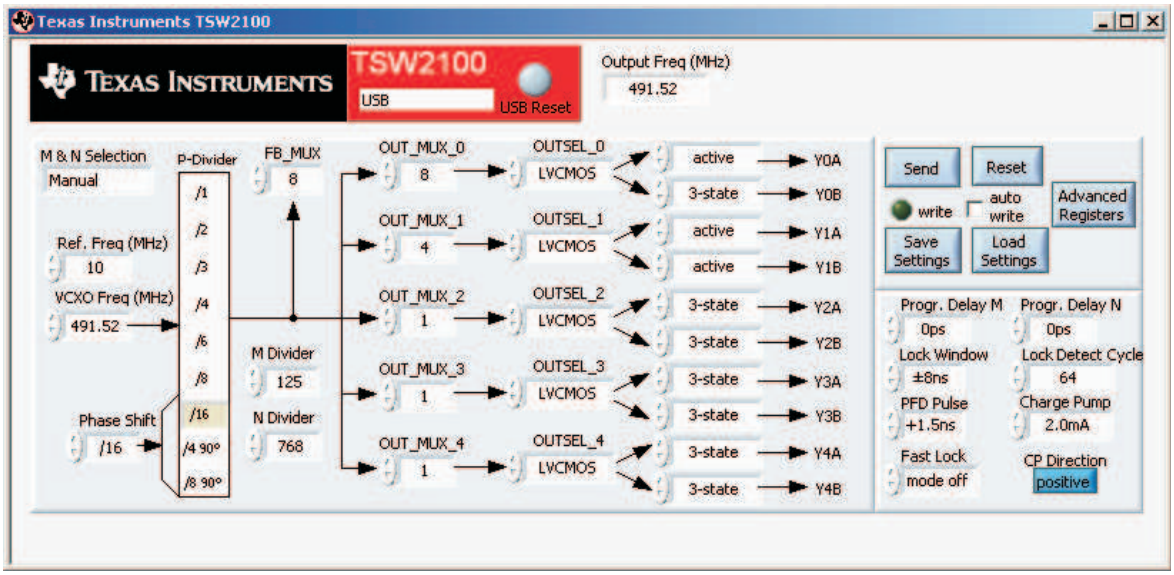
C036

30. Connect the GC101 motherboard, AFE8406 daughtercard, and TSW2100 board as described in Section 3.1.

31. Configure the TSW2100 board as shown. If sharing the parallel port for the TSW2100 board and the GC101 motherboard, release the port on GC Studio before programming the TSW2100 by toggling the connect/disconnect button.

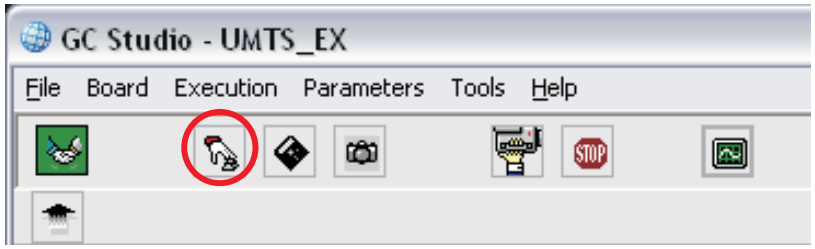


C047



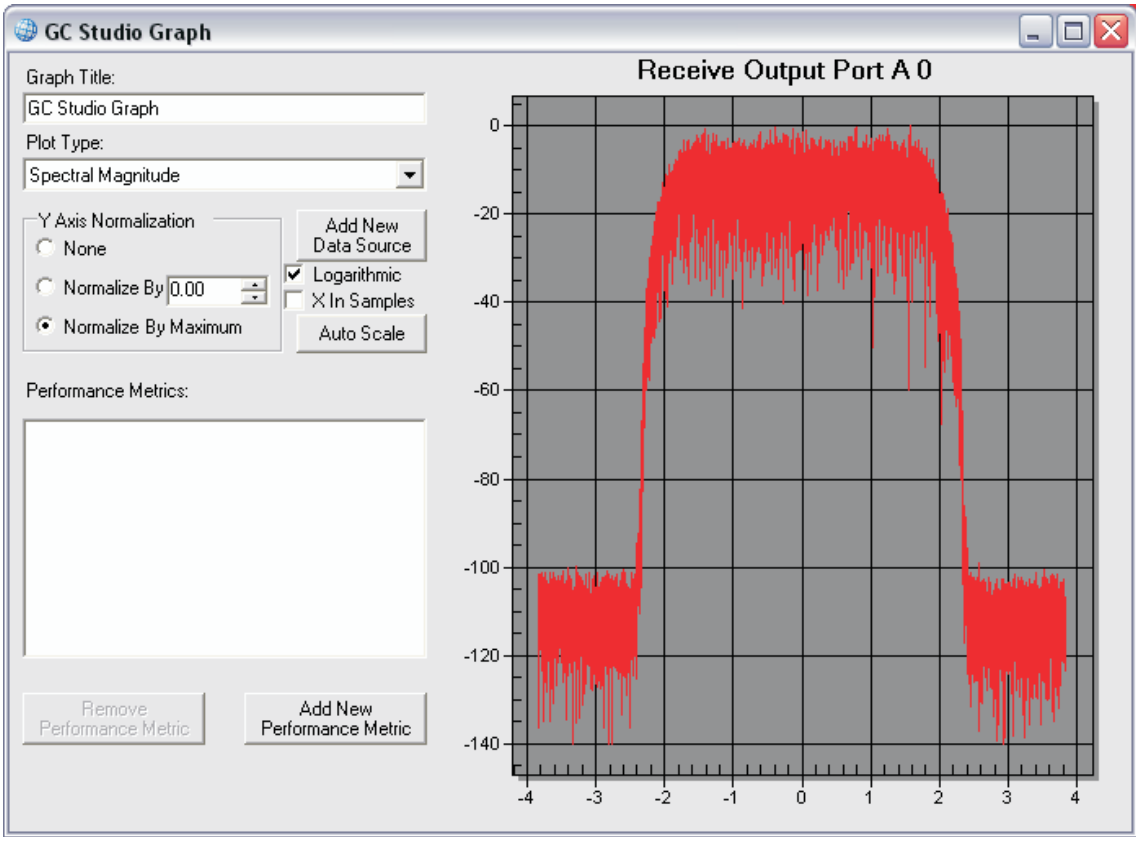
C051

32. On the GC Studio panel, toggle the connect/disconnect button and then click on the build button. The default settings in the GC Studio are set to load and capture automatically after the project is built.



C037

The graph window is automatically updated with the results.



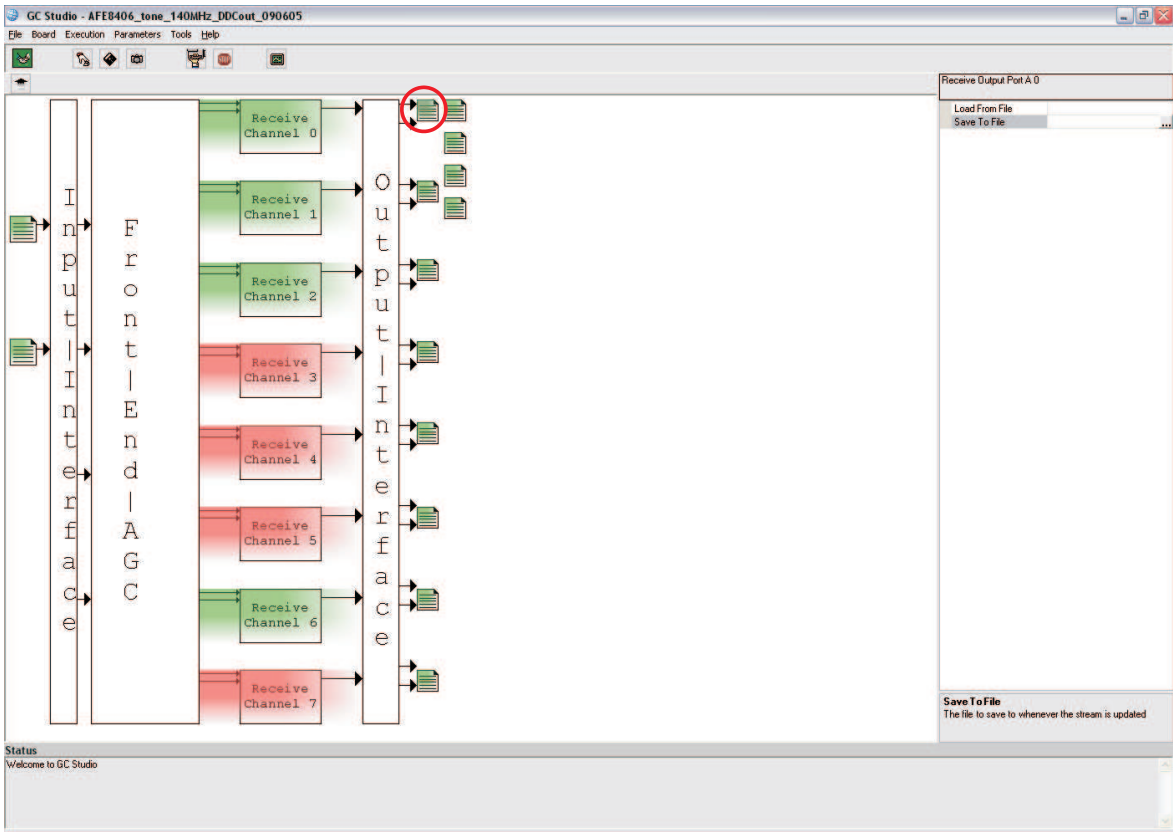
Other Options in GC Studio

GC Studio offers much flexibility in evaluating the data processed by the AFE840x. Following is a list of some of these capabilities:

4.1 Saving the Output to a File

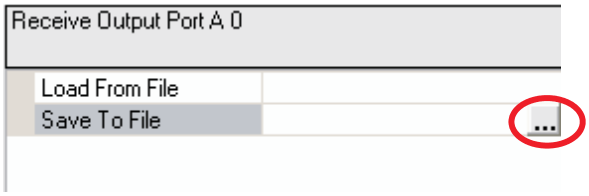
GC Studio allows one to save the data of the AFE840x to a text file for further analysis by any commercial numerical analysis software. In this example, Receive Output Port A0 is saved.

1. Double-click on the AFE840x block to go into its block diagram. Once there, click on the file corresponding to Receive Output Port A 0.



C039

2. Click on the *Save to File* box and select the file to which the data is to be saved.



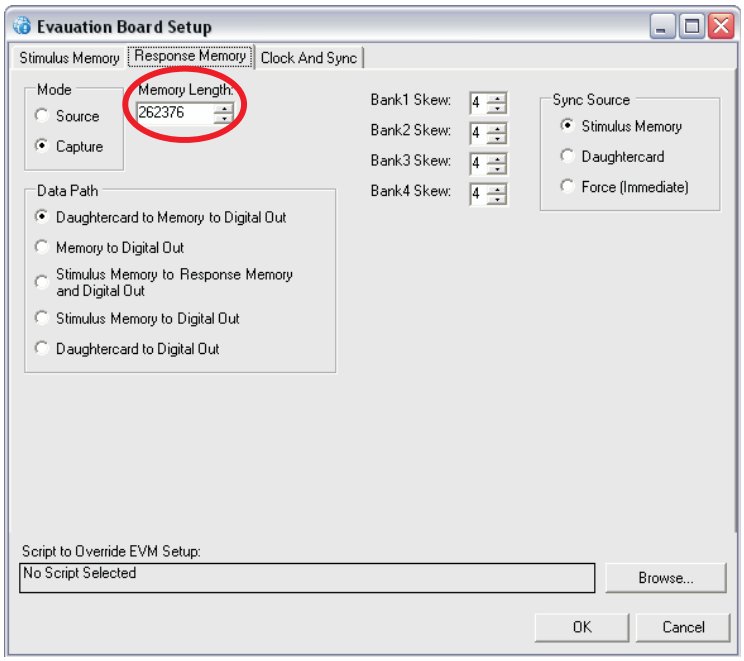
C040

3. These steps can be repeated for every signal to be captured. Every time the stream is updated, the files are also updated with the latest results. The file is saved in decimal format in two columns with the first column corresponding to the real portion of the output and the second column to the imaginary one.

4.2 Changing the Data Capture Size

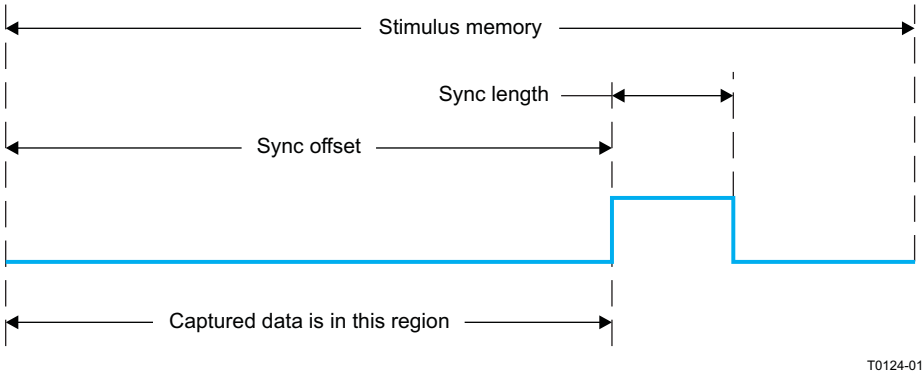
GC Studio allows you to modify the number of samples to be captured. Standard boards are delivered with a 2-megaVector (2048-kSample) memory, so ensure that this number is not exceeded.

1. Select EvalBoard Parameter Editor… from the Parameters menu. Once there, go to the Response Memory tab and enter the desired number of samples on the Memory Length box.



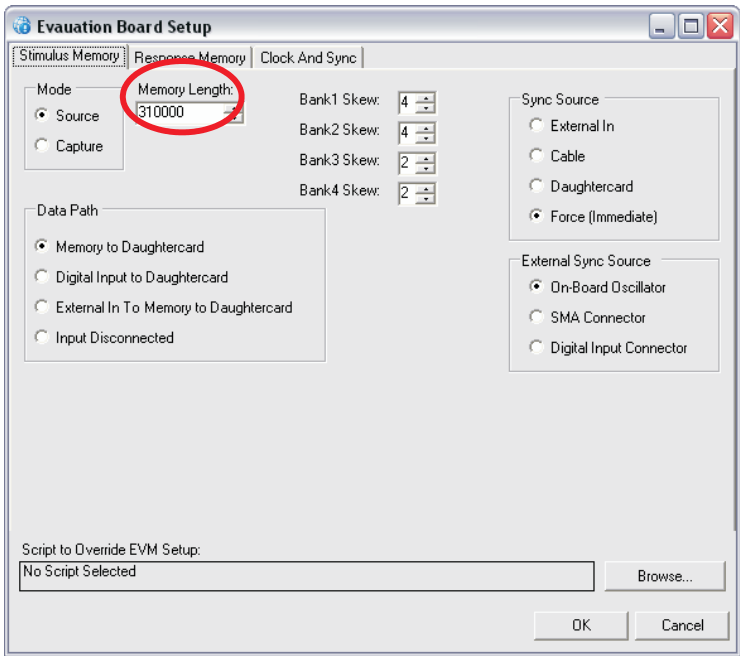
C041

2. In the current version of GC Studio, the Response Memory capture is triggered by the Stimulus Memory. Improper setting of the Stimulus Memory may result in errors in the captured data. Because of this, every time the captured data size is modified, it is necessary to corroborate that the Stimulus Memory size and the Sync Offset are set up properly.



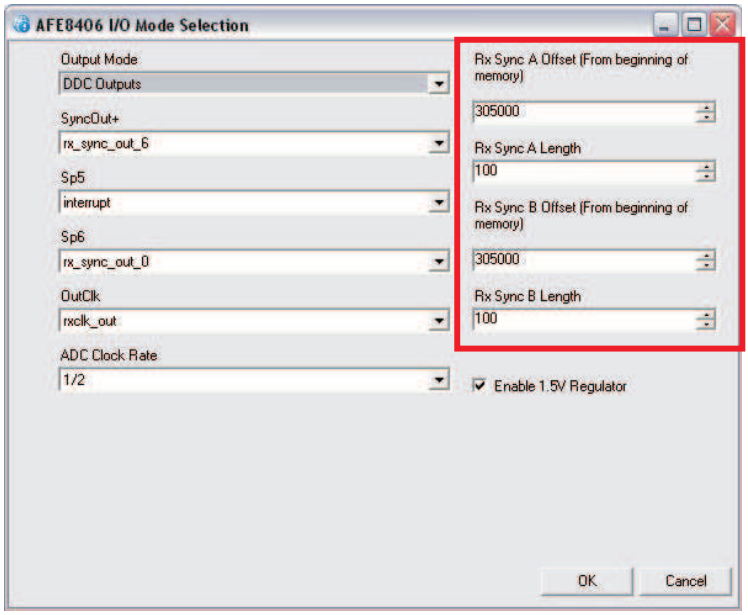
T0124-01

3. From the foregoing diagram, it is observed that the Sync Offset must be slightly bigger than the Response Memory size. Also, it is necessary to verify that the Stimulus Memory size is large enough to encompass the Sync Offset and the Sync Length. To adjust the Stimulus Memory size, select EvalBoard Parameter Editor… from the Parameters menu and go to the Stimulus Memory tab. Enter the proper number of samples in the Memory Length box.



C042

4. The last step is to modify the Sync Offset and Sync Length so that they match the selected Stimulus Memory size. To do this, select AFE840x I/O Mode Configuration from the Parameters menu. Once there, enter the appropriate Sync Offset and Sync Length values in the corresponding boxes. Sync A and Sync B should have the same values.



C043

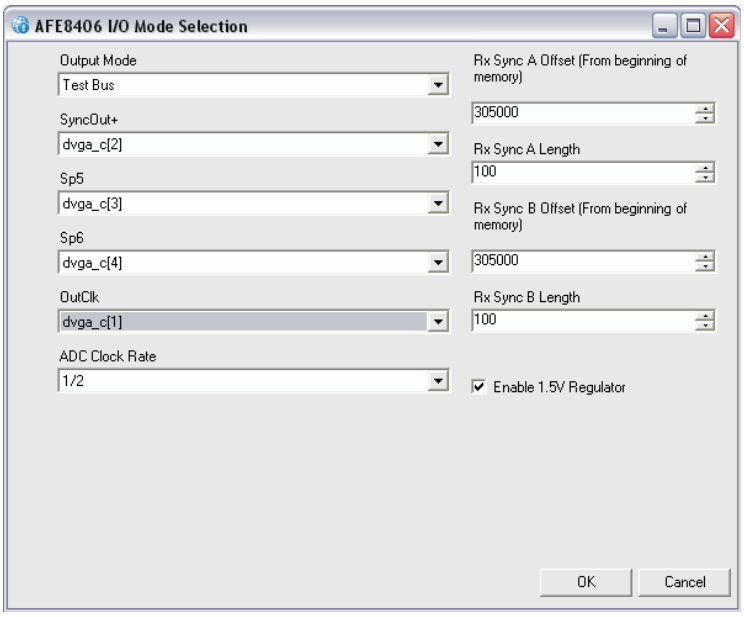
4.3 Capturing the AFE840x Test Bus Output

The AFE840x includes a test bus, allowing the user to view internal digital signals. When the test bus is enabled, the rxin_c and rxin_d (AFE8406 only) input ports become outputs and the dvga_c and dvga_d ports are multiplexed to carry test bus data, giving a 36-bit-wide output port and three additional signals. Because rxin_c and rxin_d are the test bus outputs, only the analog inputs rxin_a and rxin_b (AFE8406 only) are available in this case.

Test Bus Signal	Corresponding Signal
testbus(35:0)	rxin_d(15:0), dvga_c(3:2), rxin_c(15:0), dvga_c(5:4)
test bus clock	dvga_c(1)
test bus sync	dvga_c(0)
test bus aflag	dvga_d(5)

The GC101 evaluation platform captures a 36-bit signal into the response memory. When selecting the various test bus sources, the signals selected in the I/O Mode Selection window must be set correctly.

1. Select AFE840x I/O Mode Configuration from the Parameters menu. In this menu, set the Output Mode to Test Bus and OutClk to dvga_c(1).

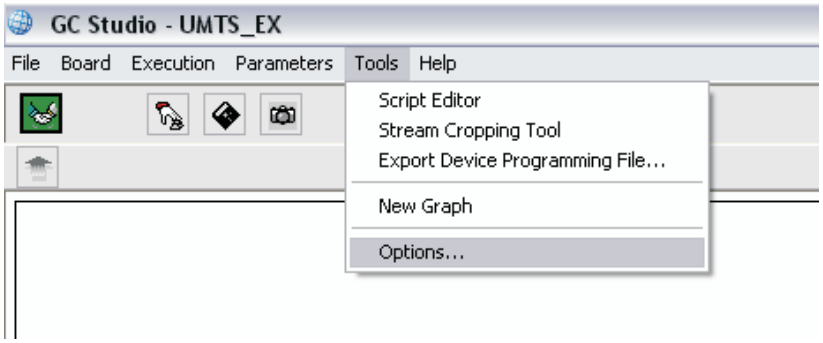


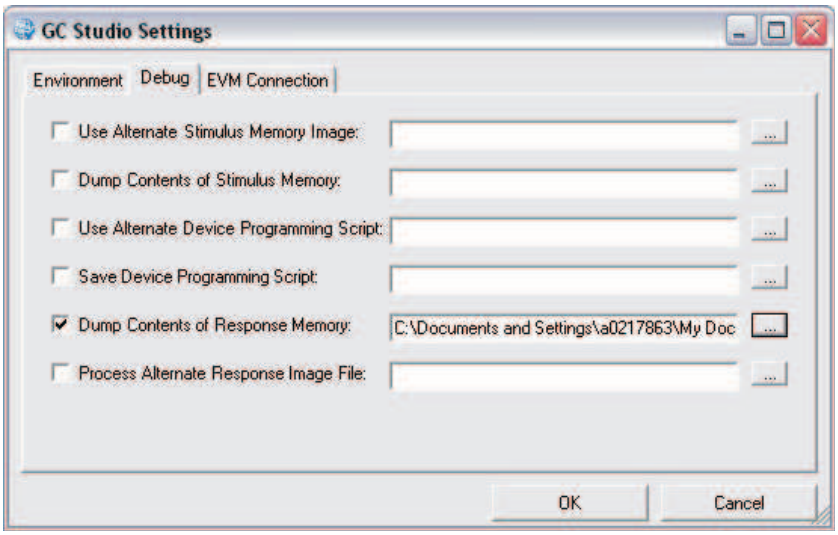
C044

2. The other signals, captured as SyncOut+, Sp5, and Sp6, should be configured as required for the specific test bus signal [Sp7 is always dvga_c(5)]. The test bus output clock is used to load the response memory, and is controlled by the tst_rate_sel.

Test Bus Signal	SyncOut+	Sp5	Sp6	OutClk	tst_rate_sel
DDC PFIR in UMTS mode	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	2*CIC decimation
DDC PFIR in CDMA mode	dvga_c(2)	dvga_c(**5**)	dvga_c(4)	dvga_c(1)	RXCLK rate
DDC CFIR in UMTS mode	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	2*CIC decimation
DDC PFIR in CDMA mode	dvga_c(2)	dvga_c(**5**)	dvga_c(4)	dvga_c(1)	RXCLK rate
DDC TADJ-A	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	RXCLK rate
DDC TADJ-B CDMA mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	RXCLK rate
DDC NCO-SINE in UMTS mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC clock rate
DDC NCO-COSINE in UMTS mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC clock rate
DDC CIC in UMTS mode	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	CIC decimation
DDC CIC in CDMA mode	dvga_c(2)	dvga_c(**5**)	dvga_c(4)	dvga_c(1)	RXCLK rate
DDC AGC in UMTS mode	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	2*CIC decimation
DDC AGC in CDMA mode	dvga_c(2)	dvga_c(**5**)	dvga_c(4)	dvga_c(1)	RXCLK rate
DDC MIXER-A	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC clock rate
DDC MIXER-B CDMA mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC clock rate
DDC DDCMUX-A	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC clock rate
DDC DDCMUX-B CDMA mode only	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC clock rate
RXIN_A and RXINB FIFO	dvga_c(2)	dvga_c(3)	dvga_c(4)	dvga_c(1)	ADC clock rate

3. The raw response memory can be captured in a text format by selecting Options… from the Tools menu and going to the Debug tab.





C045

The format of the file is hexadecimal, with the 32-bit response memory as the first 8 characters, a space, and then a single character for the other four special bits (Sp7, Sp6, Sp5, SyncOut+), shown as follows:

…
0000F0A0 0
0000F0A0 0
28D80000 0
28D80000 0
0000F2C6 0
0000F2C6 0
26750000 0
26750000 0
0000F580 0
0000F580 0
…

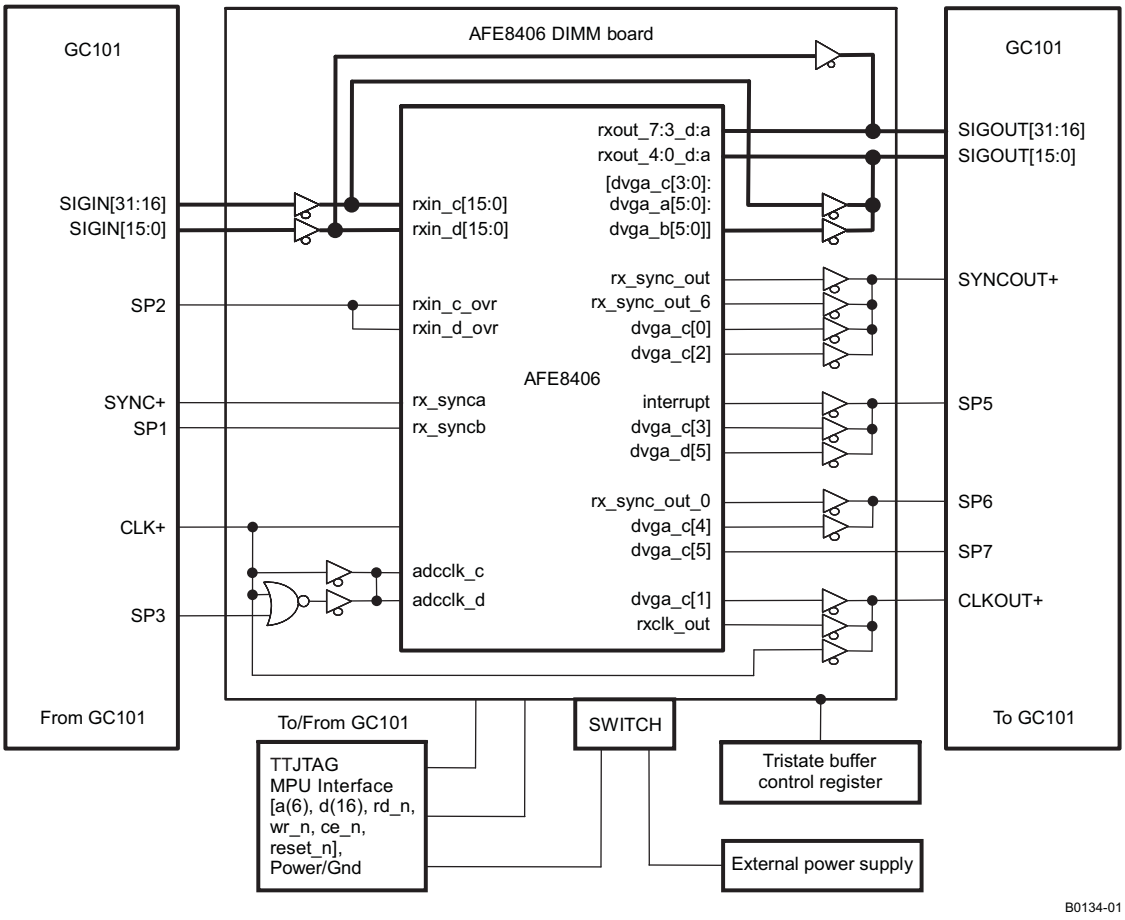
4. To capture the ADC samples, set tst_select to A-B_FIFO_OUTs, and set tst_rate_sel to generate a clock matching the ADC clock rate.

C046

5. Subsequently, the ADC samples can be directed to a graph or to an output file using the steps described in Section 4.1.

AFE840x Daughtercard Description

AFE840x DIMM–GC101 Interface Block Diagram



5.1 AFE840x Daughtercard Pin Description

The AFE840x daughtercard has a PC-133 form-factor that uses the 168-pin daughtercard memory connector. The 168-pin interface signals are divided into groups as listed in Table 5-1 thhrough Table 5-6.

Table 5-1. Memory Input Bus—36 Data Inputs Used to Stimulate the AFE840x Inputs

Signal	Alias	Description
SIGIN(35)	SP3	Clock gating signal for adcclk_a and adcclk_b
SIGIN(34)	SP2	rxin_c_ovr and rxin_d_ovr input signals
SIGIN(33)	SP1	rx_syncb input signal
SIGIN(32)	SYNC+	rx_synca input signal
SIGIN(31:16)		rxin_c(15:0) input data
SIGIN(15:0)		rxin_d(15:0) input data

Table 5-2. Memory Output Bus—36 Data Outputs From Selected AFE840x Outputs Captured by the GC101

Signal	Alias	Description
SIGOUT(35)	SP7	dvga_c(5)
SIGOUT(34)	SP6	dvga_c(4) or rx_sync_out_0
SIGOUT(33)	SP5	dvga_c(3), dvga_d(5) or interrupt
SIGOUT(32)	SYNCOUT+	rx_sync_out, rx_sync_out_6, dvga_c(0) or dvga_c(2)
SIGOUT(31:16)		rxout_7:4_d:a baseband DDC data or rxin_d(15:0) testbus output
SIGOUT(15:0)		rxout_3:0_d:a baseband DDC data or rxin_c(15:0) testbus output

Table 5-3. Clock

Signal	Description
CLK+	RXCLK clock for AFE840x; can be used as a full-rate or gated clock source when combined with the gating signal SP3 for the adcclk_a and adcclk_b (AFE8406 only) inputs.
CLKOUT	Clock signal from the daughtercard to the GC101; RXCLK, rxclk_out from the GC5018 or dvga_c(1)

Table 5-4. Microprocessor Control Bus—Bus to Program the Internal Registers

Signal	Description
d(15:0)	Control data I//O bus, active-high bidirectional I/O pins. This is the 16-bit control data I/O bus. Control registers are written to or read from through these pins. The chip drives these pins when $\overline{CE}$ is low, $\overline{RD}$ is low, and $\overline{WR}$ is high.
A(10:0)	Control address bus, active-high inputs. These pins are used to address the control registers within the chip. Each of the control register within the chip is assigned a unique address. A control retister can be written to or read from by having the page register set to the appropriate page and then setting A(10:0) to the register address.
$\overline{CE}$, $\overline{RD}$, $\overline{WR}$, and $\overline{RST}$	ce_n, rd_n, wr_n and rst_n on the AFE840x

Table 5-5. JTAG

Signal	Description
JTAG	5-pin JTAG test port for AFE840x
$\overline{TRST}$, TCK, TMS, TDI, TDO	trst_n, tck, tms, tdi, and tdo on the AFE840x

Table 5-6. Power and Ground

Signal	Description
VDUT1	3.3-V power from GC101 EVM to the daughtercard
GND	Return path for the daughtercard

See the GC101 EVM User's Guide (SLWU018) for the 168-pin connector table. Detailed Schematics and Bill of Materials (BOM) for the AFE840x daughtercard can be found on the provide CD .

5.2 AFE840x Daughtercard Jumpers

The following table describes the various jumpers on the AFE840x daughtercard card:

Jumper (Rev E and older)	Description
W2 (J7)	Pin_configure signal. Factory test only. Connect to VDD, pins 2-3 (default).
W3 (J8)	Enables ADC A outputs. Jumper installed between pins 1-2 (default). Disables ADC A outputs when jumper is installed between pins 2-3.
W4 (J9)	Enables ADC B outputs (AFE8406 only) when jumper is installed between pins 1-2 (default). Disables ADC outputs when jumper is installed between pins 2-3.
W12 (J11)	Clock doubler power down for the CDC5801. Jumper installed between pins 1-2 for 3.3 V, enabled (default). Position 2-3 for 0 V, powered down.
W13 (J12)	1× or 2× clock select for the CDC5801. Jumper installed between 2-3 for 2× output clock (default). Position 1-2 for 2× output clock.
W7 (W14)	3.3-V fuse power for ADC. Jumper installed between pins 1-2 for 3.3 V, normal operation (default). Position 2-3 for 0 V – DO NOT USE THIS POSITION.
W10 (W15)	3.3-V fuse power for DDC. Jumper installed between pins 1-2 for 3.3 V, normal operation (default). Position 2-3 for 0 V – DO NOT USE THIS POSITION.
W9 (J17)	SDI - Set to AVDD.Factory use only, jumper removed (default). SEN - ADC internal reference when set to GND. Jumper installed between pins 3-4 (default). Ext reference with jumper removed. SCLK - AVDD for AFE8405, jumper removed 9default). Power down for AFE8406, jumper installed between Pins 5-6 (default).
N/A (W13)	External DVDD power supply. Jumper installed betwwen pins 1-2 for internal 1.5 V to DVDD (default). Position 2-3 for external 1.5 V through J24.
W8 (W25)	External AVDD power supply. Jumper installed between pins 1-2 for internal 3.3 V to AVDD (default). Position 2-3 for external 3.3 V through J29.
W11 (W26)	External VDDS power supply. Jumper installed between pins 1-2 for internal 3.3 V to VDDS (default). Position 2-3 for external 3.3 V through J30.
W5 (W27)	External DRVDD power supply. Jumper installed between pins 1-2 for internal 3.3 V to DRVDD(default). Position 2-3 for external 3.3 V through J28.
W6 (J23)	1.5-V regulator software control using c10 register bit – DO NOT INSTALL.

5.3 AFE840x Daughtercard Power Supplies

The AFE840x I/O and core power supplies are 3.3 V and 1.5 V, respectively. The default configuration of the AFE840x daughtercard enables the GC101 motherboard to supply 3.3 V to the daughtercard, which includes a 1.5-V regulator. Alternatively, by modifying jumpers W13, W25, W26 and W27, on Rev E or older boards, and W5, W8, and W11, on Rev F or newer boards, external power supplies can be used to provide these voltages to the daughtercard.

5.4 AFE840x Daughtercard Clock Configurations

The AFE840x daughtercard card allows for the following clock configurations:

1. Default configuration (to be used with TSW2100): AFE840x daughtercard RX clock SMA input
   - Input RX clock rate at J5 (CLKM)
   - Install 0-Ω resistors in
     - R40
     - R72
     - R58
   - Remove resistors in
     - R36
     - R43
     - R52
     - R73
   - For CDCF5801 at 1, install
     - J12 jumper between pins 2 and 3

- For CDCF5801 at 2, install
  - J12 jumper between pins 1 and 2
- Clock path:
  J5 → R40 → R72 → C137 → U22 (pin2) → U22 (pin20) → R58 → AFE8406 (ball r22)

2. Configuration for AFE840x daughtercard RX clock from GC101 (through CDCF5801)
   - Install 0-Ω resistors in
     - R46
     - R70
     - R73
     - R58
   - Remove resistors in
     - R36
     - R43
     - R52
     - R72
   - For CDCF5801 at 1, install
     - J12 jumper between pins 2 and 3
   - For CDCF5801 at 2, install
     - J12 jumper between pins 1 and 2
   - Clock path:
     J16A (pin 34) → R46 → C148 → U2 (pin1) → U2 (pin2) → R70 →R73 → C137 → U22 (pin2) → U22 (pin20) → R58 → AFE840x (ball r22)
3. Configuration for AFE840x daughtercard RX clock from GC101 (bypass CDCF5801)
   - Install 0-Ω resistors in
     - R46
     - R36
     - R73
   - Remove resistors in
     - R43
     - R52
     - R73
     - R72
     - R58
   - Clock path:
     J16A (pin 34) → R46 → C148 → U2 (pin1) → U2 (pin2) → R36 → AFE840x (ball r22)
4. Configuration for AFE8406 daughtercard RX clock from ADC clock (GC101 separate)
   - Install 0-Ω resistors in
     - R52
     - R58
   - Remove resistors in
     - R36
     - R43
     - R52
     - R72
     - R73
   - For CDCF5801 at 1, install
     - J12 jumper between pins 2 and 3
   - For CDCF5801 at 2, install
     - J12 jumper between pins 1 and 2
   - Clock path:
     J6 (CLKP) → R52 → C137 → U22 (pin2) → U22 (pin20) → R58 → AFE840x (ball r22)

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It is important to operate this EVM within the AVDD voltage range of –0.3 V to 3.8 V and the DVDD voltage range of –0.3 V to 5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 25°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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