Texas Instruments

ADS7870/ADS7871EVM

User's Guide

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Data Acquisiton

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 3.3 to 5 VDC and the output voltage range of 0−5 VDC.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 30°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This users guide describes the characteristics, operation, and use of the ADS7870/71 EVM – an evaluation module for use with the 12/14-bit multi-channel data acquisition system ADS7870 and ADS7871 devices. A complete circuit description as well as schematic diagram and bill of materials are included.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—EVM Overview
- Chapter 2—Analog and Digital Interface
- Chapter 3—Power Supplies
- Chapter 4—EVM Operation
- Chapter 5—EVM Bill of Materials and Schematic

Related Documentation From Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this booklet by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Data Sheets:	**Literature Number:**
ADS7870	SBAS124
ADS7871	SLAS370
5−6K Interface Board	SLAU104
DAP Signal Conditioning Boards	SLAU105
Third Party Tools:	**Vendor's Website:**
HPA449 Development Board	www.SoftBaugh.com

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

Chapter 1

EVM Overview

The following section gives a general overview of the ADS7870/ ADS7871EVM.

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1.1 Features

- ❑ Full-Featured Evaluation Board for the ADS7870 and ADS7871, 12- and 14-bit Data Acquisition Systems
- ❑ 8 Single-Ended/4 Differential (or combination of both) Analog Inputs With PGA
- ❑ Built-In Reference With High-Current Buffered Output
- ❑ Synchronous Serial Interface and GPIO Functions

1.2 Introduction

The ADS7870 and ADS7871 are complete data acquisition devices composed of an input analog multiplexer (MUX), a programmable gain amplifier (PGA) and an analog-to-digital converter (A/D). Four lines of digital input/output (I/O) are also provided. Additional circuitry provides support functions including conversion clock, voltage reference, and serial interface for control and data retrieval. Control and configuration of the ADS7870/ADS7871 is accomplished by command bytes written to internal registers through the serial port.

The device Command Register includes MUX channel selection, PGA gain, A/D start conversion commands, and I/O line control. The Configuration Register controls include internal voltage reference settings and oscillator speed control.

Chapter 2

Analog and Digital Interface

This chapter describes the analog and digital interface connections to the ADS7870/71 EVM.

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2.1 Analog Interface

For maximum flexibility, the ADS7870/71 EVM is designed for easy interfacing to multiple analog sources. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J1. This header/socket provides access to the analog input pins of the ADC. Consult Samtec at www.samtec.com or call 1−800−SAMTEC−9 for a variety of mating connector options.

Pin Number	Signal	Description
J1.2	LN0	MUX Input Line 0
J1.4	LN1	MUX Input Line 1
J1.6	LN2	MUX Input Line 2
J1.8	LN3	MUX Input Line 3
J1.10	LN4	MUX Input Line 4
J1.12	LN5	MUX Input Line 5
J1.14	LN6	MUX Input Line 6
J1.16	LN7	MUX Input Line 7
J1.18	Unused	Pin is unused and should be left open for use with future amplifier and sensor input modules.
J1.20	REFIN	External Reference Source Input (2.5 V NOM, 2.525 MAX) Selected when pins 2 and 3 of W1 are shunted
J1.1–13, J1.17 −J1.19 (odd−number pins)	AGND	Analog ground connections
J1.15	VCOM Out	BufOut voltage available on this pin by shunting W4

2.2 Digital Interface

The ADS7870/71 EVM is designed for easy interface to multiple control platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the THS1218. Consult Samtec at www.samtec.com or 1−800−SAMTEC−9 for a variety of mating connector options.

Pin Number	Signal	I/O	Description
J2.1	$\overline{CS}$	I	Chip select—Enables data transfer and device configuration
J2.3	SCLK	I	Serial clock input to the ADC
J2.5	OSC_ENA	I	Enable internal oscillator
J2.7	CONVERT	I	Direct mode conversion start input— Derived from frame sync of DSP host or GPIO from uC
J2.9	$\overline{RST}$	I	Hardware reset
J2.11	SDI	I	Serial data in (Device DIN)
J2.13	SDO	O	Serial data output from DOUT pin of device
J2.15	$\overline{INT}$	O	Interrupt output—Provides an interrupt source to host processor via device BUSY pin
J2.17	TOUT	O	Timer output from host controller—Used in conjunction with W5 as conversion clock source.
J2.19	SPARE		Not Used

2.3 GPIO Connections

The following table shows the pin-out of J4. This dual row, four-position header provides access to the GPIO outputs of the ADS7870/7871. R14 provides pull downs (to DGND).

Pin Number	Signal	I/O	Description
J4.1	I/O_3	I	General-Purpose Output 3
J4.3	I/O_2	I	General-Purpose Output 3
J4.5	I/O_1	I	General-Purpose Output 1
J4.7	I/O_0	I	General-Purpose Output 0
J4.2–J4.8 (even)	DGND		Digital ground connections

Chapter 3

Power Supplies

The ADS7870/71 EVM board requires 2.7 to 5.5 VDC to power the ADC. While filters are provided for all power supply inputs, optimal performance of the EVM requires a clean, well-regulated power source. Positive 5-V and 3.3-V power is applied to J3 located on the bottom side of the printed circuit board when used in combination with the 5−6K interface or HPA449 development boards. Jumper W3 allows the user to choose 3.3 V operation (default) when pins 1−2 are shunted. Shunting pins 2−3 allows 5 V operation.

If a variable digital supply voltage is desired, completely remove the shunt jumper from W3. Apply a 100 mA current limited dc voltage of not more than 5.5 V to the test point TP5, referenced to GND (TP3).

3.1 Reference Voltage

The ADS7870/71 can be configured to use device internal reference or an external reference source through jumper W1 (see schematic for details). To use an external reference, shunt W1 pins 2−3. The external reference is then supplied through J1 pin 20. The EVM is factory configured for use with the internal reference (W1 pins 1−2 shunted).

Chapter 4

EVM Operation

Apply power to the EVM. For use in combination with one of the modular EVM interface boards, this is accomplished by simply plugging the ADS7870/71 into one of the serial positions as shown in interface board schematics/ documents. For stand alone use, apply power to TP5 (VDD) referenced to TP3 (GND).

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4.1 Analog Input

The analog input source is applied directly to J1 (top or bottom side) or through an optional amplifier and signal conditioning modules. The analog input level should not exceed 5.0 Vp-p (centered at 2.5 V) when configured for differential mode operation. The analog input range is from GND to +VREF (0 – 2.5 VDC) when inputs are configured as single-ended operation.

Up to eight single-ended inputs can be applied to connector J1, pins 2−16 (even-numbered pins). A maximum of four differential inputs may be applied to J1, using pins 2−4, 6−8, 10−12 and 14−16 as differential pair inputs. Single ended and differential modes, as well as differential polarity, can be selected via the ADC gain/MUX register.

4.2 Digital I/O

The digital control signals can be applied directly to J2 (top or bottom side). The ADS7870/71 EVM can also be connected directly to a DSP or microcontroller interface board such as the 5−6K interface board or HPA449 development board. Consult the ADS7870 and ADS7871 product folders on the TI web site for a complete list of DAP interface cards and optional analog interface modules.

4.3 Internal/External Conversion Clock

Jumper W5 is provided as a means to isolate the internal oscillator from J2; the digital control connector. The ADS7870/71 is factory configured to use an external oscillator; which means W5 is shunted by default. The OSC_ENA pin is pulled low by resistor R16, defining CCLK as an input pin and disabling the internal oscillator. J2.17 can then be used as an external CCLK source, provided the frequency is held at 2 MHz or less.

To use the internal oscillator, the CCLK pin must be defined as an output and W5 should remain open to avoid potential interference with the digital control signals on J2. The OSC_ENA pin must then be pulled high, which means a logic HIGH must be applied to J2 pin 5.

4.4 Rising/Falling Edge

Jumper W6 controls the logic level applied to the RISE/FALL pin found on the ADS7870 or ADS7871 device installed on the evaluation board. When W6 is open, the RISE/FALL pin is pulled high through R12. This sets the active SCLK edge to rising.

The factory default condition W6 shunted, configuring the installed device to respond to the falling edge of SCLK when reading/writing data to/from the DIN/DOUT pins.

4.5 Hardware Reset

The $\overline{\text{RESET}}$ pin of the device installed on the ADS7870/71 EVM is connected to J2.9 and pulled to VDD via resistor R15. To perform a hardware reset, thereby returning all internal registers to their default power-up states, simply toggle J2.9 low or apply a temporary short between J2.9 and J2.10.

4.6 Software Example

A software example using the MSP430F449 and the HPA449 development board is available for download from the ADS7870/71 product folder on the TI web site.

4.7 Jumper Defaults

The following table describes the factory jumper defaults as well as the functions the jumpers control.

Jumper	Default Position	Function
W1	1−2	Selects internal/external reference. Default is internal.
W2	closed	Connects external CONVERT signal through J2.7.
W3	1−2	Selects 3.3 V or 5 V to VDD when using an appropriate interface board. Default is 3.3V.
W4	open	Connects BUFOUT voltage to J1.15 when shunted
W5	closed	Allows external CCLK to be applied to CCLK pin through J2.17
W6	closed	Controls logic level applied to RISE/FALL pin. Default is LOW, configuring the device to respond to the falling SCLK edge (data changes on falling).

Chapter 5

EVM Bill of Materials and Schematic

This chapter contains the bill of materials table and the schematic.

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5.1 EVM Bill of Material

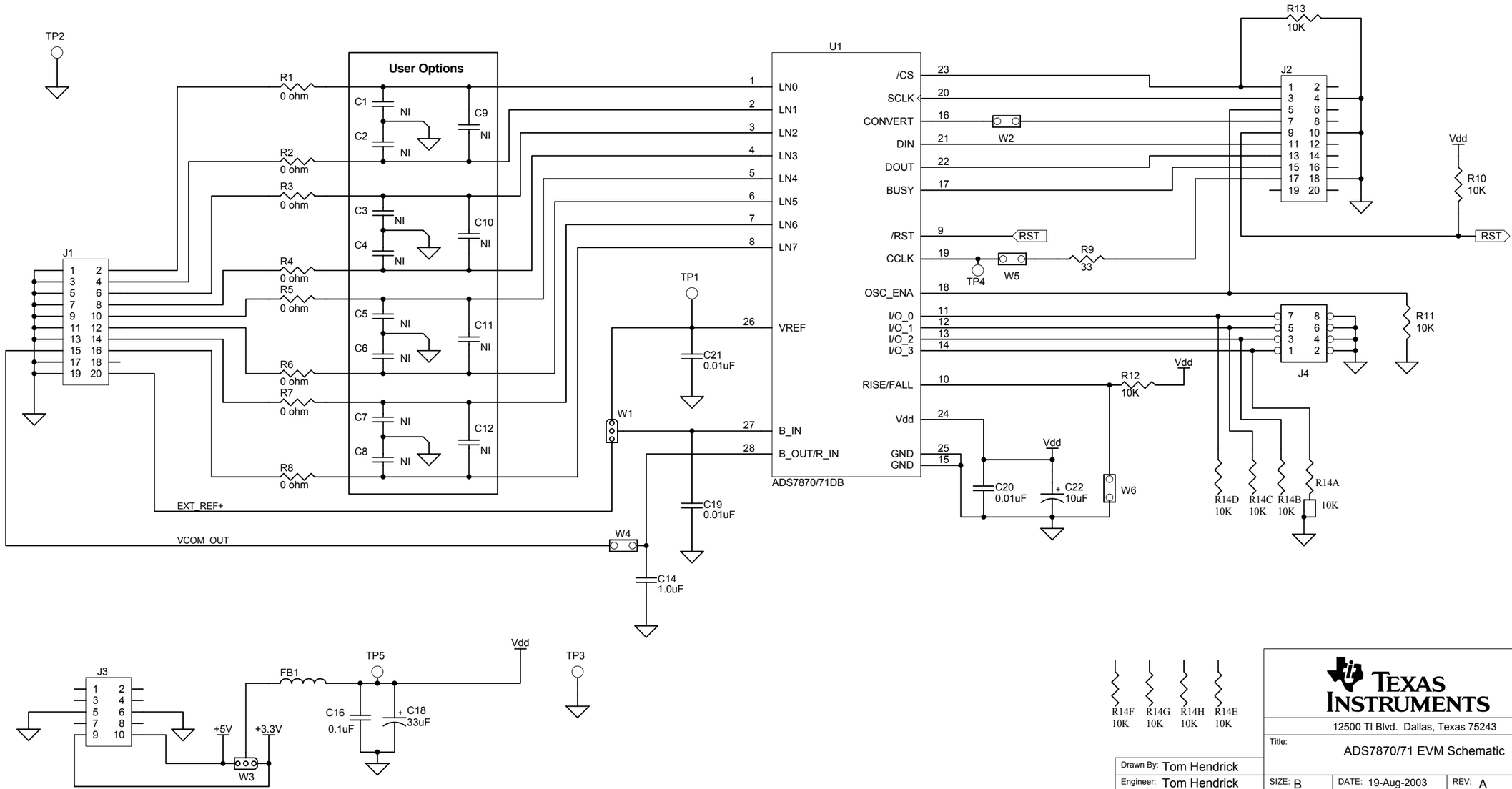
The following table contains a complete bill of materials for the ADS7870/8361 EVM. The schematic diagram is also provided for reference.

Designators	Description	Manufacturer	Mfg. Part Number
C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12	Not installed		
C14	1.0 μF, 0805, ceramic	Panasonic	ECJ−2YB1H105K
C16	0.1 μF, 0805, ceramic, X7R, 50 V, 10%	Panasonic	ECJ−2YB1H104K
C18	33 μF, 16 V, aluminum, Size C	Cornell Dubilier	AVS336M16C12T
C19 C20 C21	1 nF, 0805, ceramic, NPO, 50 V, 5%	PhyComp	0805CG102J9B200
C22	10 μF tantalum	Kemet	T491A106K010AS
FB1	SMT, EMI beads, Z=47 Ω at 100 MHz	Fair−Rite	2743019447
J1 J2 (top side)	10 Pin, dual row, SMT header (20 positive)	Samtec	TSM−110−01−T−DV−P
J1B J2B (bottom side)	10 Pin, dual row, SMT socket (20 positive)	Samtec	SSW−110−22−F−D−VS−K
J3 (bottom side)	5 Pin, dual row, SMT socket (10 positive)	Samtec	SSW−105−22−F−D−VS−K
J4	4 Pin, dual row, TH header (8 positive)	Samtec	TSW−104−07−L−D
R1 R2 R3 R4 R5 R6 R7 R8	0 Ω, 0805, 0.1 W resistor	Yageo America	9C08052A0R00JLHFT
R9	33 Ω, 0805, 0.1 W resistor	Yageo America	9C08052A33R0JLHFT
R10 R11 R12 R13	10 kΩ, 0805, 0.1 W resistor	Yageo America	9C08052A1002JLHFT
R14	10 kΩ, 8 element bussed resistor	CTS Corp.	745C101103JTR
TP1 TP4 TP5	Red test point loop	Keystone	5000
TP2 TP3	Black test point loop	Keystone	5001
U1	ADS7870 or ADS7871	TI	ADS7871E
W1 W3	3 Pin header	Samtec	TSW−103−07−L−S
W2 W4 W5 W6	2 Pin header	Samtec	TSW−103−07−L−S

5.2 EVM Schematic

The schematic diagram (PDF attachment) follows this page.

Revision History		
REV	ECN Number	Approved



TEXAS INSTRUMENTS

12500 TI Blvd. Dallas, Texas 75243

Title: ADS7870/71 EVM Schematic

Drawn By: Tom Hendrick			
Engineer: Tom Hendrick	SIZE: B	DATE: 19-Aug-2003	REV: A
FILE: EDGE #6453234			SHEET: 1 OF: 1