ADS41xx 14-/12-Bit, 65-/125-MSPS, Ultra Low-Power ADC

1 Features

- Ultralow Power with 1.8-V Single Supply:
  - 103-mW Total Power at 65MSPS
  - 153-mW Total Power at 125 MSPS
- High Dynamic Performance:
  - SNR: 72.2 dBFS at 170 MHz
  - SFDR: 81 dBc at 170 MHz
- Dynamic Power Scaling with Sample Rate
- Output Interface:
  - Double Data Rate (DDR) LVDS with Programmable Swing and Strength
    - Standard Swing: 350 mV
    - Low Swing: 200 mV
    - Default Strength: 100-Ω Termination
    - 2x Strength: 50-Ω Termination
  - 1.8-V Parallel CMOS Interface Also Supported
- Programmable Gain up to 6 dB for SNR/SFDR Trade-Off
- DC Offset Correction
- Supports Low Input Clock Amplitude Down to 200 mV_{PP}

2 Applications

- Wireless Communications Infrastructure
- Software-Defined Radio
- Power Amplifier Linearization

3 Description

The ADS412x and ADS414x are lower-sampling speed variants in the ADS41xx family of analog-to-digital converters (ADCs). These devices use innovative design techniques to achieve high dynamic performance, while consuming extremely low power at 1.8-V supply. The devices are well-suited for multi-carrier, wide bandwidth communications applications.

The ADS412x/4x have fine gain options that can be used to improve SFDR performance at lower full-scale input ranges, especially at high input frequencies. They include a dc offset correction loop that can be used to cancel the ADC offset. At lower sampling rates, the ADC automatically operates at scaled down power with no loss in performance.

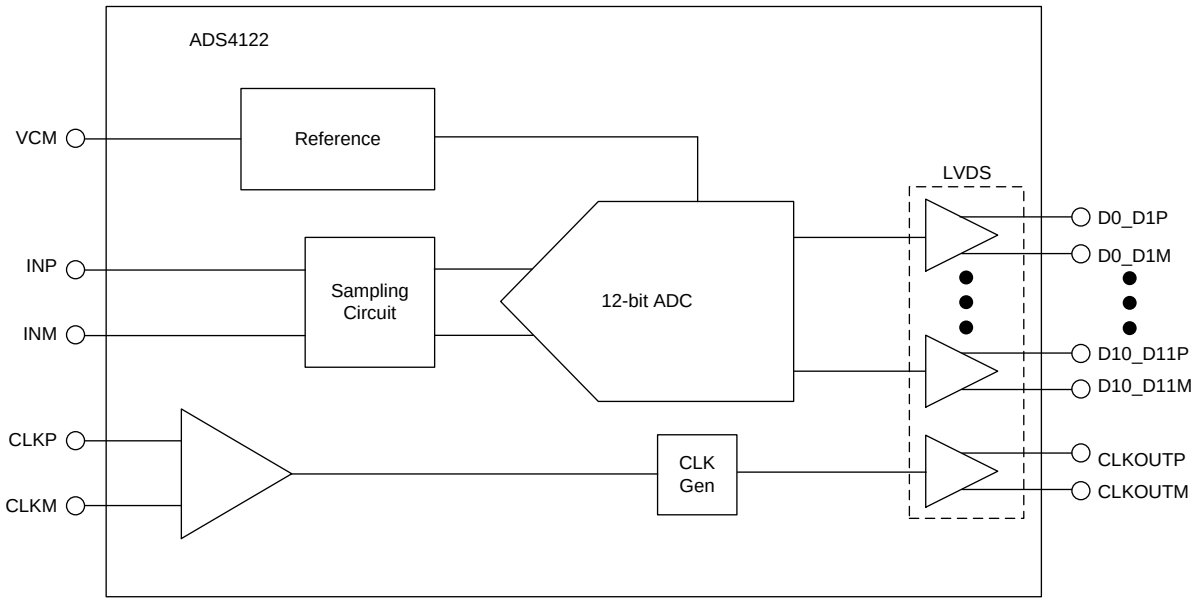
The ADS412x/4x are available in a compact VQFN-48 package and are specified over the industrial temperature range (–40°C to +85°C).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS4122	VQFN (48)	7.00 mm x 7.00 mm
ADS4125		
ADS4142		
ADS4145		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

ADS4122 Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

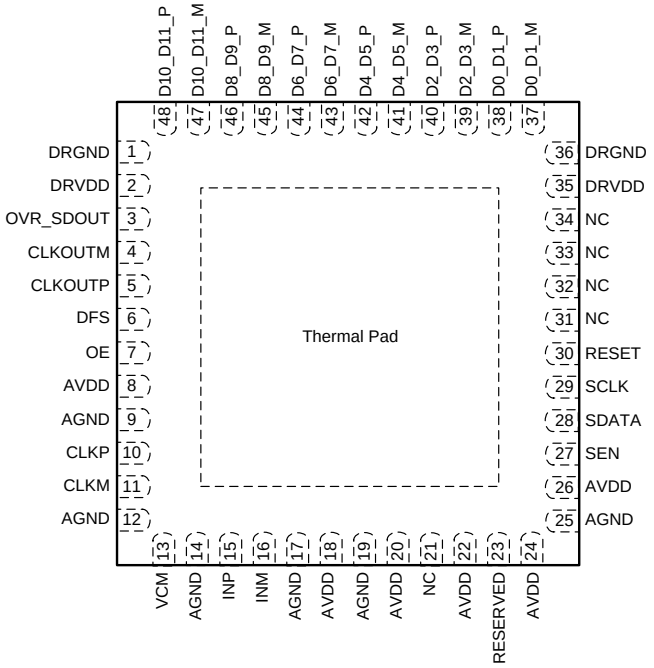
Changes from Revision A (March 2011) to Revision B	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Descriptions*section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support*section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Device Comparison

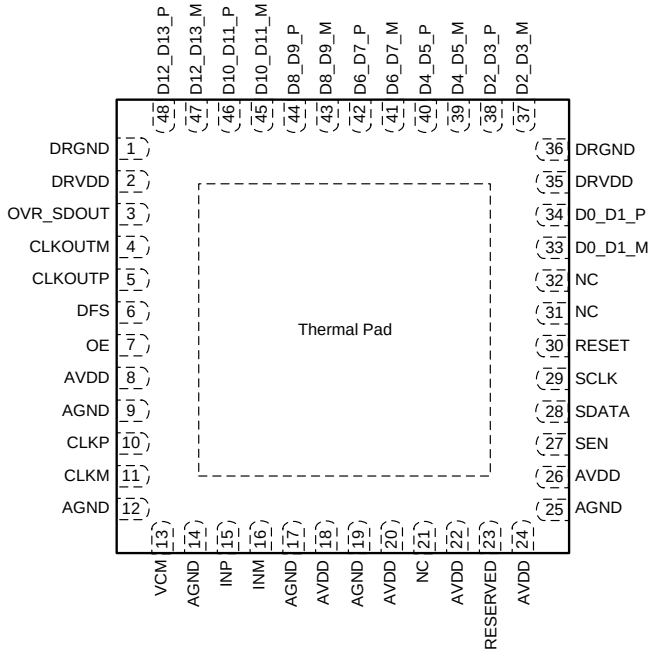
FAMILY	65 MSPS	125 MSPS	160 MSPS	250 MSPS	WITH ANALOG INPUT BUFFERS	
					200 MSPS	250 MSPS
ADS412x 12-Bit Family	ADS4122	ADS4125	ADS4126	ADS4129	—	ADS41B29
ADS414x 14-Bit Family	ADS4142	ADS4145	ADS4146	ADS4149	—	ADS41B49
9-Bit	—	—	—	—	—	ADS58B19
11-Bit	—	—	—	—	ADS58B18	—

6 Pin Configuration and Functions

ADS412x RGZ Package
48-Pin VQFN With Exposed Thermal Pad
LVDS Mode - Top View



ADS414x RGZ Package
48-Pin VQFN With Exposed Thermal Pad
LVDS Mode - Top View



The thermal pad is connected to DRGND.

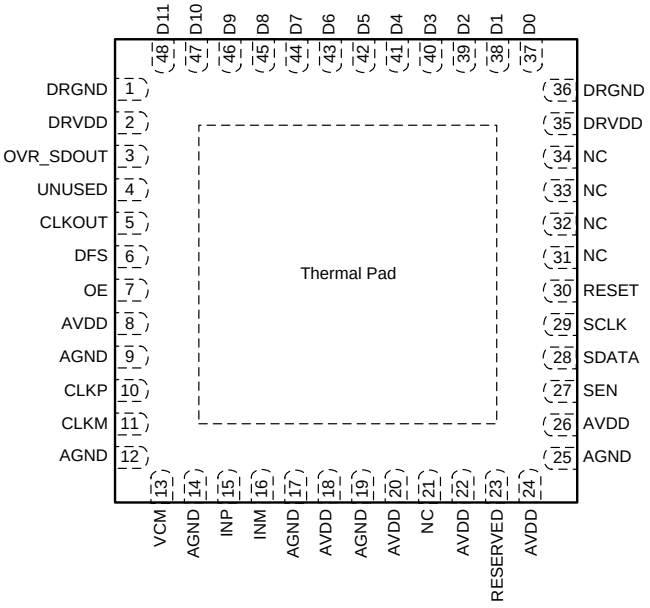
Pin Functions - LVDS Mode

PIN			I/O	DESCRIPTION
NAME	ADS412x	ADS414x		
AGND	9, 12, 14, 17, 19, 25	9, 12, 14, 17, 19, 25	I	Analog ground
AVDD	8, 18, 20, 22, 24, 26	8, 18, 20, 22, 24, 26	I	1.8-V analog power supply
CLKM	11	11	I	Differential clock input, complement
CLKP	10	10	I	Differential clock input, true
CLKOUTM	4	4	O	Differential output clock, complement
CLKOUTP	5	5	O	Differential output clock, true
D0_D1_M	37	33	O	Differential output data D0 and D1 multiplexed, complement
D0_D1_P	38	34	O	Differential output data D0 and D1 multiplexed, true
D2_D3_M	39	37	O	Differential output data D2 and D3 multiplexed, complement
D2_D3_P	40	38	O	Differential output data D2 and D3 multiplexed, true
D4_D5_M	41	39	O	Differential output data D4 and D5 multiplexed, complement
D4_D5_P	42	40	O	Differential output data D4 and D5 multiplexed, true
D6_D7_M	43	41	O	Differential output data D6 and D7 multiplexed, complement
D6_D7_P	44	42	O	Differential output data D6 and D7 multiplexed, true
D8_D9_M	45	43	O	Differential output data D8 and D9 multiplexed, complement
D8_D9_P	46	44	O	Differential output data D8 and D9 multiplexed, true
D10_D11_M	47	45	O	Differential output data D10 and D11 multiplexed, complement
D10_D11_P	48	46	O	Differential output data D10 and D11 multiplexed, true
D12_D13_M	—	47	O	Differential output data D12 and D13 multiplexed, complement
D12_D13_P	—	48	O	Differential output data D12 and D13 multiplexed, true
DFS	6	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS/CMOS output interface type. See Table 4 for detailed information.
DRGND	1, 36, PAD	1, 36, PAD	I	Digital and output buffer ground
DRVDD	2, 35	2, 35	I	1.8-V digital and output buffer supply
INM	16	16	I	Differential analog input, negative
INP	15	15	I	Differential analog input, positive

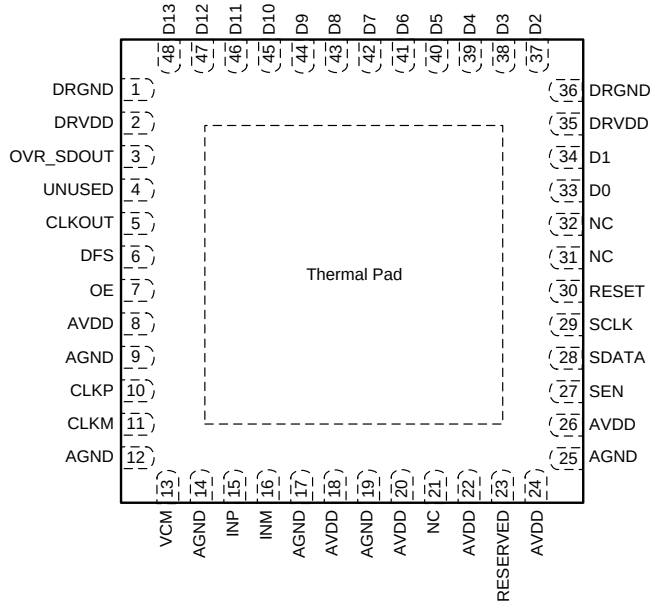
Pin Functions - LVDS Mode (continued)

PIN			I/O	DESCRIPTION
NAME	ADS412x	ADS414x		
NC	21, 31, 32, 33, 34	21, 31, 32	–	Do not connect
OE	7	7	I	Output buffer enable input, active high; this pin has an internal 180-kΩ pull-up resistor to DRVDD.
OVR_SDOUT	3	3	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1.
RESERVED	23	23	I	Digital control pin, reserved for future use
RESET	30	30	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180-kΩ pull-down resistor.
SCLK	29	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180-kΩ pull-down resistor.
SDATA	28	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 6). This pin has an internal 180-kΩ pull-down resistor.
SEN	27	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180-kΩ pull-up resistor to AVDD.
VCM	13	13	O	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.

ADS412x RGZ Package
48-PIN VQFN With Exposed Thermal Pad
CMOS Mode - Top View



ADS414x RGZ Package
48-PIN VQFN With Exposed Thermal Pad
CMOS Mode -Top View



The thermal pad is connected to DRGND.

Pin Functions - CMOS Mode

PIN			I/O	DESCRIPTION
NAME	ADS412x	ADS414x		
AVDD	8, 18, 20, 22, 24, 26	8, 18, 20, 22, 24, 26	I	1.8-V analog power supply
AGND	9, 12, 14, 17, 19, 25	9, 12, 14, 17, 19, 25	I	Analog ground
CLKM	11	11	I	Differential clock input, complement
CLKP	10	10	I	Differential clock input, true
CLKOUT	5	5	O	CMOS output clock
D0	37	33	O	12-bit/14-bit CMOS output data
D1	38	34	O	12-bit/14-bit CMOS output data
D2	39	37	O	12-bit/14-bit CMOS output data

Pin Functions - CMOS Mode (continued)

PIN			I/O	DESCRIPTION
NAME	ADS412x	ADS414x		
D3	40	38	O	12-bit/14-bit CMOS output data
D4	41	39	O	12-bit/14-bit CMOS output data
D5	42	40	O	12-bit/14-bit CMOS output data
D6	43	41	O	12-bit/14-bit CMOS output data
D7	44	42	O	12-bit/14-bit CMOS output data
D8	45	43	O	12-bit/14-bit CMOS output data
D9	46	44	O	12-bit/14-bit CMOS output data
D10	47	45	O	12-bit/14-bit CMOS output data
D11	48	46	O	12-bit/14-bit CMOS output data
D12	—	47	O	12-bit/14-bit CMOS output data
D13	—	48	O	12-bit/14-bit CMOS output data
DFS	6	6	I	Data format select input. This pin sets the DATA FORMAT (twos complement or offset binary) and the LVDS/CMOS output interface type. See Table 4 for detailed information.
DRGND	1, 36, PAD	1, 36, PAD	I	Digital and output buffer ground
DRVDD	2, 35	2, 35	I	1.8-V digital and output buffer supply
INM	16	16	I	Differential analog input, negative
INP	15	15	I	Differential analog input, positive
NC	21, 31, 32, 33, 34	21, 31, 32	–	Do not connect
OE	7	7	I	Output buffer enable input, active high; this pin has an internal 180-kΩ pull-up resistor to DRVDD.
OVR_SDOUT	3	3	O	This pin functions as an out-of-range indicator after reset, when register bit READOUT = 0, and functions as a serial register readout pin when READOUT = 1.
RESERVED	23	23	I	Digital control pin, reserved for future use
RESET	30	30	I	Serial interface RESET input. When using the serial interface mode, the internal registers must initialize through hardware RESET by applying a high pulse on this pin or by using the software reset option; refer to the *Serial Interface* section. When RESET is tied high, the internal registers are reset to the default values. In this condition, SEN can be used as an analog control pin. RESET has an internal 180-kΩ pull-down resistor.
SCLK	29	29	I	This pin functions as a serial interface clock input when RESET is low. When RESET is high, SCLK has no function and should be tied to ground. This pin has an internal 180-kΩ pull-down resistor.
SDATA	28	28	I	This pin functions as a serial interface data input when RESET is low. When RESET is high, SDATA functions as a STANDBY control pin (see Table 6). This pin has an internal 180-kΩ pull-down resistor.
SEN	27	27	I	This pin functions as a serial interface enable input when RESET is low. When RESET is high, SEN has no function and should be tied to AVDD. This pin has an internal 180-kΩ pull-up resistor to AVDD.
UNUSED	4	4	–	Unused pin in CMOS mode
VCM	13	13	O	Outputs the common-mode voltage (0.95 V) that can be used externally to bias the analog input pins.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage, AVDD		–0.3	2.1	V
Supply voltage, DRVDD		–0.3	2.1	V
Voltage between AGND and DRGND		–0.3	0.3	V
Voltage between AVDD to DRVDD (when AVDD leads DRVDD)		0	2.1	V
Voltage between DRVDD to AVDD (when DRVDD leads AVDD)		0	2.1	V
Voltage applied to input pins	INP, INM	–0.3	minimum (1.9, AVDD + 0.3)	V
	CLKP, CLKM(2), DFS, OE	–0.3	AVDD + 0.3	V
	RESET, SCLK, SDATA, SEN	–0.3	3.9	V
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) When AVDD is turned off, it is recommended to switch off the input clock (or ensure the voltage on CLKP, CLKM is less than |0.3 V|. This prevents the ESD protection diodes at the clock input pins from turning on.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
	Differential input voltage range(1)			2		V_{PP}
	Input common-mode voltage			V_{CM} ± 0.05		V
	Maximum analog input frequency with 2-V_{PP} input amplitude(2)			400		MHz
	Maximum analog input frequency with 1-V_{PP} input amplitude(2)			800		MHz
CLOCK INPUT						
	Input clock sample rate	ADS4122/ADS4142, low-speed mode enabled by default	20		65	MSPS
		ADS4125/ADS4145, low-speed mode enabled	20		80	
		ADS4125/ADS4145, low-speed mode disabled	>80		125	
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		
		LVDS, ac-coupled		0.7		
		LVCMOS, single-ended, ac-coupled		1.8		V

(1) With 0dB gain. See the *Gain* section in the *Application Information* for relation between input voltage range and gain.
(2) See *Application Information*.

Recommended Operating Conditions (continued)

Over operating free-air temperature range, unless otherwise noted.

			MIN	NOM	MAX	UNIT
	Input clock duty cycle	Low-speed enabled	40%	50%	60%	
		Low-speed disabled	35%	50%	65%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
T_A	Operating free-air temperature		–40		85	°C
HIGH PERFORMANCE MODES (3) (4) (5)						
Mode 1	Set the MODE 1 register bits to get best performance across sample clock and input signal frequencies. Register address = 03h, register data = 03h					
Mode 2	Set the MODE 2 register bit to get best performance at high input signal frequencies greater than 230 MHz. Register address = 4Ah, register data = 01h					

(3) It is recommended to use these modes to obtain best performance. These modes can be set using the serial interface only.
(4) See the *Serial Interface* section for details on register programming.
(5) Note that these modes cannot be set when the serial interface is not used (when the RESET pin is tied high); see the *Device Configuration* section.

7.4 Thermal Information

THERMAL METRIC (1)		ADS412x ADS414x RGZ (VQFN) 48 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: ADS412x

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, 0dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Resolution					12	Bits
SNR (signal-to-noise ratio), LVDS	f_{IN} = 10 MHz	ADS4122 (65MSPS)		71.1		dBFS
		ADS4125 (125MSPS)		71		
	f_{IN} = 70 MHz	ADS4122 (65MSPS)		70.9		dBFS
		ADS4125 (125MSPS)		70.8		
	f_{IN} = 100 MHz	ADS4122 (65MSPS)		70.7		dBFS
		ADS4125 (125MSPS)		70.6		
	f_{IN} = 170 MHz	ADS4122 (65MSPS)	67	70.2		dBFS
		ADS4125 (125MSPS)	68	70.1		
	f_{IN} = 300 MHz	ADS4122 (65MSPS)		68.8		dBFS
		ADS4125 (125MSPS)		69.6		

Electrical Characteristics: ADS412x (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, 0dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	SINAD (signal-to-noise and distortion ratio), LVDS	f_{IN} = 10 MHz	ADS4122 (65MSPS)		70.8		dBFS
			ADS4125 (125MSPS)		70.7		
		f_{IN} = 70 MHz	ADS4122 (65MSPS)		70.8		dBFS
			ADS4125 (125MSPS)		70.7		
		f_{IN} = 100 MHz	ADS4122 (65MSPS)		70.6		dBFS
			ADS4125 (125MSPS)		70.3		
		f_{IN} = 170 MHz	ADS4122 (65MSPS)	66	70.1		dBFS
			ADS4125 (125MSPS)	67	69.8		
		f_{IN} = 300 MHz	ADS4122 (65MSPS)		68		dBFS
			ADS4125 (125MSPS)		69		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz	ADS4122 (65MSPS)		86.5		dBc
			ADS4125 (125MSPS)		86		
		f_{IN} = 70 MHz			86		dBc
		f_{IN} = 100 MHz	ADS4122 (65MSPS)		87		dBc
			ADS4125 (125MSPS)		82		
		f_{IN} = 170 MHz	ADS4122 (65MSPS)	70	85		dBc
			ADS4125 (125MSPS)	71	81		
		f_{IN} = 300 MHz	ADS4122 (65MSPS)		72.5		dBc
			ADS4125 (125MSPS)		77		
THD	Total harmonic distortion	f_{IN} = 10 MHz	ADS4122 (65MSPS)		82.5		dBc
			ADS4125 (125MSPS)		82		
		f_{IN} = 70 MHz	ADS4122 (65MSPS)		84		dBc
			ADS4125 (125MSPS)		83.5		
		f_{IN} = 100 MHz	ADS4122 (65MSPS)		84		dBc
			ADS4125 (125MSPS)		80.5		
		f_{IN} = 170 MHz	ADS4122 (65MSPS)	69.5	81		dBc
			ADS4125 (125MSPS)	69.5	79.5		
		f_{IN} = 300 MHz	ADS4122 (65MSPS)		72		dBc
			ADS4125 (125MSPS)		75.5		
HD2	Second-harmonic distortion	f_{IN} = 10 MHz			87		dBc
		f_{IN} = 70 MHz	ADS4122 (65MSPS)		88		dBc
			ADS4125 (125MSPS)		86		
		f_{IN} = 100 MHz	ADS4122 (65MSPS)		88		dBc
			ADS4125 (125MSPS)		82		
		f_{IN} = 170 MHz	ADS4122 (65MSPS)	70	86		dBc
			ADS4125 (125MSPS)	71	83		
		f_{IN} = 300 MHz	ADS4122 (65MSPS)		72.5		dBc
			ADS4125 (125MSPS)		77		
HD3	Third-harmonic distortion	f_{IN} = 10 MHz	ADS4122 (65MSPS)		86.5		dBc
			ADS4125 (125MSPS)		86		
		f_{IN} = 70 MHz	ADS4122 (65MSPS)		86		dBc
			ADS4125 (125MSPS)		88		
		f_{IN} = 100 MHz	ADS4122 (65MSPS)		87		dBc
			ADS4125 (125MSPS)		85		
		f_{IN} = 170 MHz	ADS4122 (65MSPS)	70	85		dBc
			ADS4125 (125MSPS)	71	81		
		f_{IN} = 300 MHz	ADS4122 (65MSPS)		85		dBc
			ADS4125 (125MSPS)		82		

Electrical Characteristics: ADS412x (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1dBFS differential analog input, 0dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz	ADS4122 (65MSPS)		96		dBc
			ADS4125 (125MSPS)		95		
		f_{IN} = 70 MHz	ADS4122 (65MSPS)		96		dBc
			ADS4125 (125MSPS)		95		
		f_{IN} = 100 MHz	ADS4122 (65MSPS)		94		dBc
			ADS4125 (125MSPS)		95		
		f_{IN} = 170 MHz	ADS4122 (65MSPS)	76.5	92		dBc
			ADS4125 (125MSPS)	76.5	91		
		f_{IN} = 300 MHz			88		dBc
IMD	Two-tone intermodulation distortion	f_1 = 100 MHz, f_2 = 105 MHz, each tone at –7 dBFS	ADS4122 (65MSPS)		90		dBFS
			ADS4125 (125MSPS)		87.5		
	Input overload recovery	Recovery to within 1% (of final value) for 6dB overload with sine-wave input			1		Clock cycles
PSRR	AC power-supply rejection ratio	For 100-mV_{PP} signal on AVDD supply, up to 10 MHz			> 30		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz			11.2		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		–0.85	±0.2	1.5	LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz	ADS4122 (65MSPS)		±0.3	3.5	LSBs
			ADS4125 (125MSPS)		±0.35	3.5	

7.6 Electrical Characteristics: ADS414x

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution					14	Bits
	SNR (signal-to-noise ratio), LVDS	f_{IN} = 10 MHz	ADS4142 (65 MSPS)		73.9		dBFS
			ADS4145 (125 MSPS)		73.7		
		f_{IN} = 70 MHz	ADS4142 (65 MSPS)		73.5		dBFS
			ADS4145 (125 MSPS)		73.4		
		f_{IN} = 100 MHz	ADS4142 (65 MSPS)		73.2		dBFS
			ADS4145 (125 MSPS)		73.1		
		f_{IN} = 170 MHz	ADS4142 (65 MSPS)	69	72.4		dBFS
			ADS4145 (125 MSPS)	70	72.2		
		f_{IN} = 300 MHz	ADS4142 (65 MSPS)		70.5		dBFS
			ADS4145 (125 MSPS)		71.3		
	SINAD (signal-to-noise and distortion ratio), LVDS	f_{IN} = 10 MHz	ADS4142 (65 MSPS)		73.5		dBFS
			ADS4145 (125 MSPS)		73.2		
		f_{IN} = 70 MHz	ADS4142 (65 MSPS)		73.3		dBFS
			ADS4145 (125 MSPS)		73		
		f_{IN} = 100 MHz	ADS4142 (65 MSPS)		73		dBFS
			ADS4145 (125 MSPS)		72.6		
		f_{IN} = 170 MHz	ADS4142 (65 MSPS)	68	72.3		dBFS
			ADS4145 (125 MSPS)	69	71.8		
		f_{IN} = 300 MHz	ADS4142 (65 MSPS)		69.2		dBFS
			ADS4145 (125 MSPS)		70.6		

Electrical Characteristics: ADS414x (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz	ADS4142 (65 MSPS)		87		dBc
			ADS4145 (125 MSPS)		86		
		f_{IN} = 70 MHz	ADS4142 (65 MSPS)		86.5		dBc
			ADS4145 (125 MSPS)		85.5		
		f_{IN} = 100 MHz	ADS4142 (65 MSPS)		87		dBc
			ADS4145 (125 MSPS)		82		
		f_{IN} = 170 MHz	ADS4142 (65 MSPS)	71	85		dBc
			ADS4145 (125 MSPS)	72.5	81.5		
		f_{IN} = 300 MHz	ADS4142 (65 MSPS)		72.5		dBc
			ADS4145 (125 MSPS)		77		
THD	Total harmonic distortion	f_{IN} = 10 MHz	ADS4142 (65 MSPS)		84		dBc
			ADS4145 (125 MSPS)		83		
		f_{IN} = 70 MHz	ADS4142 (65 MSPS)		84		dBc
			ADS4145 (125 MSPS)		83.5		
		f_{IN} = 100 MHz	ADS4142 (65 MSPS)		84		dBc
			ADS4145 (125 MSPS)		81		
		f_{IN} = 170 MHz	ADS4142 (65 MSPS)	69.5	82.5		dBc
			ADS4145 (125 MSPS)	70.5	80		
		f_{IN} = 300 MHz	ADS4142 (65 MSPS)		72.5		dBc
			ADS4145 (125 MSPS)		75.5		
HD2	Second-harmonic distortion	f_{IN} = 10 MHz	ADS4142 (65 MSPS)		88		dBc
			ADS4145 (125 MSPS)		87		
		f_{IN} = 70 MHz	ADS4142 (65 MSPS)		87		dBc
			ADS4145 (125 MSPS)		85.5		
		f_{IN} = 100 MHz	ADS4142 (65 MSPS)		88		dBc
			ADS4145 (125 MSPS)		82		
		f_{IN} = 170 MHz	ADS4142 (65 MSPS)	71	87		dBc
			ADS4145 (125 MSPS)	72.5	84		
		f_{IN} = 300 MHz	ADS4142 (65 MSPS)		72.5		dBc
			ADS4145 (125 MSPS)		77		
HD3	Third-harmonic distortion	f_{IN} = 10 MHz	ADS4142 (65 MSPS)		87		dBc
			ADS4145 (125 MSPS)		86		
		f_{IN} = 70 MHz	ADS4142 (65 MSPS)		86.5		dBc
			ADS4145 (125 MSPS)		87		
		f_{IN} = 100 MHz	ADS4142 (65 MSPS)		87		dBc
			ADS4145 (125 MSPS)		85		
		f_{IN} = 170 MHz	ADS4142 (65 MSPS)	71	85		dBc
			ADS4145 (125 MSPS)	72.5	81.5		
		f_{IN} = 300 MHz	ADS4142 (65 MSPS)		85		dBc
			ADS4145 (125 MSPS)		84		

Electrical Characteristics: ADS414x (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, and DDR LVDS interface, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz	ADS4142 (65 MSPS)		96		dBc
			ADS4145 (125 MSPS)		95		
		f_{IN} = 70 MHz			95		dBc
		f_{IN} = 100 MHz	ADS4142 (65 MSPS)		94		dBc
			ADS4145 (125 MSPS)		95		
		f_{IN} = 170 MHz	ADS4142 (65 MSPS)	77.5	92		dBc
			ADS4145 (125 MSPS)	78.5	91		
		f_{IN} = 300 MHz	ADS4142 (65 MSPS)		87		dBc
			ADS4145 (125 MSPS)		88		
IMD	Two-tone intermodulation distortion	f_1 = 100 MHz, f_2 = 105 MHz, each tone at –7 dBFS	ADS4142 (65 MSPS)		88.5		dBFS
			ADS4145 (125 MSPS)		87.5		
	Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine-wave input			1		Clock cycles
PSRR	AC power-supply rejection ratio	For 100-mV_{PP} signal on AVDD supply, up to 10 MHz			> 30		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz	ADS4142 (65 MSPS)		11.5		LSBs
			ADS4145 (125 MSPS)		11.3		
DNL	Differential nonlinearity	f_{IN} = 170 MHz		–0.95	±0.5	1.7	LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz			±1.5	±4.5	LSBs

7.7 Electrical Characteristics: General

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER			MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Differential input voltage range			2		V_{PP}
	Differential input resistance (at DC); see Figure 106			> 1		MΩ
	Differential input capacitance; see Figure 107			4		pF
	Analog input bandwidth			550		MHz
	Analog input common-mode current (per input pin)			0.6		µA/MSPS
VCM	Common-mode output voltage			0.95		V
	VCM output current capability			4		mA
DC ACCURACY						
	Offset error		–15	2.5	15	mV
	Temperature coefficient of offset error			0.003		mV/°C
E_{GREF}	Gain error as a result of internal reference inaccuracy alone		–2		2	%FS
E_{GCHAN}	Gain error of channel alone			–0.2		%FS
	Temperature coefficient of E_{GCHAN}			0.001		Δ%/°C
POWER SUPPLY						
	IAVDD Analog supply current	ADS4122/ADS4142 (65MSPS)		42	55	mA
		ADS4125/ADS4145 (125MSPS)		62	75	
	IDRVDD(1) Output buffer supply current LVDS interface with 100-Ω external termination Low LVDS swing (200 mV)	ADS4122/ADS4142 (65MSPS)		28.5		mA
		ADS4125/ADS4145 (125MSPS)		35.5		

(1) The maximum DRVDD current with CMOS interface depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance on each digital output line is 10 pF.

Electrical Characteristics: General (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, 50% clock duty cycle, and 0-dB gain, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		MIN	TYP	MAX	UNIT
IDRVDD Output buffer supply current LVDS interface with 100-Ω external termination Standard LVDS swing (350 mV)	ADS4122/ADS4142 (65MSPS)		40	53	mA
	ADS4125/ADS4145 (125MSPS)		48	57	
IDRVDD output buffer supply current(1)(2) CMOS interface(2) 8-pF external load capacitance f_{IN} = 2.5 MHz	ADS4122/ADS4142 (65MSPS)		15		mA
	ADS4125/ADS4145 (125MSPS)		23		
Analog power	ADS4122/ADS4142 (65MSPS)		76		mW
	ADS4125/ADS4145 (125MSPS)		112		
Digital power, LVDS interface, low LVDS swing	ADS4122/ADS4142 (65MSPS)		52		mW
	ADS4125/ADS4145 (125MSPS)		66.5		
Digital power CMOS interface(2) 8-pF external load capacitance f_{IN} = 2.5 MHz	ADS4122/ADS4142 (65MSPS)		27		mW
	ADS4125/ADS4145 (125MSPS)		41.5		
Global power-down			10	15	mW
Standby	ADS4122/ADS4142 (65MSPS)		105		mW
	ADS4125/ADS4145 (125MSPS)		130		

(2) In CMOS mode, the DRVDD current scales with the sampling frequency, the load capacitance on output pins, input frequency, and the supply voltage (see the *CMOS Interface Power Dissipation* section in the *Application Information*).

7.8 Digital Characteristics

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, and 50% clock duty cycle for the ADS4122, ADS4125, ADS4142, and ADS4145, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, OE)						
High-level input voltage		RESET, SCLK, SDATA, and SEN support 1.8-V and 3.3-V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input voltage		OE only supports 1.8-V CMOS logic levels	1.3			V
Low-level input voltage					0.4	V
High-level input current: SDATA, SCLK(1)		V_{HIGH} = 1.8 V		10		µA
High-level input current: SEN		V_{HIGH} = 1.8 V		0		µA
Low-level input current: SDATA, SCLK		V_{LOW} = 0 V		0		µA
Low-level input current: SEN		V_{LOW} = 0 V		–10		µA
DIGITAL OUTPUTS (CMOS INTERFACE: D0 TO D13, OVR_SDOUT)						
High-level output voltage			DRVDD – 0.1	DRVDD		V
Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS (LVDS INTERFACE: DA0P/M TO DA13P/M, DB0P/M TO DB13P/M, CLKOUTP/M)						
High-level output voltage(2)	V_{ODH}	Standard swing LVDS	270	350	430	mV
Low-level output voltage(2)	V_{ODL}	Standard swing LVDS	–430	–350	–270	mV
High-level output voltage(2)	V_{ODH}	Low swing LVDS		200		mV
Low-level output voltage(2)	V_{ODL}	Low swing LVDS		–200		mV
Output common-mode voltage	V_{OCM}		0.85	1.05	1.25	V

(1) SDATA and SCLK have an internal 180-kΩ pull-down resistor.
(2) With an external 100-Ω termination.

7.9 Timing Requirements: LVDS and CMOS Modes[1]

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 125 MSPS, sine wave input clock, C_{LOAD} = 5 pF[2], and R_{LOAD} = 100 Ω[3], unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay		0.6	0.8	1.2	ns
	Variation of aperture delay	Between two devices at the same temperature and DRVDD supply		±100		ps
t_J	Aperture jitter			100		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		5	25	µs
		Time to valid data after coming out of PDN GLOBAL mode		100	500	µs
	ADC latency[4]	Low-latency mode (default after reset)		10		Clock cycles
		Low-latency mode disabled (gain enabled, offset correction disabled)		16		Clock cycles
		Low-latency mode disabled (gain and offset correction enabled)		17		Clock cycles
DDR LVDS MODE[5][6]						
t_{SU}	Data setup time[3]	Data valid[7] to zero-crossing of CLKOUTP	2.3	3		ns
t_H	Data hold time[3]	Zero-crossing of CLKOUTP to data becoming invalid[7]	0.35	0.6		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over *Sampling frequency ≤ 125 MSPS*	3	4.2	5.4	ns
	Variation of t_{PDI}	Between two devices at the same temperature and DRVDD supply		±0.6		ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP – CLKOUTM) *Sampling frequency ≤ 125 MSPS*		48%		
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from –100mV to 100mV Fall time measured from 100mV to –100mV *Sampling frequency ≤ 125 MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to 100 mV Fall time measured from 100 mV to –100 mV *Sampling frequency ≤ 125 MSPS*		0.14		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		50	100	ns
PARALLEL CMOS MODE[8]						
t_{SETUP}	Data setup time	Data valid[9] to 50% of CLKOUT rising edge	3.1	3.7		ns
t_{HOLD}	Data hold time	50% of of CLKOUT rising edge to data becoming invalid[9]	3.2	4		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to 50% of output clock rising edge *Sampling frequency ≤ 125 MSPS*	4	5.5	7	ns
	Output clock duty cycle	Duty cycle of output clock, CLKOUT *Sampling frequency ≤ 125 MSPS*		47%		

(1) Timing parameters are ensured by design and characterization but are not production tested.
(2) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(3) R_{LOAD} is the differential load resistance between the LVDS output pair.
(4) At higher frequencies, t_{PDI} is greater than one clock period and overall latency = ADC latency + 1.
(5) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and the load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) The LVDS timings are unchanged for low latency disabled and enabled.
(7) Data valid refers to a logic high of 100 mV and a logic low of –100 mV.
(8) Low latency mode enabled.
(9) Data valid refers to a logic high of 1.25 V and a logic low of 0.54 V.

Timing Requirements: LVDS and CMOS Modes(1) (continued)

Typical values are at 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, sampling frequency = 125 MSPS, sine wave input clock, C_{LOAD} = 5 pF(2), and R_{LOAD} = 100 Ω(3), unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.7 V to 1.9 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RISE}, t_{FALL}	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *Sampling frequency ≤ 125 MSPS*		0.35		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD *Sampling frequency ≤ 125 MSPS*		0.35		ns
t_{OE}	Output enable (OE) to data delay	Time to valid data after OE becomes active		20	40	ns

7.10 Serial Interface Timing Characteristics

Typical values at 25°C, minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, AVDD = 1.8 V, and DRVDD = 1.8 V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1/t_{SCLK})	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

7.11 Reset Timing Requirements

Typical values at 25°C and minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C, unless otherwise noted.

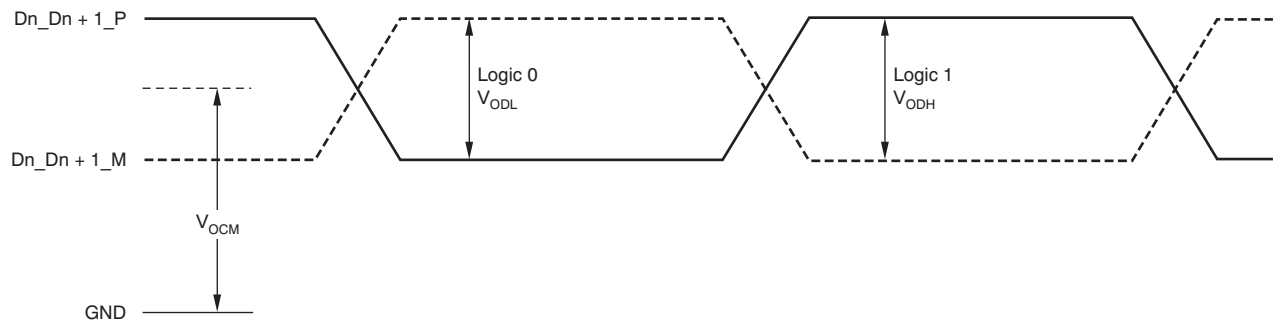
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	1			ms
t_2	Reset pulse width	Pulse width of active RESET signal that resets the serial registers	10			ns
					1(1)	µs
t_3		Delay from RESET disable to SEN active	100			ns

(1) The reset pulse is needed only when using the serial interface configuration. If the pulse width is greater than 1µs, the device could enter the parallel configuration mode briefly and then return back to serial interface mode.

7.12 Timing Characteristics at Lower Sampling Frequencies

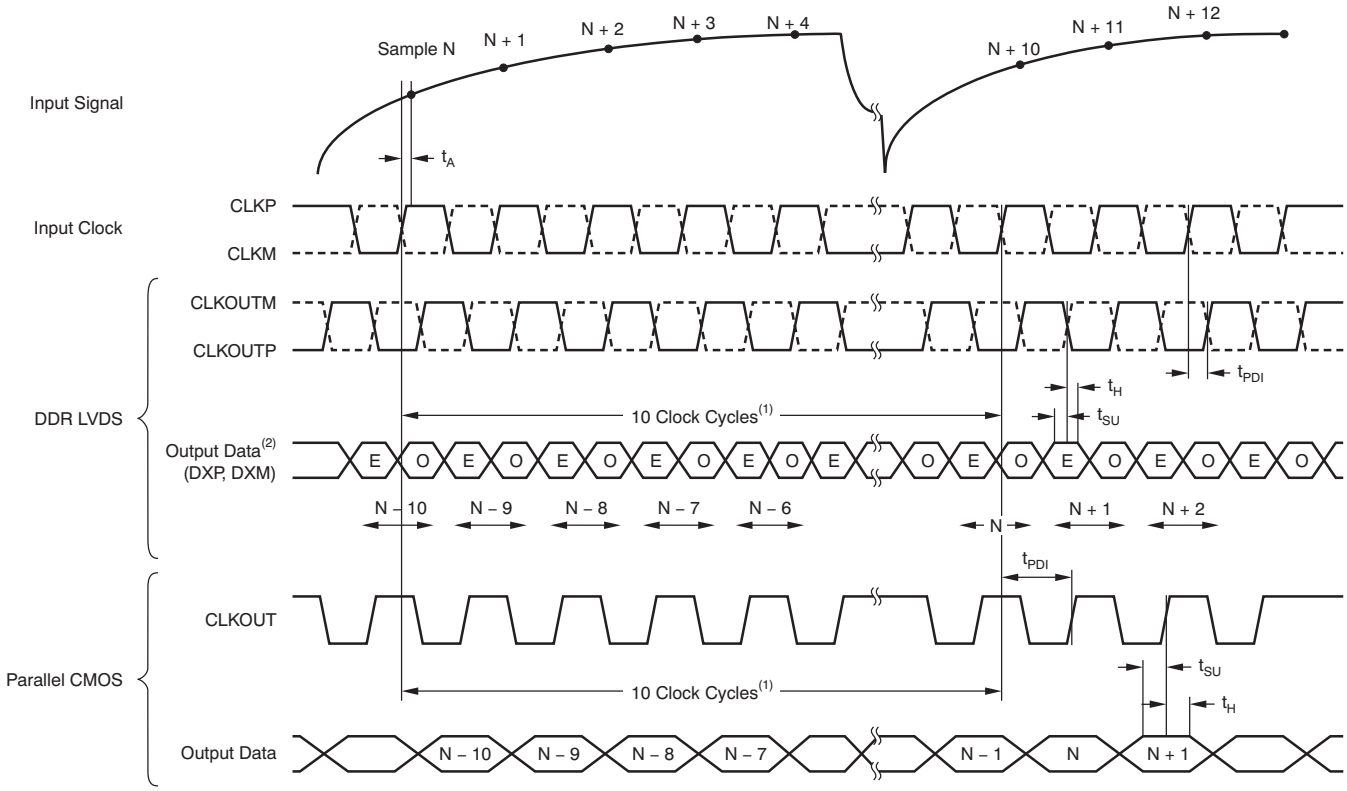
SAMPLING FREQUENCY (MSPS)	t_{su}, SETUP TIME (ns)			t_h, HOLD TIME (ns)			t_{PDI}, CLOCK PROPAGATION DELAY (ns)		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
DDR LVDS									
65	5.5	6.5		0.35	0.6				
80	4.5	5.2		0.35	0.6				
CMOS (LOW LATENCY ENABLED)(1)									
65	6.5	7.5		6.5	7.5		4	5.5	7
80	5.4	6		5.4	6		4	5.5	7
CMOS (LOW LATENCY DISABLED)(1)									
65	6	7		7	8		4	5.5	7
80	4.8	5.5		5.7	6.5		4	5.5	7
125	2.5	3.2		3.5	4.3		4	5.5	7

(1) Timing specified with respect to output clock



(1) With external 100-Ω termination.

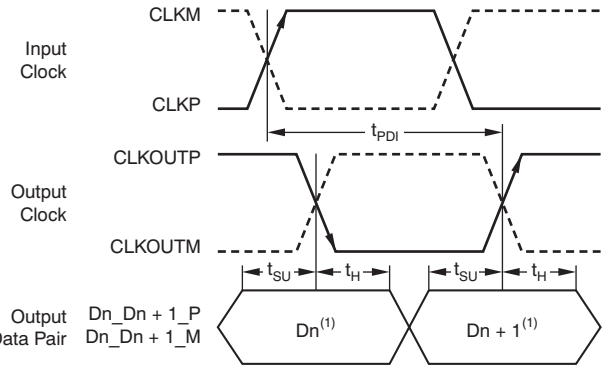
Figure 1. LVDS Output Voltage Levels



(1) ADC latency in low-latency mode. At higher sampling frequencies, t_{DPI} is greater than one clock cycle which then makes the overall latency = ADC latency + 1.

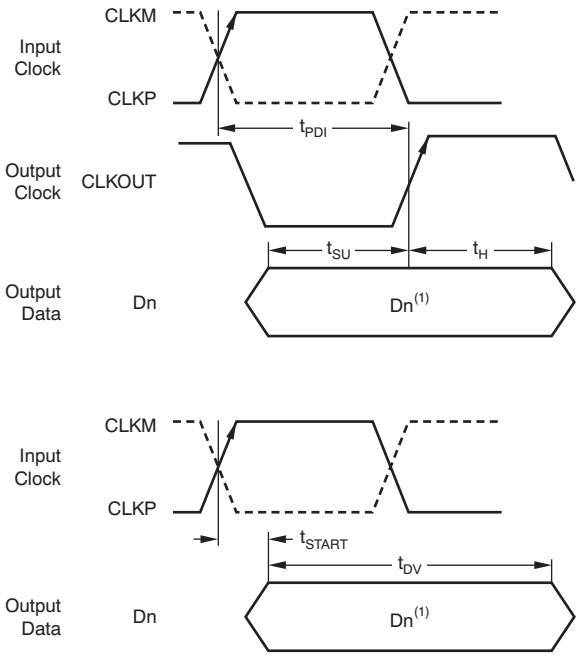
(2) E = Even bits (D0, D2, D4, etc). O = Odd bits (D1, D3, D5, and so forth).

Figure 2. Latency Diagram



(1) Dn = bits D0, D2, D4, etc. Dn + 1 = Bits D1, D3, D5, and so forth.

Figure 3. LVDS Mode Timing



Dn = bits D0, D1, D2, and so forth.

Figure 4. CMOS Mode Timing

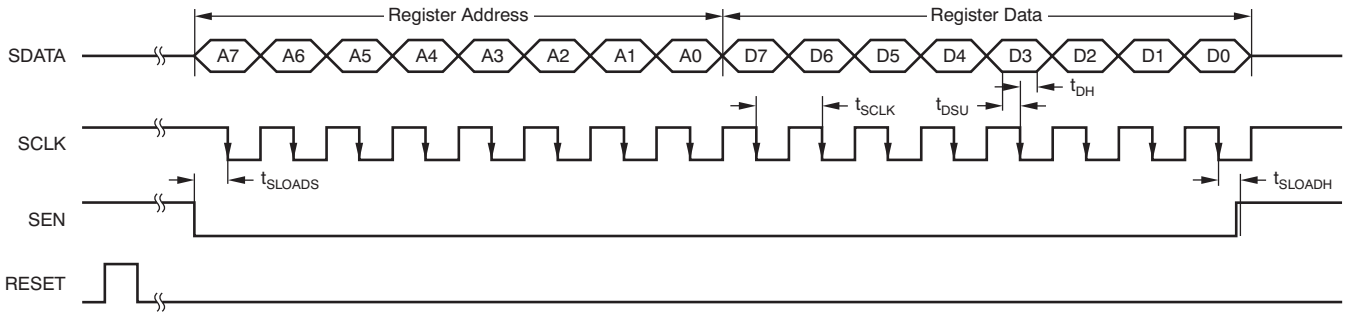
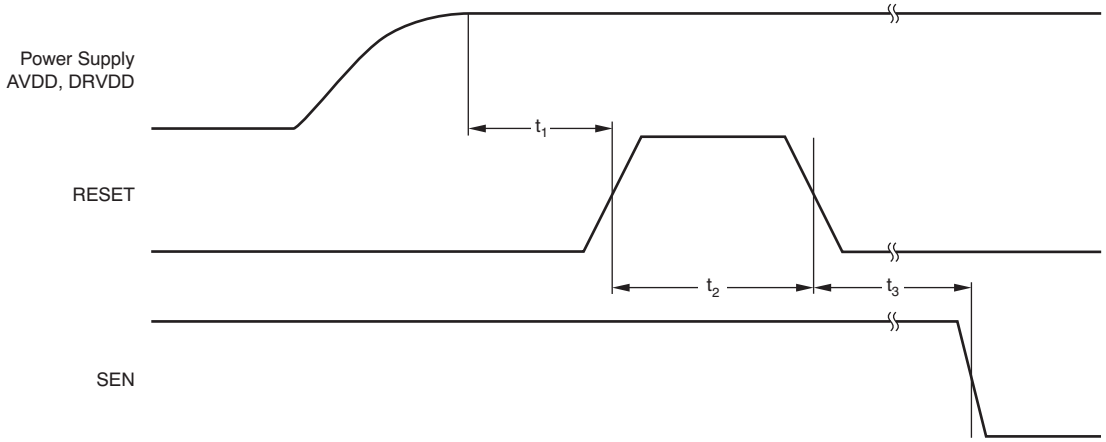


Figure 5. Serial Interface Timing



A high pulse on the RESET pin is required in the serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET must be permanently tied high.

Figure 6. Reset Timing Diagram

7.13 Typical Characteristics

7.13.1 Typical Characteristics: ADS4122

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

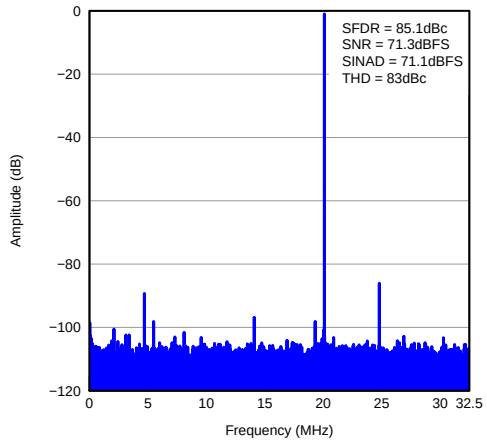


Figure 7. FFT for 20-MHz Input Signal

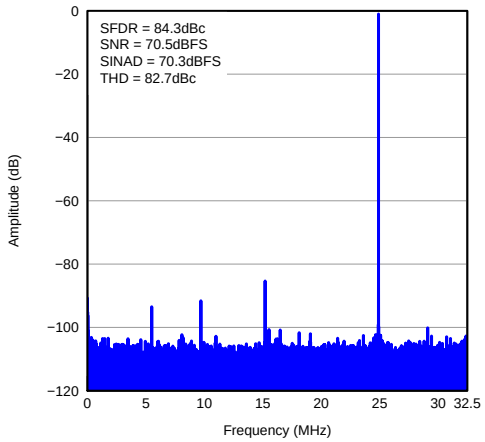


Figure 8. FFT for 170-MHz Input Signal

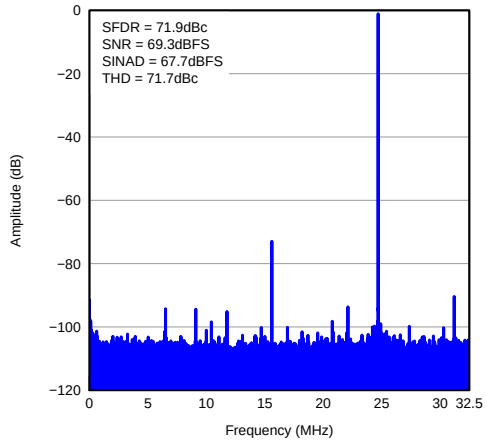


Figure 9. FFT for 300-MHz Input Signal

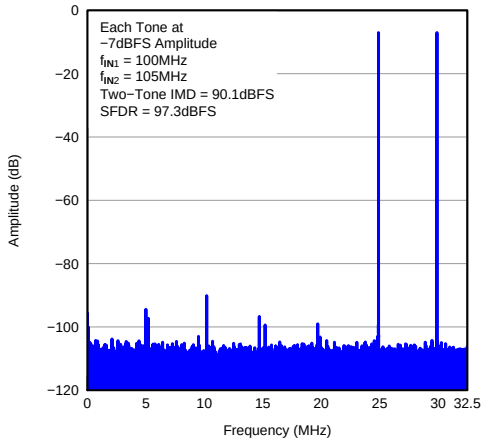


Figure 10. FFT for Two-Tone Input Signal

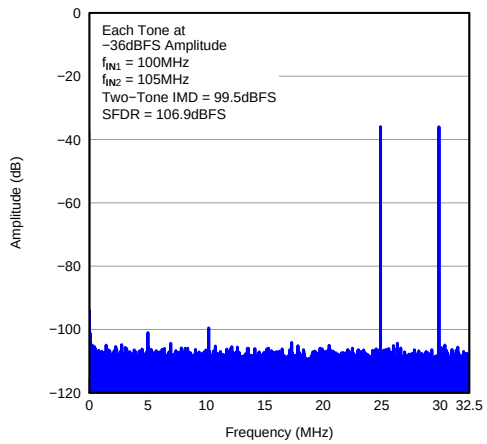


Figure 11. FFT for Two-Tone Input Signal

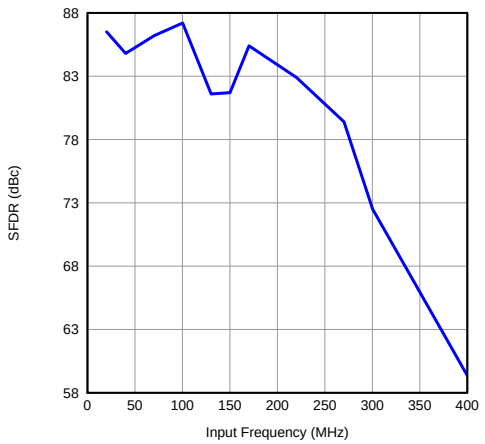


Figure 12. SFDR vs Input Frequency

Typical Characteristics: ADS4122 (continued)

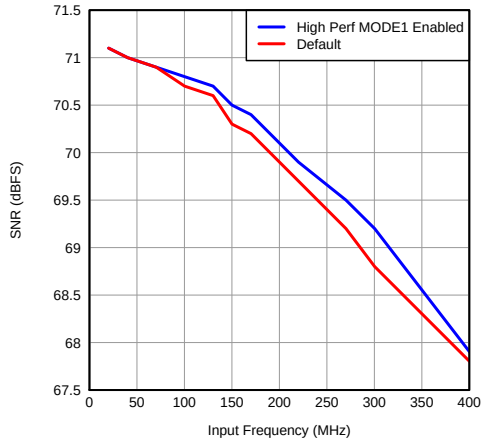


Figure 13. SNR vs Input Frequency

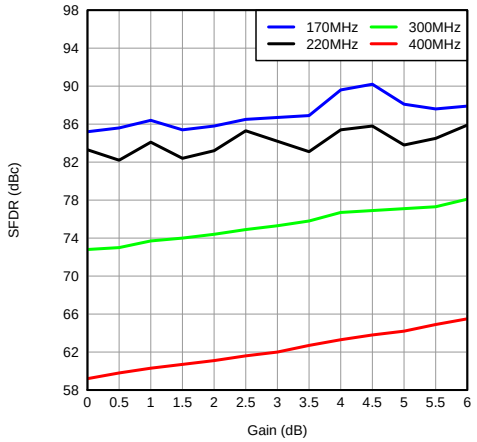


Figure 14. SFDR Across Gain and Input Frequency

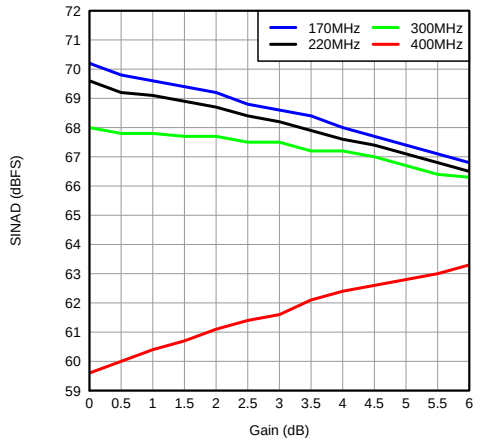


Figure 15. SINAD Across Gain and Input Frequency

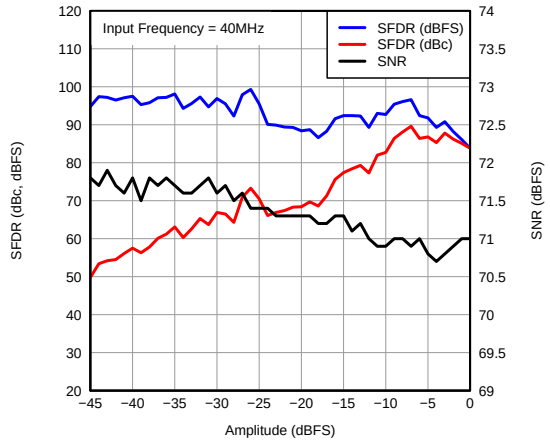


Figure 16. Performance Across Input Amplitude (Single Tone)

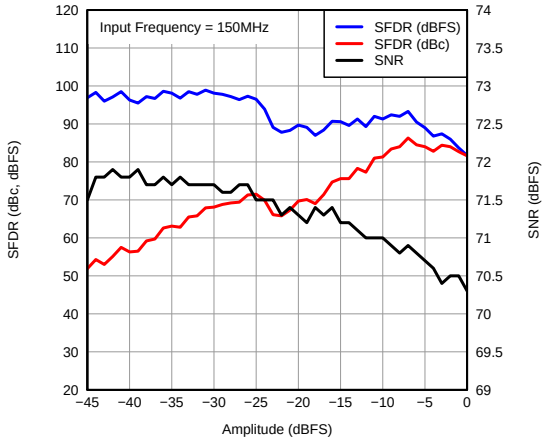


Figure 17. Performance Across Input Amplitude (Single Tone)

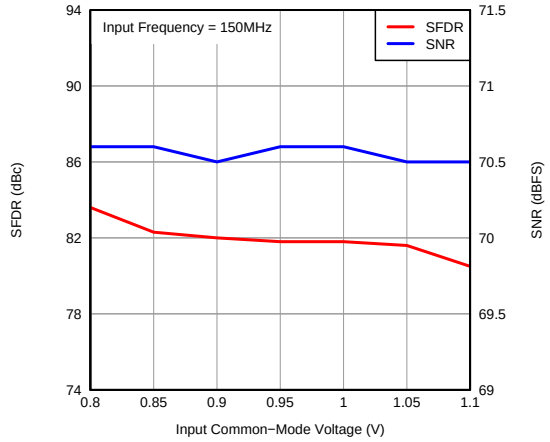


Figure 18. Performance vs Input Common-Mode Voltage

Typical Characteristics: ADS4122 (continued)

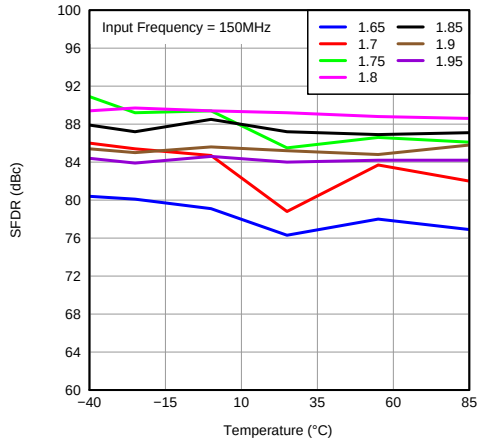


Figure 19. SFDR Across Temperature vs AVDD Supply

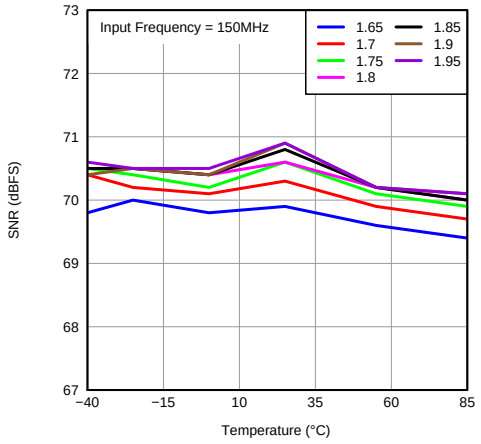


Figure 20. SNR Across Temperature vs AVDD Supply

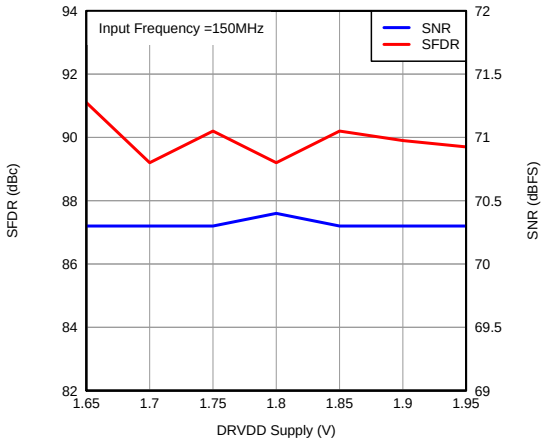


Figure 21. Performance Across DRVDD Supply Voltage

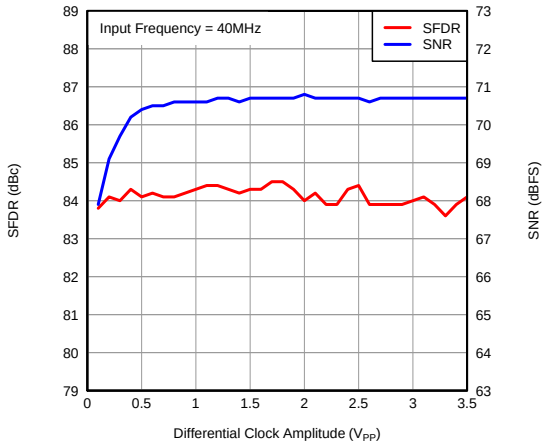


Figure 22. Performance Across Input Clock Amplitude

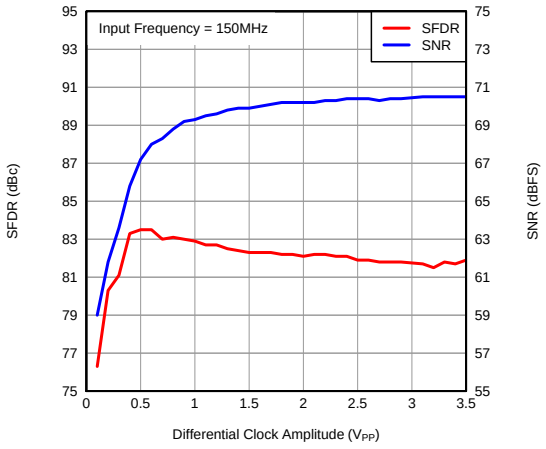


Figure 23. Performance Across Input Clock Amplitude

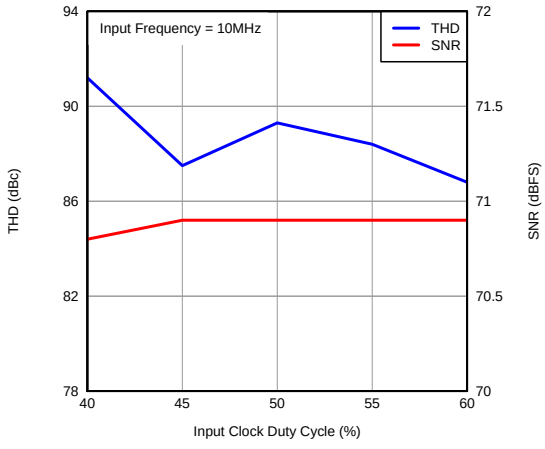


Figure 24. Performance Across Input Clock Duty Cycle

7.13.2 Typical Characteristics: ADS4125

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

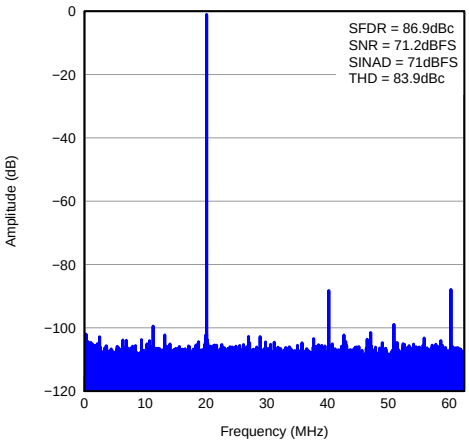


Figure 25. FFT for 20-MHz Input Signal

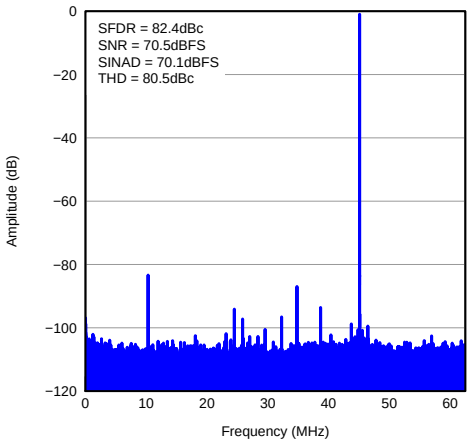


Figure 26. FFT for 170-MHz Input Signal

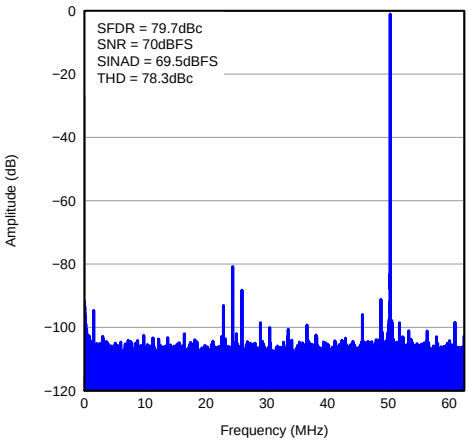


Figure 27. FFT for 300-MHz Input Signal

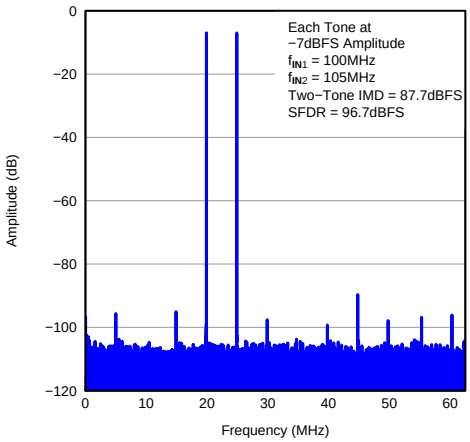


Figure 28. FFT for Two-Tone Input Signal

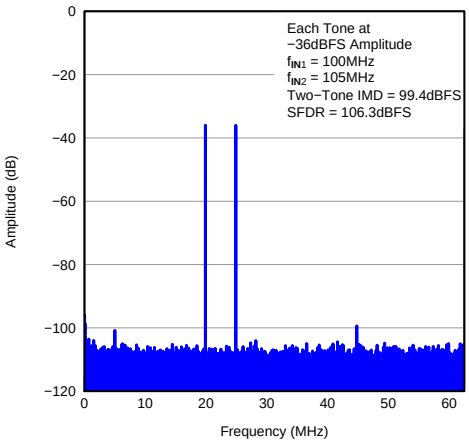


Figure 29. FFT for Two-Tone Input Signal

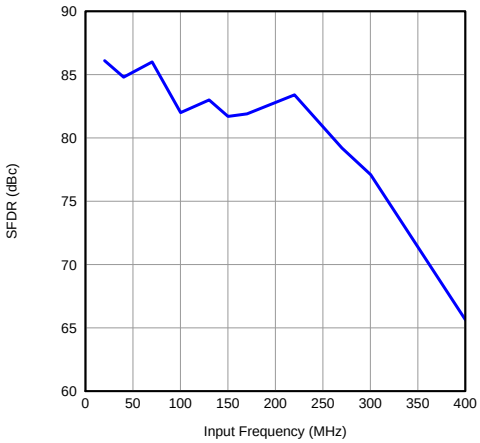


Figure 30. SFDR vs Input Frequency

Typical Characteristics: ADS4125 (continued)

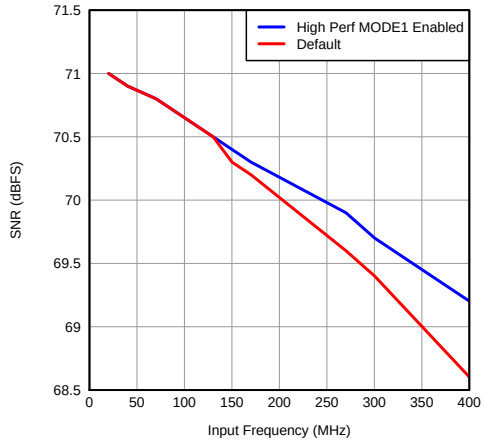


Figure 31. SNR vs Input Frequency

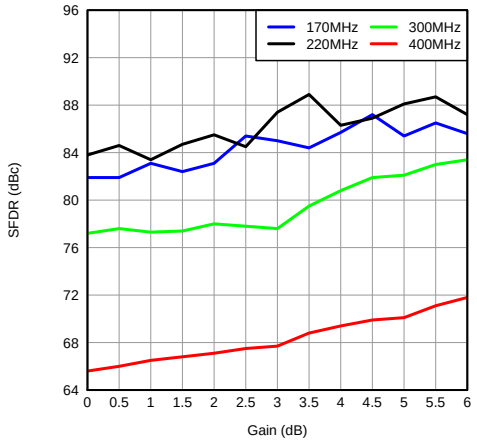


Figure 32. SFDR Across Gain and Input Frequency

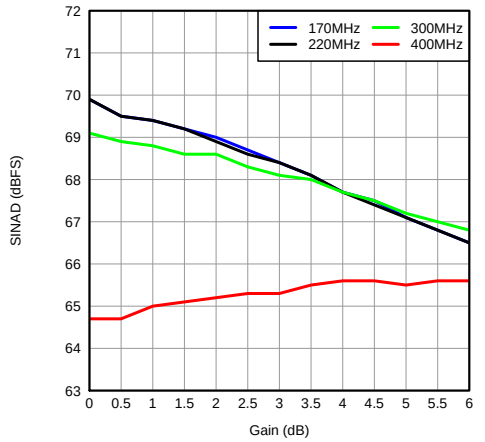


Figure 33. SINAD Across Gain and Input Frequency

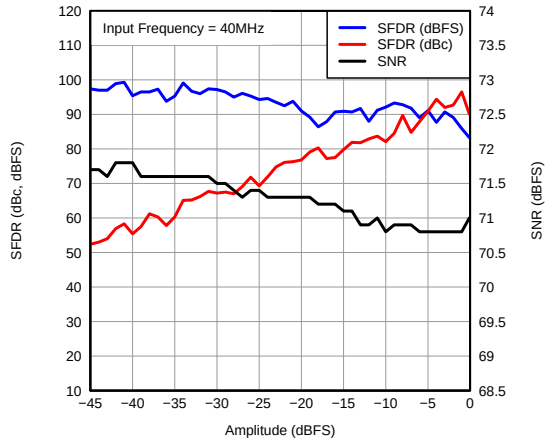


Figure 34. Performance Across Input Amplitude (Single Tone)

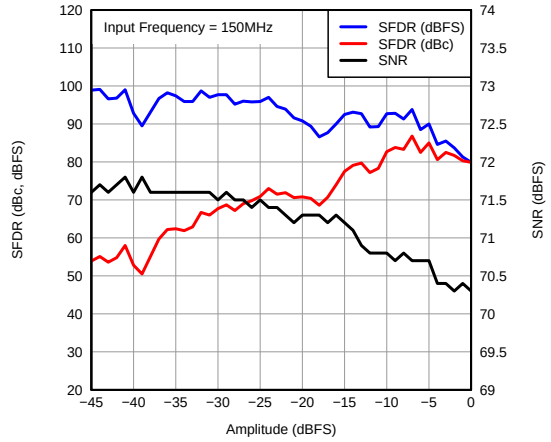


Figure 35. Performance Across Input Amplitude (Single Tone)

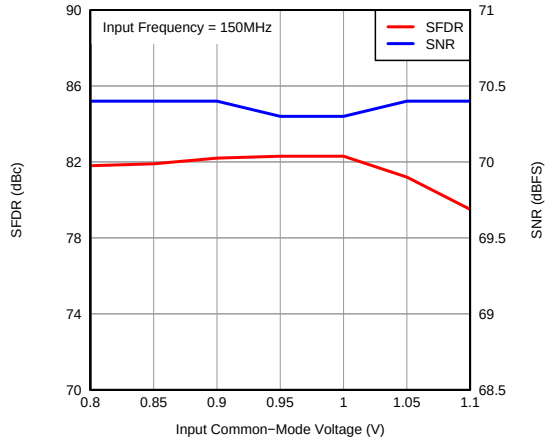


Figure 36. Performance vs Input Common-Mode Voltage

Typical Characteristics: ADS4125 (continued)

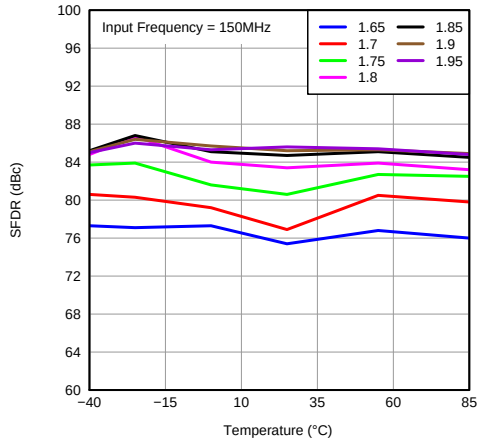


Figure 37. SFDR Across Temperature vs AVDD Supply

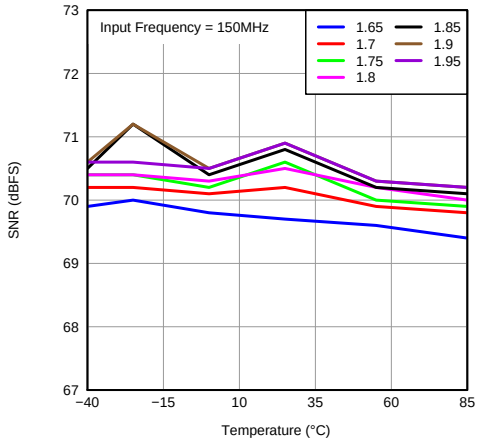


Figure 38. SNR Across Temperature vs AVDD Supply

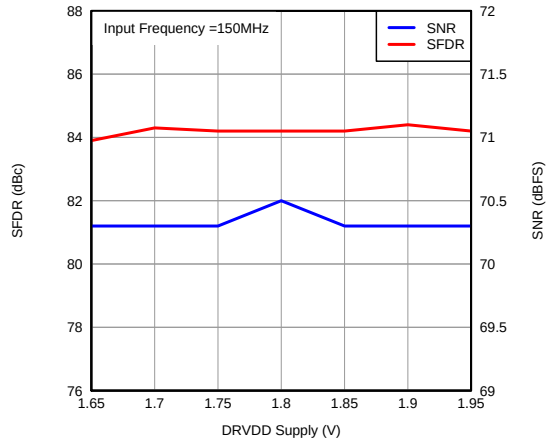


Figure 39. Performance Across DRVDD Supply Voltage

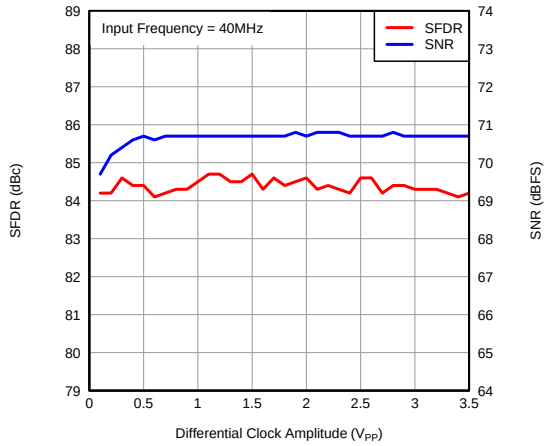


Figure 40. Performance Across Input Clock Amplitude

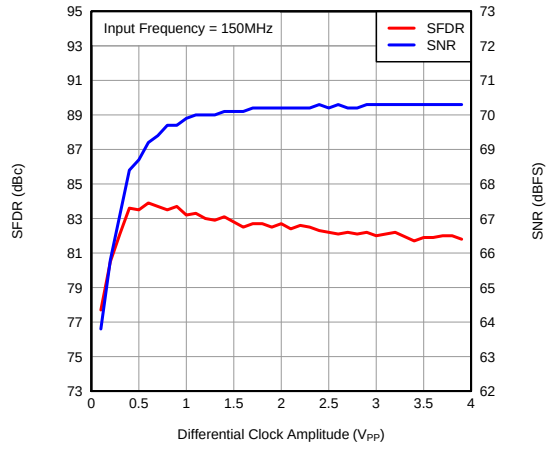


Figure 41. Performance Across Input Clock Amplitude

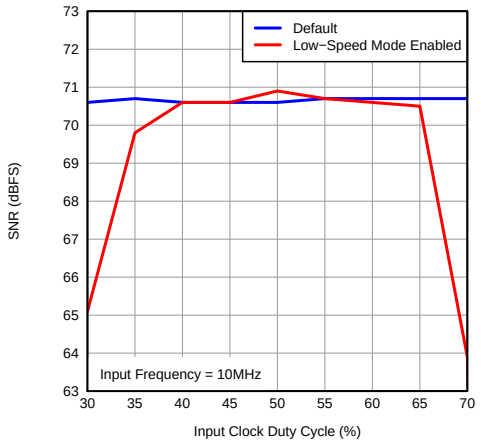


Figure 42. SNR Across Input Clock Duty Cycle

7.13.3 Typical Characteristics: ADS4142

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

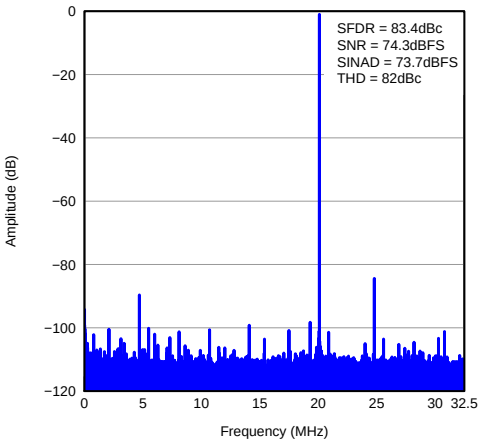


Figure 43. FFT for 20-MHz Input Signal

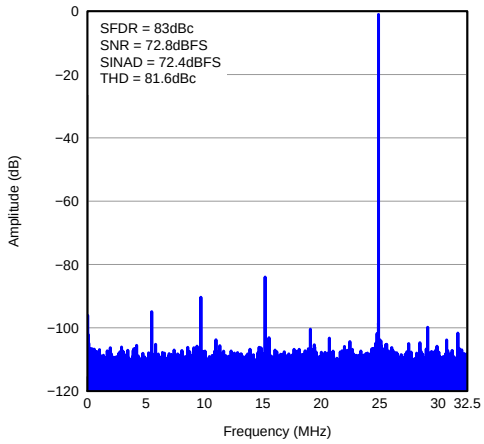


Figure 44. FFT for 170-MHz Input Signal

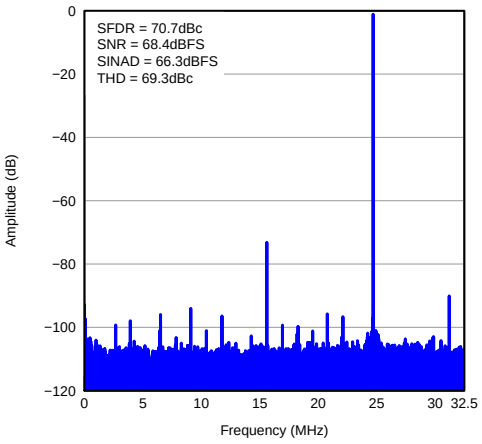


Figure 45. FFT for 300-MHz Input Signal

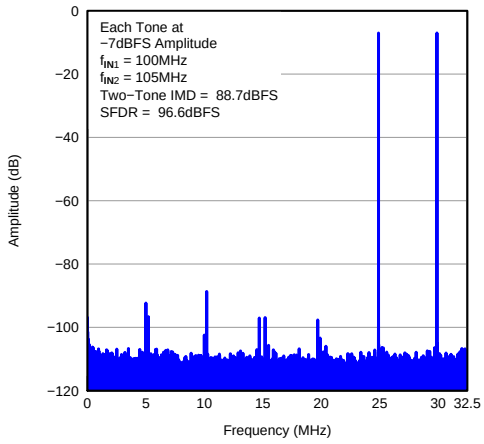


Figure 46. FFT for Two-Tone Input Signal

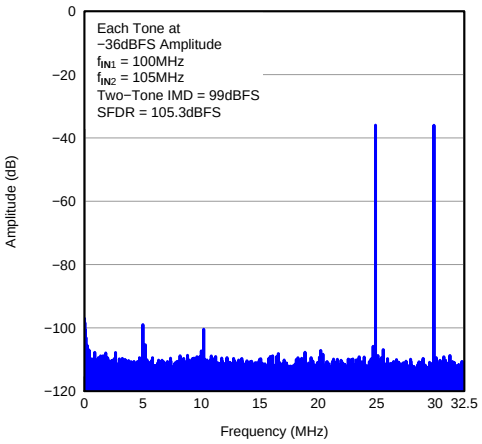


Figure 47. FFT for Two-Tone Input Signal

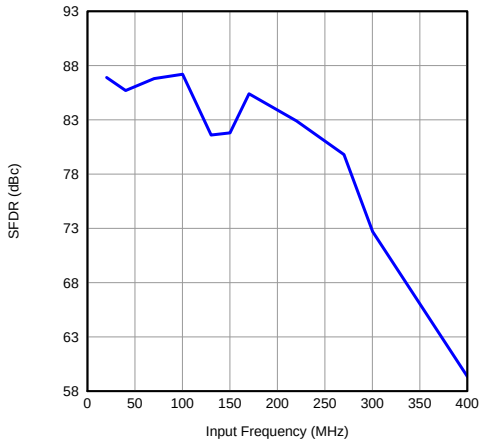


Figure 48. SFDR vs Input Frequency

Typical Characteristics: ADS4142 (continued)

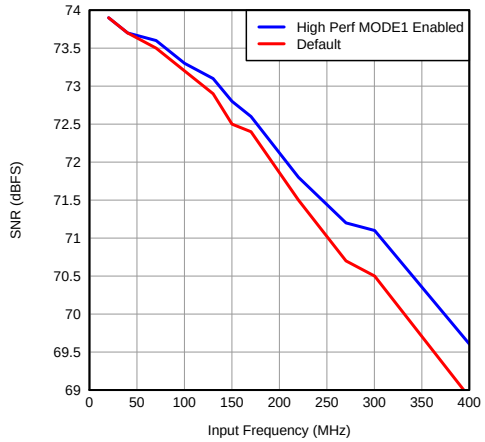


Figure 49. SNR vs Input Frequency

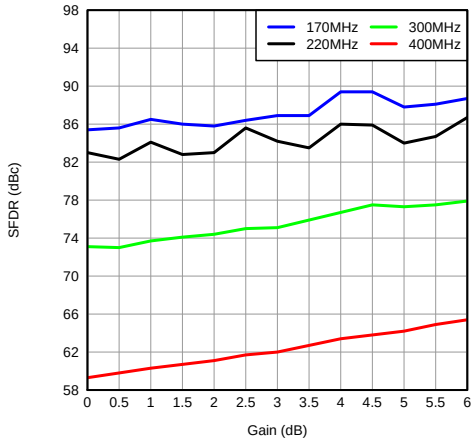


Figure 50. SFDR Across Gain and Input Frequency

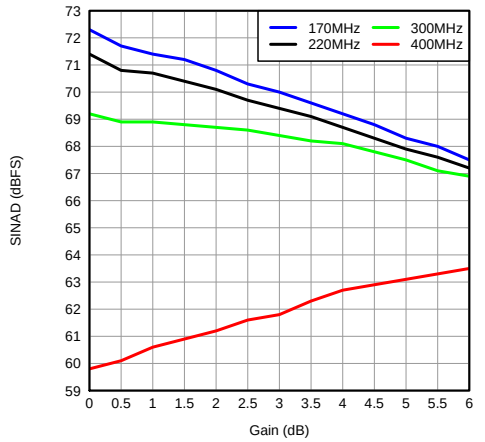


Figure 51. SINAD Across Gain and Input Frequency

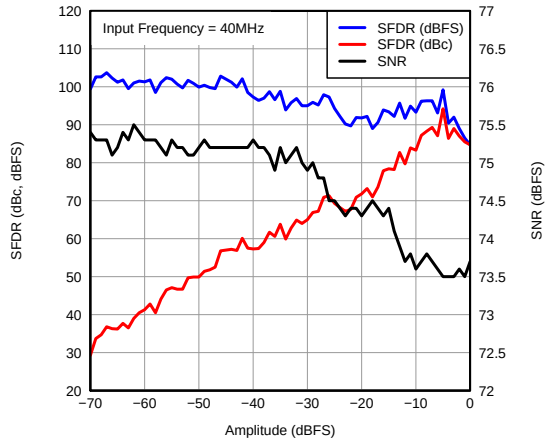


Figure 52. Performance Across Input Amplitude (Single Tone)

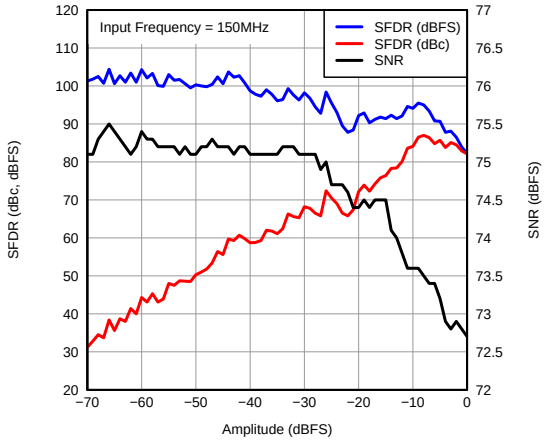


Figure 53. Performance Across Input Amplitude (Single Tone)

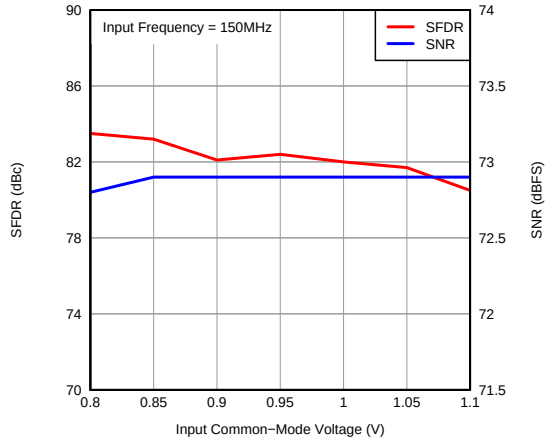


Figure 54. Performance vs Input Common-Mode Voltage

Typical Characteristics: ADS4142 (continued)

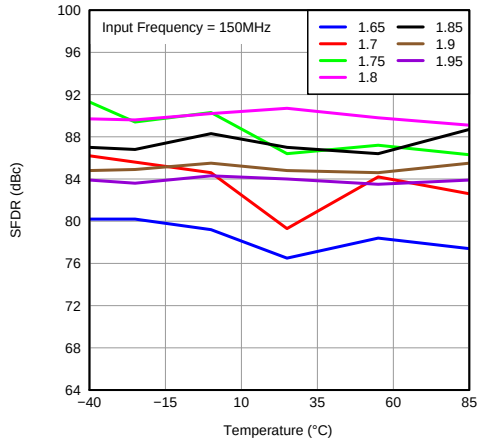


Figure 55. SFDR Across Temperature vs AVDD Supply

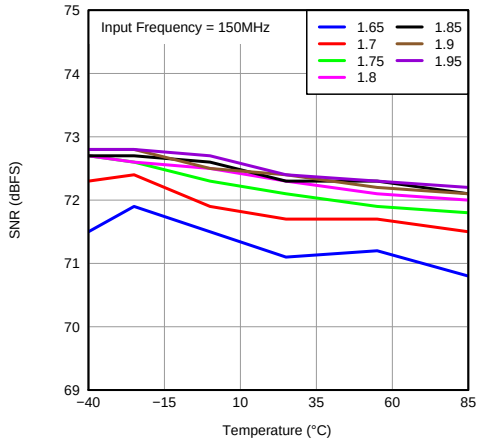


Figure 56. SNR Across Temperature vs AVDD Supply

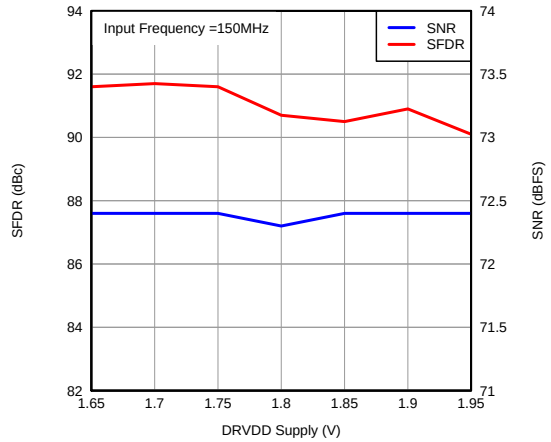


Figure 57. Performance Across DRVDD Supply Voltage

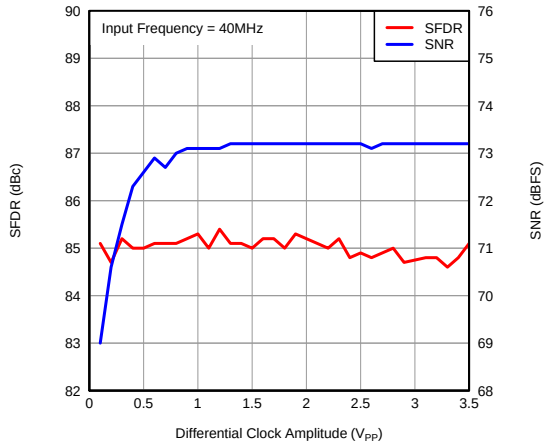


Figure 58. Performance Across Input Clock Amplitude

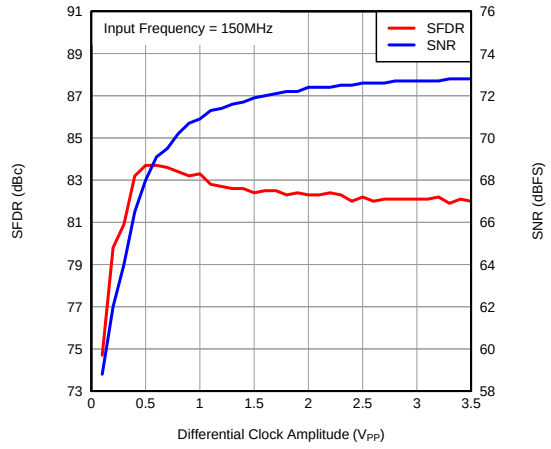


Figure 59. Performance Across Input Clock Amplitude

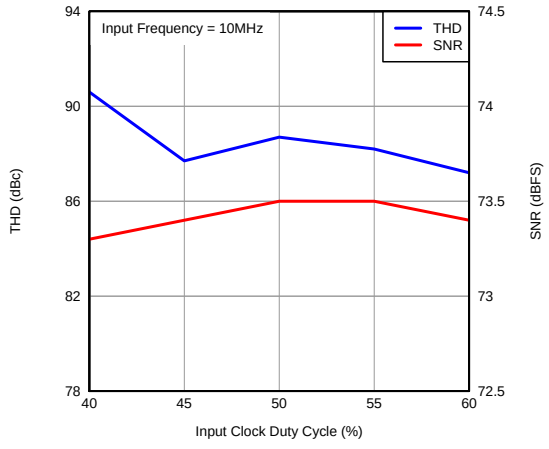


Figure 60. Performance Across Input Clock Duty Cycle

Typical Characteristics: ADS4142 (continued)

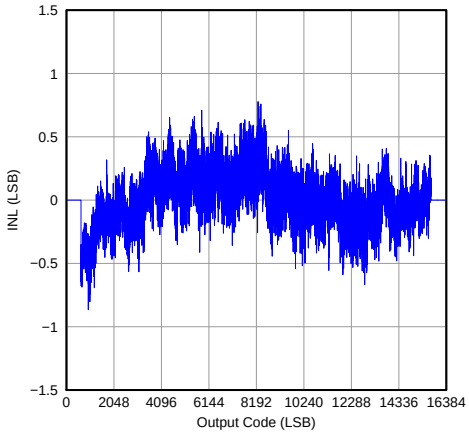


Figure 61. Integral Nonlinearity

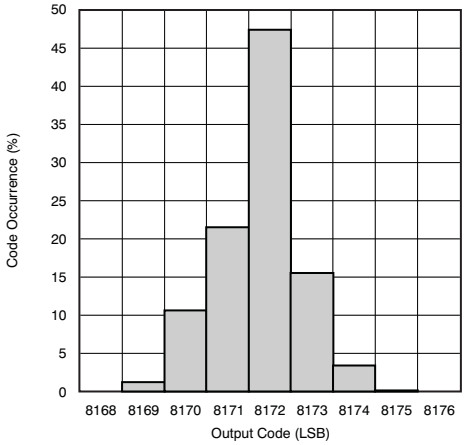


Figure 62. Output Noise Histogram (with Inputs Shorted to VCM)

7.13.4 Typical Characteristics: ADS4145

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

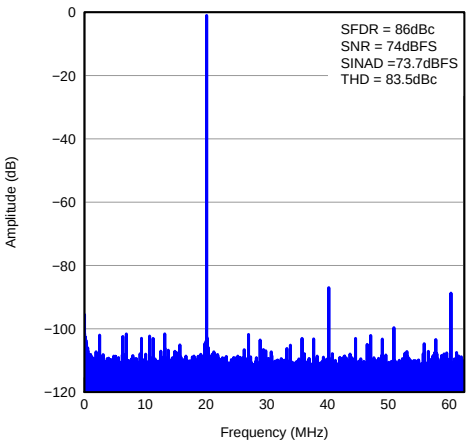


Figure 63. FFT for 20-MHz Input Signal

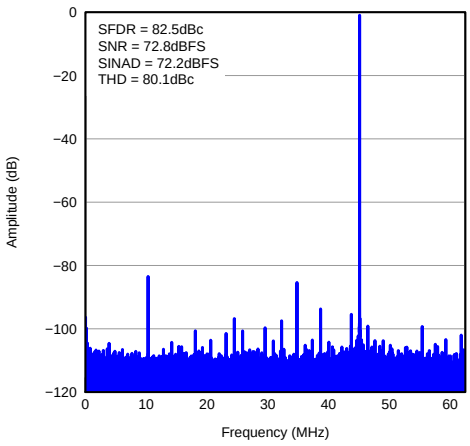


Figure 64. FFT for 170-MHz Input Signal

Typical Characteristics: ADS4145 (continued)

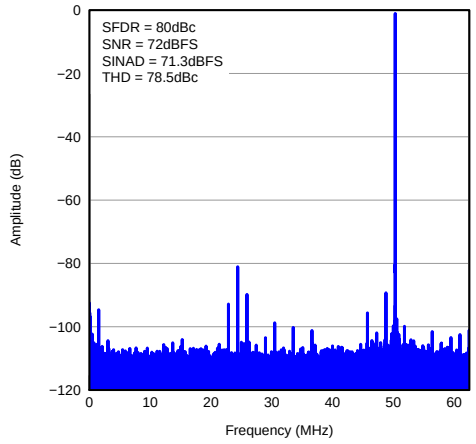


Figure 65. FFT for 300-MHz Input Signal

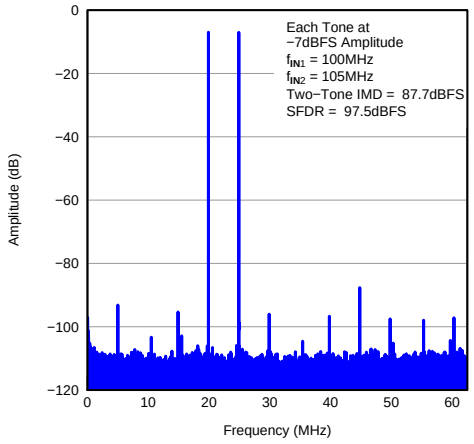


Figure 66. FFT for Two-Tone Input Signal

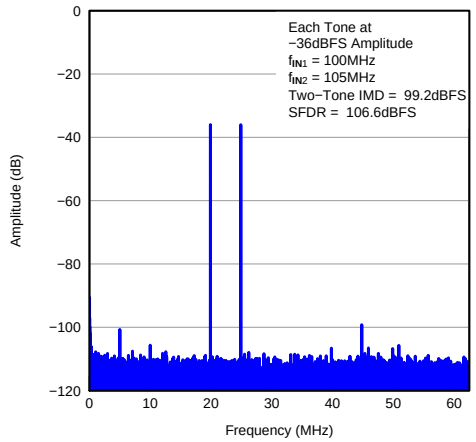


Figure 67. FFT for Two-Tone Input Signal

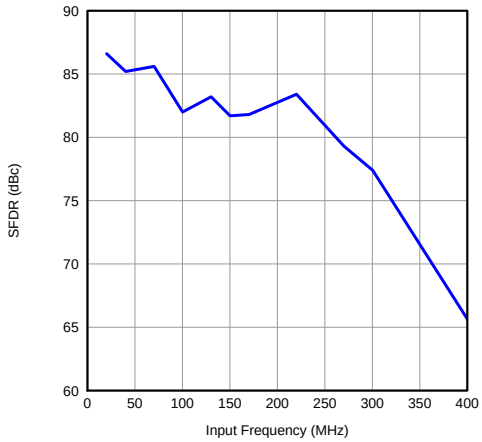


Figure 68. SFDR vs Input Frequency

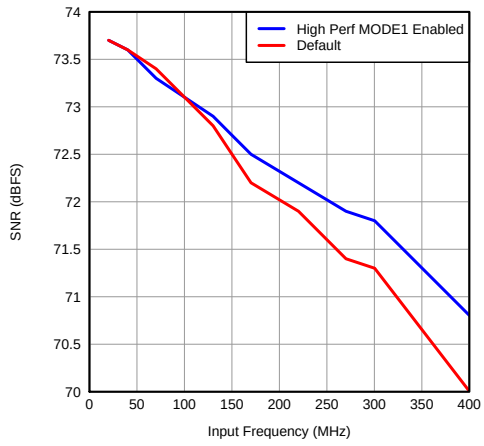


Figure 69. SNR vs Input Frequency

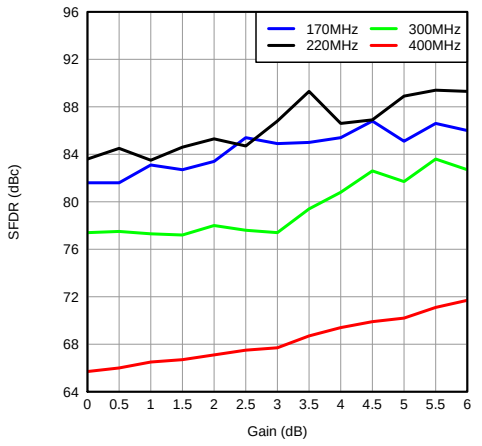


Figure 70. SFDR Across Gain and Input Frequency

Typical Characteristics: ADS4145 (continued)

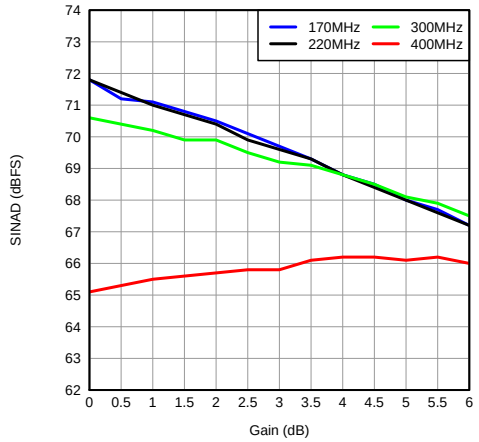


Figure 71. SINAD Across Gain and Input Frequency

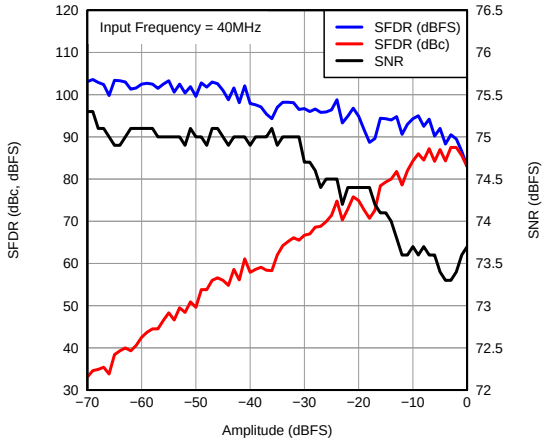


Figure 72. Performance Across Input Amplitude (Single Tone)

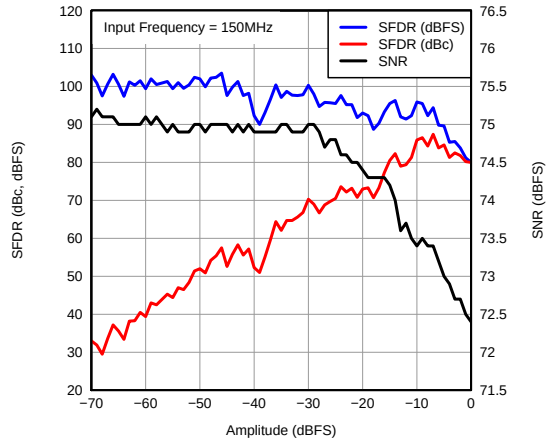


Figure 73. Performance Across Input Amplitude (Single Tone)

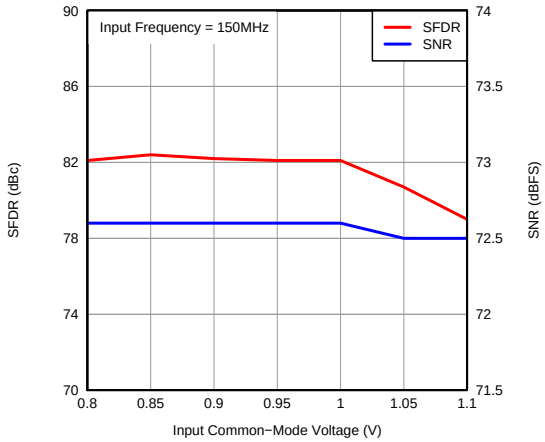


Figure 74. Performance vs Input Common-Mode Voltage

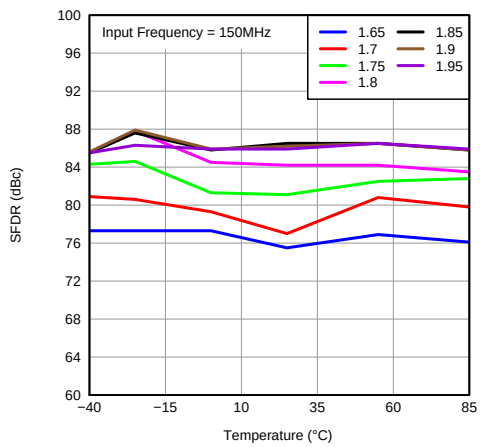


Figure 75. SFDR Across Temperature vs AVDD Supply

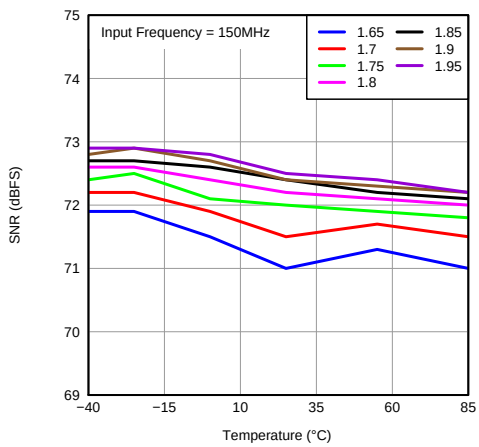


Figure 76. SNR Across Temperature vs AVDD Supply

Typical Characteristics: ADS4145 (continued)

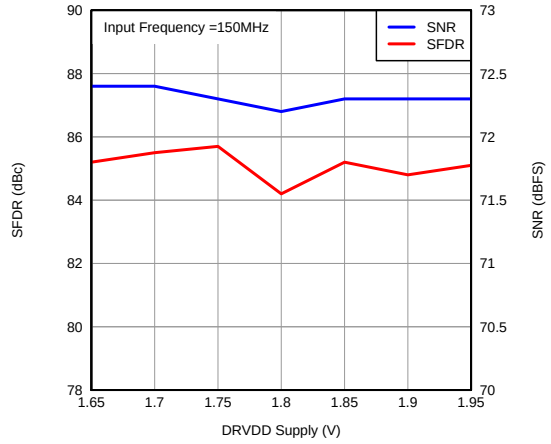


Figure 77. Performance Across DRVDD Supply Voltage

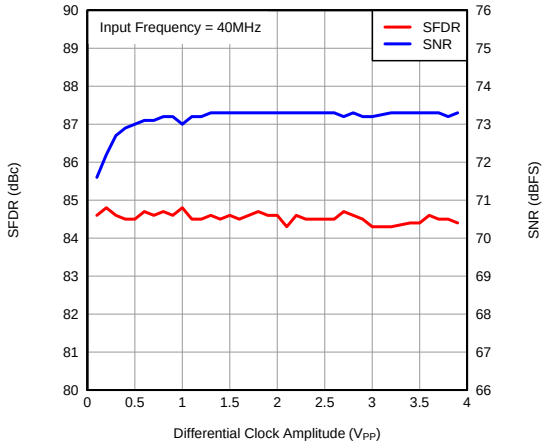


Figure 78. Performance Across Input Clock Amplitude

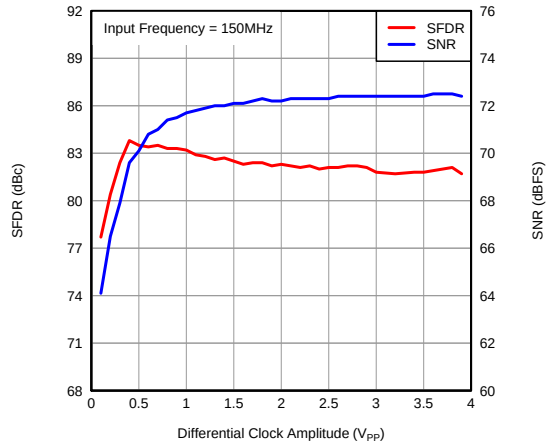


Figure 79. Performance Across Input Clock Amplitude

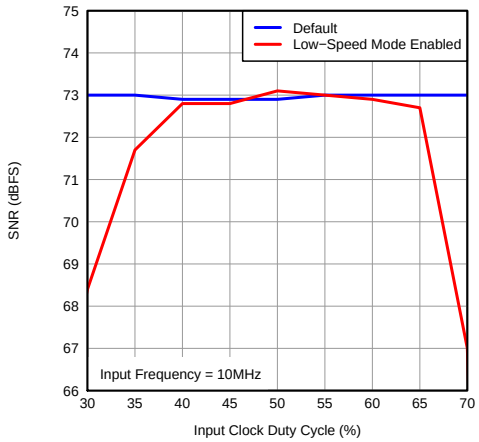


Figure 80. SNR Across Input Clock Duty Cycle

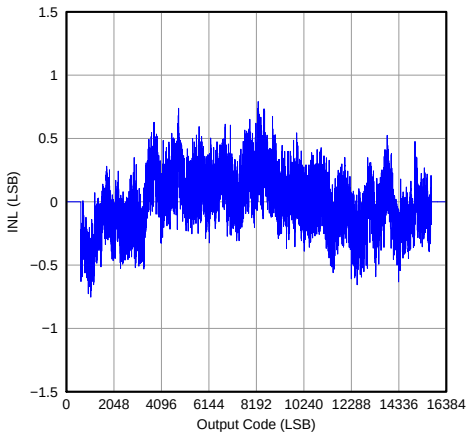


Figure 81. Integral Nonlinearity

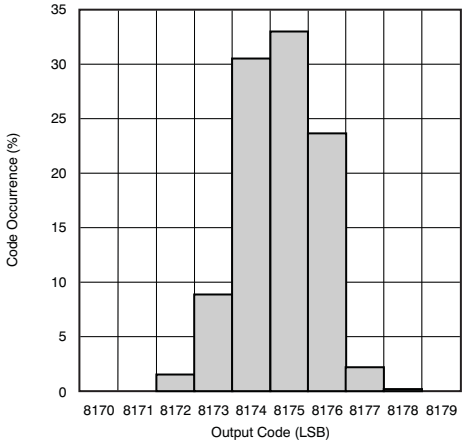


Figure 82. Output Noise Histogram (With Inputs Shorted to VCM)

7.13.5 Typical Characteristics: Common

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

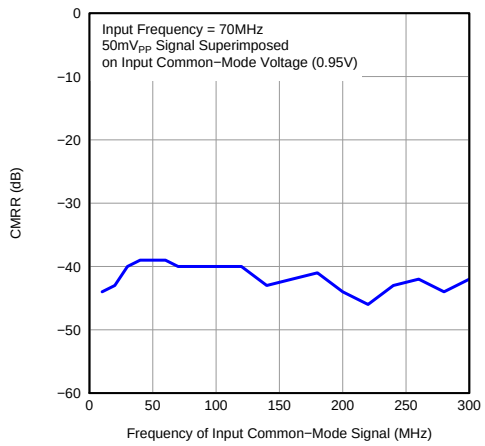


Figure 83. CMRR vs Frequency

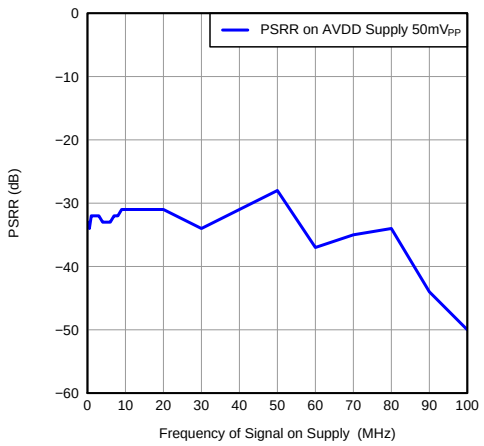


Figure 84. PSRR vs Frequency

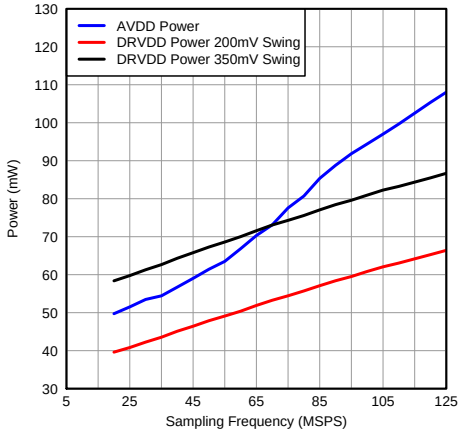


Figure 85. Power vs Sample Rate

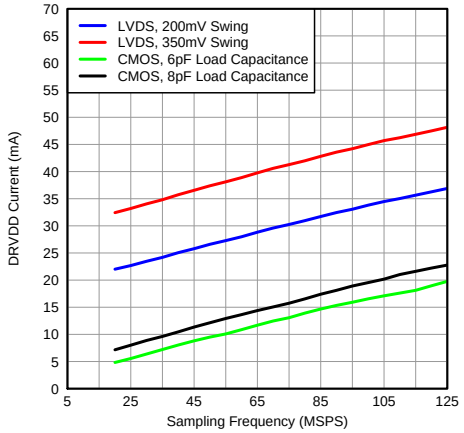


Figure 86. DRVDD Current vs Sample Rate

7.13.6 Typical Characteristics: Contour

At 25°C, AVDD = 1.8 V, DRVDD = 1.8 V, maximum rated sampling frequency, sine wave input clock, 1.5-V_{PP} differential clock amplitude, 50% clock duty cycle, –1-dBFS differential analog input, 0-dB gain, low-latency mode, DDR LVDS output interface, and 32k-point FFT, unless otherwise noted.

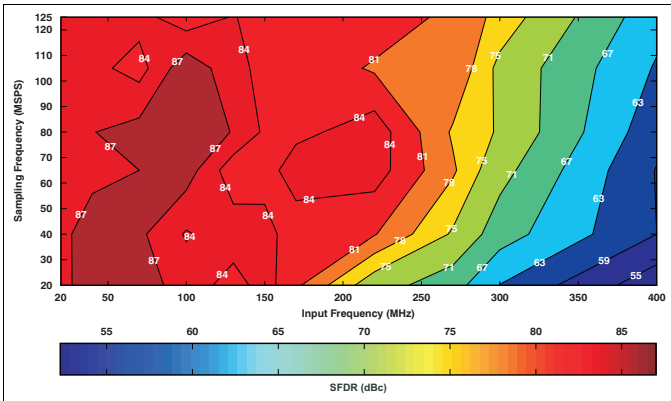


Figure 87. SFDR Across Input and Sampling Frequencies (0-dB Gain)

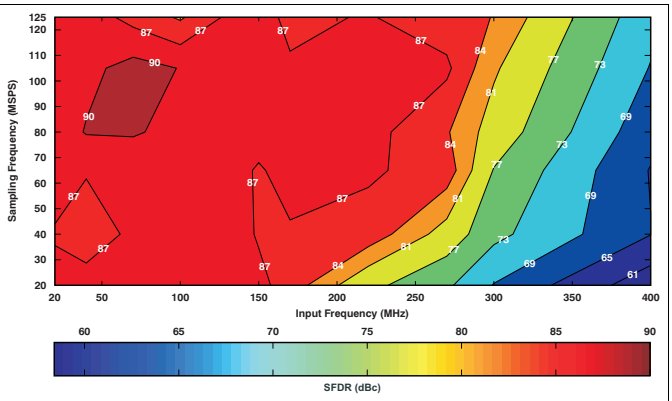


Figure 88. SFDR Across Input and Sampling Frequencies (6-dB Gain)

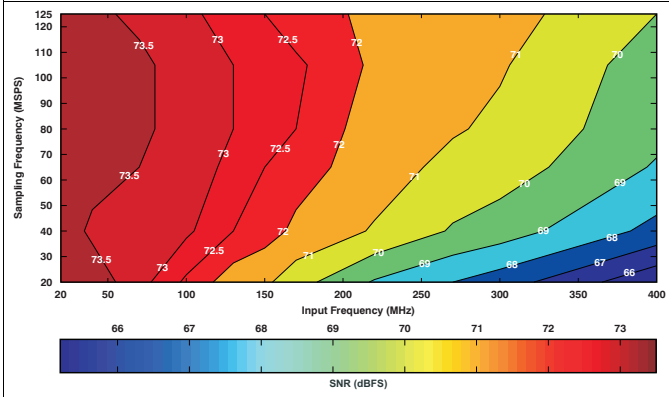


Figure 89. ADS414x: SNR ACROSS Input and Sampling Frequencies (0-dB Gain)

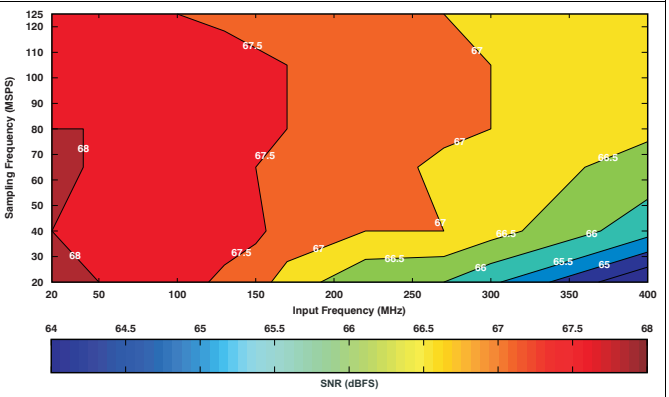


Figure 90. ADS414x: SNR Across Input and Sampling Frequencies (6-dB Gain)

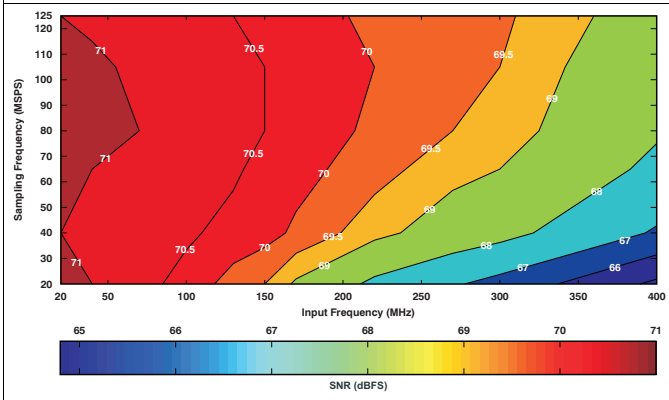


Figure 91. ADS412x SNR Across Input and Sampling Frequencies (0-dB Gain)

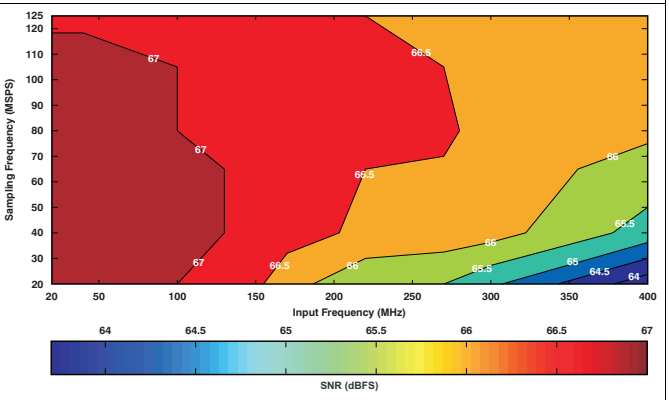


Figure 92. ADS412x SNR Across Input and Sampling Frequencies (6-dB Gain)

8 Detailed Description

8.1 Overview

The ADS412x and ADS414x devices are high-performance, low-power, 12-bit and 14-bit analog-to-digital converters (ADC) with maximum sampling rates up to 65/125 MSPS. The conversion process is initiated by a rising edge of the external input clock when the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline, resulting in a data latency of 10 clock cycles. The output is available as 12-bit and 14-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

The ADS412x and ADS414x family is pin-compatible to the previous generation ADS6149 family; this architecture enables easy migration. However, there are some important differences between the generations, summarized in Table 1.

Table 1. Migrating from the ADS6149 Family

ADS6149 FAMILY	ADS4145 FAMILY
PINS	
Pin 21 is NC (not connected)	Pin 21 is NC (not connected)
Pin 23 is MODE	Pin 23 is RESERVED in the ADS4145 family. It is reserved as a digital control pin for an (as yet) undefined function in the next-generation ADC series.
SUPPLY	
AVDD is 3.3 V	AVDD is 1.8 V
DRVDD is 1.8 V	No change
INPUT COMMON-MODE VOLTAGE	
VCM is 1.5 V	VCM is 0.95 V
SERIAL INTERFACE	
Protocol: 8-bit register address and 8-bit register data	No change in protocol
	New serial register map
EXTERNAL REFERENCE MODE	
Supported	Not supported
ADS61B49 FAMILY	**ADS41B29/B49/ADS58B18 FAMILY**
PINS	
Pin 21 is NC (not connected)	Pin 21 is 3.3 V AVDD_BUF (supply for the analog input buffers)
Pin 23 is MODE	Pin 23 is a digital control pin for the RESERVED function. Pin 23 functions as SNR Boost enable (B18 only).
SUPPLY	
AVDD is 3.3 V	AVDD is 1.8 V, AVDD_BUF is 3.3 V
DRVDD is 1.8 V	No change
INPUT COMMON-MODE VOLTAGE	
VCM is 1.5 V	VCM is 1.7 V
SERIAL INTERFACE	
Protocol: 8-bit register address and 8-bit register data	No change in protocol New serial register map
EXTERNAL REFERENCE MODE	
Supported	Not supported

8.2 Functional Block Diagrams

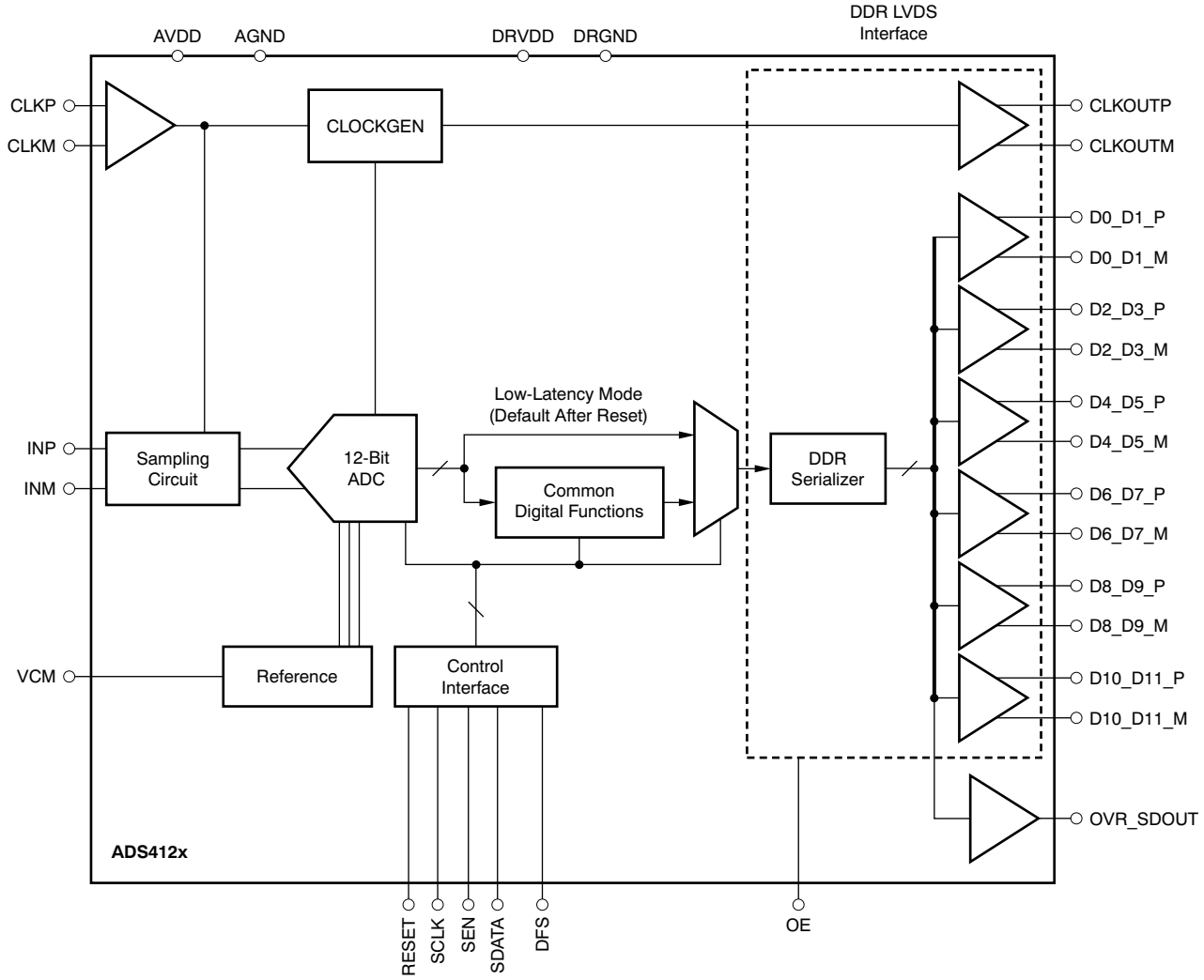


Figure 93. ADS412x Block Diagram

Functional Block Diagrams (continued)

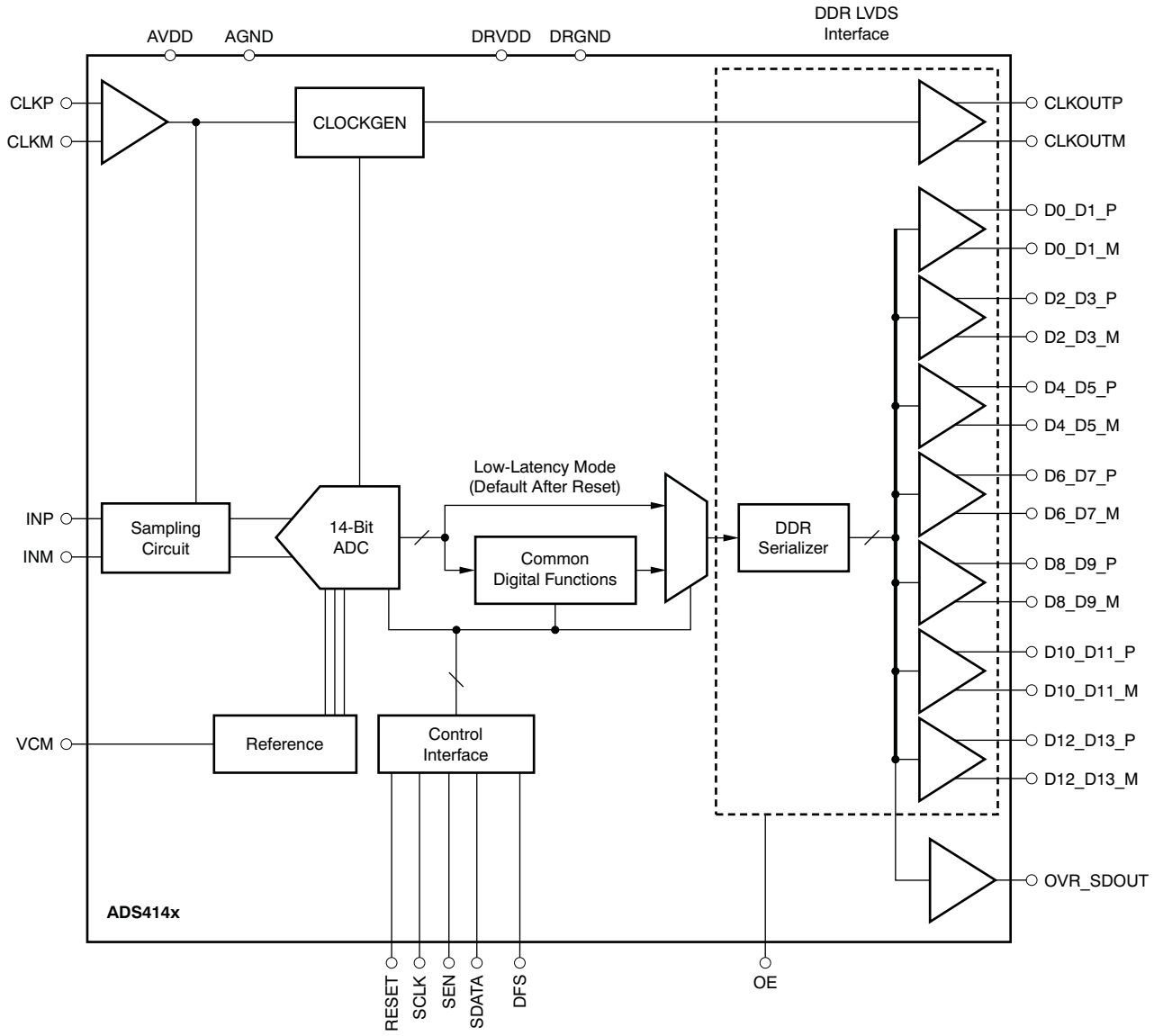


Figure 94. ADS414x Block Diagram

8.3 Feature Description

8.3.1 Digital Functions and Low Latency Mode

The device has several useful digital functions such as test patterns, gain, and offset correction. All of these functions require extra clock cycles for operation and increase the overall latency and power of the device. Alternately, the device has a low-latency mode in which the raw ADC output is routed to the output data pins with a latency of 10 clock cycles. In this mode, the digital functions are bypassed. Figure 95 shows more details of the processing after the ADC.

The device is in low-latency mode after reset. In order to use any of the digital functions, the low-latency mode must first be disabled by setting the DIS LOW LATENCY register bit to 1. After this, the respective register bits must be programmed as described in the following sections and in the *Serial Register Map* section.

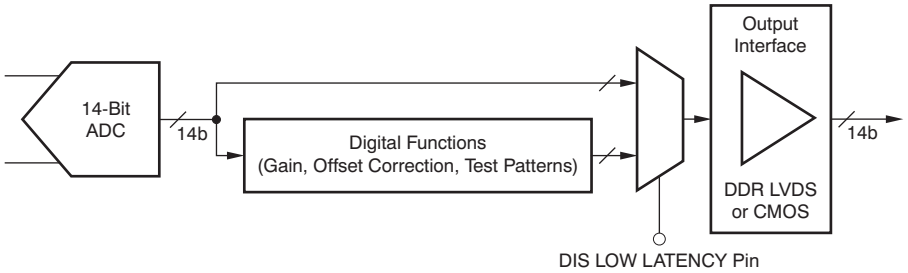


Figure 95. Digital Processing Block Diagram

8.3.2 Gain for SFDR/SNR Trade-Off

The ADS412x and ADS414x include gain settings that can be used to improve SFDR performance. The gain is programmable from 0 dB to 6 dB (in 0.5-dB steps) using the GAIN register bits. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 2.

The SFDR improvement is achieved at the expense of SNR; for each gain setting, the SNR degrades approximately between 0.5 dB and 1 dB. The SNR degradation is reduced at high input frequencies. As a result, the gain is very useful at high input frequencies because the SFDR improvement is significant with marginal degradation in SNR. Therefore, the gain can be used to trade-off between SFDR and SNR.

After a reset, the device is in low-latency mode and gain function is disabled. To use gain:

- First, disable the low-latency mode (DIS LOW LATENCY = 1).
- This setting enables the gain and puts the device in a 0-dB gain mode.
- For other gain settings, program the GAIN bits.

Table 2. Full-Scale Range Across Gains

GAIN (dB)	TYPE	FULL-SCALE (V_{PP})
0	Default after reset	2
1	Programmable	1.78
2	Programmable	1.59
3	Programmable	1.42
4	Programmable	1.26
5	Programmable	1.12
6	Programmable	1

8.3.3 Offset Correction

The ADS412x and ADS414x has an internal offset corretion algorithm that estimates and corrects DC offset up to ±10 mV. The correction can be enabled using the EN OFFSET CORR serial register bit. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using the OFFSET CORR TIME CONSTANT register bits, as described in Table 3.

Table 3. Time Constant of Offset Correction Loop

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (sec)(1)
0000	1M	8 ms
0001	2M	16 ms
0010	4M	33.4 ms
0011	8M	67 ms
0100	16M	134 ms
0101	32M	268 ms

(1) Sampling frequency, f_S = 125 MSPS.

Table 3. Time Constant of Offset Correction Loop (continued)

OFFSET CORR TIME CONSTANT	TIME CONSTANT, TC_{CLK} (Number of Clock Cycles)	TIME CONSTANT, $TC_{CLK} \times 1/f_S$ (sec)(1)
0110	64M	537 ms
0111	128M	1.08 s
1000	256M	2.15 s
1001	512M	4.3 s
1010	1G	8.6 s
1011	2G	17.2 s
1100	Reserved	—
1101	Reserved	—
1110	Reserved	—
1111	Reserved	—

After the offset is estimated, the correction can be frozen by setting FREEZE OFFSET CORR = 1. Once frozen, the last estimated value is used for the offset correction of every clock cycle. Note that offset correction is disabled by a default after reset.

After a reset, the device is in low-latency mode and offset correction is disabled. To use offset correction:

- First, disable the low-latency mode (DIS LOW LATENCY = 1).
- Then set EN OFFSET CORR to 1 and program the required time constant.

Figure 96 shows the time response of the offset correction algorithm after it is enabled.

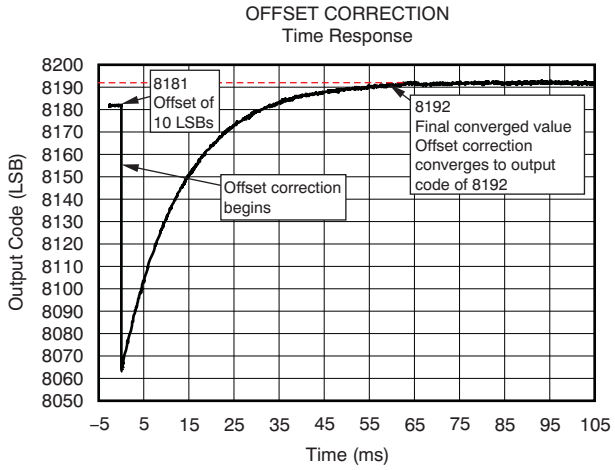


Figure 96. Time Response of Offset Correction

8.3.4 Power Down

The ADS412x and ADS414x has three power-down modes: power-down global, standby, and output buffer disable.

8.3.4.1 Power-Down Global

In this mode, the entire chip (including the ADC, internal reference, and the output buffers) are powered down, resulting in reduced total power dissipation of about 10 mW. The output buffers are in a high-impedance state. The wake-up time from the global power-down to data becoming valid in normal mode is typically 100 µs. To enter the global power-down mode, set the PDN GLOBAL register bit.

8.3.4.2 Standby

In this mode, only the ADC is powered down and the internal references are active, resulting in a fast wake-up time of 5 µs. The total power dissipation in standby mode is approximately 130 mW at 125 MSPS. To enter the standby mode, set the STBY register bit.

8.3.4.3 Output Buffer Disable

The output buffers can be disabled and put in a high-impedance state; wake-up time from this mode is fast, approximately 100 ns. This can be controlled using the PDN OBUF register bit or using the OE pin.

8.3.4.4 Input Clock Stop

In addition, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is approximately 80 mW.

8.3.5 Output Data Format

Two output data formats are supported: twos complement and offset binary. Each mode can be selected using the DATA FORMAT serial interface register bit or controlling the DFS pin in parallel configuration mode. In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level.

8.4 Device Functional Modes

8.4.1 Digital Output Information

The ADS412x and ADS414x provide either 14-bit data or 12-bit data, respectively, and an output clock synchronized with the data.

8.4.1.1 Output Interface

Two output interface options are available: double data rate (DDR) LVDS and parallel CMOS. They can be selected using the LVDS CMOS serial interface register bit or using the DFS pin.

8.4.1.2 DDR LVDS Outputs

In this mode, the data bits and clock are output using low voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 97 and Figure 98.

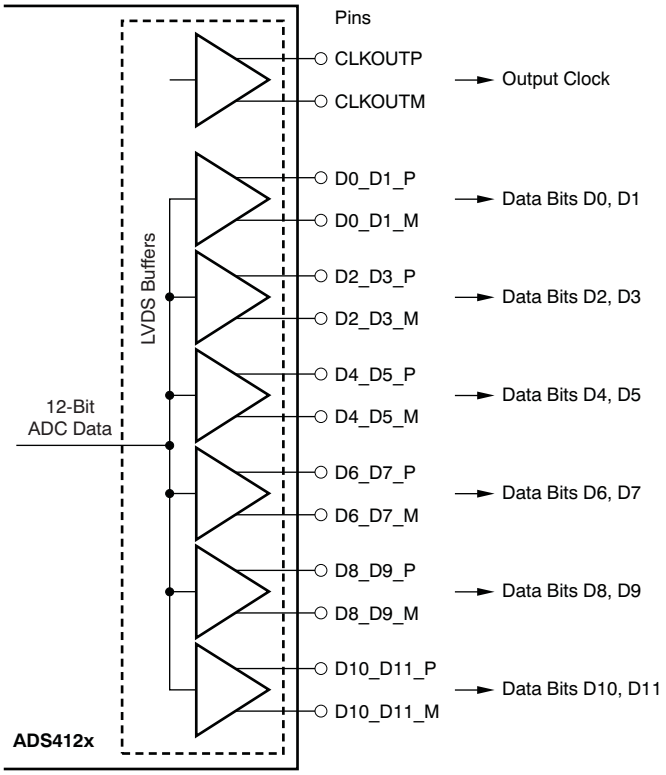


Figure 97. ADS412x LVDS Data Outputs

Device Functional Modes (continued)

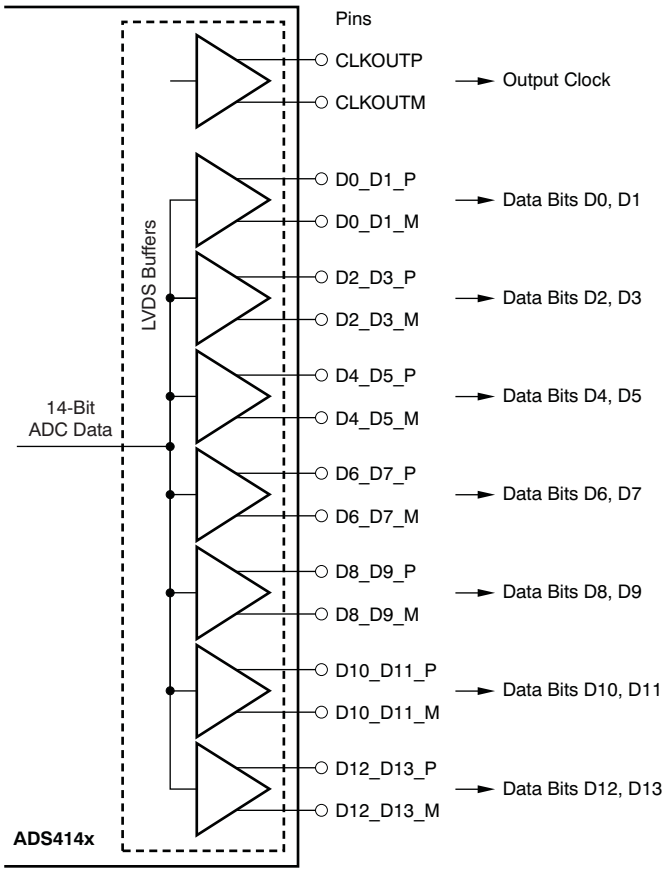


Figure 98. ADS414x LVDS Data Outputs

Even data bits (D0, D2, D4, and so forth) are output at the falling edge of CLKOUTP and the odd data bits (D1, D3, D5, and so forth) are output at the rising edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all 14 data bits, as shown in Figure 99.

Device Functional Modes (continued)

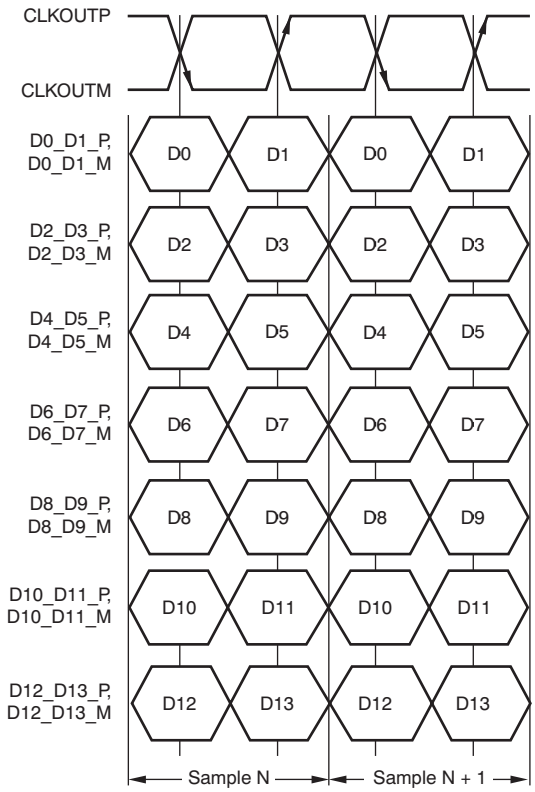


Figure 99. DDR LVDS Interface

8.4.1.3 LVDS Output Data and Clock Buffers

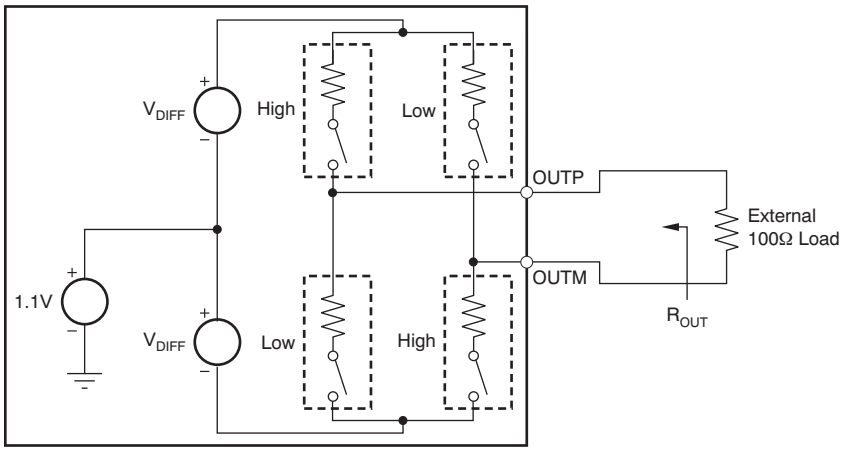
The equivalent circuit of each LVDS output buffer is shown in Figure 100. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100-Ω termination.

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled using the LVDS DATA STRENGTH and LVDS CLKOUT STRENGTH register bits for data and output clock buffers, respectively.

The buffer output impedance behaves in the same way as a source-side series termination. By absorbing reflections from the receiver end, it helps to improve signal integrity.

Device Functional Modes (continued)



Use the default buffer strength to match 100-Ω external termination (R_{OUT} = 100 Ω). To match with a 50-Ω external termination, set the LVDS STRENGTH bit (R_{OUT} = 50 Ω).

Figure 100. LVDS Buffer Equivalent Circuit

8.4.1.4 Parallel CMOS Interface

In CMOS mode, each data bit is output on a separate pin as the CMOS voltage level, for every clock cycle. The rising edge of the output clock CLKOUT can be used to latch data in the receiver. Figure 101 depicts the CMOS output interface.

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs and degrade SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this degradation, the CMOS output buffers are designed with controlled drive strength. The default drive strength ensures a wide data stable window. It is recommended to use short traces (one to two inches or 2.54 cm to 5.08 cm) terminated with less than 5-pF load capacitance, as shown in Figure 102.

Device Functional Modes (continued)

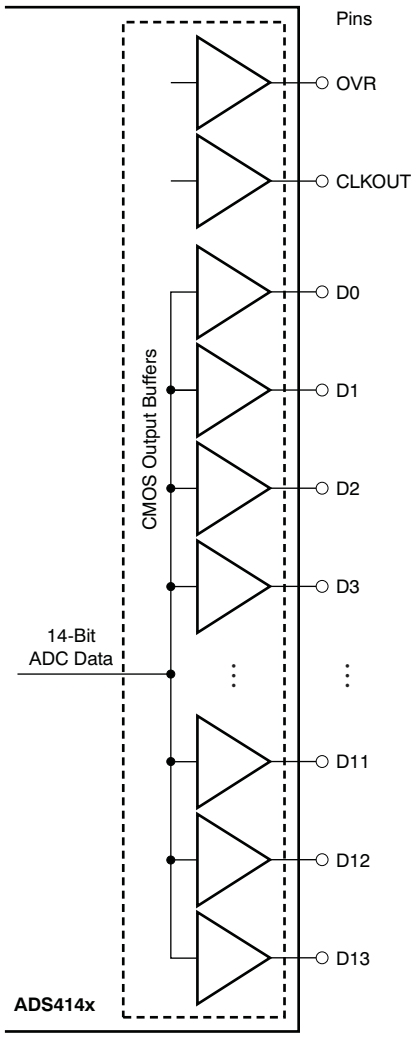


Figure 101. CMOS Output Interface

Device Functional Modes (continued)

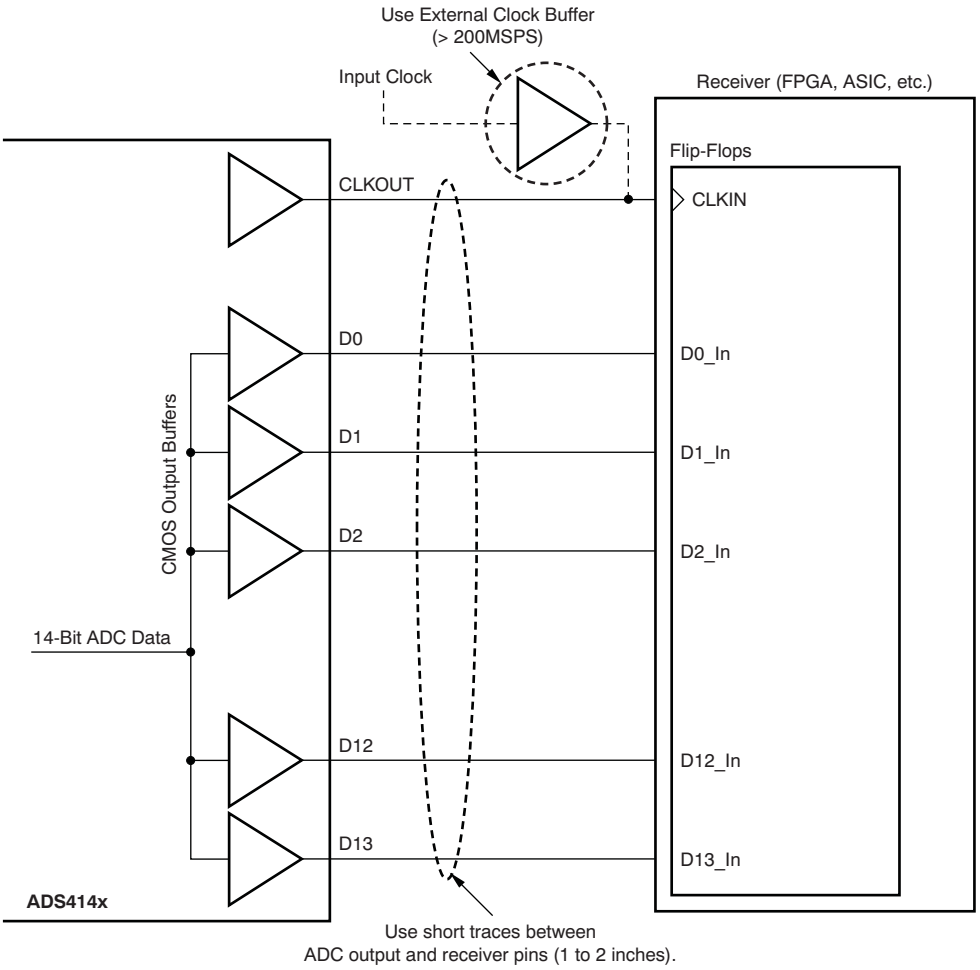


Figure 102. Using the CMOS Data Outputs

8.4.1.5 CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

Digital Current as a Result of CMOS Output Switching = $C_L \times DRVDD \times (N \times f_{AVG})$

where:

C_L = load capacitance,

$N \times F_{AVG}$ = average number of output bits switching. (1)

Figure 86 details the current across sampling frequencies at 2-MHz analog input frequency.

8.5 Programming

8.5.1 Device Configuration

The ADS412x and ADS414x have several modes that can be configured using a serial programming interface, as described in Table 4, Table 5, and Table 6. In addition, the devices have two dedicated parallel pins for quickly configuring commonly used functions. The parallel pins are DFS (analog 4-level control pin) and OE (digital control pin). The analog control pins can be easily configured using a simple resistor divider (with 10% tolerance resistors).

Table 4. DFS: Analog Control Pin

VOLTAGE APPLIED ON DFS	DESCRIPTION (Data Format/Output Interface)
0, 100 mV/–0 mV	Twos complement/DDR LVDS
(3/8) AVDD ± 100 mV	Twos complement/parallel CMOS
(5/8) AVDD ± 100 mV	Offset binary/parallel CMOS
AVDD, 0 mV/–100 mV	Offset binary/DDR LVDS

Table 5. OE: Digital Control Pin

VOLTAGE APPLIED ON OE	DESCRIPTION
0	Output data buffers disabled
AVDD	Output data buffers enabled

When the serial interface is not used, the SDATA pin can also be used as a digital control pin to place the device in standby mode. To enable this, the RESET pin must be tied high. In this mode, SEN and SCLK do not have any alternative functions. Keep SEN tied high and SCLK tied low on the board.

Table 6. SDATA: Digital Control Pin

VOLTAGE APPLIED ON SDATA	DESCRIPTION
0	Normal operation
Logic high	Device enters standby

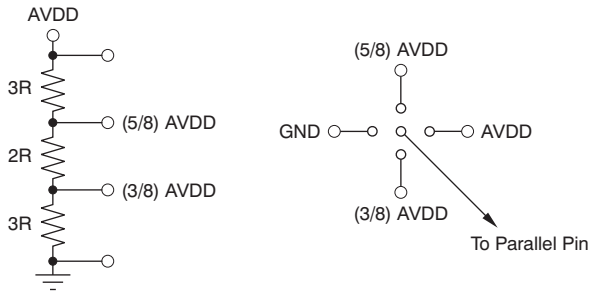


Figure 103. Simplified Diagram to Configure DFS Pin

8.5.2 Serial Interface

The analog-to-digital converter (ADC) has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), and SDATA (serial interface data) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every falling edge of SCLK when SEN is active (low). The serial data are loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The first eight bits form the register address and the remaining eight bits are the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (a few hertz) and also with non-50% SCLK duty cycle.

8.5.2.1 Register Initialization

After power-up, the internal registers must be initialized to the default values. This initialization can be accomplished in one of two ways:

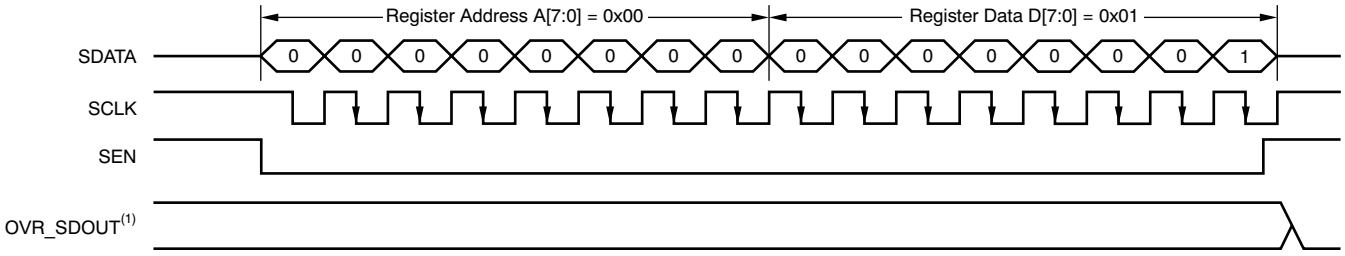
1. Either through hardware reset by applying a high pulse on RESET pin (of width greater than 10 ns), as shown in Figure 5; or
2. By applying a software reset. When using the serial interface, set the RESET bit (D7 in register 00h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

8.5.3 Serial Register Readout

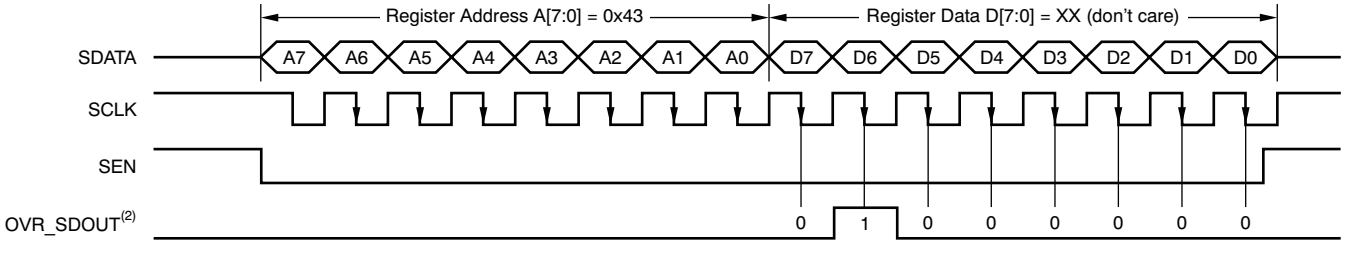
The serial register readout function allows the contents of the internal registers to be read back on the OVR_SDOUT pin. This readback may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

After power-up and device reset, the OVR_SDOUT pin functions as an over-range indicator pin by default. When the readout mode is enabled, OVR_SDOUT outputs the contents of the selected register serially:

1. Set the READOUT register bit to 1. This setting puts the device in serial readout mode and disables any further writes to the internal registers **except** the register at address 0. Note that the READOUT bit itself is also located in register 0. The device can exit readout mode by writing READOUT = 0. Only the contents of the register at address 0 cannot be read in the register readout mode.
2. Initiate a serial interface cycle specifying the address of the register (A7 to A0) whose content has to be read.
3. The device serially outputs the contents (D7 to D0) of the selected register on the OVR_SDOUT pin.
4. The external controller can latch the contents at the falling edge of SCLK.
5. To exit the serial readout mode, the reset register bit READOUT = 0 enables writes into all registers of the device. At this point, the OVR_SDOUT pin becomes an over-range indicator pin.



a) Enable Serial Readout (READOUT = 1)



b) Read Contents of Register 0x43. This Register Has Been Initialized with 0x40 (device is put into global power-down mode).

(1) The OVR_SDOUT pin finctions as OVR (READOUT = 0).

(2) The OVR_SDOUT pin finctions as a serial readout (READOUT = 1).

Figure 104. Serial Readout Timing Diagram

8.6 Register Maps

8.6.1 Serial Register Map

Table 7 summarizes the functions supported by the serial interface.

Table 7. Serial Interface Register Map(1)

REGISTER ADDRESS	DEFAULT VALUE AFTER RESET	REGISTER DATA							
A[7:0] (Hex)	D[7:0] (Hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	00	0	0	0	0	0	0	RESET	READOUT
01	00	LVDS SWING						0	0
03	00	0	0	0	0	0	0	HIGH PERF MODE 1	
25	00	GAIN				DISABLE GAIN	TEST PATTERNS		
26	00	0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH
3D	00	DATA FORMAT		EN OFFSET CORR	0	0	0	0	0
3F	00	CUSTOM PATTERN HIGH D[13:6]							
40	00	CUSTOM PATTERN D[5:0]						0	0
41	00	LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL
42	00	CLKOUT FALL POSN		0	0	DIS LOW LATENCY	STBY	0	0
43	00	0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	
4A	00	0	0	0	0	0	0	0	HIGH PERF MODE 2
BF	00	OFFSET PEDESTAL						0	0
CF	00	FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0
DF	00	0	0	LOW SPEED		0	0	0	0

(1) Multiple functions in a register can be programmed in a single write operation.

8.6.2 Description of Serial Registers

For best performance, two special mode register bits must be enabled: HI PERF MODE 1 and HI PERF MODE 2.

Table 8. Register Address 00h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	RESET	READOUT

Bits[7:2] Always write '0'

Bit 1 RESET: Software reset applied

This bit resets all internal registers to the default values and self-clears to 0 (default = 1).

Bit 0 READOUT: Serial readout

This bit sets the serial readout of the registers.
0 = Serial readout of registers disabled; the OVR_SDOUT pin functions as an over-voltage indicator.
1 = Serial readout enabled; the OVR_SDOUT pin functions as a serial data readout.

Table 9. Register Address 01h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS SWING						0	0

Bits[7:2] LVDS SWING: LVDS swing programmability(1)

000000 = Default LVDS swing; ±350 mV with external 100-Ω termination
011011 = LVDS swing *increases* to ±410 mV
110010 = LVDS swing *increases* to ±465 mV
010100 = LVDS swing *increases* to ±570 mV
111110 = LVDS swing *decreases* to ±200 mV
001111 = LVDS swing *decreases* to ±125 mV

Bits[1:0] Always write '0'

(1) The EN LVDS SWING register bits must be set to enable LVDS swing control.

Table 10. Register Address 03h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HI PERF MODE 1	

Bits[7:2] Always write '0'

Bits[1:0] HI PERF MODE 1: High performance mode 1

00 = Default performance after reset
01 = Do not use
10 = Do not use
11 = For best performance across sampling clock and input signal frequencies, set the HIGH PERF MODE 1 bits

Table 11. Register Address 25h (Default = 00h)

7	6	5	4	3	2	1	0
GAIN				DISABLE GAIN	TEST PATTERNS		

Bits[7:4] GAIN: Gain programmability

These bits set the gain programmability in 0.5dB steps.

0000 = 0-dB gain (default after reset)
0001 = 0.5-dB gain
0010 = 1.0-dB gain
0011 = 1.5-dB gain
0100 = 2.0-dB gain
0101 = 2.5-dB gain
0110 = 3.0-dB gain
0111 = 3.5-dB gain
1000 = 4.0-dB gain
1001 = 4.5-dB gain
1010 = 5.0-dB gain
1011 = 5.5-dB gain
1100 = 6-dB gain

Bit 3 DISABLE GAIN: Gain setting

This bit sets the gain.
0 = Gain enabled; gain is set by the GAIN bits only if low-latency mode is disabled
1 = Gain disabled

Bits[2:0] TEST PATTERNS: Data capture

These bits verify data capture.
000 = Normal operation
001 = Outputs all 0s
010 = Outputs all 1s
011 = Outputs toggle pattern

In the ADS4122/25, output data D[11:0] is an alternating sequence of *010101010101* and *101010101010*.
In the ADS4142/45, output data D[13:0] is an alternating sequence of *01010101010101* and *10101010101010*.

100 = Outputs digital ramp

In ADS4122/25, output data increments by one LSB (12-bit) every fourth clock cycle from code 0 to code 4095
In ADS4142/45, output data increments by one LSB (14-bit) every clock cycle from code 0 to code 16383

101 = Output custom pattern (use registers 3Fh and 40h for setting the custom pattern)
110 = Unused
111 = Unused

Table 12. Register Address 26h (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	LVDS CLKOUT STRENGTH	LVDS DATA STRENGTH

Bits[7:2] Always write '0'

Bit 1 LVDS CLKOUT STRENGTH: LVDS output clock buffer strength

This bit determines the external termination to be used with the LVDS output clock buffer.
0 = 100-Ω external termination (default strength)
1 = 50-Ω external termination (2x strength)

Bit 0 LVDS DATA STRENGTH: LVDS data buffer strength

This bit determines the external termination to be used with all of the LVDS data buffers.
0 = 100-Ω external termination (default strength)
1 = 50-Ω external termination (2x strength)

Table 13. Register Address 3Dh (Default = 00h)

7	6	5	4	3	2	1	0
DATA FORMAT		EN OFFSET CORR	0	0	0	0	0

Bits[7:6] DATA FORMAT: Data format selection

These bits selects the data format.
00 = The DFS pin controls data format selection
10 = Twos complement
11 = Offset binary

Bit 5 ENABLE OFFSET CORR: Offset correction setting

This bit sets the offset correction.
0 = Offset correction disabled
1 = Offset correction enabled

Bits[4:0] Always write '0'

Table 14. Register Address 3Fh (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D13	CUSTOM PATTERN D12	CUSTOM PATTERN D11	CUSTOM PATTERN D10	CUSTOM PATTERN D9	CUSTOM PATTERN D8	CUSTOM PATTERN D7	CUSTOM PATTERN D6

Bits[7:0] CUSTOM PATTERN(1)

These bits set the custom pattern.

(1) For the ADS414x, output data bits 13 to 0 are CUSTOM PATTERN D[13:0]. For the ADS412x, output data bits 11 to 0 are CUSTOM PATTERN D[13:2].

Table 15. Register Address 40h (Default = 00h)

7	6	5	4	3	2	1	0
CUSTOM PATTERN D5	CUSTOM PATTERN D4	CUSTOM PATTERN D3	CUSTOM PATTERN D2	CUSTOM PATTERN D1	CUSTOM PATTERN D0	0	0

Bits[7:2] CUSTOM PATTERN(1)

These bits set the custom pattern.

Bits[1:0] Always write '0'

(1) For the ADS414x, output data bits 13 to 0 are CUSTOM PATTERN D[13:0]. For the ADS412x, output data bits 11 to 0 are CUSTOM PATTERN D[13:2].

Table 16. Register Address 41h (Default = 00h)

7	6	5	4	3	2	1	0
LVDS CMOS		CMOS CLKOUT STRENGTH		EN CLKOUT RISE	CLKOUT RISE POSN		EN CLKOUT FALL

Bits[7:6] LVDS CMOS: Interface selection

These bits select the interface.
00 = The DFS pin controls the selection of either LVDS or CMOS interface
10 = The DFS pin controls the selection of either LVDS or CMOS interface
01 = DDR LVDS interface
11 = Parallel CMOS interface

Bits[5:4] CMOS CLKOUT STRENGTH

Controls strength of CMOS output clock only.
00 = Maximum strength (recommended and used for specified timings)
01 = Medium strength
10 = Low strength
11 = Very low strength

Bit 3 ENABLE CLKOUT RISE

0 = Disables control of output clock rising edge
1 = Enables control of output clock rising edge

Bits[2:1] CLKOUT RISE POSN: CLKOUT rise control

Controls position of output clock rising edge

LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 500 ps, hold increases by 500 ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200 ps, hold increases by 200 ps

CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 100 ps, hold increases by 100 ps
10 = Setup reduces by 200 ps, hold increases by 200 ps
11 = Setup reduces by 1.5 ns, hold increases by 1.5 ns

Bit 0 ENABLE CLKOUT FALL

0 = Disables control of output clock fall edge
1 = Enables control of output clock fall edge

Table 17. Register Address 42h (Default = 00h)

7	6	5	4	3	2	1	0
CLKOUT FALL CTRL		0	0	DIS LOW LATENCY	STBY	0	0

Bits[7:6] CLKOUT FALL CTRL

Controls position of output clock falling edge

LVDS interface:
00 = Default position (timings are specified in this condition)
01 = Setup reduces by 400 ps, hold increases by 400 ps
10 = Data transition is aligned with rising edge
11 = Setup reduces by 200 ps, hold increases by 200 ps

CMOS interface:
00 = Default position (timings are specified in this condition)
01 = Falling edge is advanced by 100 ps
10 = Falling edge is advanced by 200 ps
11 = Falling edge is advanced by 1.5 ns

Bits[5:4] Always write '0'

Bit 3 DIS LOW LATENCY: Disable low latency

This bit disables low-latency mode,
0 = Low-latency mode is enabled. Digital functions such as gain, test patterns and offset correction are disabled
1 = Low-latency mode is disabled. This setting enables the digital functions. See the *Digital Functions and Low Latency Mode* section.

Bit 2 STBY: Standby mode

This bit sets the standby mode.
0 = Normal operation
1 = Only the ADC and output buffers are powered down; internal reference is active; wake-up time from standby is fast

Bits[1:0] Always write '0'

Table 18. Register Address 43h (Default = 00h)

7	6	5	4	3	2	1	0
0	PDN GLOBAL	0	PDN OBUF	0	0	EN LVDS SWING	

Bit 0 Always write '0'

Bit 6 PDN GLOBAL: Power-down

This bit sets the state of operation.
0 = Normal operation
1 = Total power down; the ADC, internal references, and output buffers are powered down; slow wake-up time.

Bit 5 Always write '0'

Bit 4 PDN OBUF: Power-down output buffer

This bit set the output data and clock pins.
0 = Output data and clock pins enabled
1 = Output data and clock pins powered down and put in high- impedance state

Bits[3:2] Always write '0'

Bits[1:0] EN LVDS SWING: LVDS swing control

00 = LVDS swing control using LVDS SWING register bits is disabled
01 = Do not use
10 = Do not use
11 = LVDS swing control using LVDS SWING register bits is enabled

Table 19. Register Address 4Ah (Default = 00h)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	HI PERF MODE 2

Bits[7:1] Always write '0'

Bit[0] HI PERF MODE 2: High performance mode 2

This bit is recommended for high input signal frequencies greater than 230 MHz.
0 = Default performance after reset
1 = For best performance with high-frequency input signals, set the HIGH PERF MODE 2 bit

Table 20. Register Address BFh (Default = 00h)

7	6	5	4	3	2	1	0
OFFSET PEDESTAL						0	0

Bits[7:2] OFFSET PEDESTAL

These bits set the offset pedestal.
When the offset correction is enabled, the final converged value after the offset is corrected is the ADC mid-code value. A pedestal can be added to the final converged value by programming these bits.

ADS414x VALUE	PEDESTAL
011111	31LSB
011110	30LSB
011101	29LSB
—	—
000000	0LSB
—	—
111111	–1LSB
111110	–2LSB
—	—
100000	–32LSB

Bits[1:0] Always write '0'

Table 21. Register Address CFh (Default = 00h)

7	6	5	4	3	2	1	0
FREEZE OFFSET CORR	0	OFFSET CORR TIME CONSTANT				0	0

Bit 7 FREEZE OFFSET CORR

This bit sets the freeze offset correction.
0 = Estimation of offset correction is not frozen (bit EN OFFSET CORR must be set)
1 = Estimation of offset correction is frozen (bit EN OFFSET CORR must be set). When frozen, the last estimated value is used for offset correction every clock cycle. See the *Offset Correction* section.

Bit 6 Always write '0'

Bits[5:2] OFFSET CORR TIME CONSTANT

These bits set the offset correction time constant for the correction loop time constant in number of clock cycles.

VALUE	TIME CONSTANT (Number of Clock Cycles)
0000	1M
0001	2M
0010	4M
0011	8M
0100	16M
0101	32M
0110	64M
0111	128M
1000	256M
1001	512M
1010	1G
1011	2G

Bits[1:0] Always write '0'

Table 22. Register Address DFh (Default = 00h)

7	6	5	4	3	2	1	0
0	0	LOW SPEED		0	0	0	0

Bits[7:6] Always write '0'

Bits[5:4] LOW SPEED: Low-speed mode

For the ADS4122/42, the low-speed mode is enabled by default after reset.
00, 01, 10, 11 = Do not use

For the ADS4125/55 only:
00, 01, 10 = Low-speed mode disabled (default state after reset); this setting is recommended for sampling rates greater than 80 MSPS.
11 = Low-speed mode enabled; this setting is recommended for sampling rates less than or equal to 80 MSPS.

Bits[3:0] Always write '0'

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS412x and ADS414x are lower sampling speed members of the ADS41xx family of ultralow power analog-to-digital converters (ADCs). The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 10 clock cycles. The output is available as 14-bit data or 12-bit data, in DDR LVDS mode or CMOS mode, and coded in either straight offset binary or binary twos complement format.

9.1.1 Analog Input

The analog input consists of a switched-capacitor-based, differential, sample-and-hold architecture. This differential topology results in very good ac performance even for high input frequencies at high sampling rates. The INP and INM pins must be externally biased around a common-mode voltage of 0.95 V, available on the VCM pin. For a full-scale differential input, each input INP and INM pin must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} differential input swing. The input sampling circuit has a high 3-dB bandwidth that extends up to 550 MHz (measured from the input pins to the sampled voltage). Figure 105 shows an equivalent circuit for the analog input.

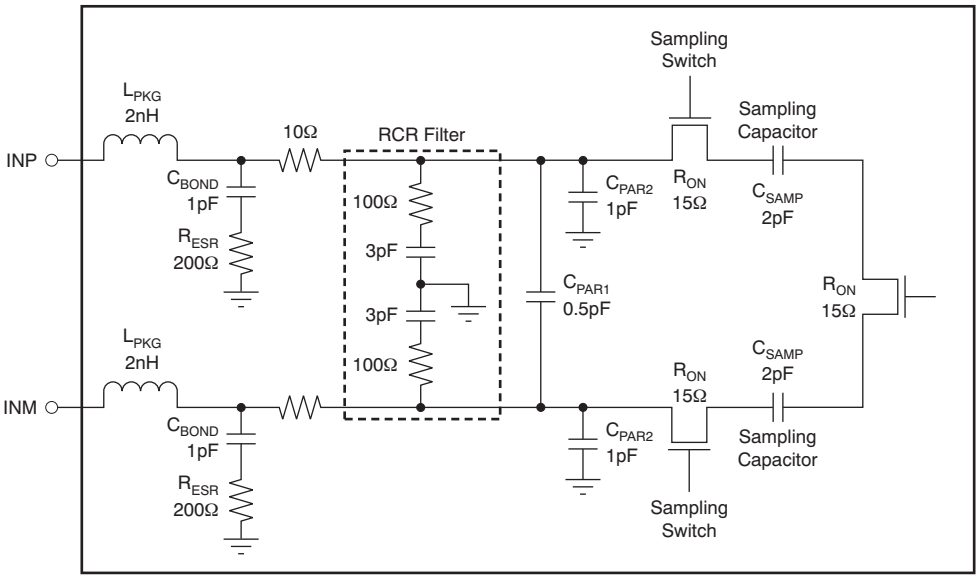


Figure 105. Analog Input Equivalent Circuit

9.1.1.1 Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A 5-Ω to 15-Ω resistor in series with each input pin is recommended to damp out ringing caused by package parasitics. It is also necessary to present low impedance (less than 50 Ω) for the common-mode switching currents. This impedance can be achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

Application Information (continued)

Note that the device includes an internal R-C filter from each input to ground. The purpose of this filter is to absorb the glitches caused by the opening and closing of the sampling capacitors. The cutoff frequency of the R-C filter involves a trade-off. A lower cutoff frequency (larger C) absorbs glitches better, but also reduces the input bandwidth and the maximum input frequency that can be supported. On the other hand, with no internal R-C filter, high input frequency can be supported but now the sampling glitches must be supplied by the external driving circuit. The inductance of the package bond wires limits the ability of the external driving circuit to support the sampling glitches.

In the ADS412x and ADS414x, the R-C component values have been optimized while supporting high input bandwidth (550 MHz). However, in applications where very high input frequency support is not required, filtering of the glitches can be improved further with an external R-C-R filter; see Figure 108 and Figure 109).

In addition, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While designing the drive circuit, the ADC impedance must be considered. Figure 106 and Figure 107 show the impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) looking into the ADC input pins.

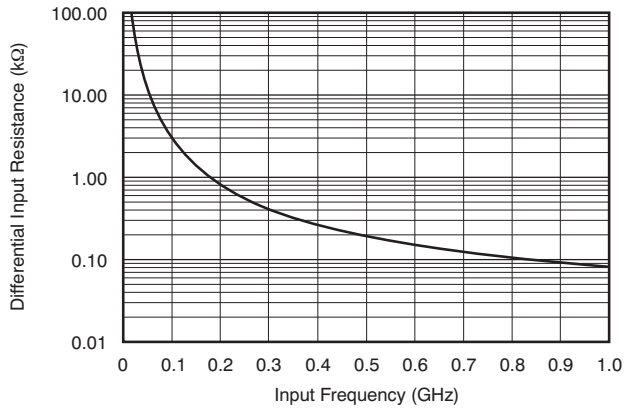


Figure 106. ADC Analog Input Resistance (R_{IN}) Across Frequency

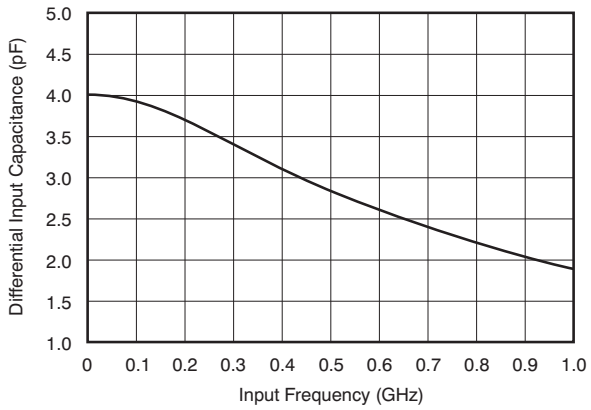


Figure 107. ADC Analog Input Capacitance (C_{IN}) Across Frequency

9.1.1.2 Driving Circuit

Two example driving circuit configurations are shown in Figure 108 and Figure 109—one optimized for low bandwidth (low input frequencies) and the other one for high bandwidth to support higher input frequencies. In Figure 108, an external R-C-R filter with 3.3 pF is used to help absorb sampling glitches. The R-C-R filter limits the bandwidth of the drive circuit, making it suitable for low input frequencies (up to 250 MHz). Transformers such as ADT1-1WT or WBC1-1 can be used up to 250 MHz.

For higher input frequencies, the R-C-R filter can be dropped. Together with the lower series resistors (5 Ω to 10 Ω), this drive circuit provides higher bandwidth to support frequencies up to 500 MHz (as shown in Figure 109). A transmission line transformer such as ADTL2-18 can be used.

Note that both the drive circuits have been terminated by 50 Ω near the ADC side. The termination is accomplished by a 25-Ω resistor from each input to the 0.95-V common-mode (VCM) from the device. This termination allows the analog inputs to be biased around the required common-mode voltage.

Application Information (continued)

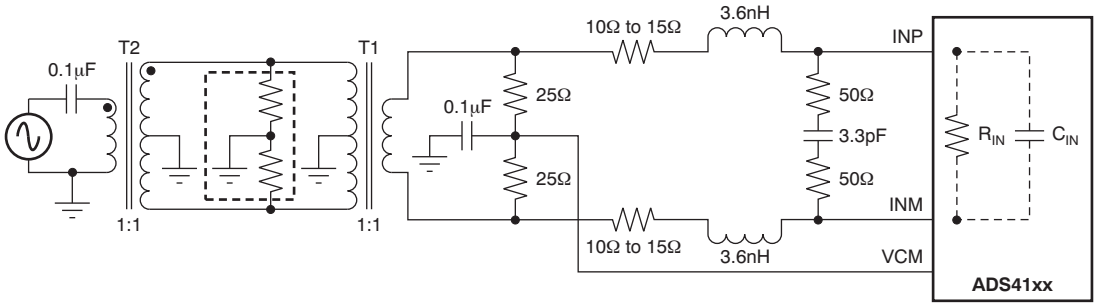


Figure 108. Drive Circuit with Low Bandwidth (for Low Input Frequencies)

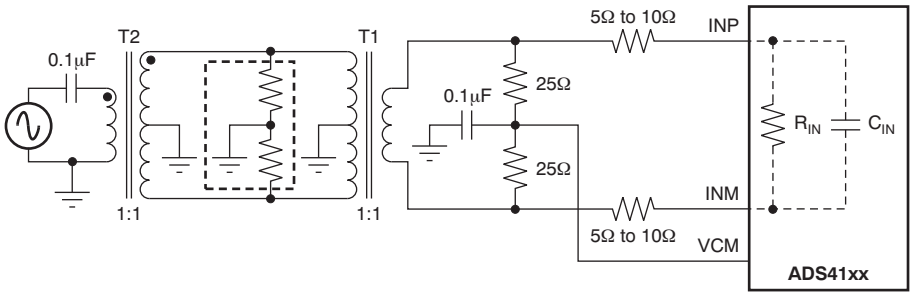


Figure 109. Drive Circuit with High Bandwidth (for High Input Frequencies)

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 108 and Figure 109. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance).

Figure 108 and Figure 109 use 1:1 transformers with a 50-Ω source. As explained in the *Drive Circuit Requirements* section, this architecture helps to present a low source impedance to absorb sampling glitches. With a 1:4 transformer, the source impedance is 200 Ω. The higher source impedance is unable to absorb the sampling glitches effectively and can lead to degradation in performance (compared to using 1:1 transformers).

In almost all cases, either a bandpass or low-pass filter is needed to obtain the desired dynamic performance, as shown in Figure 110. Such a filter presents low source impedance at the high frequencies corresponding to the sampling glitch and helps avoid the performance loss with the high source impedance.

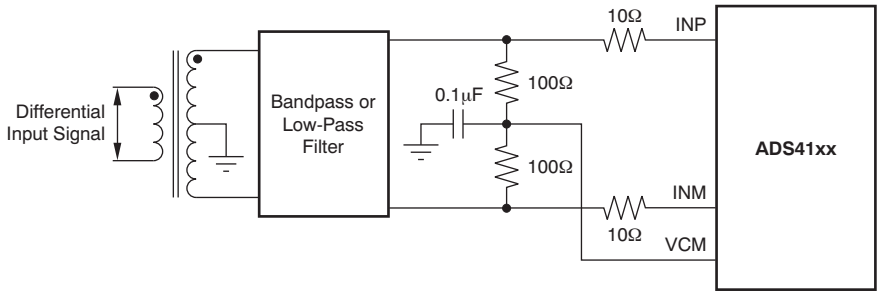


Figure 110. Drive Circuit with 1:4 Transformer

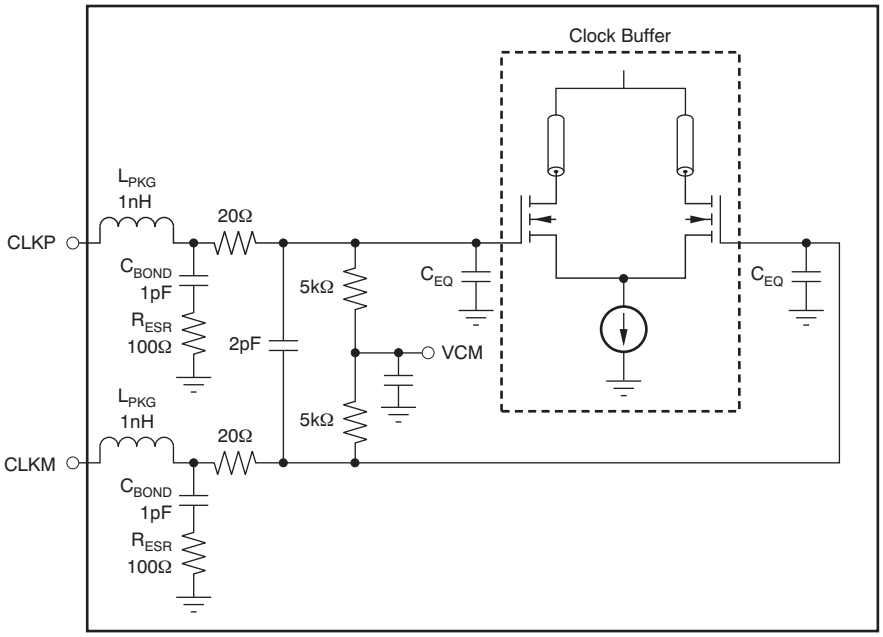
Application Information (continued)

9.1.1.3 Input Common-Mode

To ensure a low-noise, common-mode reference, the VCM pin is filtered with a 0.1-µF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. Each ADC input pin sinks a common-mode current of approximately 0.6 µA per MSPS of clock frequency.

9.1.2 Clock Input

The ADS412x and ADS414x clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors. This setting allows the use of transformer-coupled drive circuits for sine-wave clock or ac-coupling for LVPECL and LVDS clock sources. Figure 111 shows an equivalent circuit for the input clock.



NOTE: C_{EQ} is 1 pF to 3 pF, and is the equivalent input capacitance of the clock buffer.

Figure 111. Input Clock Equivalent Circuit

Application Information (continued)

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 112. For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 113 shows a differential circuit.

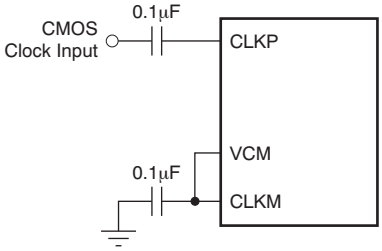


Figure 112. Single-Ended Clock Driving Circuit

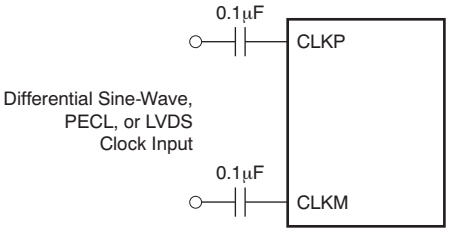


Figure 113. Differential Clock Driving Circuit

9.1.3 Input Overvoltage Indication (OVR Pin)

The device has an OVR pin that provides information about analog input overload. At any clock cycle, if the sampled input voltage exceeds the positive or negative full-scale range, the OVR pin goes high. The OVR remains high as long as the overload condition persists. The OVR pin is a CMOS output buffer (running off DRVDD supply), independent of the type of output data interface (DDR LVDS or CMOS).

For a positive overload, the D[13:0] output data bits are 3FFFh in offset binary output format and 1FFFh in twos complement output format. For a negative input overload, the output code is 0000h in offset binary output format and 2000h in twos complement output format.

9.2 Typical Application

An example schematic for a typical application of the ADS414x is shown in Figure 114.

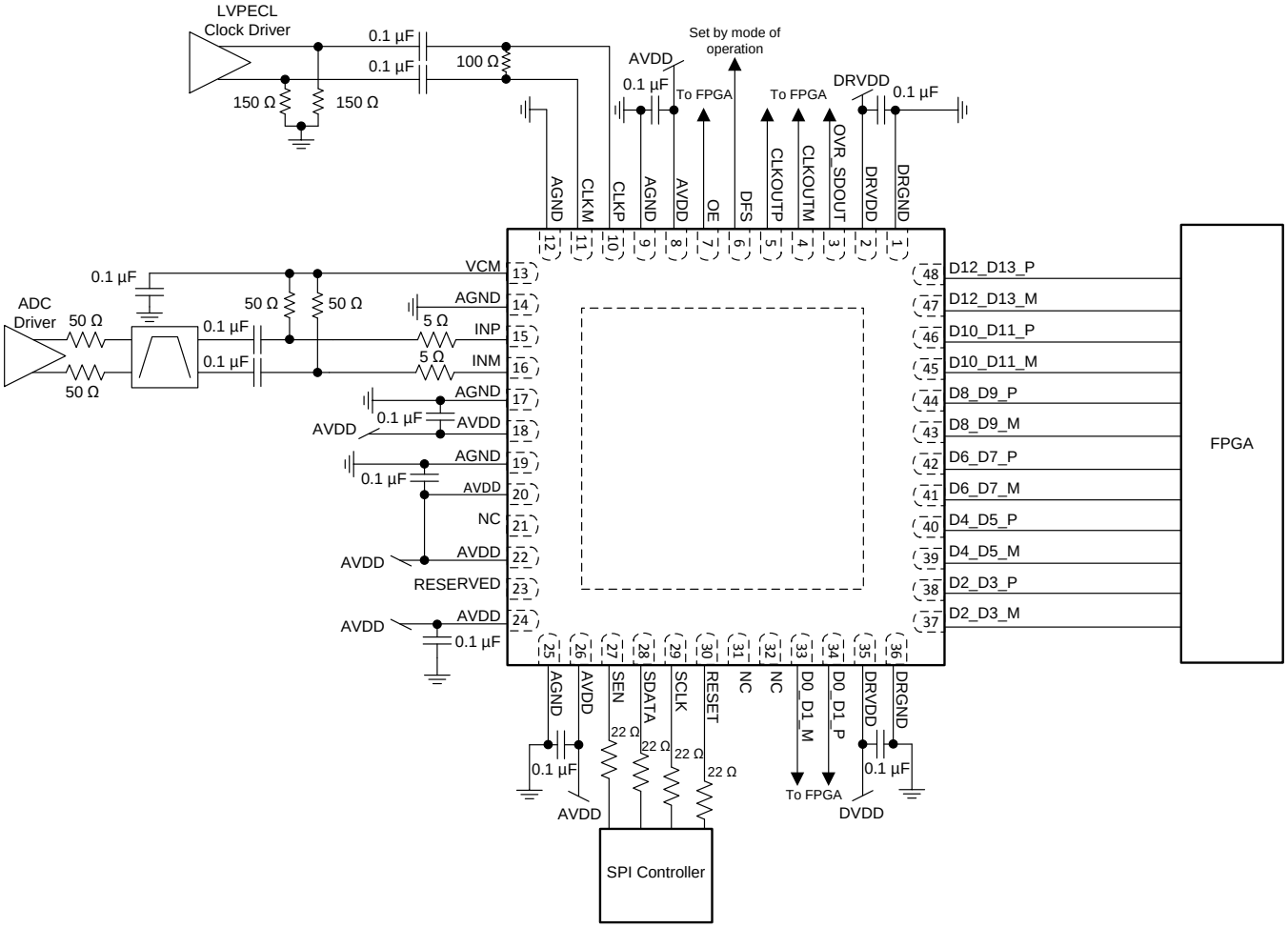


Figure 114. Example Schematic for ADS414x

9.2.1 Design Requirements

Example design requirements are listed in Table 23 for the ADC portion of the signal chain. These do not necessary reflect the requirements of an actual system, but rather demonstrate why the ADS412x and ADS414x may be chosen for a system based on a set of requirements.

Table 23. Example Design Requirements for ADS412x and ADS414x

DESIGN PARAMETER	EXAMPLE DESIGN REQUIREMENT	ADS4128 CAPABILITY
Sampling rate	≥ 122.88 Msps	Max sampling rate: 125 Msps
Input frequency	> 125 MHz to accommodate full 2nd nyquist zone	Large signal –3 dB bandwith: 400 MHz operation
SNR	> 68 dBFS at –1dFBS, 170 MHz	72.2 dBFS at –1dBFS, 170 MHz
SFDR	>77dBc at –1dFBS, 170 MHz	81 dBc at –1 dBFS, 170 MHz
Input full scale voltage	2 Vpp	2 Vpp
Overload recovery time	< 3 clock cycles	1 clock cycle
Digital interface	Parallel LVDS	Parallel LVDS
Power consumption	< 200 mW per channel	153 mW per channel

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Analog Input

The analog input of the ADS412x and ADS414x is typically driven by a fully differential amplifier. The amplifier must have sufficient bandwidth for the frequencies of interest. The noise and distortion performance of the amplifier will affect the combined performance of the ADC and amplifier. The amplifier is often AC coupled to the ADC to allow both the amplifier and ADC to operate at the optimal common mode voltages. It is possible to DC couple the amplifier to the ADC if required. An alternate approach is to drive the ADC using transformers. DC coupling cannot be used with the transformer approach.

9.2.2.2 Clock Driver

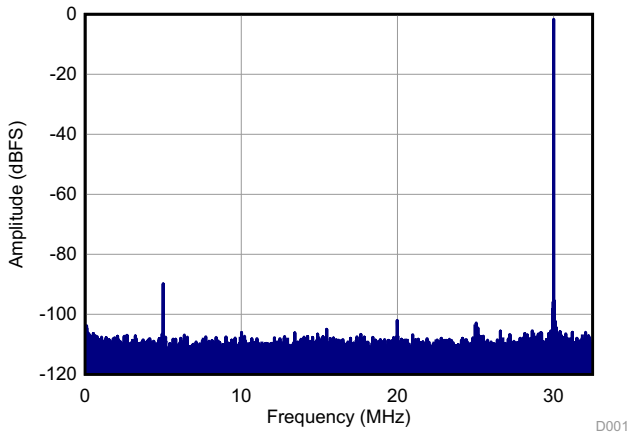
The ADS412x and ADS414x should be driven by a high performance clock driver such as a clock jitter cleaner. The clock needs to have low noise to maintain optimal performance. LVPECL is the most common clocking interface, but LVDS and LVCMOS can be used as well. It is not advised to drive the clock input from an FPGA unless the noise degradation can be tolerated, such as for input signals near DC where the clock noise impact is minimal.

9.2.2.3 Digital Interface

The ADS412x and ADS414x supports both LVDS and CMOS interfaces. The LVDS interface should be used for best performance when operating at maximum sampling rate. The LVDS outputs can be connected directly to the FPGA without any additional components. When using CMOS outputs resistors should be placed in series with the outputs to reduce the output current spikes to limit the performance degradation. The resistors should be large enough to limit current spikes but not so large as to significantly distort the digital output waveform. An external CMOS buffer should be used when driving distances greater than a few inches to reduce ground bounce within the ADC.

9.2.3 Application Curve

Figure 115 shows the results of a 100-MHz signal sampled at 65 MHz captured by the ADS4122.



SNR = 70.11 dBFs SFDR= 87.74 dBFs

THD= 84.33 dBs SINAD= 70.03 dBFs

Figure 115. 100-MHz Signal Captured by ADS4122

10 Power Supply Recommendations

The ADS412x and ADS414x has two power supplies, one analog (AVDD) and one digital (DRVDD) supply. Both supplies have a nominal voltage of 1.8 V. The AVDD supply is noise sensitive and the digital supply is not.

10.1 Sharing DRVDD and AVDD Supplies

For best performance the AVDD supply should be driven by a low noise linear regulator (LDO) and separated from the DRVDD supply. It is possible to have AVDD and DRVDD share a single supply but they should be isolated by a ferrite bead and bypass capacitors, in a PI-filter configuration, at a minimum. The digital noise will be concentrated at the sampling frequency and harmonics of the sampling frequency and could contain noise related to the sampled signal. While developing schematics, it is a good idea to leave extra placeholders for additional supply filtering.

10.2 Using DC-DC Power Supplies

DC-DC switching power supplies can be used to power DRVDD without issue. It is also possible to power AVDD from a switching regulator. Noise and spurs on the AVDD power supply will affect the SNR and SFDR of the ADC and will show up near DC and as a modulated component around the input frequency. If a switching regulator is used, then it should be designed to have minimal voltage ripple. Supply filtering should be used to limit the amount of spurious noise at the AVDD supply pins. Extra placeholders should be placed on the schematic for additional filtering. Optimization of filtering in the final system will likely be needed to achieve the desired performance. The choice of power supply ultimately depends on the system requirements. For instance if very low phase noise is required then use of a switching regulator is not recommended.

10.3 Power Supply Bypassing

Because the ADS412x and ADS414x already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise; thus, the optimum number of capacitors depends on the actual application. A 0.1-µF capacitor is recommended near each supply pin. The decoupling capacitors should be placed very close to the converter supply pins.

11 Layout

11.1 Layout Guidelines

11.1.1 Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See *ADS414x, ADS412x EVM User Guide*SLWU067 for details on layout and grounding.

11.1.2 Supply Decoupling

Because the ADS412x and ADS414x already include internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power-supply noise, so the optimum number of capacitors depends on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

11.1.3 Exposed Pad

In addition to providing a path for heat dissipation, the thermal pad is also electrically internally connected to the digital ground. Therefore, it is necessary to solder the exposed pad to the ground plane for best thermal and electrical performance. For detailed information, see application notes *QFN Layout Guidelines*, SLOA122) and *QFN/SON PCB Attachment*, SLUA271, both available for download at www.ti.com.

11.2 Layout Example

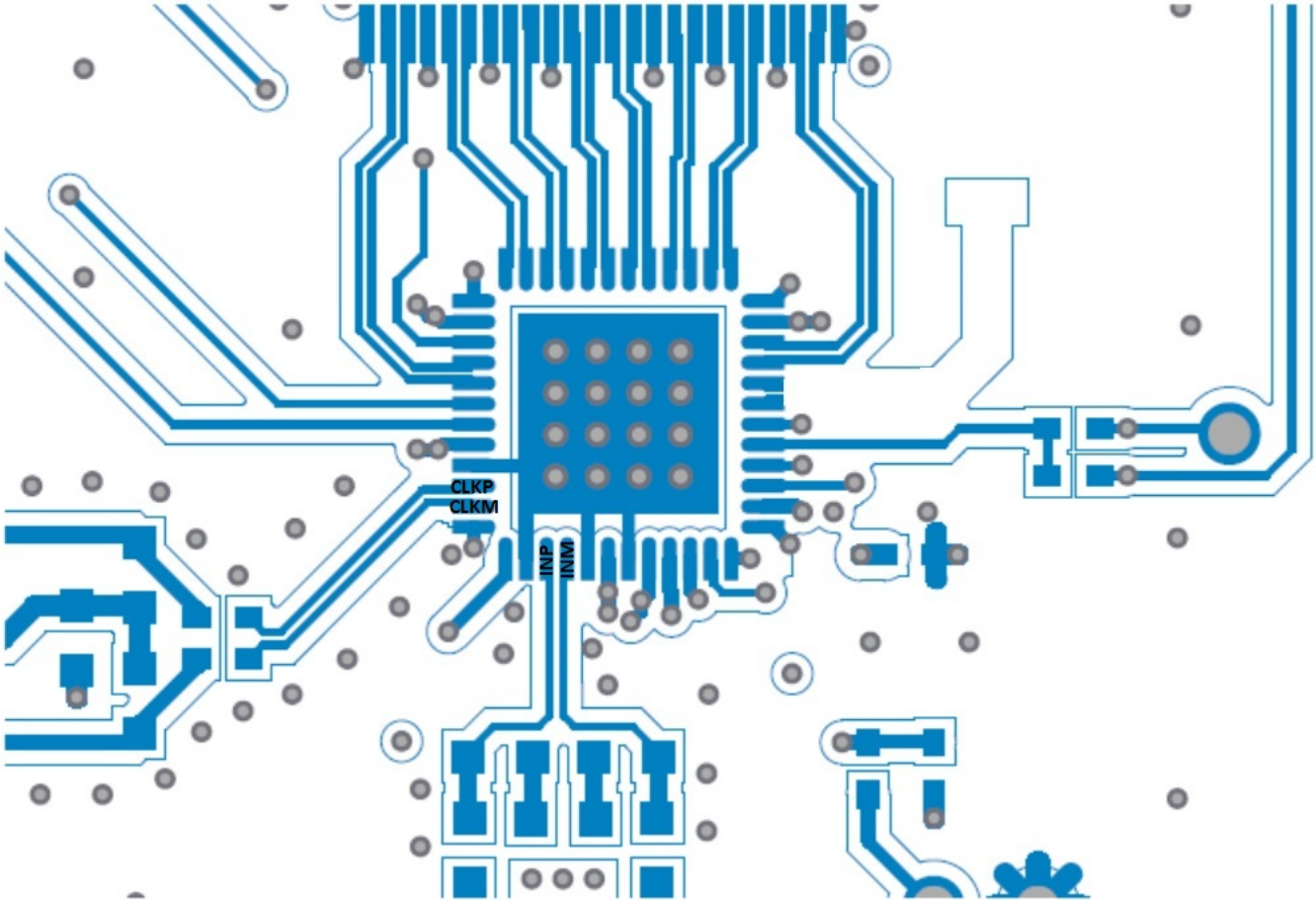


Figure 116. ADS412x and ADS414x EVM PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.1.2 Device Nomenclature

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low-frequency value.

Aperture Delay The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

This delay is different across channels. The maximum variation is specified as aperture delay variation (channel-to-channel).

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal.

Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Maximum Conversion Rate The maximum sampling rate at which specified operation is given.

All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart.

Integral Nonlinearity (INL) The INL is the deviation of the ADC transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

Gain Error Gain error is the deviation of the ADC actual input full-scale range from its ideal value.

The gain error is given as a percentage of the ideal input full-scale range. Gain error has two components: error as a result of reference inaccuracy and error as a result of the channel. Both errors are specified independently as E_{GREF} and E_{GCHAN}.

To a first-order approximation, the total gain error is $E_{TOTAL} \sim E_{GREF} + E_{GCHAN}$.

For example, if $E_{TOTAL} = \pm 0.5\%$, the full-scale input varies from $(1 - 0.5/100) \times FS_{ideal}$ to $(1 + 0.5/100) \times FS_{ideal}$.

Offset Error The offset error is the difference, given in number of LSBs, between the ADC actual average idle channel output code and the ideal average idle channel output code.

This quantity is often mapped into millivolts.

Temperature Drift The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from T_{MIN} to T_{MAX}.

It is calculated by dividing the maximum deviation of the parameter across the T_{MIN} to T_{MAX} range by the difference $T_{MAX} - T_{MIN}$.

Signal-to-Noise Ratio SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10} \frac{P_S}{P_N} \quad (2)$$

Device Support (continued)

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10Log^{10} \frac{P_S}{P_N + P_D} \quad (3)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB) ENOB is a measure of the converter performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (4)$$

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first nine harmonics (P_D).

$$THD = 10Log^{10} \frac{P_S}{P_N} \quad (5)$$

THD is typically given in units of dBc (dB to carrier).

Spurious-Free Dynamic Range (SFDR) The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic).

SFDR is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion IMD3 is the ratio of the power of the fundamental (at frequencies f_1 and f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$.

IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale) when the power of the fundamental is extrapolated to the converter full-scale range.

DC Power-Supply Rejection Ratio (DC PSRR) DC PSSR is the ratio of the change in offset error to a change in analog supply voltage.

The dc PSRR is typically given in units of mV/V.

AC Power-Supply Rejection Ratio (AC PSRR) AC PSRR is the measure of rejection of variations in the supply voltage by the ADC.

If ΔV_{SUP} is the change in supply voltage and ΔV_{OUT} is the resultant change of the ADC output code (referred to the input), then:

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (6)$$

Voltage Overload Recovery The number of clock cycles taken to recover to less than 1% error after an overload on the analog inputs.

This is tested by separately applying a sine wave signal with 6dB positive and negative overload. The deviation of the first few samples after the overload (from the expected values) is noted.

Common-Mode Rejection Ratio (CMRR) CMRR is the measure of rejection of variation in the analog input common-mode by the ADC.

If ΔV_{CM_IN} is the change in the common-mode voltage of the input pins and ΔV_{OUT} is the resulting change of the ADC output code (referred to the input), then:

Device Support (continued)

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (7)$$

Crosstalk (only for multi-channel ADCs) This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest. It is specified separately for coupling from the immediate neighboring channel (near-channel) and for coupling from channel across the package (far-channel).

It is usually measured by applying a full-scale signal in the adjacent channel. Crosstalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

12.2 Documentation Support

12.2.1 Related Documentation

For Related documentation, see the following:

- QFN Layout Guidelines (SLOA122)
- QFN/SON PCB Attachment (SLUA271)
- ADS4226 Evaluation Module (SLWU067)

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 24. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS4122	Click here	Click here	Click here	Click here	Click here
ADS4125	Click here	Click here	Click here	Click here	Click here
ADS4142	Click here	Click here	Click here	Click here	Click here
ADS4145	Click here	Click here	Click here	Click here	Click here

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS4122IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4122	Samples
ADS4122IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4122	Samples
ADS4125IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4125	Samples
ADS4125IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4125	Samples
ADS4142IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4142	Samples
ADS4142IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4142	Samples
ADS4145IRGZ25	ACTIVE	VQFN	RGZ	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4145	Samples
ADS4145IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4145	Samples
ADS4145IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ4145	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

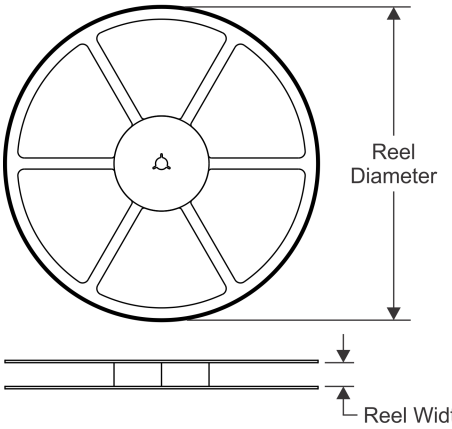
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

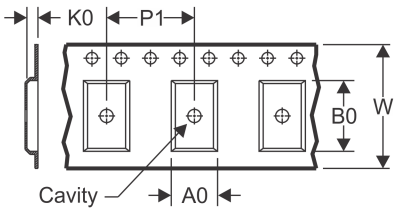
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

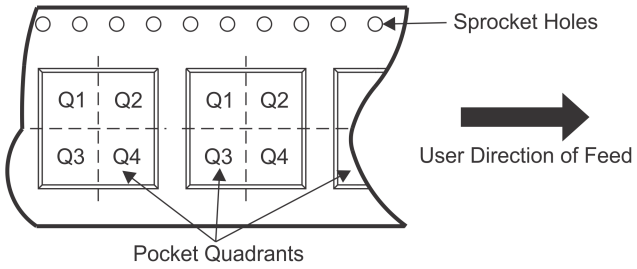


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

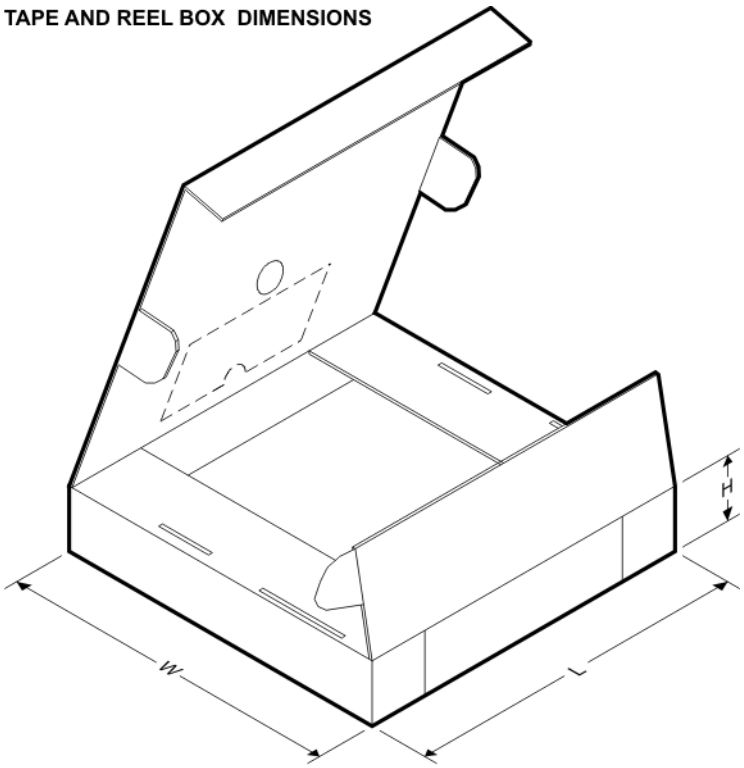
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS4122IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4122IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4125IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4125IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4142IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4142IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4145IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS4145IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

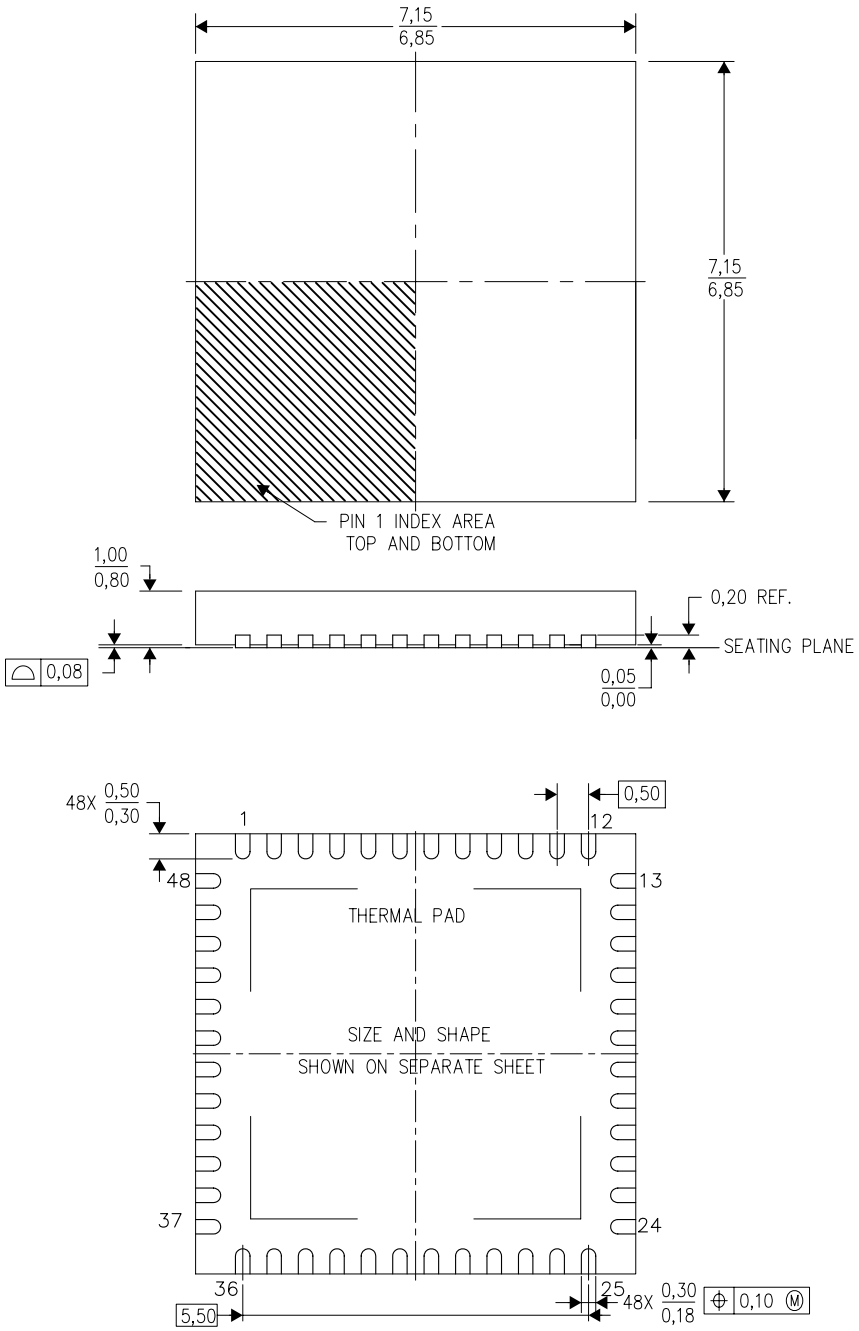
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS4122IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS4122IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS4125IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS4125IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS4142IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS4142IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0
ADS4145IRGZR	VQFN	RGZ	48	2500	336.6	336.6	28.6
ADS4145IRGZT	VQFN	RGZ	48	250	213.0	191.0	55.0

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

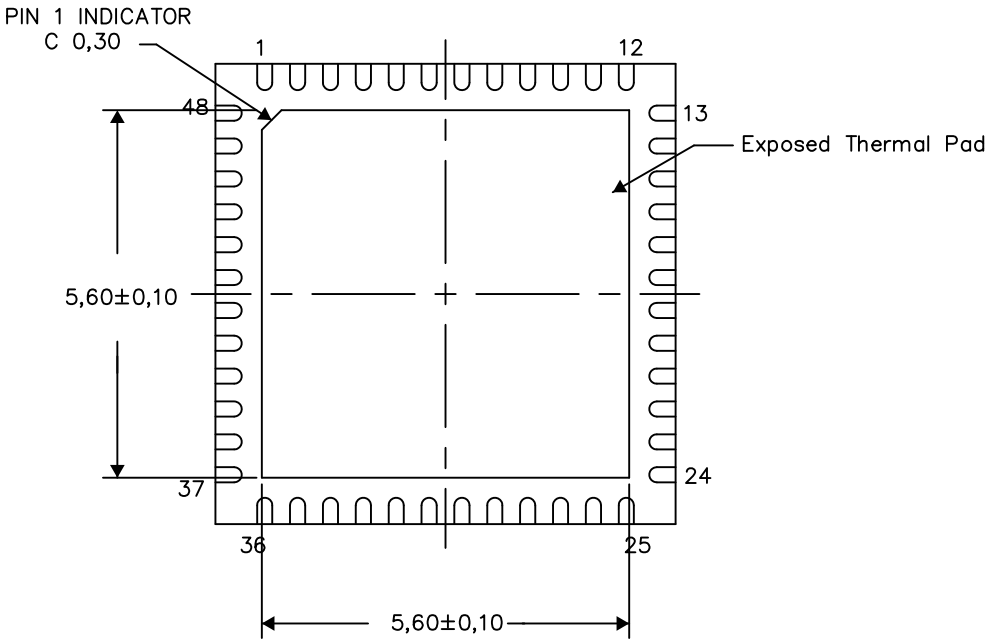
RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



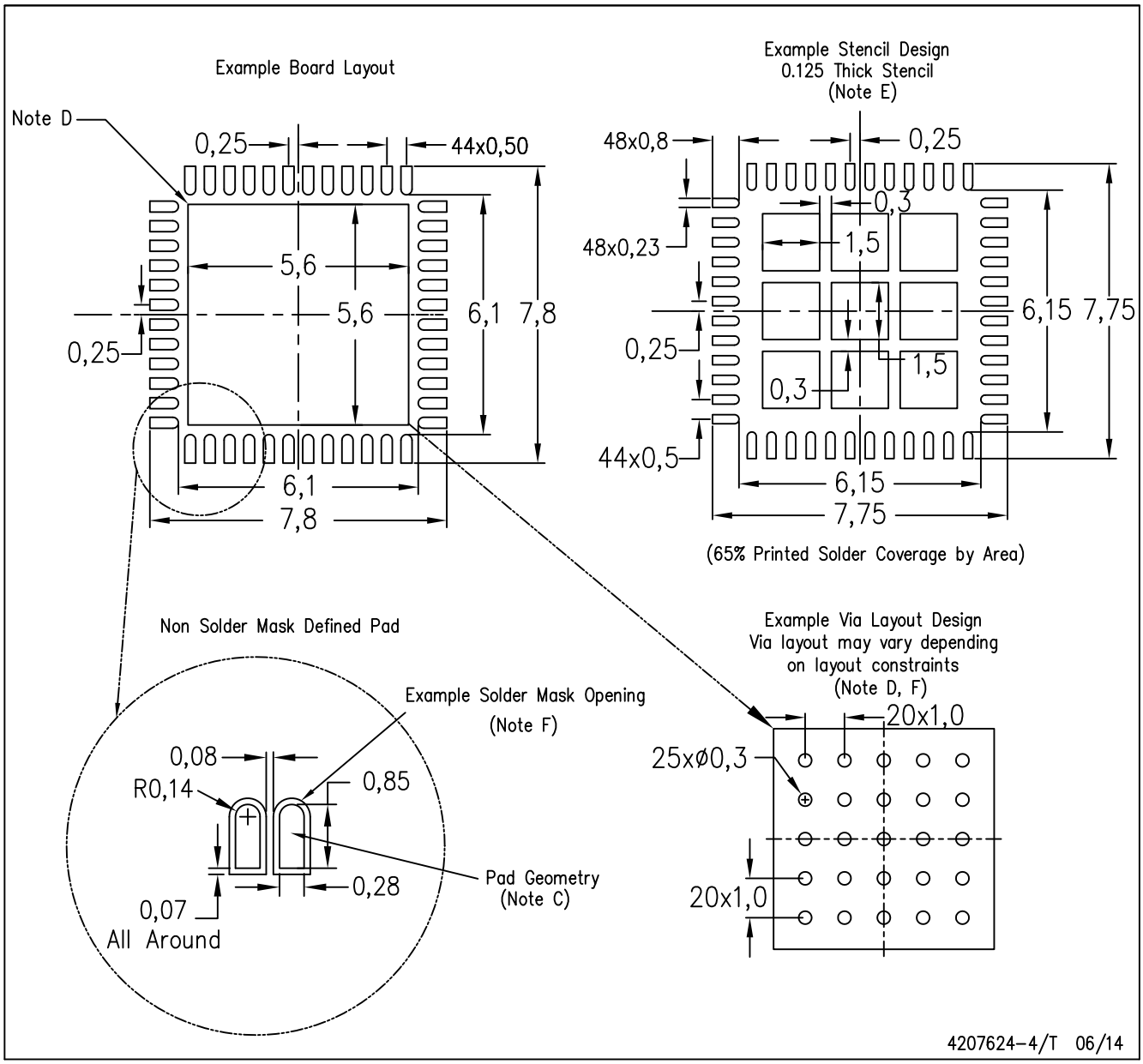
Bottom View

Exposed Thermal Pad Dimensions

4206354–5/Z 03/15

NOTE: All linear dimensions are in millimeters

RGZ (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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