16-Bit, 10 MHz Bandwidth, 30 MSPS to 160 MSPS Continuous Time Sigma-Delta ADC

AD9261

FEATURES

SNR: 83 dB (85 dBFS) to 10 MHz input
SFDR: 87 dBc to 10 MHz input
Noise figure: 15 dB
Input impedance: 1 kΩ
Power: 340 mW
1.8 V analog supply operation
1.8 V to 3.3 V output supply
Selectable bandwidth
2.5 MHz/5 MHz/10 MHz
Output data rate: 30 MSPS to 160 MSPS
Integrated decimation filters
Integrated sample rate converter
On-chip PLL clock multiplier
On-chip voltage reference
Offset binary, Gray code, or twos complement data format
Serial control interface (SPI)

APPLICATIONS

Data acquisition
Automated test equipment
Instrumentation
Medical imaging

FUNCTIONAL BLOCK DIAGRAM

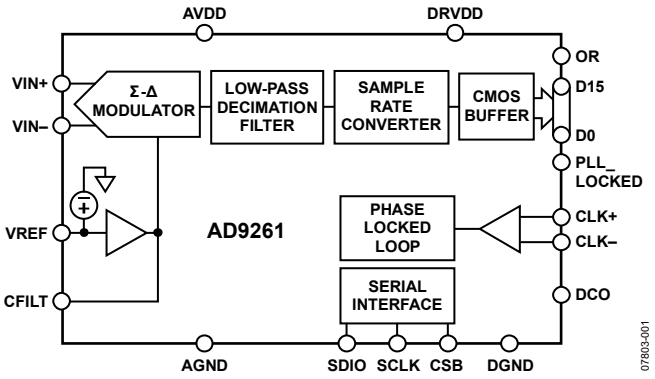

Figure 1.

GENERAL DESCRIPTION

The AD9261 is a single 16-bit analog-to-digital converter (ADC) based on a continuous time (CT) sigma-delta (Σ-Δ) architecture that achieves 87 dBc of dynamic range over a 10 MHz input bandwidth. The integrated features and characteristics unique to the continuous time Σ-Δ architecture significantly simplify its use and minimize the need for external components.

The AD9261 has a resistive input impedance that relaxes the requirements of the driver amplifier. In addition, a 32× oversampled fifth-order continuous time loop filter significantly attenuates out-of-band signals and aliases, reducing the need for external filters at the input.

An external clock input or the integrated integer-N PLL provides the 640 MHz internal clock needed for the oversampled continuous time Σ-Δ modulator. On-chip decimation filters and sample rate converters reduce the modulator data rate from 640 MSPS to a user-defined output data rate from 30 MSPS to 160 MSPS, enabling a more efficient and direct interface.

The digital output data is presented in offset binary, Gray code, or twos complement format. A data clock output (DCO) is provided to ensure proper timing with the receiving logic.

The AD9261 operates on a 1.8 V analog supply and a 1.8 V to 3.3 V digital supply, consuming 340 mW. The AD9261 is available in a 48-lead LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Continuous time Σ-Δ architecture efficiently achieves high dynamic range and wide bandwidth.
2. Passive input structure reduces or eliminates the requirements for a driver amplifier.
3. An oversampling ratio of 32× and high order loop filter provide excellent alias rejection reducing or eliminating the need for antialiasing filters.
4. An integrated decimation filter, sample rate converter, PLL clock multiplier, and voltage reference provide ease of use.
5. This part operates from a single 1.8 V analog power supply and 1.8 V to 3.3 V output supply.

Rev. A

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REVISION HISTORY

9/2020—Rev. 0 to Rev. A

Changed CP-48-1 to CP-49-9 ... Throughout
Changes to Figure 3 ... 8
Updated Outline Dimensions ... 27
Changes to Ordering Guide ... 27

4/2010—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

All power supplies set to 1.8 V, 640 MHz sample rate, 0.5 V internal reference, PLL disabled, 40 MSPS output data rate, AIN[1] = −2.0 dBFS, unless otherwise noted.

Table 1.

Parameter	Temp	Min	Typ	Max	Unit
RESOLUTION	Full		16		Bits
ANALOG INPUT BANDWIDTH				10	MHz
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full		±0.02	±0.15	% FSR
Gain Error	Full		±0.7	±3.0	% FSR
Integral Nonlinearity (INL)[2]	Full		±1.5		LSB
TEMPERATURE DRIFT					
Offset Error	Full		±1.5		ppm/°C
Gain Error	Full		±50		ppm/°C
INTERNAL VOLTAGE REFERENCE		490	500	510	mV
ANALOG INPUT					
Input Span, VREF = 0.5 V	Full		2		V p-p diff
Common-Mode Voltage	Full	1.7	1.8	1.9	V
Input Resistance	Full		1		kΩ
POWER SUPPLIES					
Supply Voltage					
AVDD	Full	1.7	1.8	1.9	V
CVDD	Full	1.7	1.8	1.9	V
DVDD	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	3.6	V
Supply Current					
I_{AVDD}[2]	Full		74	83	mA
I_{CVDD}[2] PLL Enabled	Full		57	654	mA
I_{CVDD}[2] PLL Disabled	Full		8.0	8.8	mA
I_{DVDD}[2]	Full		100	108	mA
I_{DRVDD}[2] (1.8 V)	Full		5.5	5.8	mA
I_{DRVDD}[2] (3.3 V)	Full		10		mA
POWER CONSUMPTION					
Sine Wave Input[2] PLL Disabled	Full		340	370	mW
Sine Wave Input[2] PLL Enabled	Full		425	465	mW
Power-Down Power	Full		20		mW
Standby Power[2]	Full		7		mW
Sleep Power	Full		3	4	mW

[1] Input power is referenced to full scale. Therefore, all measurements were taken with a 2 dB signal below full scale, unless otherwise noted.
[2] Measured with a low input frequency, full-scale sine wave.

AC SPECIFICATIONS

All power supplies set to 1.8 V, 640 MHz sample rate, 0.5 V internal reference, PLL disabled, 40 MSPS output data rate, AIN = −2.0 dBFS, unless otherwise noted.

Table 2.

Parameter[1]	Temp	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO (SNR)					
f_{IN} = 2.4 MHz	Full	81	83		dB
f_{IN} = 4.2 MHz	25°C		83		dB
f_{IN} = 8.4 MHz	25°C		83		dB
EFFECTIVE NUMBER OF BITS (ENOB)					
f_{IN} = 2.4 MHz	25°C		13.5		Bits
f_{IN} = 4.2 MHz	25°C		13.5		Bits
f_{IN} = 8.4 MHz	25°C		13.5		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)					
f_{IN} = 2.4 MHz	Full		87	80	dBc
f_{IN} = 4.2 MHz	25°C		87		dBc
f_{IN} = 8.4 MHz	25°C		<120		dBc
NOISE SPECTRAL DENSITY (NSD)					
AIN= −2 dBFS	Full		−155	−153	dB/Hz
AIN = −40 dBFS	Full		−156	−154.5	dB/Hz
NOISE FIGURE[2]	25°C		15		dB
TWO-TONE SFDR					
f_{IN1} = 2.1 MHz at −8 dBFS, f_{IN2} = 2.4 MHz at −8 dBFS	25°C		93		dBc
f_{IN1} = 3.6 MHz at −8 dBFS, f_{IN2} = 4.2 MHz at −8 dBFS	25°C		92.5		dBc
f_{IN1} = 7.2 MHz at −8 dBFS, f_{IN2} = 8.4 MHz at −8 dBFS	25°C		92.5		dBc
ANALOG INPUT BANDWIDTH	25°C			10	MHz
APERTURE JITTER	25°C			1	ps rms

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Noise figure with respect to 50 Ω. AD9261 internal impedance is 1000 Ω differential. See the AN-835 Application Note for a definition.

DIGITAL DECIMATION FILTERING CHARACTERISTICS

All power supplies set to 1.8 V, 640 MHz sample rate, 0.5 V internal reference, PLL disabled, AIN = −2.0 dBFS, unless otherwise noted.

Table 3.

	2.5 MHz BW			5 MHZ BW			10 MHz BW			
Parameter[1]	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Pass-Band Transition	2.5		3.75	5		6.5	10		13	MHz
Pass-Band Ripple		<0.1			<0.1			<0.1		dB
Stop Band		3.75 MHz – f_S/2			6.5 MHz – f_S/2			13 MHz – f_S/2		MHz
Stop Band Attenuation		>85			>85			>85		dB

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

DIGITAL SPECIFICATIONS

All power supplies set to 1.8 V, 640 MHz sample rate, 0.5 V internal reference, PLL disabled, 40 MSPS output data rate, AIN = −2.0 dBFS, unless otherwise noted.

Table 4.

Parameter[1]	Temp	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVPECL		
Differential Input Voltage	Full	0.4	0.8	2	V p-p
Input Common-Mode Range	Full	0.3	0.450	0.5	V
High Level Input Current	Full	−60		+60	µA
Low Level Input Current	Full	−60		+60	µA
Input Resistance	Full		20		kΩ
Input Capacitance	Full		1		pF
LOGIC INPUTS (SCLK)					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−50		−75	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		30		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO, CSB, RESET)					
High Level Input Voltage	Full	1.2		DRVDD + 0.3	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	+40		+135	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
DRVDD = 3.3 V					
High Level Output Voltage (V_{OH}, I_{OH} = 50 µA)	Full	3.29			V
High Level Output Voltage (V_{OH}, I_{OH} = 0.5 mA)	Full	3.25			V
Low Level Output Voltage (V_{OL}, I_{OL} = 1.6 mA)	Full			0.2	V
Low Level Output Voltage (V_{OL}, I_{OL} = 50 µA)	Full			0.05	V
DRVDD = 1.8 V					
High Level Output Voltage (V_{OH}, I_{OH} = 50 µA)	Full	1.79			V
High Level Output Voltage (V_{OH}, I_{OH} = 0.5 mA)	Full	1.75			V
Low Level Output Voltage (V_{OL}, I_{OL} = 1.6 mA)	Full			0.2	V
Low Level Output Voltage (V_{OL}, I_{OL} = 50 µA)	Full			0.05	V

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

SWITCHING SPECIFICATIONS

All power supplies set to 1.8 V, 640 MHz sample rate, 0.5 V internal reference, PLL disabled, 40 MSPS output data rate, AIN = −2.0 dBFS, unless otherwise noted.

Table 5.

Parameter[1]	Temp	Min	Typ	Max	Unit
CLOCK INPUT (USING CLOCK MULTIPLIER)					
Conversion Rate	Full	30		160	MSPS
CLK± Period	Full	6.25		33	ns
CLK± Duty Cycle	Full	40	50	60	%
CLOCK INPUT (DIRECT CLOCKING)					
Conversion Rate	Full	608	640	672	MSPS
CLK± Period	Full	1.49	1.5625	1.64	ns
CLK± Duty Cycle	Full	40	50	60	%
DATA OUTPUT PARAMETERS					
Output Data Rate	Full	20		168	MSPS
DCO to Data Skew (t_{SKEW})[2]	Full	3			ns
Sample Latency	Full		960		Cycles
WAKE-UP TIME[3]	Full				
Power Down Power	Full		3		µs
Standby Power	Full		9		µs
Sleep Power	Full		15		µs
OUT-OF-RANGE RECOVERY TIME	Full		960		Cycles
SERIAL PORT INTERFACE[4]					
SCLK Period	Full	40			ns
SCLK Pulse Width High Time (t_{SHIGH})	Full	16			ns
SCLK Pulse Width Low Time (t_{SLOW})	Full	16			ns
SDIO to SCLK Setup Time (t_{SDS})	Full	5			ns
SDIO to SCLK Hold Time (t_{SDH})	Full	2			ns
CSB to SCLK Setup Time (t_{SS})	Full	5			ns
CSB to SCLK Hold Time (t_{SH})	Full	2			ns

[1] See the AN-83 5 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Data skew is measured from DCO 50% transition to data (D0 to D15) 50% transition, with 5 pF load.
[3] Wake-up time is dependent on the value of the decoupling capacitors. Values are shown with 10 µF capacitor on VREF and CFILT.
[4] See Figure 50 and the Serial Port Interface (SPI) section.

Timing Diagram

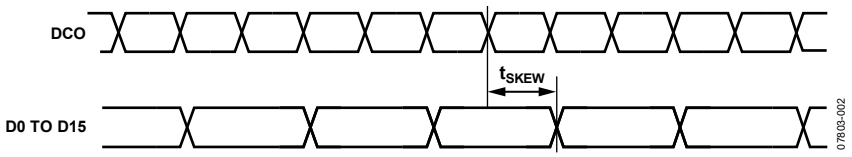


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
AVDD to AGND	−0.3 V to +2.0 V
DVDD to DGND	−0.3 V to +2.0 V
DRVDD to DGND	−0.3 V to +3.9 V
AGND to DGND	−0.3 V to +0.3 V
AVDD to DRVDD	−3.9 V to +2.0 V
CVDD to CGND	−0.3 V to +2.0 V
CGND to DGND	−0.3 V to +0.3 V
D0 to D15 to DGND	−0.3 V to +2.0 V
DCO to DGND	−0.3 V to +2.0 V
OR to DGND	−0.3 V to +2.0 V
PDWN to GND	−0.3 V to +2.0 V
PLLMULTx to DGND	−0.3 V to +2.0 V
SDIO to DGND	−0.3 V to +3.9 V
CSB to AGND	−0.3 V to +3.9 V
SCLK to AGND	−0.3 V to +3.9 V
VIN+, VIN− to AGND	−0.3 V to +2.5 V
CLK+, CLK− to CGND	−0.3 V to +2.0 V
Environmental	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 Sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the PCB increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JB}	θ_{JC}	Unit
48-Lead LFCSP (CP-48-9)	27.7	11.8	1.1	°C/W

Typical θ_{JA} and θ_{JC} are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

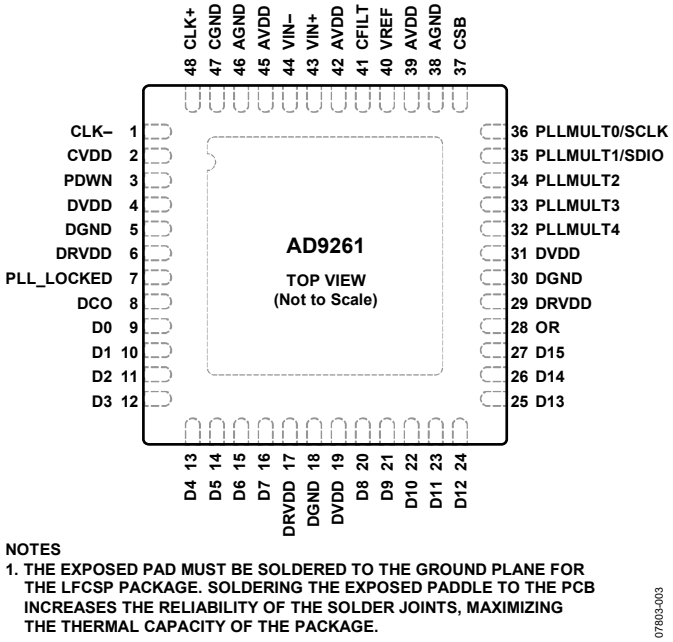


Figure 3. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK–	Clock Input (–).
2	CVDD	Clock Supply (1.8 V).
3	PDWN	External Power-Down Pin.
4, 19, 31	DVDD	Digital Supply (1.8 V).
5, 18, 30	DGND	Digital Ground.
6, 17, 29	DRVDD	Digital Output Driver Supply (1.8 V to 3.3 V).
7	PLL_LOCKED	PLL Lock Indicator.
8	DCO	Data Clock Output.
9 to 16, 20 to 27	D0 to D15	Data Output Bits. D0 is the LSB and D15 is the MSB.
28	OR	Overrange Indicator.
32, 33, 34	PLLMULT4, PLLMULT3, PLLMULT2	PLL Mode Selection Pins.
35	PLLMULT1/SDIO	PLL Mode Selection Pin/Serial Port Interface Data Input/Output.
36	PLLMULT0/SCLK	PLL Mode Selection Pin/Serial Port Interface Clock.
37	CSB	Serial Port Interface Chip Select. Active low.
38, 46	AGND	Analog Ground.
39, 42, 45	AVDD	Analog Supply (1.8 V).
40	VREF	Voltage Reference Input/Output.
41	CFILT	Noise Limiting Filter Capacitor.
43	VIN+	Analog Input (+).
44	VIN–	Analog Input (–).
47	CGND	Clock Ground.
48	CLK+	Clock Input (+).
49	EPAD	Analog Ground. Pin 49 is the exposed thermal pad on the bottom of the package.

TYPICAL PERFORMANCE CHARACTERISTICS

All power supplies set to 1.8 V, 640 MHz sample rate, 2 V p-p differential input, 0.5 V internal reference, PLL disabled, AIN = −2.0 dBFS, T_A = 25°C, unless otherwise noted.

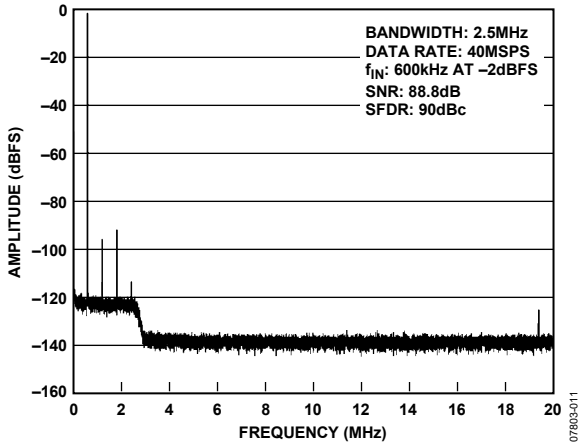


Figure 4. Single-Tone FFT with f_{IN} = 600 kHz and BW = 2.5 MHz

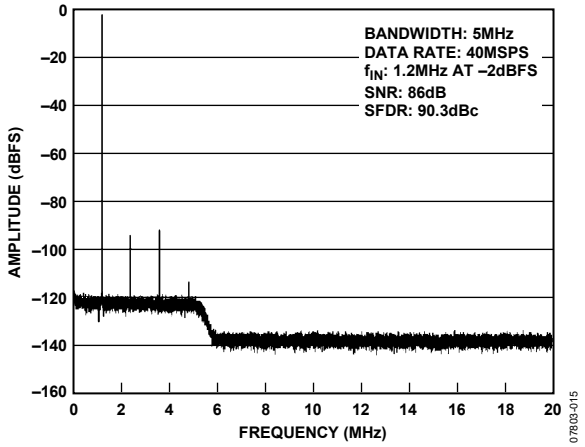


Figure 5. Single-Tone FFT with f_{IN} = 1.2 MHz and BW = 5 MHz

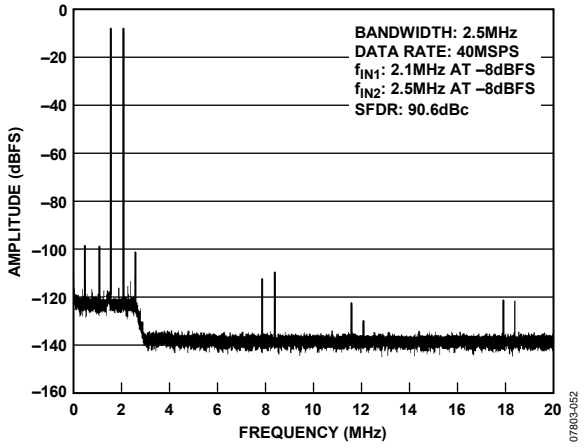


Figure 6. Two-Tone FFT with f_{IN1} = 2.1 MHz, f_{IN2} = 2.5 MHz, and BW = 2.5 MHz

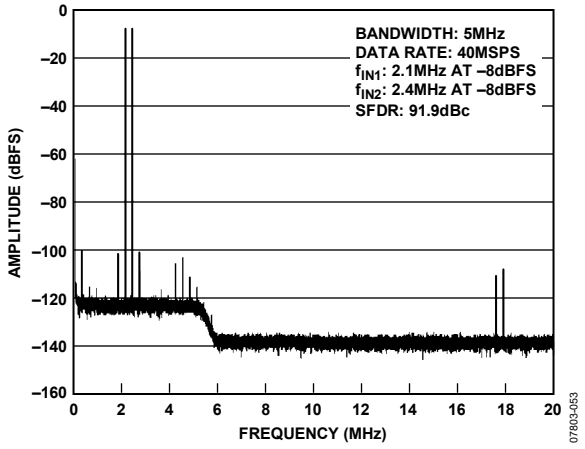


Figure 7. Two-Tone FFT with f_{IN1} = 2.1 MHz, f_{IN2} = 2.4 MHz and BW = 5 MHz

All power supplies set to 1.8 V, 640 MHz sample rate, 2 V p-p differential input, 0.5 V internal reference, PLL disabled, AIN = −2.0 dBFS, 10 MHz bandwidth, output data rate 40 MSPS, T_A = 25°C, unless otherwise noted.

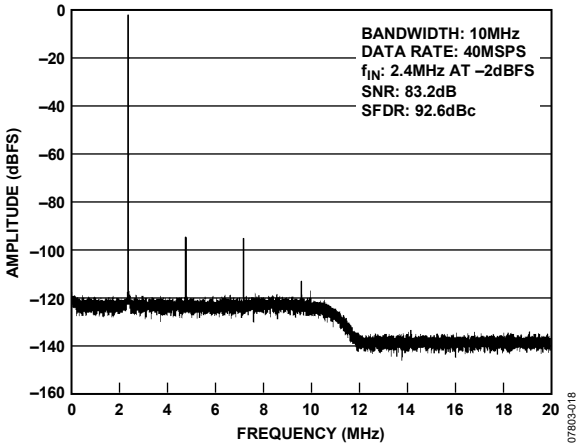


Figure 8. Single-Tone FFT with f_{IN} = 2.4 MHz

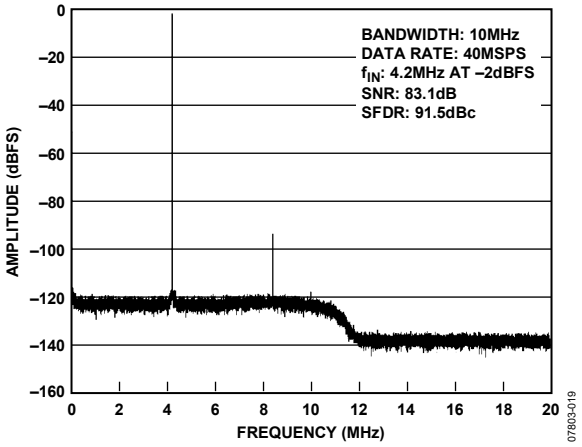


Figure 9. Single-Tone FFT with f_{IN} = 4.2 MHz

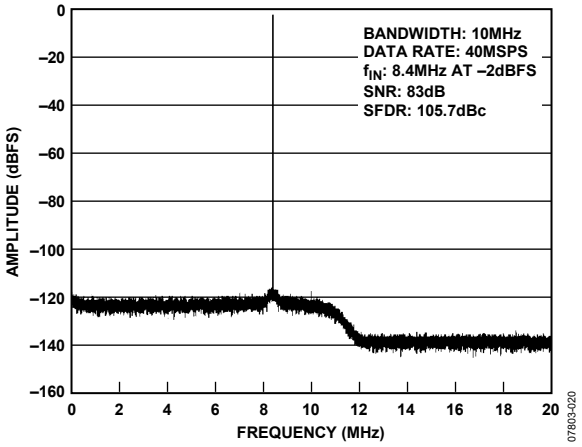


Figure 10. Single-Tone FFT with f_{IN} = 8.4 MHz

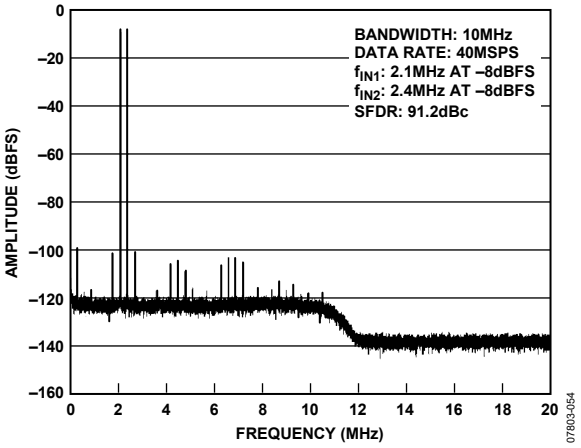


Figure 11. Two-Tone FFT with f_{IN1} = 2.1 MHz and f_{IN2} = 2.4 MHz

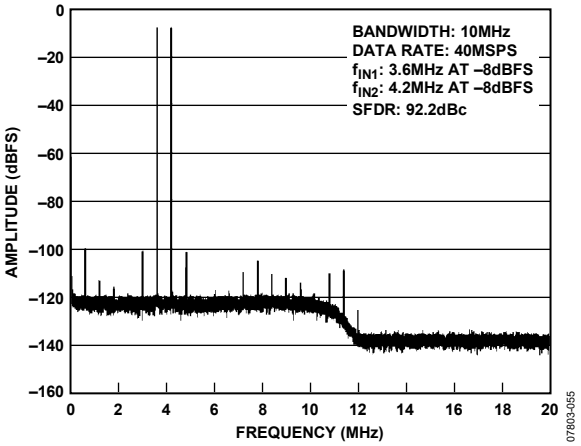


Figure 12. Two-Tone FFT with f_{IN1} = 3.6 MHz and f_{IN2} = 4.2 MHz

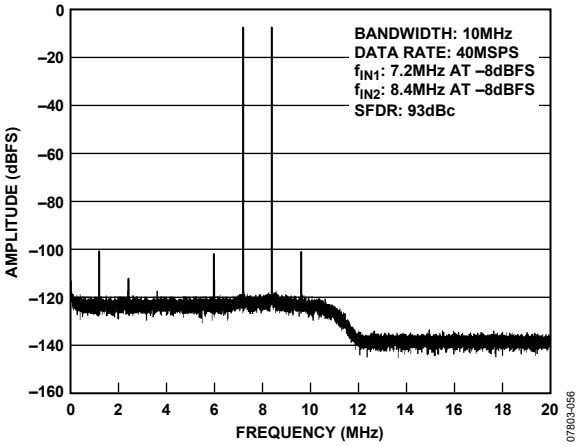


Figure 13. Two-Tone FFT with f_{IN1} = 7.2 MHz and f_{IN2} = 8.4 MHz

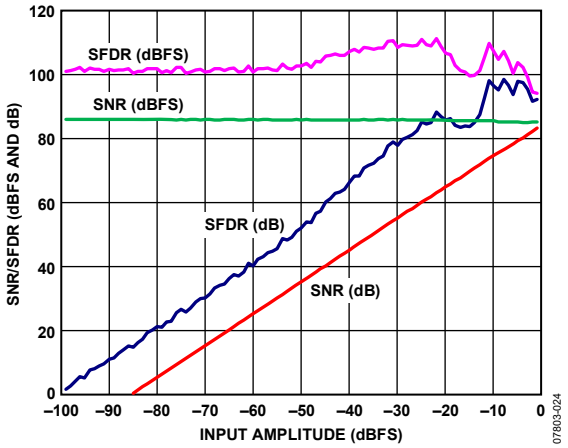


Figure 14. Single-Tone SNR and SFDR vs. Input Amplitude with f_{IN} = 2.4 MHz

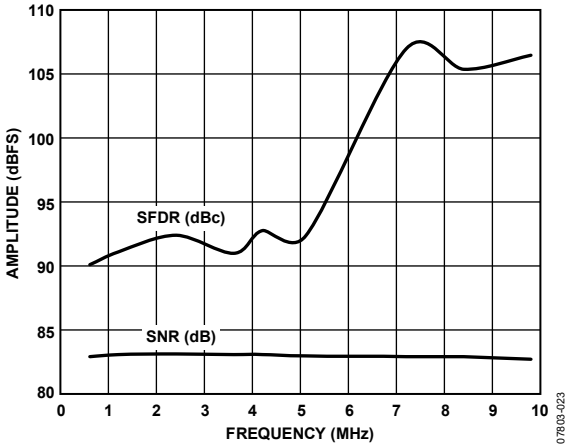


Figure 17. SNR/SFDR vs. Input Frequency

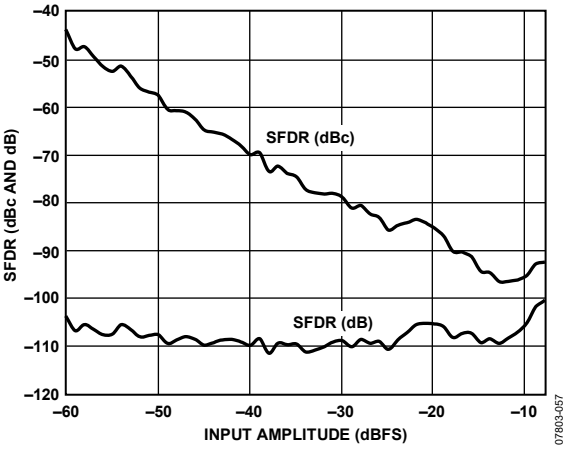


Figure 15. Two-Tone SFDR/IMD3 vs. Input Amplitude with f_{IN1} = 2.1 MHz and f_{IN2} = 2.4 MHz

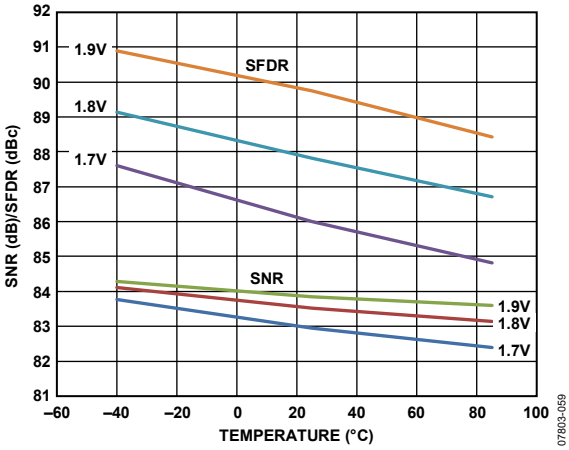


Figure 18. SFDR/SNR vs. Temperature with f_{IN} = 2.4 MHz

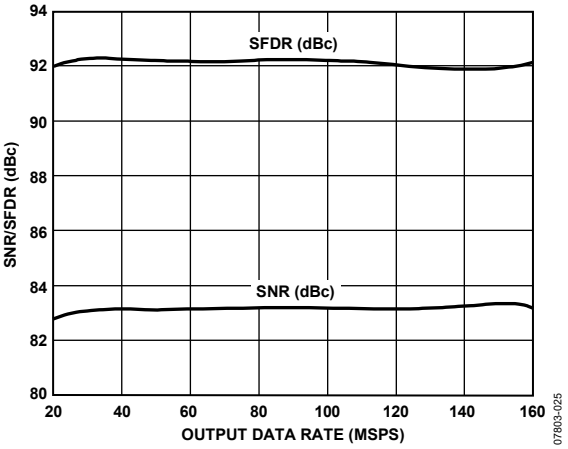


Figure 16: SNR/SFDR vs. Output Data Rate with f_{IN} = 2.4 MHz

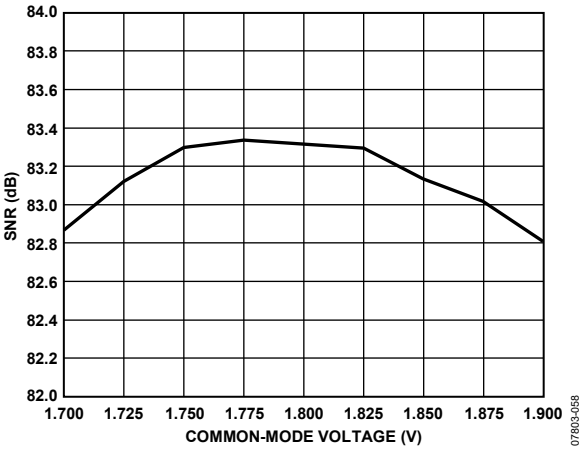


Figure 19. SNR vs. Input Common Mode Voltage with f_{IN} = 2.4 MHz

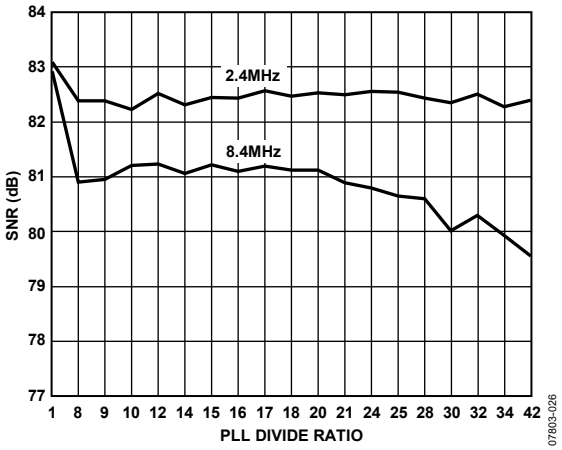


Figure 20. Single-Tone SNR vs. PLL Divide Ratio

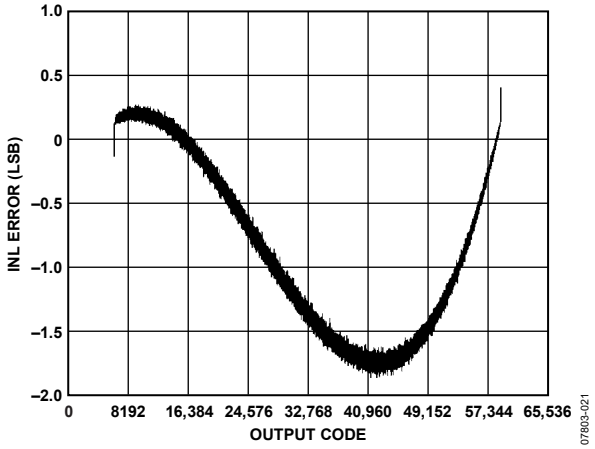


Figure 21. INL with f_{IN} = 2.4 MHz

EQUIVALENT CIRCUITS

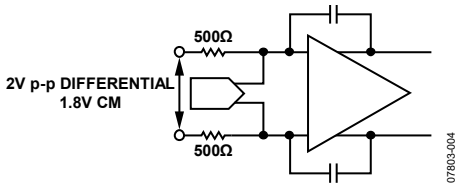


Figure 22. Equivalent Analog Input Circuit

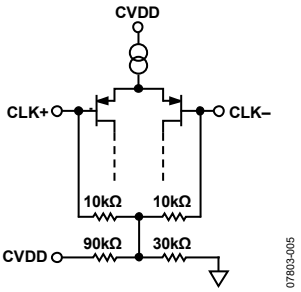


Figure 23. Equivalent Clock Input Circuit

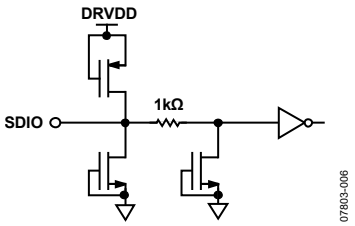


Figure 24. Equivalent SDIO Input Circuit

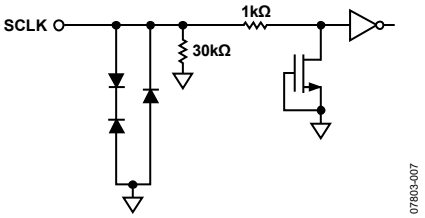


Figure 25. Equivalent SCLK Input Circuit

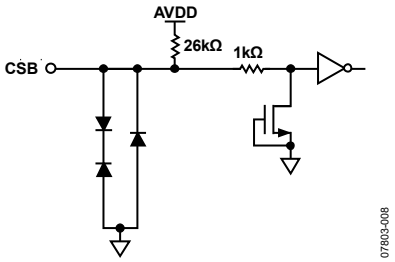


Figure 26. Equivalent CSB Input Circuit

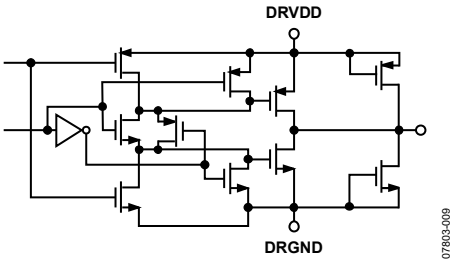


Figure 27. Equivalent Digital Output Circuit

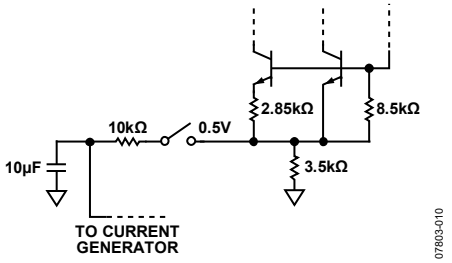


Figure 28. Equivalent VREF Circuit

THEORY OF OPERATION

The AD9261 uses a continuous time Σ-Δ modulator to convert the analog input to a digital word. The digital word is processed by the decimation filter and rate-adjusted by the sample rate converter (see Figure 29). The modulator consists of a continuous time loop filter preceding a quantizer that samples at f_{MOD} = 640 MSPS. This produces an oversampling ratio (OSR) of 32 for a 10 MHz input bandwidth. The output of the quantizer is fed back to a DAC that ideally cancels the input signal. The incomplete input cancellation residue is filtered by the loop filter and is used to form the next quantizer sample.

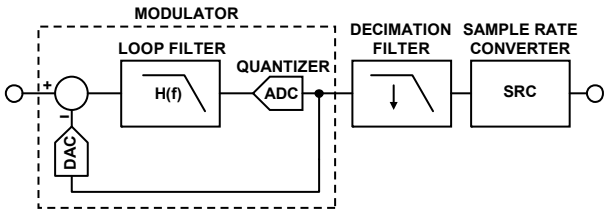


Figure 29. Σ-Δ Modulator Overview

The quantizer produces a nine-level digital word. The quantization noise is spread uniformly over the Nyquist band (see Figure 30), but the feedback loop causes the quantization noise present in the nine-level output to have a nonuniform spectral shape. This noise-shaping technique (see Figure 31) pushes the in-band noise out of band; therefore, the amount of quantization noise in the frequency band of interest is minimal.

The digital decimation filter that follows the modulator removes the large out-of-band quantization noise (see Figure 32), while also reducing the data rate from f_{MOD} to $f_{MOD}/16$. If the internal PLL is enabled, the sample rate converter generates samples at the same frequency as the input clock frequency. If the internal PLL is disabled, the sample rate converter can be programmed to give an output frequency that is a divide ratio of the modulator clock. The sample rate converter is designed to attenuate images outside the band of interest (see Figure 33).

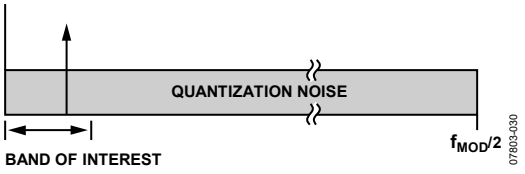


Figure 30. Quantization Noise

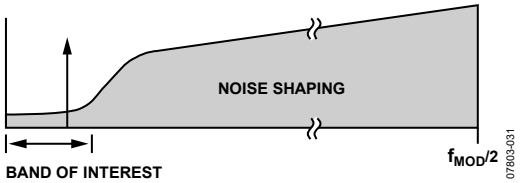


Figure 31. Noise Shaping

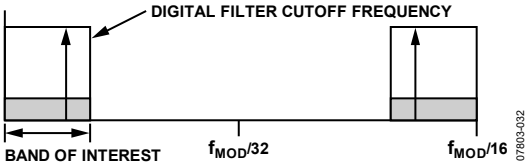


Figure 32. Digital Filter Cutoff Frequency

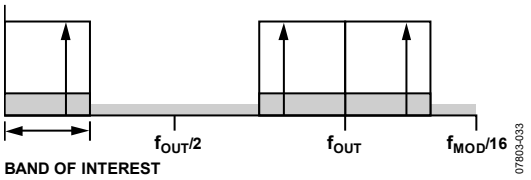


Figure 33. Sample Rate Converter

ANALOG INPUT CONSIDERATIONS

The continuous time modulator removes the need for an antialias filter at the input to the AD9261. A discrete time converter aliases signals around the sample clock frequency and its multiples to the band of interest (see Figure 34). Therefore, an external antialias filter is needed to reject these signals.

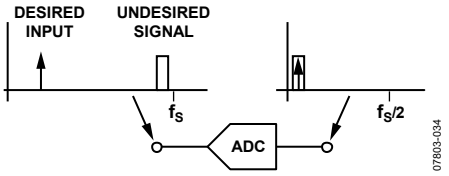


Figure 34. Discrete Time Converter

In contrast, the continuous time Σ-Δ modulator used within the AD9261 has inherent antialiasing. The antialiasing property results from sampling occurring at the output of the loop filter (see Figure 35), and thus aliasing occurs at the same point in the loop as quantization noise is injected; aliases are shaped by the same mechanism as quantization noise. The quantization noise transfer function, NTF(f), has zeros in the band of interest and in all alias bands because NTF(f) is a discrete time transfer function, whereas the loop filter transfer function, LF(f), is a continuous time transfer function, which introduces poles only in the band of interest. The signal transfer function, being the product of NTF(f) and LF(f), only has zeros in alias bands and therefore suppresses all aliases.

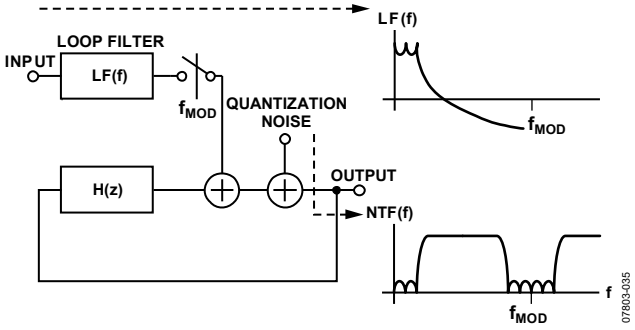


Figure 35. Continuous Time Converter

Input Common Mode

The analog inputs of the AD9261 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device such that V_{CM} = AVDD is recommended for optimum performance. The analog inputs are 500 Ω resistors, and the internal reference loop aims to develop 0.5 V across each input resistor (see Figure 36). With 0 V differential input, the driver sources 1 mA into each analog input.

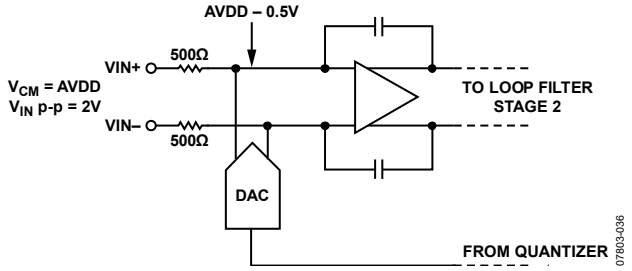


Figure 36. Input Common Mode

Differential Input Configurations

The AD9261 can also be configured for differential inputs. The ADA4937-1 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the ADA4937-1 is easily set by connecting AVDD to the V_{OCM} pin of the ADA4937-1 (see Figure 37). The noise and linearity of the ADA4937-1 needs important consideration because the system performance may be limited by the ADA4937-1.

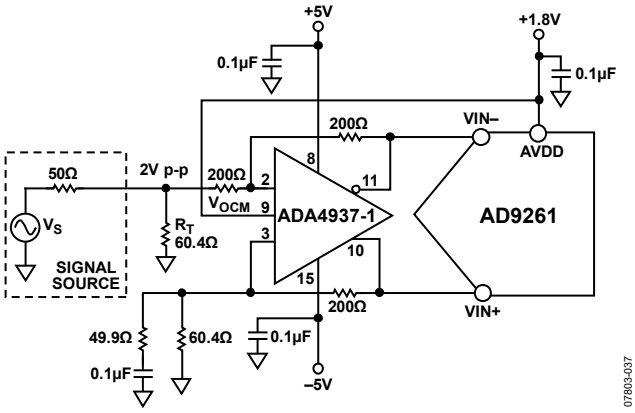


Figure 37. Differential Input Configuration Using the ADA4937-1

For frequencies offset from dc, where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 38. The center tap of the secondary winding of the transformer is connected to AVDD to bias the analog input.

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a couple of megahertz (MHz), and excessive signal power can cause core saturation, which leads to distortion.

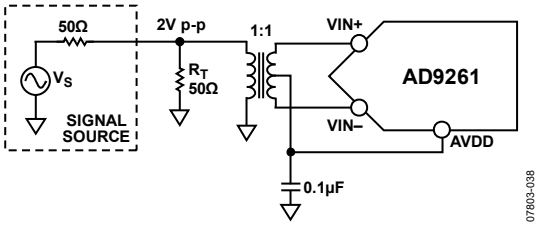


Figure 38. Differential Transformer Configuration

Voltage Reference

A stable and accurate 0.5 V voltage reference is built into the AD9261. The reference voltage should be decoupled to minimize the noise bandwidth using a 10 µF capacitor. The reference is used to generate a bias current into a matched resistor such that, when used to bias the current in the feedback DAC, a voltage
of AVDD − 0.5 V is developed at the internal side of the input resistors (see Figure 39). The current bias circuit should also be decoupled on the CFILT pin with a 10 µF capacitor. For this reason, the VREF voltage should always be 0.5 V.

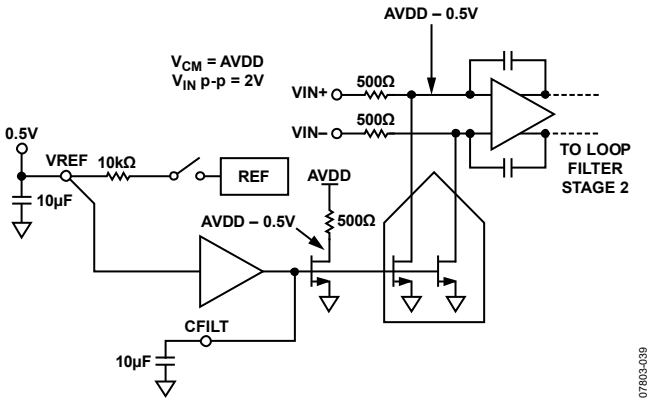


Figure 39. Voltage Reference Loop

Internal Reference Connection

To minimize thermal noise, the internal reference on the AD9261 is an unbuffered 0.5 V. It has an internal 10 kΩ series resistor, which, when externally decoupled with a 10 µF capacitor, limits the noise (see Figure 40). The unbuffered reference should not be used to drive any external circuitry. The internal reference is used by default.

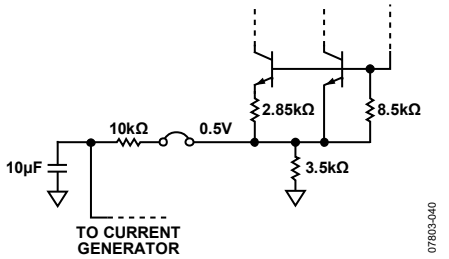


Figure 40. Internal Reference Configuration

External Reference Operation

If an external reference is desired, the internal reference can be disabled by setting Register 0x18[6] high. Figure 41 shows an application using the ADR130B as a stable external reference.

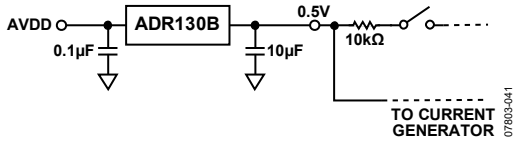


Figure 41. External Reference Configuration

CLOCK INPUT CONSIDERATIONS

The AD9261 offers two modes of sourcing the ADC sample clock (CLK+ and CLK–). The first mode uses an on-chip clock multiplier that accepts a reference clock operating at the lower input frequency. The on-chip phase-locked loop (PLL) then multiplies the reference clock up to a higher frequency, which is then used to generate all the internal clocks required by the ADC

The clock multiplier provides a high quality clock that meets the performance requirements of most applications. Using the on-chip clock multiplier removes the burden of generating and distributing the high speed clock.

The second mode bypasses the clock multiplier circuitry and allows the clock to be directly sourced. This mode enables the user to source a very high quality clock directly to the Σ-Δ modulator. Sourcing the ADC clock directly may be necessary in demanding applications that require the lowest possible ADC output noise. Refer to Figure 20, which shows the degradation in SNR performance for the various PLL settings.

In either case, when using the on-chip clock multiplier or sourcing the high speed clock directly, it is necessary that the clock source have low jitter to maximize the ADC noise performance. High speed, high resolution ADCs are sensitive to the quality of the clock input. As jitter increases, the SNR performance of the AD9261 degrades from that specified in Table 2. The jitter inherent to the part due to the PLL root sum squares with any external clock jitter, thereby degrading performance. To prevent jitter from dominating the performance of the AD9261, the input clock source should be no greater than 1 ps rms of jitter.

The CLK± inputs are self-biased to 450 mV (see Figure 23); if dc-coupled, it is important to maintain the specified 450 mV input common-mode voltage. Each input pin can safely swing from 200 mV p-p to 1 V p-p single-ended about the 450 mV common-mode voltage. The recommended clock inputs are CMOS or LVPECL.

The specified clock rate of the Σ-Δ modulator, f_{MOD}, is 640 MHz. The clock rate possesses a direct relationship with the available input bandwidth of the ADC.

$$Bandwidth = f_{MOD} \div 64$$

In either case, using the on-chip clock multiplier to generate the Σ-Δ modulator clock rate or directly sourcing the clock, any deviation from 640 MHz results in a change in input bandwidth. The input range of the clock is limited to 640 MHz ± 5%.

Direct Clocking

The default configuration of the AD9261 is for direct clocking where the PLL is bypassed. Figure 42 shows one preferred method for clocking the AD9261. A low jitter clock source is converted from a single-ended signal to a differential signal using an RF transformer. The back-to-back Schottky diodes across the secondary side of the transformer limits clock excursions into the AD9261 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9261 while preserving the fast rise and fall times of the signal, which are critical to achieving low jitter.

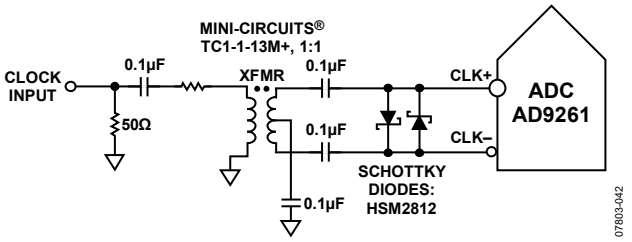


Figure 42. Transformer-Coupled Differential Clock

If a differential clock is not available, the AD9261 can be driven by a single-ended signal into the CLK+ terminal with the CLK– terminal ac-coupled to ground. Figure 43 shows the circuit configuration.

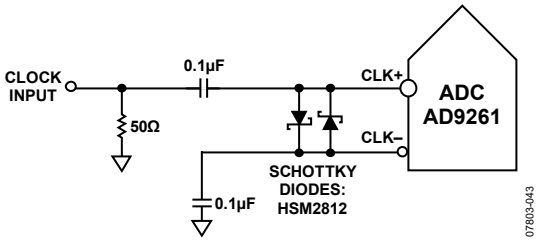
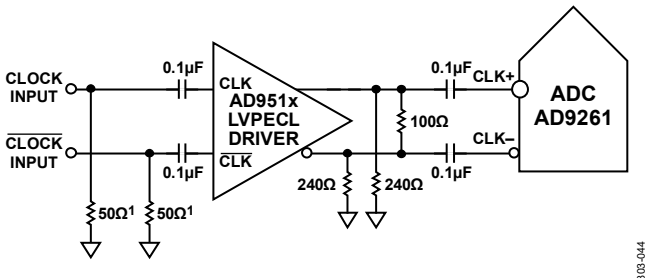


Figure 43. Single-Ended Clock

Another option is to ac couple a differential LVPECL signal to the sample clock input pins, as shown in Figure 44. The AD951x family of clock drivers is recommended because it offers excellent jitter performance.



1 50Ω RESISTORS ARE OPTIONAL.

Figure 44. Differential LVPECL Sample Clock

Internal PLL Clock Distribution

The alternative clocking option available on the AD9261 is to apply a low frequency reference clock and use the on-chip clock multiplier to generate the high frequency f_{MOD} rate. The internal clock architecture is shown in Figure 45.

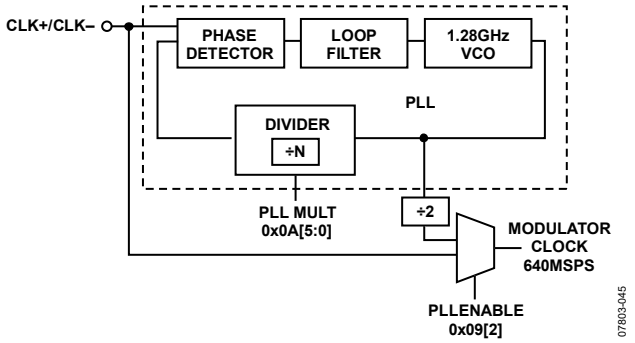


Figure 45. Internal Clock Architecture

The clock multiplication circuit operates such that the VCO outputs a frequency, f_{VCO}, equal to the reference clock input multiplied by N

$$f_{VCO} = (CLK\pm) \times (N)$$

where *N* is the PLL multiplication (PLLMULT) factor.

The Σ-Δ modulator clock frequency, f_{MOD}, is equal to

$$f_{MOD} = f_{VCO} \div 2$$

The reference clock, CLK±, is limited to 30 MHz to 160 MHz when configured to use the on-chip clock multiplier. Given the input range of the reference clock and the available multiplication factors, the f_{VCO} is approximately 1280 MHz. This results in the desired f_{MOD} rate of 640 MHz with a 50% duty cycle.

Before the PLL enable (PLLENABLE) register bit is set, the PLL multiplication factor should be programmed into Register 0x0A[5:0]. After setting the PLLENABLE bit, the PLL locks and reports a locked state in Register 0x0A[7]. If the PLL multiplication factor is changed, the PLL enable bit should be reset and set again. Some common clock multiplication factors are shown in Table 11.

The recommended sequence for enabling and programming the on-chip clock multiplier is summarized in Table 9.

Table 9. Sequence for Enabling and Programming the PLL

Step	Procedure
1	Apply a reference clock to the CLK± pins.
2	Program the PLL multiplication factor in Register 0x0A[5:0]. See Table 10.
3	Enable the PLL; Register 0x09 = 04 (decimal).
4	Enable the PLL autoband select.
5	Initiate an SRC reset; Register 0x101[5:0] = 0.
6	Set SRC to the desired value via Register 0x101[5:0].

Table 10. Internal PLL Multiplication Factors

0x0A[5:0]	PLLMULT (N)	0x0A[5:0]	PLLMULT (N)
1	8	33	32
2	8	34	34
3	8	35	34
4	8	36	34
5	8	37	34
6	8	38	34
7	8	39	34
8	8	40	34
9	9	41	34
10	10	42	42
11	10	43	42
12	12	44	42
13	12	45	42
14	14	46	42
15	15	47	42
16	16	48	42
17	17	49	42
18	18	50	42
19	18	51	42
20	20	52	42
21	21	53	42
22	21	54	42
23	21	55	42
24	24	56	42
25	25	57	42
26	25	58	42
27	25	59	42
28	28	60	42
29	28	61	42
30	30	62	42
31	30	63	42
32	32	64	42

External PLL Control

At power-up, the serial interface is disabled until the first serial port access. If the serial interface is disabled, the PLLMULTx pins control the PLL multiplication factor. The five PLLMULTx pins (Pin 32 to Pin 36) offer all the available multiplication factors. If all PLLMULTx pins are tied high, the PLL is disabled and the AD9261 assumes the high frequency modulator clock rate that is applied to the CLK± pins. Table 12 shows the relationship between PLLMULTx pins and the PLL multiplication factor.

PLL Autoband Select

The PLL VCO has a wide operating range that is covered by overlapping frequency bands. For any desired VCO output frequency, there are multiple valid PLL band select values. The AD9261 possesses an automatic PLL band select feature on chip that determines the optimal PLL band setting. This feature can be enabled by writing to Register 0x0A[6] and is the recommended configuration with the PLL clocking option. Follow the sequence shown in Table 9 for enabling the autoband select and configuring the PLL.

When the device is taken out of sleep or standby mode, Register 0x0A[6] must be toggled to reinitiate the autoband detect.

Table 11. Common Modulator Clock Multiplication Factors

CLK± (MHz)	0x0A[5:0] (PLLMULT)	f_{VCO} (MHz)	f_{MOD} (MHz)	BW (MHz)
30.72	42	1290.24	645.12	10.08
39.3216	32	1258.29	629.15	9.83
52.00	25	1300.00	650.00	10.16
61.44	21	1290.24	645.12	10.08
76.80	17	1305.60	652.80	10.20
78.00	17	1326.00	663.00	10.36
78.6432	16	1258.29	629.15	9.83
89.60	15	1344.00	672.00	10.50
92.16	14	1290.24	645.12	10.08
122.88	10	1228.80	614.40	9.60
134.40	10	1344.00	672.00	10.50
153.60	8	1228.80	614.40	9.60
157.2864	8	1258.29	629.15	9.83

Table 12. External PLLMULTx Pins and PLL Multiplication Factor

PLLMULTx[4:0] Pins	PLL Multiplication Factors (N)
0	8
1	9
2	10
3	12
4	14
5	15
6	16
7	17
8	18
9	20
10	21
11	24
12	25
13	28
14	30
15	32
16	34
17 to 30	42
31	Direct clocking

Jitter Considerations

The aperture jitter requirements for continuous time Σ-Δ converters may be more forgiving than Nyquist rate converters. The continuous time Σ-Δ architecture is an oversampled system, and to accurately represent the analog input signal to the ADC, a large number of output samples must be averaged together. As a result, the jitter contribution from each sample is root sum squared, resulting in a more subtle impact on noise performance as compared to Nyquist converters where aperture jitter has a direct impact on each sampled output.

In the block diagram of the continuous time Σ-Δ modulator (see Figure 29), the two building blocks most susceptible to jitter are the quantizer and the DAC. The error introduced through the sampling process or quantizer is reduced by the loop gain and shaped in the same way as the quantization noise and, therefore, its effect can be neglected. On the contrary, the jitter error associated to the DAC directly adds to the input signal, thus increasing the in-band noise power and degrading the modulator performance. The SNR degradation due to jitter can be represented by the following equation:

$$SNR = -20 \log (2\pi f_{analog} t_{jitter\_rms}) \text{ dB}$$

where f_{analog} is the analog input frequency and t_{jitter_rms} is the jitter.

The SNR performance of the AD9261 remains constant within the input bandwidth of the converter, from dc to 10 MHz. Therefore, the minimal jitter specification is determined at the highest input frequency. From the calculation, the aperture jitter of the input clock must be no greater than 1 ps to achieve optimal SNR performance.

POWER DISSIPATION AND STANDBY MODE

The AD9261 power consumption can be further reduced by configuring the chip in channel power-down, standby, or sleep mode. The low power modes turn off internal blocks of the chip including the reference. As a result, the wake-up time is dependent on the amount of circuitry that is turned off. Fewer internal circuits that are powered down result in proportionally shorter wake-up time. The different low power modes are shown in Table 13. In the standby mode, all clock related activity and the output channels are disabled. Only the references and CMOS outputs remain powered up to ensure a short recovery and link integrity. During sleep mode, all internal circuits are powered down, putting the device into its lowest power mode, and the CMOS outputs are disabled.

If the serial port interface is not available, the AD9261 can be configured in power-down mode by connecting Pin 3 (PDWN) to AVDD.

Table 13. Low Power Modes

Mode	0x08[1:0]	Analog Circuitry	Clock	Ref
Normal	0x0	On	On	On
Power-Down	0x1	Off	On	On
Standby	0x2	Off	Off	On
Sleep	0x3	Off	Off	Off

DIGITAL ENGINE

Bandwidth Selection

The digital engine (see Figure 46) selects the decimation signal bandwidth by cascading third-order sinc (sinc^3) decimate-by-2 filters. For a 10 MHz signal band, no filters are cascaded; for a 5 MHz signal band, a single filter is used; and for a 2.5 MHz signal band, the 5 MHz filter is cascaded with a second filter. Depending on the signal bandwidth, this drops the data rate into the fixed decimation filter. As a result, lower signal bandwidth options result in lower power. Bandwidth selection is determined by setting Register 0x0F[6:5].

Decimation Filters

A fixed frequency low-pass filter is used to define the signal band. This filter incorporates magnitude equalization for the droop of the preceding sinc decimation filters and the sinc filters of the sample rate converter. Table 14 and Table 15 detail the coefficients for the DEC4 and LPF/EQZ filters. The preceding sinc decimation filters are a standard sinc filter implementation.

Table 14. DEC4 Filter Coefficients

Coefficient Number	Coefficient	Coefficient Number	Coefficient
C0, C22	−21	C6, C16	1121
C1, C21	0	C7, C15	0
C2, C20	122	C8, C14	−2796
C3, C19	0	C9, C13	0
C4, C18	−418	C10, C12	10,184
C5, C17	0	C11	16,384

Table 15. LPF/EQZ Filter Coefficients

Coefficient Number	Coefficient	Coefficient Number	Coefficient
C0, C62	17	C16, C46	694
C1, C61	31	C17, C45	−744
C2, C60	−15	C18, C44	−677
C3, C59	−52	C19, C43	1271
C4, C58	36	C20, C42	450
C5, C57	78	C21, C41	−1909
C6, C56	−84	C22, C40	103
C7, C55	−98	C23, C39	2612
C8, C54	170	C24, C38	−1147
C9, C53	97	C25, C37	−3326
C10, C52	−291	C26, C36	3022
C11, C51	−42	C27, C35	4051
C12, C50	441	C28, C34	−6870
C13, C49	−98	C29, C33	−5305
C14, C48	−592	C30, C32	21,141
C15, C47	353	C31	38,956

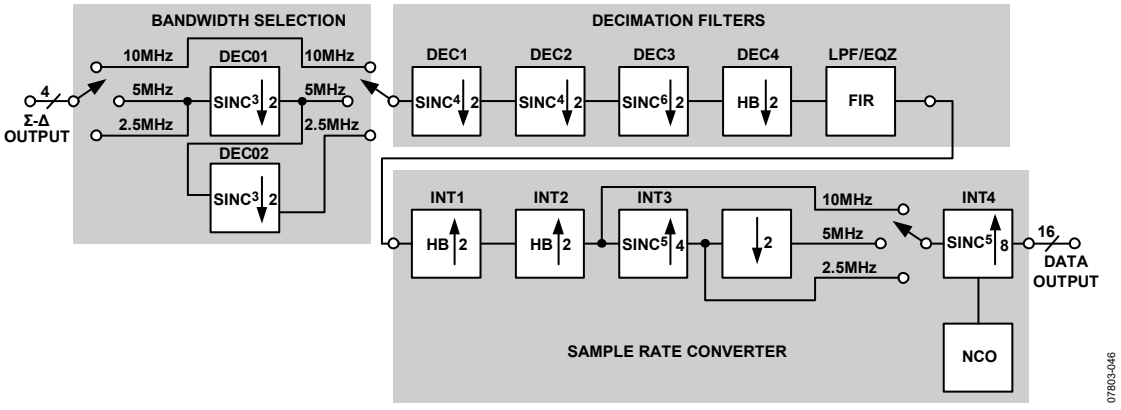


Figure 46. Digital Engine

Sample Rate Converter

The sample rate converter (SRC) allows the flexibility of a user-defined output sample rate, enabling a more efficient and direct interface to the digital receiver blocks.

The sample rate converter performs an interpolation and resampling procedure to provide an output data rate of 20 MSPS to 168 MSPS. Table 16 and Table 17 detail the coefficients for the INT1 and INT2 filters. The sinc filters are a standard implementation.

Table 16. INT1 Filter Coefficients

Coefficient Number	Coefficient	Coefficient Number	Coefficient
C0, C26	15	C7, C19	0
C1, C25	0	C8, C18	2450
C2, C24	−97	C9, C17	0
C3, C23	0	C10, C16	−5761
C4, C22	361	C11, C15	0
C5, C21	0	C12, C14	20433
C6, C20	−1017	C13	32768

Table 17. INT2 Filter Coefficients

Coefficient Number	Coefficient	Coefficient Number	Coefficient
C0, C14	−27	C4, C10	−1032
C1, C13	0	C5, C9	0
C2, C12	227	C6, C8	4928
C3, C11	0	C7	8192

The relationship between the output sample rate and the Σ-Δ modulator clock rate is expressed as follows:

$$f_{OUT} = f_{MOD} \div K_{OUT}$$

Table 18 shows the available K_{OUT} conversion factors.

If the main clocking source of the AD9261 is provided by the PLL, it is important that once the PLL has been programmed and locked, to initiate an SRC reset before programming the desired K_{OUT} factor. This is done by first writing 0x101[5:0] = 0 and then rewriting to the same register with the appropriate K_{OUT} value. In addition, if the AD9261 loses its clock source and then later regains it, an SRC reset should be initiated.

Table 18. SRC Conversion Factors

0x101[5:0]	K_{OUT}	0x101[5:0]	K_{OUT}	0x101[5:0]	K_{OUT}
0	SRC reset	22	11	44	22
1	4	23	11.5	45	22.5
2	4	24	12	46	23
3	4	25	12.5	47	23.5
4	4	26	13	48	24
5	4	27	13.5	49	24.5
6	4	28	14	50	25
7	4	29	14.5	51	25.5
8	4	30	15	52	26
9	4.5	31	15.5	53	26.5
10	5	32	16	54	27
11	5.5	33	16.5	55	27.5
12	6	34	17	56	28
13	6.5	35	17.5	57	28.5
14	7	36	18	58	29
15	7.5	37	18.5	59	29.5
16	8	38	19	60	30
17	8.5	39	19.5	61	30.5
18	9	40	20	62	31
19	9.5	41	20.5	63	31.5
20	10	42	21		
21	10.5	43	21.5		

Cascaded Filter Responses

The cascaded filter responses for the three signal bandwidth settings are for a 160 MSPS output data rate, as shown in Figure 47, Figure 48, and Figure 49.

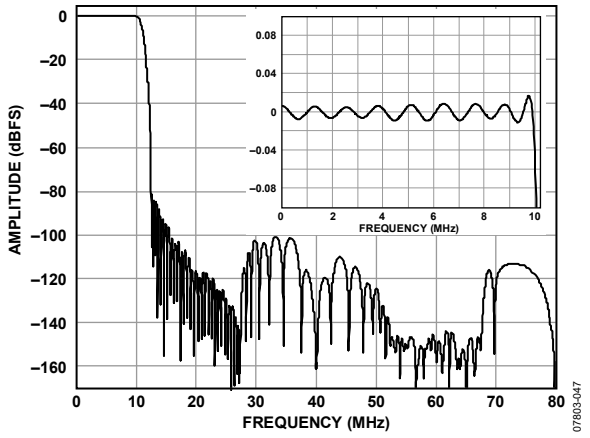


Figure 47. 10 MHz Signal Bandwidth, 160 MSPS

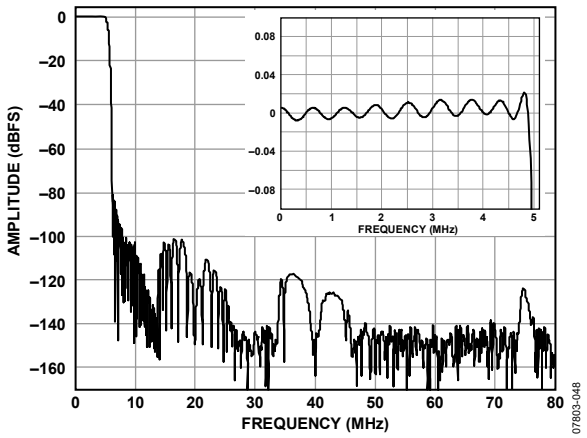


Figure 48. 5 MHz Signal Bandwidth, 160 MSPS

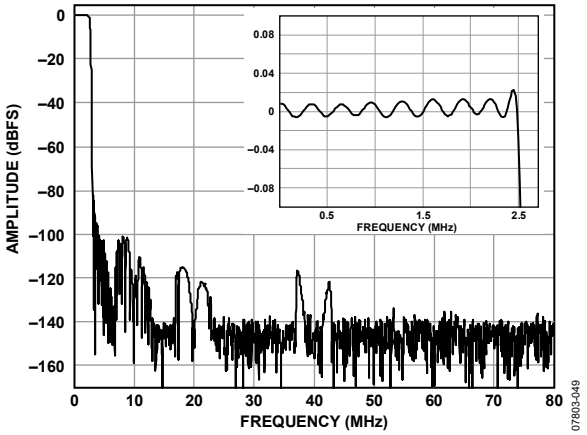


Figure 49. 2.5 MHz Signal Bandwidth, 160 MSPS

DIGITAL OUTPUTS

Digital Output Format

The AD9261 offers a variety of digital output formats for ease of system integration. The digital output consists of 16 data bits and an output clock signal (DCO) for data latching. The data bits can be configured for offset binary, twos complement, or Gray code by writing to Register 0x14[1:0]. In addition, the voltage swing of the digital outputs can be configured to 3.3 V TTL levels or a reduced voltage swing of 1.8 V by accessing Register 0x14[7]. When 3.3 V voltage levels are desirable, the DRVDD power supply must be set to 3.3 V.

Overrange (OR) Condition

The OR pin serves as an indicator for an overrange condition. The OR pin is triggered by in-band signals that exceed the full-scale range of the ADC. In addition, the AD9261 possesses out-of-band gain above 10 MHz; therefore, a large out-of-band signal may trip an overrange condition.

The OR pin is a synchronous output that is updated at the output data rate. Ideally, OR should be latched on the falling edge of DCO to ensure proper setup-and-hold time. However, because an overrange condition typically extends well beyond one clock cycle—that is, it does not toggle at the DCO rate—data can usually be successfully detected on the rising edge of DCO or monitored asynchronously.

The AD9261 has two trip points that can trigger an overrange condition: analog and digital. The analog trip point is located in the modulator, and the second trip point is in the digital engine. In normal operation, it is possible for the analog trip point to toggle the OR pin for a number of clock cycles as the analog input approaches full scale. Because the OR pin is a pulse-width modulated (PWM) signal, as the analog input increases in amplitude, the duration of overrange pin toggling increases. Eventually, when the OR pin is high for an extended period of time, the ADC is overloaded, and there is little correspondence between analog input and digital output.

The second trip point is in the digital block. If the input signal is large enough to cause the data bits to clip to the maximum full-scale level, an overrange condition occurs. The overrange trip point can be adjusted by specifying a threshold level.

Table 19 shows the corresponding threshold level in dBFS vs. register setting. If the input signal crosses this level, the OR pin is set. In the case where 0x111[5:0] is set to all 0s, the threshold level is set to the maximum code of $32{,}767_{10}$. This feature provides a means of reporting the instantaneous amplitude as it crosses a user-provided threshold. This gives the user a sense for the signal level without needing to perform a full power measurement.

The user has the ability to select how the overrange conditions are reported, and this is controlled through Register 0x111 via AUTORST, OR_IND, and ORTHRESH (see Table 20). By enabling the AUTORST bit, Register 0x111[7], if an overrange occurs, the ADC automatically resets itself. The OR pin remains high until the automatic reset has completed. If an analog trip occurs, the modulator resets itself after 16 consecutive clock cycles of overrange.

If the AD9261 is used in a system that incorporates automatic gain control (AGC), the OR signal can be used to indicate that the signal amplitude should be reduced. This may be particularly effective for use in maximizing the signal dynamic range if the signal includes high occurrence components that occasionally exceed full scale by a small amount.

TIMING

The AD9261 provides a data clock out (DCO) pin to assist in capturing the data in an external register. The data outputs are valid on the rising edge of DCO, unless changed by setting Register 0x16[7]. See Figure 2 for a graphical timing description.

Table 19. OR Threshold Levels

0x111[5:0]	Threshold (dBFS)	0x111[5:0]	Threshold (dBFS)	0x111[5:0]	Threshold (dBFS)
1	−36.12	16	−9.28	2B	−3.45
2	−30.10	17	−8.89	2C	−3.25
3	−26.58	18	−8.52	2D	−3.06
4	−24.08	19	−8.16	2E	−2.87
5	−22.14	1A	−7.82	2F	−2.68
6	−20.56	1B	−7.50	30	−2.50
7	−19.22	1C	−7.18	31	−2.32
8	−18.06	1D	−6.88	32	−2.14
9	−17.04	1E	−6.58	33	−1.97
A	−16.12	1F	−6.30	34	−1.80
B	−15.29	20	−6.02	35	−1.64
C	−14.54	21	−5.75	36	−1.48
D	−13.84	22	−5.49	37	−1.32
E	−13.20	23	−5.24	38	−1.16
F	−12.60	24	−5.00	39	−1.00
10	−12.04	25	−4.76	3A	−0.86
11	−11.51	26	−4.53	3B	−0.71
12	−11.02	27	−4.30	3C	−0.56
13	−10.56	28	−4.08	3D	−0.42
14	−10.10	29	−3.87	3E	−0.28
15	−9.68	2A	−3.66	3F	−0.14

Table 20. OR Conditions

OR Conditions	AUTORST	OR_IND	ORTHRESH[5:0]	ORTHRESH[4:0]	Description
Normal, Reset Off	0	0	0	00000	Digital trip: if 16-bit output > 32,767, OR = 1, else OR = 0
Digital Threshold, Reset Off	0	0	>0		Digital threshold: If 16-bit output > ORTHRESH, OR = 1, else OR = 0
Full Overrange, Reset Off	0	1	0	X[1]	If analog trip or digital trip, OR = 1, else OR = 0
Data Valid, No Reset	0	1	1	X[1]	If analog trip or digital trip or calibration, OR = 0, else OR = 1
Normal, Reset On	1	0	0	00000	Digital trip: if 16-bit output > 32,767, OR = 1, else OR = 0
Digital Threshold, Reset On	1	0	>0		Digital threshold: if 16-bit output > ORTHRESH, OR = 1, else OR = 0
Full Overrange, Reset On	1	1	0	X[1]	If analog trip or digital trip, OR = 1, else OR = 0
Data Valid, Reset On	1	1	1	X[1]	If analog trip or digital trip or calibration, OR = 0 else OR = 1

[1] X = don't care.

SERIAL PORT INTERFACE (SPI)

The AD9261 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This provides the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that are further divided into fields, as documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

As summarized in Table 21, three pins define the SPI of this ADC. The SCLK pin synchronizes the read and write data presented to the ADC. The SDIO pin allows data to be sent and read from the internal ADC memory map registers. The CSB pin is an active low control that enables or disables the read and write cycles.

Table 21. Serial Port Interface Pins

Pin Name	Description
SCLK	SCLK (serial clock) is the serial shift clock. SCLK synchronizes serial interface reads and writes.
SDIO	SDIO (serial data input/output) is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (chip select bar) is an active low control that gates the read and write cycles.

The falling edge of CSB in conjunction with the rising edge of SCLK determines the start of the framing. Figure 50 and Table 22 provide an example of the serial timing and its definitions.

Other modes involving CSB are available. CSB can be held low indefinitely to permanently enable the device (this is called streaming). CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in a high impedance mode.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase and the length is determined by the W0 bit and the W1 bit. All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip as well as to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/
output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB-first or in LSB-first mode. MSB first is the default setting on power-up and can be changed via the configuration register. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Table 22. SPI Timing Diagram Specifications

Parameter	Description
t_{SDS}	Setup time between data and rising edge of SCLK
t_{SDH}	Hold time between data and rising edge of SCLK
t_{SCLK}	Period of the clock
t_{SS}	Setup time between CSB and SCLK
t_{SH}	Hold time between CSB and SCLK
t_{SHIGH}	Minimum period that SCLK should be in a logic high state
t_{SLOW}	Minimum period that SCLK should be in a logic low state

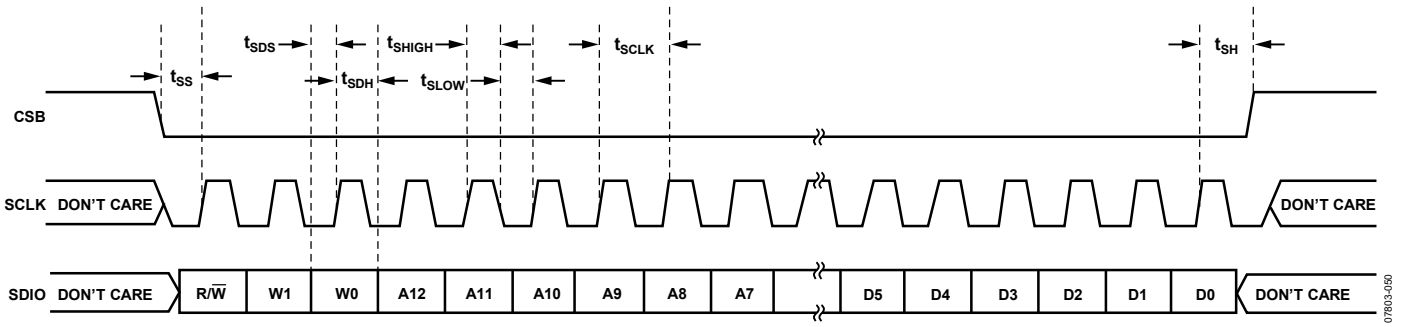


Figure 50. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 21 comprise the physical interface between the programming device of the user and the serial port of the AD9261. The SCLK and CSB pins function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either PROM or PIC microcontrollers. This provides the user with the ability to use an alternate method to program the ADC. One such method is described in detail in the AN-812 Application Note, *MicroController-Based Serial Port Interface (SPI) Boot Circuit*.

When the SPI interface is not used, some pins serve a dual function. When strapped to AVDD or ground during device power-on, the pins are associated with a specific function.

MEMORY MAP

Table 23. Memory Map

Register Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Port Config	0x00	0	LSBFIRST	SOFTRESET	1	1	SOFTRESET	LSBFIRST	0
Chip ID	0x01	CHIPID[7:0]							
Chip Grade	0x02			CHILDID[2:0]					
Power Modes	0x08							PWRDWN[1:0]	
PLLENABLE	0x09						PLLENABLE		
PLL	0x0A	PLLLOCKED	PLLAUTO	PLLMULT[5:0]					
Analog Input	0x0F		BW[1:0]						
Output Modes	0x14	DRVSTD		Interleave	OUTENB		OUTINV	Format[1:0]	
Output Adjust	0x15					DRVSTR33[1:0]		DRVSTR18[1:0]	
Output Clock	0x16	DCOINV							
Reference	0x18		EXTREF						
Output Data	0x101			K_{OUT}[5:0]					
Overrange	0x111	AUTORST	OR_IND	ORTHRESH[5:0]					

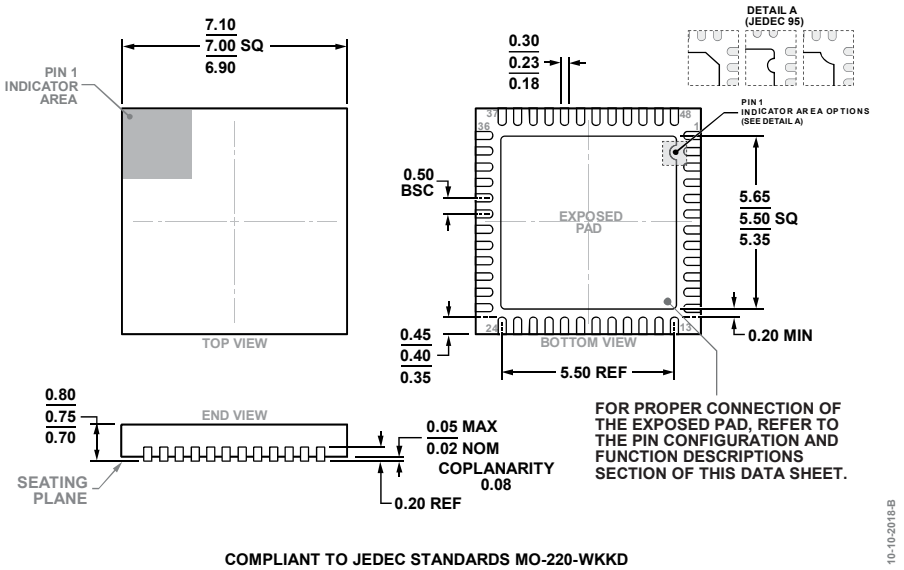
MEMORY MAP DEFINITIONS

Table 24. Memory Map Definitions

Register	Address	Bit(s)	Mnemonic	Default	Description
SPI Port Config	0x00	6, 1	LSBFIRST	0	0: serial interface uses MSB first format 1: serial interface uses LSB first format
		5, 2	SOFTRESET	0	1: default all serial registers except 0x00, 0x09, and 0x0A
Chip ID	0x01	[7:0]	CHIPID	0x26	0x26: AD9261
Chip Grade	0x02	[5:4]	CHILDID	0	0x00: 10 MHz bandwidth
Power Modes	0x08	[1:0]	PWRDWN	0	0x0: normal operation 0x1: power-down (local) 0x2: standby (everything except reference circuits) 0x3: sleep
PLLENABLE	0x09	2	PLLENABLE	0	1: enable PLL
PLL	0x0A	7	PLLLOCKED	0	0: PLL is not locked 1: PLL is locked
		6	PLLAUTO	0	1: PLL autoband enabled
		[5:0]	PLLMULT	0	See Table 10
Analog Input	0x0F	[6:5]	BW	0	0x0: 10 MHz 0x1: 5 MHz 0x2: 2.5 MHz 0x3: 10 MHz
Output Modes	0x14	7	DRVSTD	0	0: 3.3 V 1: 1.8 V
		5	Interleave	0	1: interleave both channels onto D[15:0]
		4	OUTENB	0	1: data outputs tristated
		2	OUTINV	0	1: data outputs bitwise inverted
		[1:0]	Format	0	0: offset binary 1: twos complement 2: Gray code 3: offset binary

Register	Address	Bit(s)	Mnemonic	Default	Description
Output Adjust	0x15	[3:2]	DRVSTR33	0	Typical output sink current to DGND 0: 33 mA 1: 63 mA 2: 93 mA 3: 120 mA
		[1:0]	DRVSTR18	2	Typical output sink current to DGND 0: 10 mA 1: 20 mA 2: 30 mA 3: 39 mA
Output Clock	0x16	7	DCOINV	0	1: invert DCO
Reference	0x18	6	EXTREF	0	1: use external reference
Output Data	0x101	[5:0]	K_{OUT}	0	Output data rate, see Table 18
Overrange	0x111	7	AUTORST	0	1: enable loop filter reset indicator on OR pin
		6	OR_IND	0	See Table 20
		[5:0]	ORTHRESH	0	See Table 19

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WKKD

Figure 51. 48-Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9261BCPZ-10	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP)	CP-48-9
AD9261BCPZRL7-10	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package (LFCSP)	CP-48-9
AD9261-10EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D07803-9/20(A)