# Dual-Current Output, Parallel Input, 16-Bit Multiplying DAC with 4-Quadrant Resistors

Data Sheet

# AD5547-EP

## FEATURES

- Dual channel
- 16-bit resolution: AD5547-EP
- 2- or 4-quadrant, 6.8 MHz bandwidth multiplying DAC
- ±1 LSB DNL
- ±2 LSB INL
- Operating supply voltage: 2.7 V to 5.5 V
- Low noise: 12 nV/√Hz
- Low power: $I_{DD}$ = 10 µA maximum
- 0.5 µs settling time
- Built-in $R_{FB}$ facilitates current-to-voltage conversion
- Built-in 4-quadrant resistors allow 0 V to −10 V, 0 V to +10 V, or ±10 V outputs
- 2 mA full-scale current ± 20%, with $V_{REF}$ = 10 V
- Extended automotive operating temperature range −55°C to +125°C
- Selectable zero-scale/midscale power-on presets
- Compact 38-lead TSSOP package

## ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (such as −55°C to +125°C).
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

## APPLICATIONS

- Automatic test equipment
- Instrumentation
- Digitally controlled calibration
- Digital waveform generation

## FUNCTIONAL BLOCK DIAGRAM

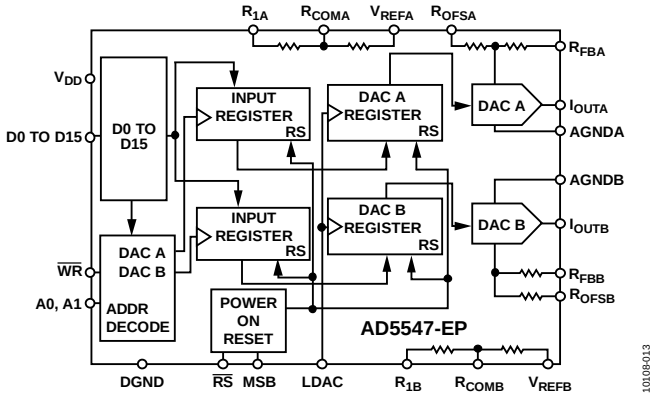


*Figure 1.*

## GENERAL DESCRIPTION

The AD5547-EP is a dual precision, 16-bit, multiplying, low power, current-output, parallel input, digital-to-analog converter (DAC). It is designed to operate from a single +5 V supply with ±10 V multiplying references for 4-quadrant outputs with a 6.8 MHz bandwidth.

The built-in, 4-quadrant resistors facilitate resistance matching and temperature tracking, which minimize the number of components needed for multiquadrant applications. In addition, the feedback resistor ($R_{FB}$) simplifies the I-to-V conversion with an external buffer.

The AD5547-EP is available in a compact, 38-lead TSSOP package and operates at the extended automotive temperature range of −55°C to +125°C. Additional application and technical information can be found in the AD5547 data sheet.

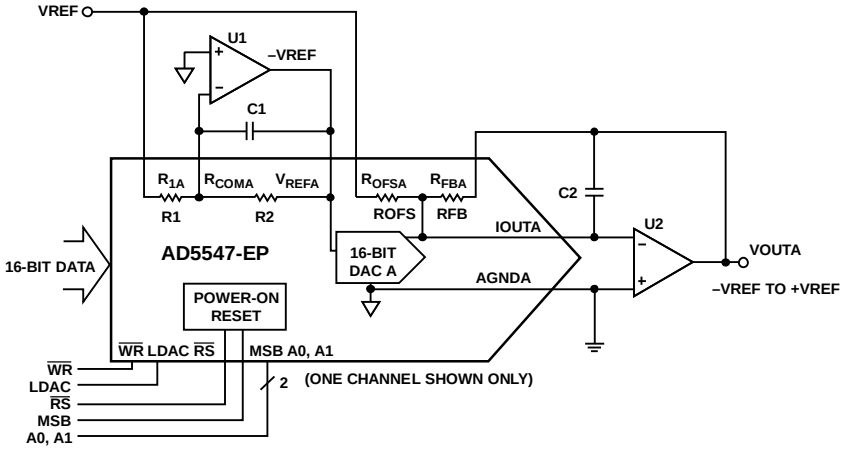


*Figure 2. 16-Bit 4-Quadrant Multiplying DAC with Minimum of External Components (Only One Channel Is Shown)*

**Rev. 0**



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## REVISION HISTORY

**9/11—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 2.7 V to 5.5 V, $I_{OUT}$ = virtual GND, GND = 0 V, $V_{REF}$ = −10 V to +10 V, $T_A$ = −55°C to +125°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| STATIC PERFORMANCE[1] | | | | | | |
| Resolution | N | 1 LSB = $V_{REF}/2^{16}$ = 153 µV at $V_{REF}$ = 10 V | | 16 | | Bits |
| Relative Accuracy | INL | | | | ±2 | LSB |
| Differential Nonlinearity | DNL | Monotonic | | | ±1 | LSB |
| Output Leakage Current | $I_{OUT}$ | Data = zero scale, $T_A$ = 25°C | | | 10 | nA |
| | | Data = zero scale, $T_A$ = $T_A$ maximum | | | 20 | nA |
| Full-Scale Gain Error | $G_{FSE}$ | Data = full scale | | ±1 | ±5 | mV |
| Bipolar Mode Gain Error | $G_E$ | Data = full scale | | ±1 | ±5 | mV |
| Bipolar Mode Zero-Scale Error | $G_{ZSE}$ | Data = full scale | | ±1 | ±4 | mV |
| Full-Scale Temperature Coefficient[2] | $TCV_{FS}$ | | | 1 | | ppm/°C |
| REFERENCE INPUT | | | | | | |
| $V_{REF}$ Range | $V_{REF}$ | | −18 | | +18 | V |
| REF Input Resistance | REF | | 4 | 5 | 6 | kΩ |
| R1 and R2 Resistance | R1 and R2 | | 4 | 5 | 6 | kΩ |
| R1-to-R2 Mismatch | Δ(R1 to R2) | | | ±0.5 | ±1.5 | Ω |
| Feedback and Offset Resistance | $R_{FB}$, $R_{OFS}$ | | 8 | 10 | 12 | kΩ |
| Input Capacitance[2] | $C_{REF}$ | | | 5 | | pF |
| ANALOG OUTPUT | | | | | | |
| Output Current | $I_{OUT}$ | Data = full scale | | 2 | | mA |
| Output Capacitance[2] | $C_{OUT}$ | Code dependent | | 200 | | pF |
| LOGIC INPUT AND OUTPUT | | | | | | |
| Logic Input Low Voltage | $V_{IL}$ | $V_{DD}$ = 5 V | | | 0.8 | V |
| | | $V_{DD}$ = 3 V | | | 0.4 | V |
| Logic Input High Voltage | $V_{IH}$ | $V_{DD}$ = 5 V | 2.4 | | | V |
| | | $V_{DD}$ = 3 V | 2.1 | | | V |
| Input Leakage Current | $I_{IL}$ | | | | 10 | µA |
| Input Capacitance[2] | $C_{IL}$ | | | | 10 | pF |
| INTERFACE TIMING[2, 3] | | See Figure 3 | | | | |
| Data to $\overline{WR}$ Setup Time | $t_{DS}$ | $V_{DD}$ = 5 V | 20 | | | ns |
| | | $V_{DD}$ = 3 V | 35 | | | ns |
| Data to $\overline{WR}$ Hold Time | $t_{DH}$ | $V_{DD}$ = 5 V | 0 | | | ns |
| | | $V_{DD}$ = 3 V | 0 | | | ns |
| $\overline{WR}$ Pulse Width | $t_{\overline{WR}}$ | $V_{DD}$ = 5 V | 20 | | | ns |
| | | $V_{DD}$ = 3 V | 35 | | | ns |
| LDAC Pulse Width | $t_{LDAC}$ | $V_{DD}$ = 5 V | 20 | | | ns |
| | | $V_{DD}$ = 3 V | 35 | | | ns |
| $\overline{RS}$ Pulse Width | $t_{RS}$ | $V_{DD}$ = 5 V | 20 | | | ns |
| | | $V_{DD}$ = 3 V | 35 | | | ns |
| $\overline{WR}$ to LDAC Delay Time | $t_{LWD}$ | $V_{DD}$ = 5 V | 0 | | | ns |
| | | $V_{DD}$ = 3 V | 0 | | | ns |
| SUPPLY CHARACTERISTICS | | | | | | |
| Power Supply Range | $V_{DD\ RANGE}$ | | 2.7 | | 5.5 | V |
| Positive Supply Current | $I_{DD}$ | Logic inputs = 0 V | | | 10 | µA |
| Power Dissipation | $P_{DISS}$ | Logic inputs = 0 V | | | 0.055 | mW |
| Power Supply Sensitivity | $P_{SS}$ | $\Delta V_{DD}$ = ±5% | | | 0.003 | %/% |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AC CHARACTERISTICS[4] | | | | | | |
| Output Voltage Settling Time | $t_S$ | To ±0.1% of full scale, data cycles from zero scale to full scale to zero scale | | 0.5 | | µs |
| Reference Multiplying Bandwidth | BW | $V_{REF}$ = 100 mV rms, data = full scale | | 6.8 | | MHz |
| DAC Glitch Impulse | Q | $V_{REF}$ = 0 V, midscale – 1 to midscale | | −3.5 | | nV-s |
| Multiplying Feedthrough Error | $V_{OUT}/V_{REF}$ | $V_{REF}$ = 100 mV rms, f = 10 kHz | | −78 | | dB |
| Digital Feedthrough | $Q_D$ | $\overline{WR}$ = 1, LDAC toggles at 1 MHz | | 7 | | nV-s |
| Total Harmonic Distortion | THD | $V_{REF}$ = 5 V p-p, data = full scale, f = 1 kHz | | −104 | | dB |
| Output Noise Density | $e_N$ | f = 1 kHz, BW = 1 Hz | | 12 | | nV/√Hz |
| Analog Crosstalk | $C_{AT}$ | Signal input at Channel A and measures the output at Channel B, f = 1 kHz | | −95 | | dB |

[1] All static performance tests (except $I_{OUT}$) are performed in a closed-loop system using an external precision OP97 I-to-V converter amplifier. The device $R_{FB}$ terminal is tied to the amplifier output. The +IN pin of the OP97 is grounded, and the $I_{OUT}$ of the DAC is tied to the OP97's –IN pin. Typical values represent average readings measured at 25°C.
[2] Guaranteed by design; not subject to production testing.
[3] All input control signals are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and are timed from a voltage level of 1.5 V.
[4] All ac characteristic tests are performed in a closed-loop system using an AD8038 I-to-V converter amplifier except for THD where the AD8065 was used.

### *Timing Diagram*

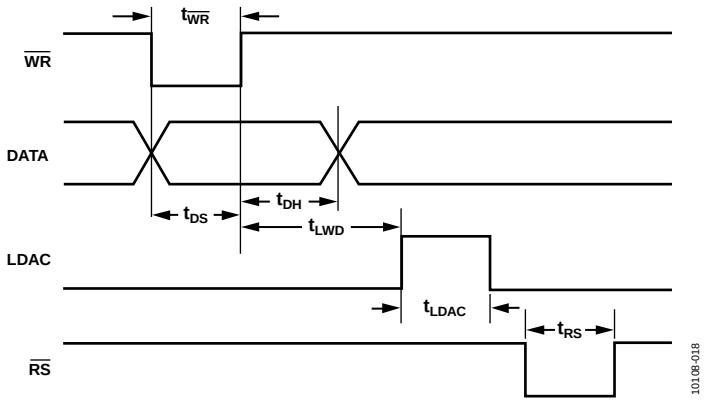


*Figure 3. AD5547-EP Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 2.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to GND | −0.3 V to +8 V |
| $R_{FB}$, $R_{OFS}$, R1, $R_{COM}$, and VREF to GND | −18 V to +18 V |
| Logic Inputs to GND | −0.3 V to +8 V |
| V($I_{OUT}$) to GND | −0.3 V to $V_{DD}$ + 0.3 V |
| Input Current to Any Pin except Supplies | ±50 mA |
| Thermal Resistance ($\theta_{JA}$)[1] | |
| Maximum Junction Temperature ($T_{J\ MAX}$) | 150°C |
| Operating Temperature Range | −55°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature | |
| Vapor Phase, 60 sec | 215°C |
| Infrared, 15 sec | 220°C |

[1] Package power dissipation = ($T_{J\ MAX}$ − $T_A$)/$\theta_{JA}$.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

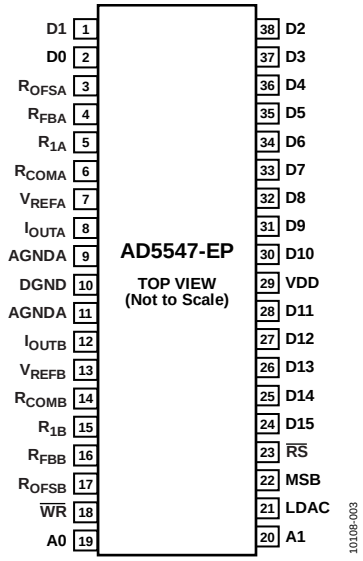


*Figure 4. Pin Configuration*

**Table 3. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 2, 24 to 28, 30 to 38 | D0 to D15 | Digital Input Data Bits D0 to D15. Signal level must be ≤ $V_{DD}$ + 0.3 V. |
| 3 | $R_{OFSA}$ | Bipolar Offset Resistor A. Accepts up to ±18 V. In 2-quadrant mode, $R_{OFSA}$ ties to $R_{FBA}$. In 4-quadrant mode, $R_{OFSA}$ ties to $R_{1A}$ and the external reference. |
| 4 | $R_{FBA}$ | Internal Matching Feedback Resistor A. Connects to the external op amp for I-to-V conversion. |
| 5 | $R_{1A}$ | 4-Quandrant Resistor. In 2-quadrant mode, $R_{1A}$ shorts to the $V_{REFA}$ pin. In 4-quadrant mode, $R_{1A}$ ties to $R_{OFSA}$. Do not connect when operating in unipolar mode. |
| 6 | $R_{COMA}$ | Center Tap Point of the Two 4-Quadrant Resistors, $R_{1A}$ and $R_{2A}$. In 4-quadrant mode, $R_{COMA}$ ties to the inverting node of the reference amplifier. In 2-quadrant mode, $R_{COMA}$ shorts to the associated $V_{REFA}$ pin. Do not connect if operating in unipolar mode. |
| 7 | $V_{REFA}$ | DAC A Reference Input in 2-Quadrant Mode, R2 Terminal in 4-Quadrant Mode. In 2-quadrant mode, $V_{REFA}$ is the reference input with constant input resistance vs. code. In 4-quadrant mode, $V_{REFA}$ is driven by the external reference amplifier. |
| 8 | $I_{OUTA}$ | DAC A Current Output. Connects to the inverting terminal of external precision I-to-V op amp for voltage output. |
| 9 | AGNDA | DAC A Analog Ground. |
| 10 | DGND | Digital Ground. |
| 11 | AGNDB | DAC B Analog Ground. |
| 12 | $I_{OUTB}$ | DAC B Current Output. Connects to inverting terminal of external precision I-to-V op amp for voltage output. |
| 13 | $V_{REFB}$ | DAC B Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance vs. code. If configured with an external op amp for 4-quadrant multiplying, $V_{REFB}$ becomes $-V_{REF}$. |
| 14 | $R_{COMB}$ | Center Tap Point of the Two 4-Quadrant Resistors, $R_{1B}$ and $R_{2B}$. In 4-quadrant mode, $R_{COMB}$ ties to the inverting node of the reference amplifier. In 2-quadrant mode, $R_{COMB}$ shorts to the $V_{REFB}$ pin. Do not connect if operating in unipolar mode. |
| 15 | $R_{1B}$ | 4-Quandrant Resistor. In 2-quadrant mode, $R_{1B}$ shorts to the $V_{REFB}$ pin. In 4-quadrant mode, $R_{1B}$ ties to $R_{OFSB}$. Do not connect if operating in unipolar mode. |
| 16 | $R_{FBB}$ | Internal Matching Feedback Resistor B. Connects to external op amp for I-to-V conversion. |
| 17 | $R_{OFSB}$ | Bipolar Offset Resistor B. Accepts up to ±18 V. In 2-quadrant mode, $R_{OFSB}$ ties to $R_{FBB}$. In 4-quadrant mode, $R_{OFSB}$ ties to $R_{1B}$ and an external reference. |
| 18 | $\overline{WR}$ | Write Control Digital Input In, Active Low. $\overline{WR}$ transfers shift register data to the DAC register on the rising edge. Signal level must be ≤$V_{DD}$ + 0.3 V. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 19 | A0 | Address Pin 0. Signal level must be ≤$V_{DD}$ + 0.3 V. |
| 20 | A1 | Address Pin 1. Signal level must be ≤$V_{DD}$ + 0.3 V. |
| 21 | LDAC | Digital Input Load DAC Control. Signal level must be ≤$V_{DD}$ + 0.3 V. |
| 22 | MSB | Power-On Reset State. MSB = 0 corresponds to zero-scale reset; MSB = 1 corresponds to midscale reset. The signal level must be ≤$V_{DD}$ + 0.3 V. |
| 23 | $\overline{RS}$ | Active low resets both input and DAC registers. Resets to zero-scale if MSB = 0 and resets to midscale if MSB = 1. Signal level must be ≤$V_{DD}$ + 0.3 V. |
| 29 | VDD | Positive Power Supply Input. The specified range of operation is 2.7 V to 5.5 V. |

**Table 4. Address Decoder Pins**

| A1 | A0 | Output Update |
|---|---|---|
| 0 | 0 | DAC A |
| 0 | 1 | None |
| 1 | 0 | DAC A and DAC B |
| 1 | 1 | DAC B |

**Table 5. Control Inputs**

| $\overline{RS}$ | $\overline{WR}$ | LDAC | Register Operation |
|---|---|---|---|
| 0 | X | X | Reset the output to 0 with MSB = 0; reset the output to midscale with MSB = 1. |
| 1 | 0 | 0 | Load the input register with data bits. |
| 1 | 1 | 1 | Load the DAC register with the contents of the input register. |
| 1 | 0 | 1 | The input and DAC registers are transparent. |
| 1 | ⊓ | ⊓ | When LDAC and $\overline{WR}$ are tied together and programmed as a pulse, the data bits are loaded into the input register on the falling edge of the pulse and are then loaded into the DAC register on the rising edge of the pulse. |
| 1 | 1 | 0 | No register operation. |

# TYPICAL PERFORMANCE CHARACTERISTICS

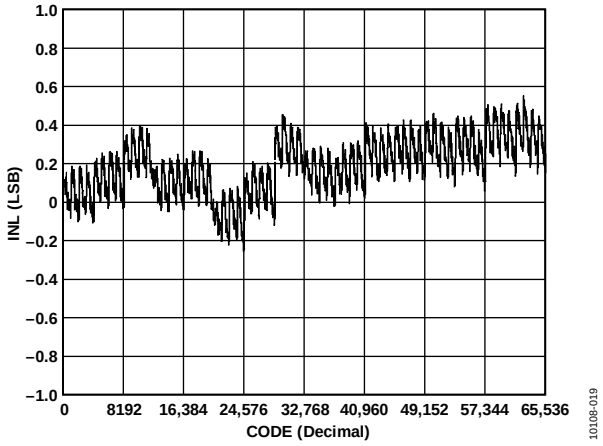


Figure 5. AD5547-EP Integral Nonlinearity Error

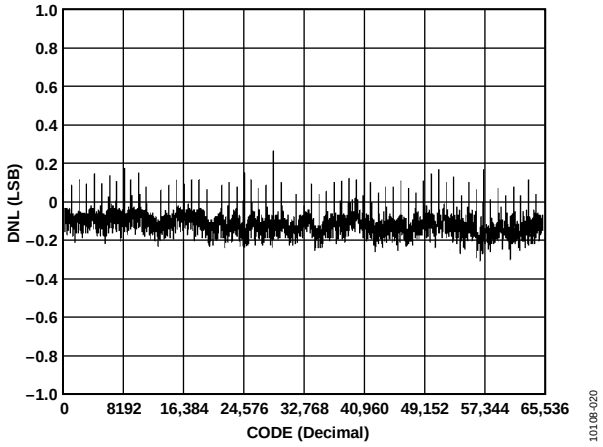


Figure 6. AD5547-EP Differential Nonlinearity Error

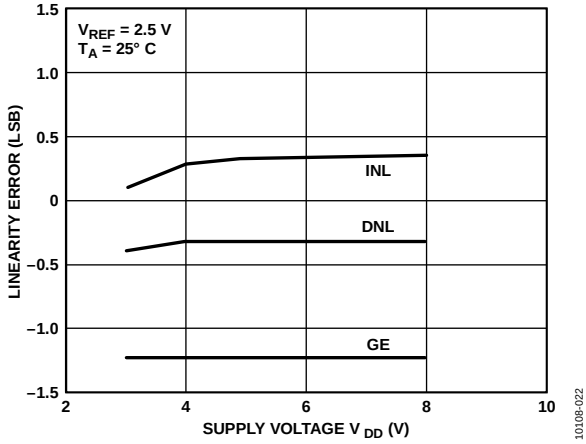


Figure 7. Linearity Error vs. Supply Voltage, $V_{DD}$

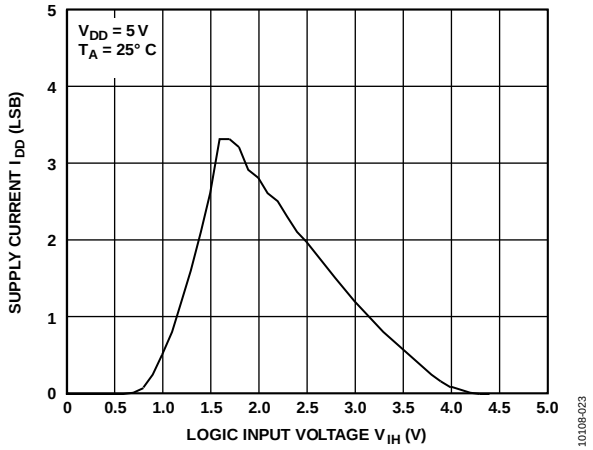


Figure 8. Supply Current vs. Logic Input Voltage

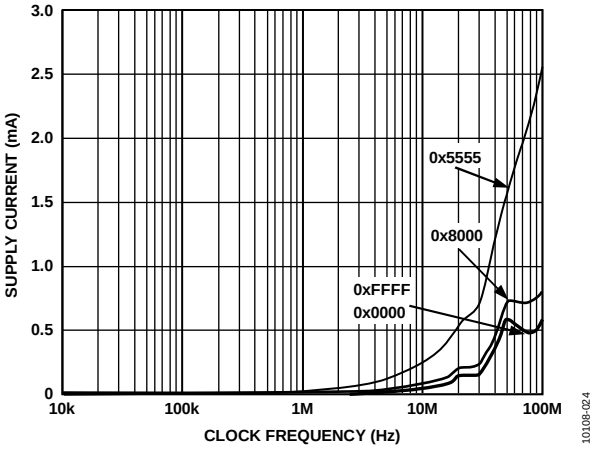


Figure 9. AD5547-EP Supply Current vs. Clock Frequency

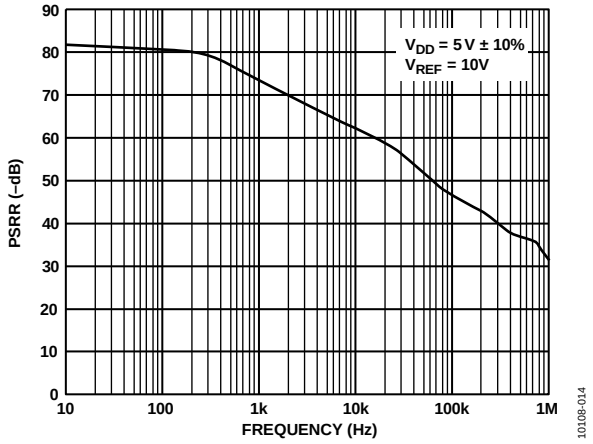


Figure 10. Power Supply Rejection Ratio (PSRR) vs. Frequency

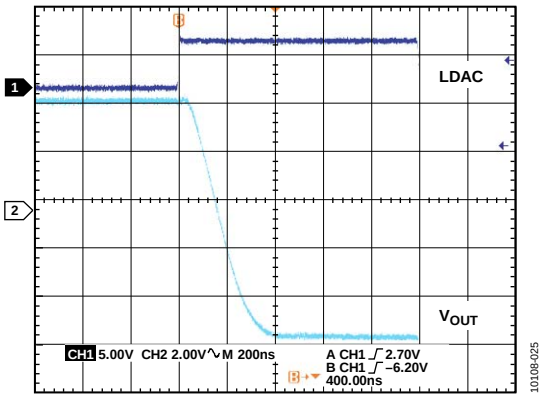


Figure 11. Settling Time from Full Scale to Zero Scale

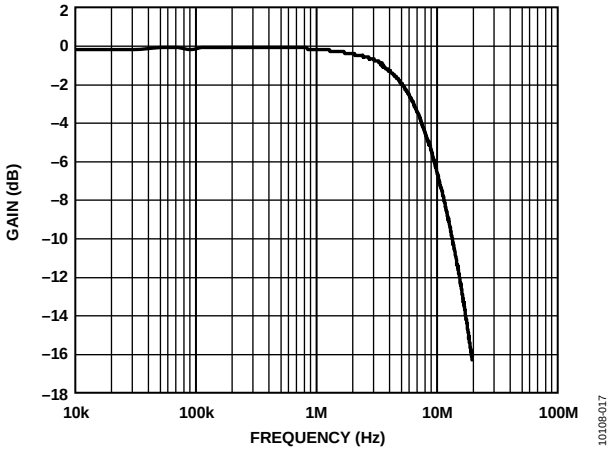


Figure 13. AD5547-EP Unipolar Reference Multiplying Bandwidth

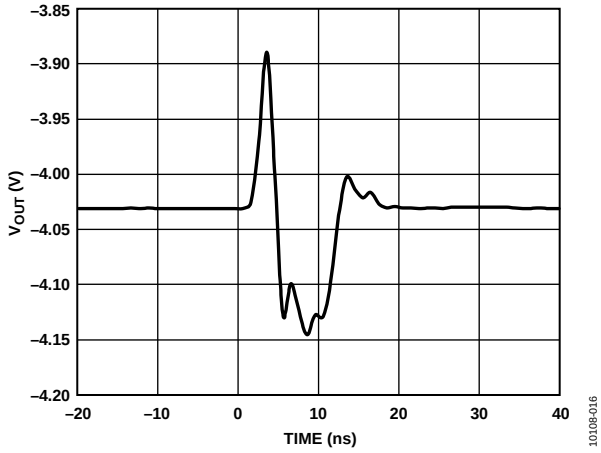


Figure 12. AD5547-EP Midscale Transition and Digital Feedthrough

# OUTLINE DIMENSIONS

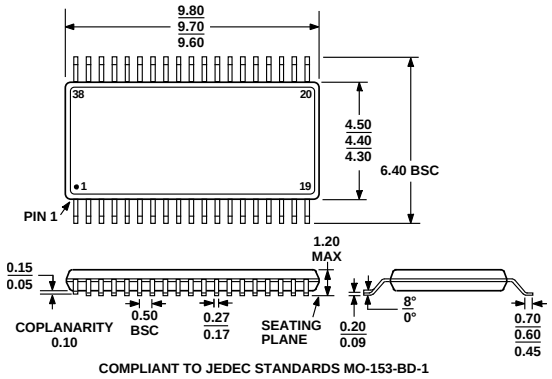


*Figure 14. 38-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-38)*
*Dimension s shown in millimeters*

## ORDERING GUIDE

| Model[1] | Resolution (Bits) | DNL (LSB) | INL (LSB) | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|---|---|
| AD5547SRU-EP | 16 | ±1 | ±2 | −55°C to +125°C | 38-Lead TSSOP | RU-38 |

[1] Z = RoHS Compliant Part.

## NOTES

## NOTES