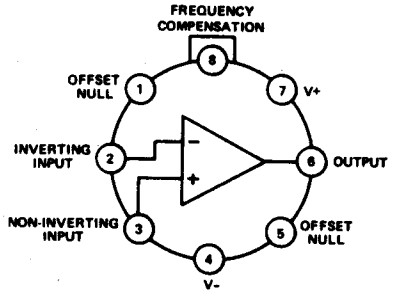
IC, Wideband, Fast Slewing, General Purpose Operational Amplifier

AD507

FEATURES
Gain Bandwidth: 100MHz
Slew Rate: 20V/μs min
I_B: 15nA max (AD507K)
V_{os}: 3mV max (AD507K)
V_{os} Drift: 15μV/°C max (AD507K)
High Capacitive Drive

AD507 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the extended temperature range, −55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.

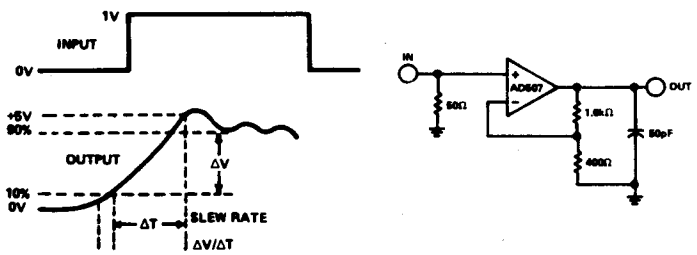
PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.

SPECIFICATIONS (typical at +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD507J	AD507K	AD507S
OPEN LOOP GAIN			
R_L = 2kΩ, C_L = 50pF	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T min to T max	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, C_L = 50pF, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ V_o = ±10V	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	1MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (±35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (500MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	12nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	-55°C to +125°C
Operating	-25°C to +85°C	*	-65°C to +150°C
Storage	-65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08A)	AD507JH	AD507KH	AD507SH

NOTES
*Specifications same as AD507J.
[1] See Section 19 for package outline information.
Specifications subject to change without notice.



Slew Rate Definition and Test Circuit

APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

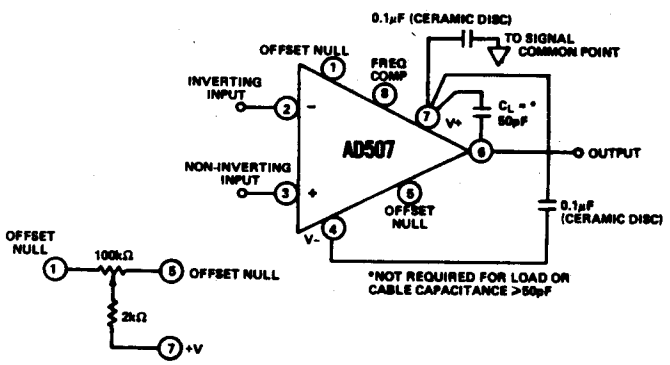


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

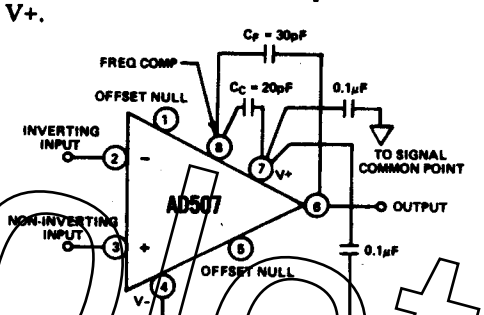


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.

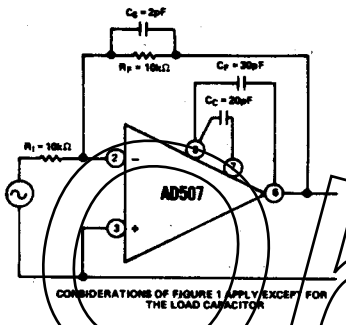
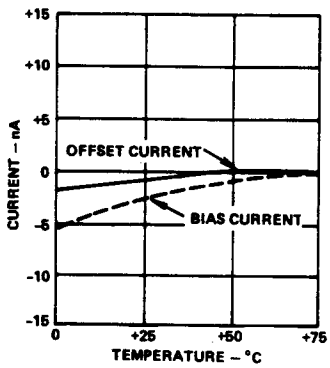
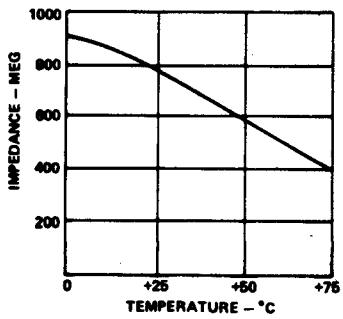


Figure 3. Fast Settling Time Configuration

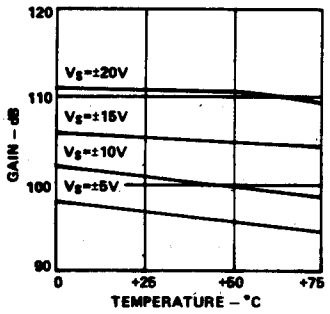
TYPICAL PERFORMANCE CURVES



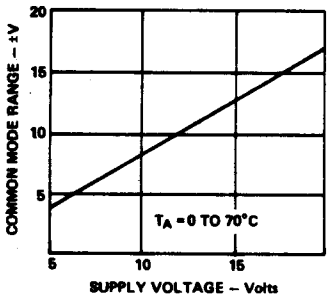
Input Bias Current and Offset Current vs Temperature



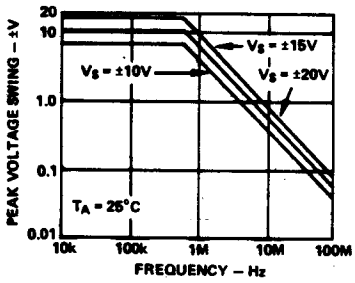
Input Impedance vs Temperature



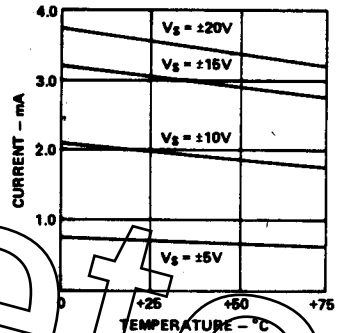
Open Loop Voltage Gain vs Temperature



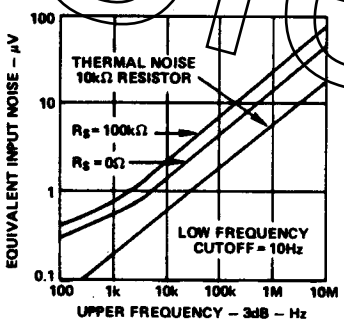
Common Mode Voltage Range vs Supply Voltage



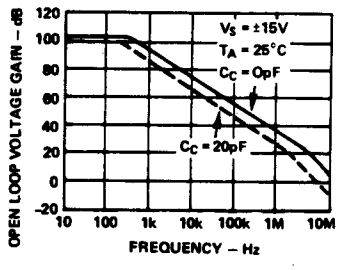
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency