

# AB-EZPC-96

## High Power Current Regulator with Bias Voltage Rectification

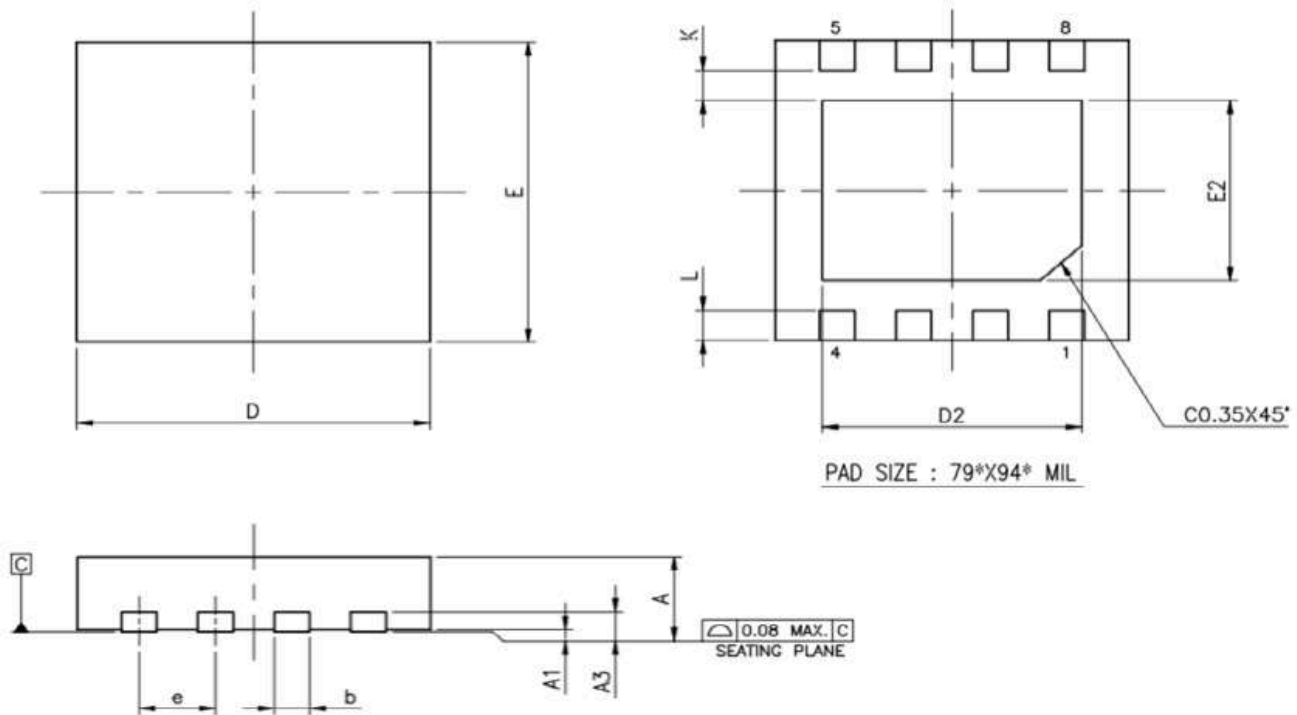
### Features

- DFN3030 package (MSOP available)
- Built-in rectification circuit
- Accurate constant current
- Over Current Protection (OCP)
- Over temperature protection (OTP)

### Description

AB-EZPC series is a constant current regulator with built-in bias voltage rectification circuit. It is designed to maintain constant current and hence constant luminance for DC powered LED lighting applications. AB-EZPC series rectifies power input for the LED string to operate regardless of the polarity of the bias voltage. Additionally, to ensure system reliability, AB-EZPC series is built with thermal protection function (OTP). The AB-EZPC series is available in 3030 DFN & MSOP 8 PIN packages.

## Pin Description\_3030 DFN



Pin No.	Name	Function
5	VA	Power input pin A
4	VB	Power input pin B
8	P+	Output pin to connect external LED positive.
1	N-	Output pin to connect external LED negative

## Absolute Maximum Ratings

Parameter	Value
Supply Voltage   VA-VB	38V
Output current	400mA
Junction Temperature	150°C
Operating Ambient Temperature TA	-20°C~85°C
Storage Temperature Range	-40°C~150 °C
Package Thermal Resistance (junction to ambient)	50°C/W
Lead Temperature (All Pb free packages, soldering, 10 sec)	260°C
ESD voltage protection, human body model	4KV

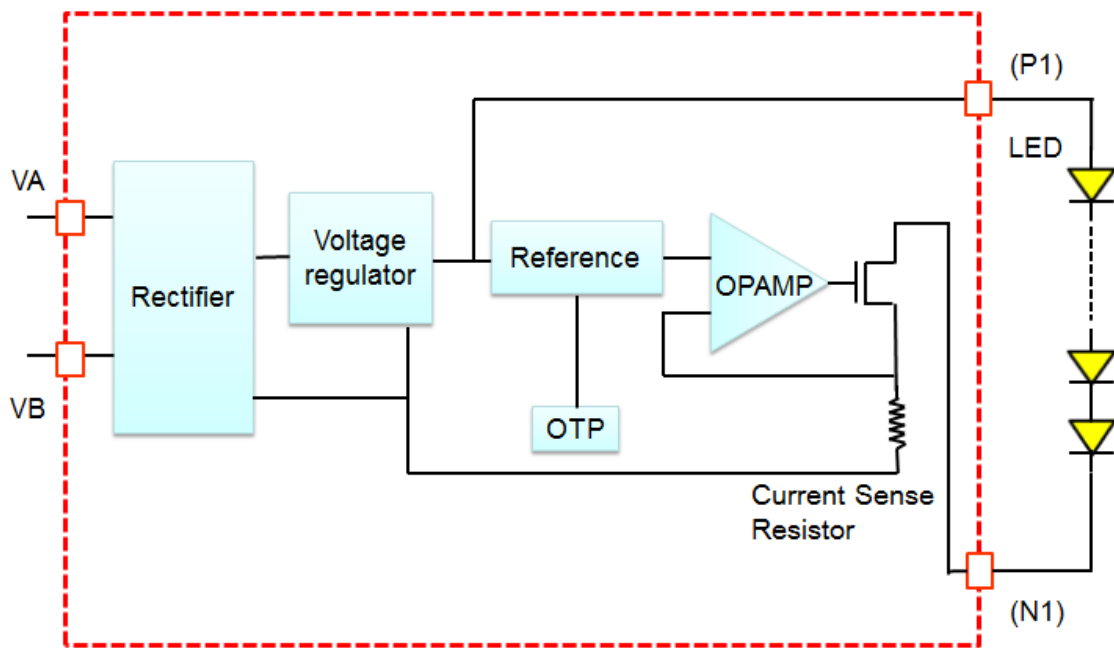
## Recommended Operating Conditions

Symbol	Parameter	Min/Max	Unit
VA-VB	Supply Voltage	1.8 to 38	V
TA	Operating Ambient Temperature	-20 to 85	°C

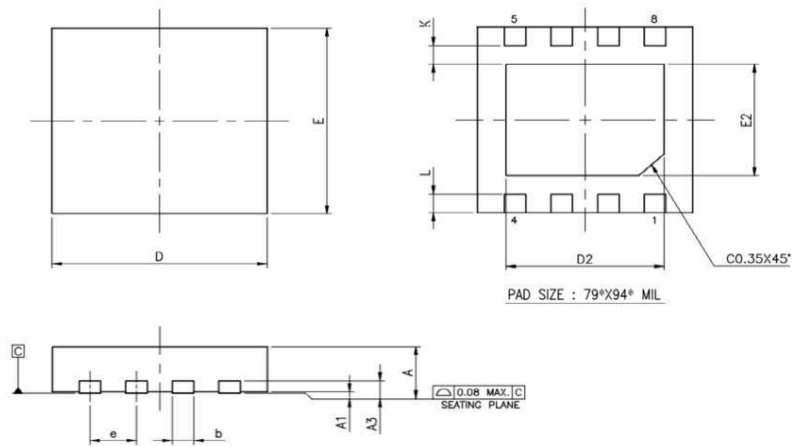
## Electrical Characteristics (TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Current	Is	VA-VB   >1.8		400		mA
Output Ramp Down Temperature	T1	Start point (100% current)		120		°C
Shutdown Temperature	T2	IP=0mA (0% current)		160		°C

## Function Block



## Appendix I\_ DFN3030 8 PIN



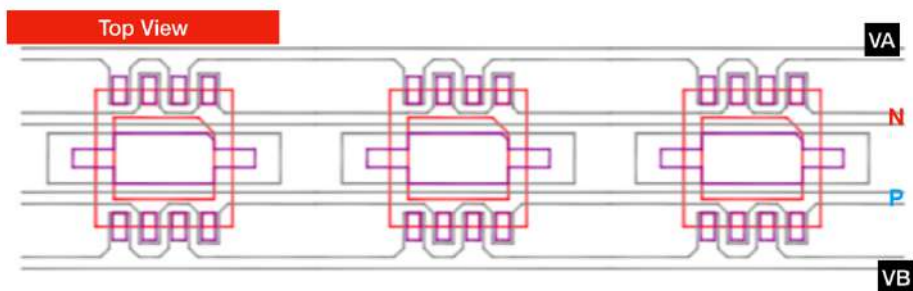
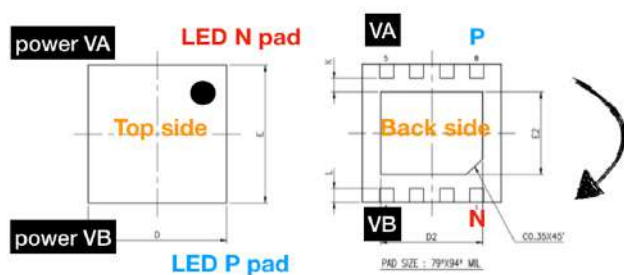
JEDEC OUTLINE	PACKAGE TYPE								
	MO-229			MO-229			MO-24B		
PKG CODE	WDFN(X308)			VDFN(Y308)			UDFN(W308)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90	0.50	0.55	0.60
A1	0.00	0.02	0.05	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.			0.150 REF.		
D	3.00 BSC			3.00 BSC			3.00 BSC		
E	3.00 BSC			3.00 BSC			3.00 BSC		
e	0.65 BSC			0.65 BSC			0.65 BSC		
K	0.20	-	-	0.20	-	-	0.20	-	-

PAD SIZE	D2			E2			L			b			LEAD FINISH		JEDEC CODE	VDFN	WDFN	UDFN
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF				
75*87* MIL	1.95	2.00	2.05	1.60	1.65	1.70	0.35	0.40	0.45	0.25	0.30	0.35	Y	V	W3030C-2	V	V	-
79*91* MIL	1.95	2.00	2.05	1.65	1.70	1.75	0.25	0.35	0.45	0.25	0.30	0.35	V	X	W3030C-2	V	V	-
63*94* MIL	2.25	2.30	2.35	1.45	1.50	1.55	0.425	0.475	0.525	0.20	0.25	0.30	Y	X	N/A	V	V	-
75*10* MIL	2.55	2.60	2.65	1.75	1.80	1.85	0.20	0.30	0.40	0.25	0.30	0.35	V	X	N/A	V	V	-
71*10* MIL	2.25	2.30	2.35	1.45	1.50	1.55	0.25	0.30	0.35	0.25	0.30	0.35	V	X	N/A	V	V	-
79*94* MIL	2.15	2.20	2.25	1.75	1.80	1.85	0.25	0.30	0.35	0.25	0.30	0.35	V	X	N/A	-	-	V

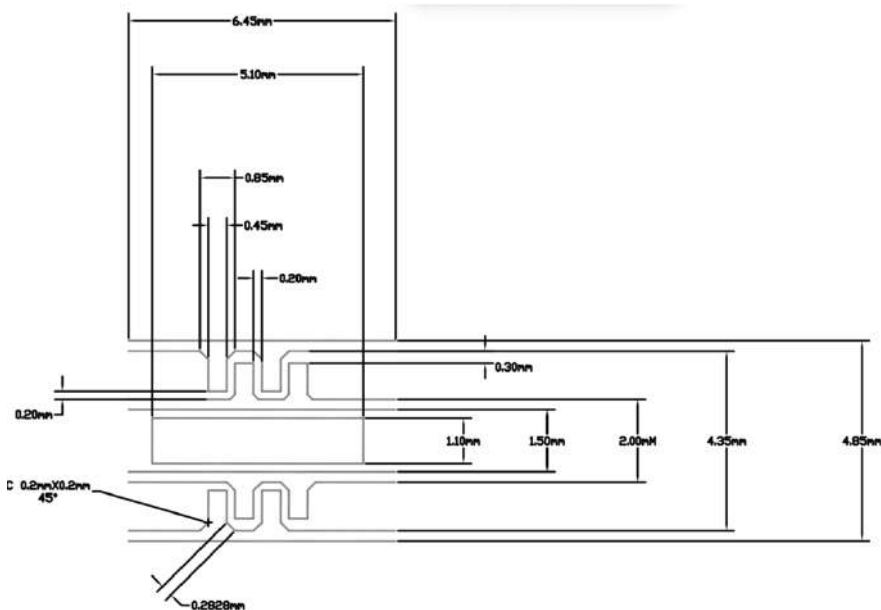
## Appendix II

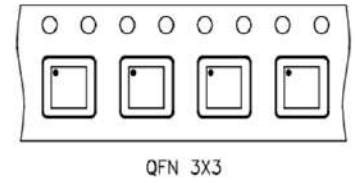
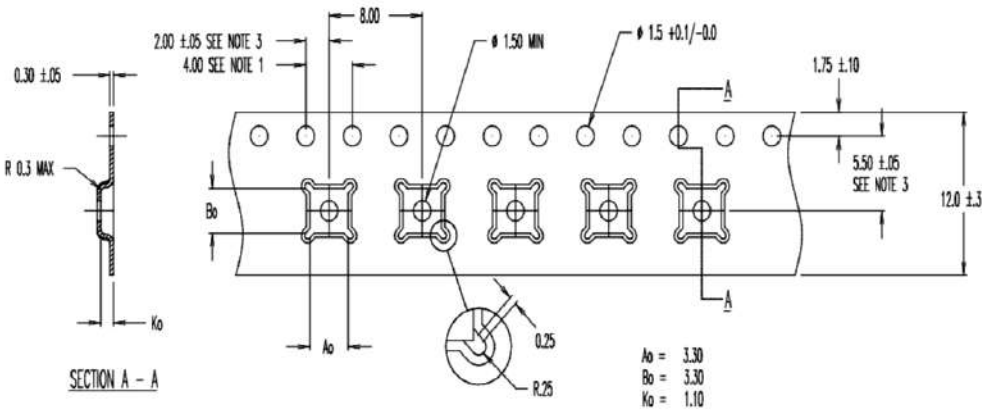
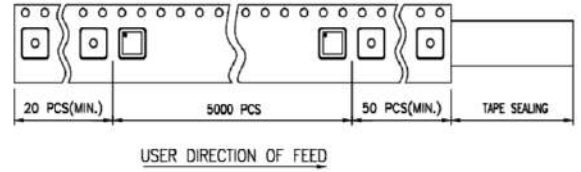
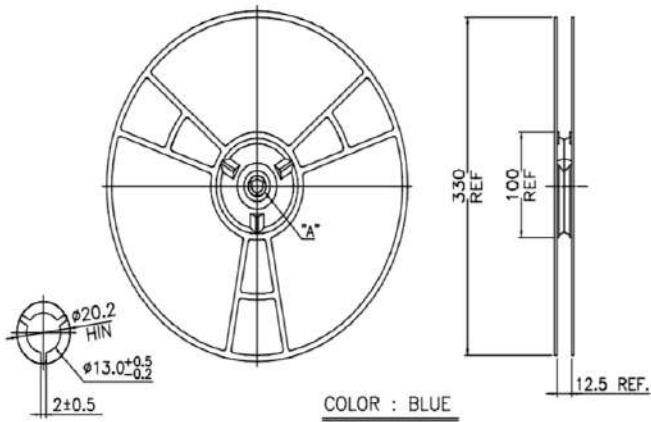
Please follow the guidelines below for PCB layout design

### DFN3030 8 PIN



Metal layer





包裝方式：5000 EA/PER REEL 1 REEL/BOX