

A5G35H110N

Airfast RF Power GaN Transistor

Rev. 1 — November 2022

Data Sheet: Technical Data

This 15.1 W asymmetrical Doherty RF power GaN transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 3300 to 3700 MHz.

This part is characterized and performance is guaranteed for applications operating in the 3300 to 3700 MHz band. There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

3500 MHz

- Typical Doherty Single-Carrier W-CDMA Reference Circuit Performance: $V_{DD} = 48$ Vdc, $I_{DQA} = 70$ mA, $V_{GSB} = -4.1$ Vdc, $P_{out} = 15.1$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

| Frequency | G_{ps} (dB) | η_D (%) | Output PAR (dB) | ACPR (dBc) |
|-----------|---------------|--------------|-----------------|------------|
| 3300 MHz | 14.8 | 57.6 | 7.5 | -27.9 |
| 3400 MHz | 15.4 | 55.7 | 7.8 | -29.3 |
| 3500 MHz | 15.8 | 54.0 | 8.0 | -30.8 |
| 3600 MHz | 15.8 | 54.3 | 7.8 | -31.1 |
| 3700 MHz | 14.9 | 54.3 | 7.4 | -31.0 |

1. All data measured in reference circuit with device soldered to printed circuit board.

Features

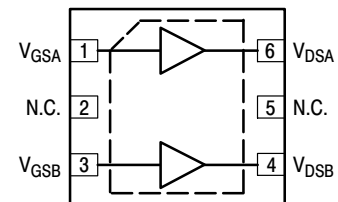
- High terminal impedances for optimal broadband performance
- Improved linearized error vector magnitude with next generation signal
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for low complexity linearization systems
- Optimized for massive MIMO active antenna systems for 5G base stations

A5G35H110N

**3300–3700 MHz, 15.1 W Avg., 48 V
AIRFAST RF POWER GaN
TRANSISTOR**



**DFN 7 × 6.5
PLASTIC**



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|---|------------|-------------|------------------|
| Drain–Source Voltage | V_{DSS} | 125 | Vdc |
| Gate–Source Voltage | V_{GS} | –16, 0 | Vdc |
| Operating Voltage | V_{DD} | 55 | Vdc |
| Maximum Forward Gate Current, $I_{G(A+B)}$, @ $T_C = 25^\circ\text{C}$ | I_{GMAX} | 13.3 | mA |
| Storage Temperature Range | T_{stg} | –65 to +150 | $^\circ\text{C}$ |
| Case Operating Temperature Range | T_C | –55 to +150 | $^\circ\text{C}$ |
| Maximum Channel Temperature | T_{CH} | 225 | $^\circ\text{C}$ |

Table 2. Recommended Operating Conditions

| Characteristic | Symbol | Value | Unit |
|-------------------|----------|-------|------|
| Operating Voltage | V_{DD} | 48 | Vdc |

Table 3. Thermal Characteristics

| Characteristic | Symbol | Value | Unit |
|--|---------------------------|---------|--------------------|
| Thermal Resistance by Infrared Measurement, Active Die Surface–to–Case Case Temperature 120°C , $P_D = 14.2\text{ W}$ | $R_{\theta JC}$ (IR) | 2.8 (1) | $^\circ\text{C/W}$ |
| Thermal Resistance by Finite Element Analysis, Channel–to–Case Case Temperature 120°C , $P_D = 14.2\text{ W}$ | $R_{\theta CHC}$ (FEA) | 5.9 (2) | $^\circ\text{C/W}$ |

Table 4. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|-------|
| Human Body Model (per JS–001–2017) | 1A |
| Charge Device Model (per JS–002–2014) | C3 |

Table 5. Moisture Sensitivity Level

| Test Methodology | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------------------|
| Per JESD22–A113, IPC/JEDEC J–STD–020 | 3 | 260 | $^\circ\text{C}$ |

Table 6. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Off Characteristics (3)

| | | | | | | |
|---|--------------------|-------------|--------------|--------|------------|------|
| Off–State Drain Leakage ($V_{DS} = 150\text{ Vdc}$, $V_{GS} = -8\text{ Vdc}$) ($V_{DS} = 150\text{ Vdc}$, $V_{GS} = -8\text{ Vdc}$) | Carrier Peaking | $I_{D(BR)}$ | — — | — — | 2.1 3.9 | mAdc |
| Off–State Gate Leakage ($V_{DS} = 48\text{ Vdc}$, $V_{GS} = -8\text{ Vdc}$) ($V_{DS} = 48\text{ Vdc}$, $V_{GS} = -8\text{ Vdc}$) | Carrier Peaking | I_{GLK} | –1.0 –1.0 | — — | — — | mAdc |

On Characteristics — Side A, Carrier

| | | | | | |
|---|--------------|------|------|------|------|
| Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 4.6\text{ mAdc}$) | $V_{GS(th)}$ | –4.6 | –3.0 | –1.9 | Vdc |
| Gate Quiescent Voltage ($V_{DD} = 48\text{ Vdc}$, $I_{DA} = 60\text{ mAdc}$, Measured in Functional Test) | $V_{GSA(Q)}$ | –3.0 | –2.4 | –2.0 | Vdc |
| Gate–Source Leakage Current ($V_{DS} = 150\text{ Vdc}$, $V_{GS} = -8\text{ Vdc}$) | I_{GSS} | –2.1 | — | — | mAdc |

On Characteristics — Side B, Peaking

| | | | | | |
|---|--------------|------|------|------|------|
| Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 8.7\text{ mAdc}$) | $V_{GS(th)}$ | –4.6 | –3.0 | –1.9 | Vdc |
| Gate–Source Leakage Current ($V_{DS} = 150\text{ Vdc}$, $V_{GS} = -8\text{ Vdc}$) | I_{GSS} | –3.9 | — | — | mAdc |

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
2. $R_{\theta CHC}$ (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression $MTTF$ (hours) = $10^{[A + B/(T + 273)]}$, where T is the channel temperature in degrees Celsius, $A = -11.1$ and $B = 8366$.
3. Each side of device measured separately.

(continued)

Table 6. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------------------|------|-------|------|-------|
| Functional Tests ⁽¹⁾ (In NXP Doherty Production Test Fixture, 50 ohm system) $V_{DD} = 48\text{ Vdc}$, $I_{DQA} = 60\text{ mA}$, $V_{GSB} = (V_t - 1.65)\text{ Vdc}$, $P_{out} = 12.6\text{ W Avg.}$, $f = 3500\text{ MHz}$, 1-tone CW. | | | | | |
| Power Gain | G_{ps} | 13.0 | 15.3 | 19.0 | dB |
| Drain Efficiency | η_D | 40.0 | 45.3 | — | % |
| P_{out} @ 6 dB Compression Point | P6dB | 46.0 | 47.6 | — | dBm |
| Wideband Ruggedness ⁽²⁾ (In NXP Doherty Reference Circuit, 50 ohm system) $I_{DQA} = 70\text{ mA}$, $V_{GSB} = -4.1\text{ Vdc}$, $f = 3500\text{ MHz}$, Additive White Gaussian Noise (AWGN) with 10 dB PAR | | | | | |
| ISBW of 400 MHz at 55 Vdc, 30.2 W Avg. Modulated Output Power (3 dB Input Overdrive from 15.1 W Avg. Modulated Output Power) | No Device Degradation | | | | |
| Typical Performance ⁽²⁾ (In NXP Doherty Reference Circuit, 50 ohm system) $V_{DD} = 48\text{ Vdc}$, $I_{DQA} = 70\text{ mA}$, $V_{GSB} = -4.1\text{ Vdc}$, 3400–3600 MHz Bandwidth | | | | | |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | VBW_{res} | — | 300 | — | MHz |
| Gain Flatness in 200 MHz Bandwidth @ $P_{out} = 15.1\text{ W Avg.}$ | G_F | — | 0.4 | — | dB |
| Fast CW, 27 ms Sweep | | | | | |
| P_{out} @ 6 dB Compression Point | P6dB | — | 87 | — | W |
| AM/PM (Maximum value measured at the P6dB compression point across the 3400–3600 MHz bandwidth) | Φ | — | -6 | — | ° |
| Gain Variation over Temperature (-40°C to +85°C) | ΔG | — | 0.03 | — | dB/°C |
| Output Power Variation over Temperature (-40°C to +85°C) | ΔP_{6dB} | — | 0.001 | — | dB/°C |

Table 7. Ordering Information

| Device | Tape and Reel Information | Package |
|--------------|---|-------------|
| A5G35H110NT4 | T4 Suffix = 2,500 Units, 16 mm Tape Width, 13-inch Reel | DFN 7 × 6.5 |

1. Part internally input matched.
2. All data measured in reference circuit with device soldered to printed circuit board.

Correct Biasing Sequence for GaN Depletion Mode Transistors in a Doherty Configuration

Bias ON the device

1. Set gate voltage V_{GSA} and V_{GSB} to -5 V.
2. Set drain voltage V_{DSA} and V_{DSB} to nominal supply voltage (+48 V).
3. Increase V_{GSA} (carrier side) until I_{DQA} current is attained.
4. Increase V_{GSB} (peaking side) to target bias voltage.
5. Apply RF input power to desired level.

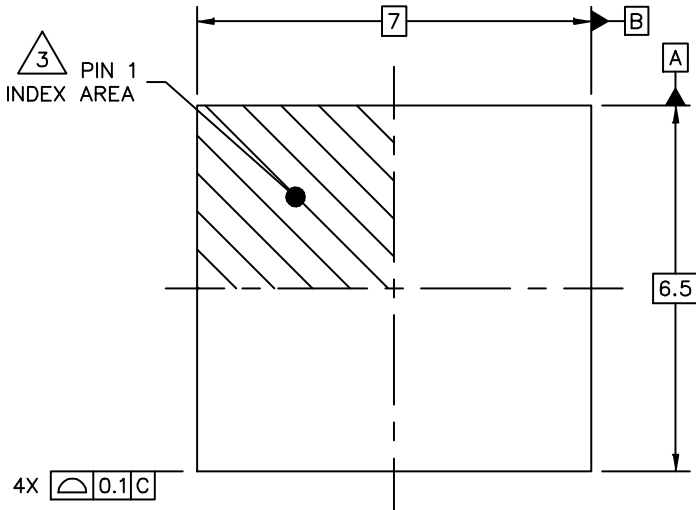
Bias OFF the device

1. Disable RF input power.
2. Adjust gate voltage V_{GSA} and V_{GSB} to -5 V.
3. Adjust drain voltage V_{DSA} and V_{DSB} to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Disable V_{GSA} and V_{GSB} .

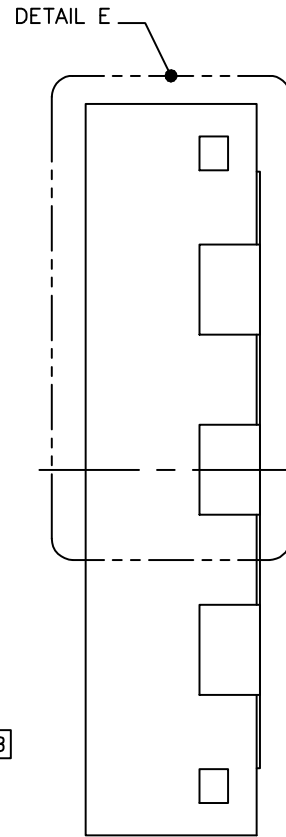
Package Information

H-PDFN-6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

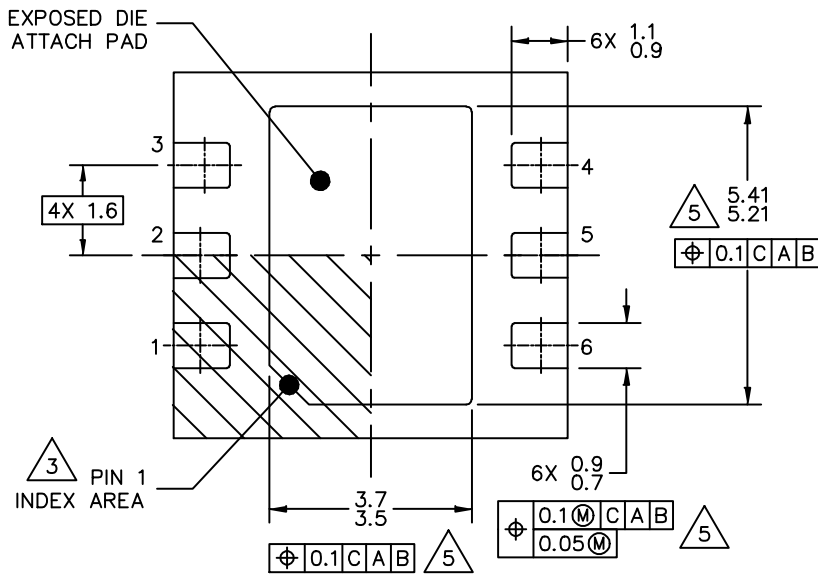
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TOP VIEW



VIEW D-D



BOTTOM VIEW

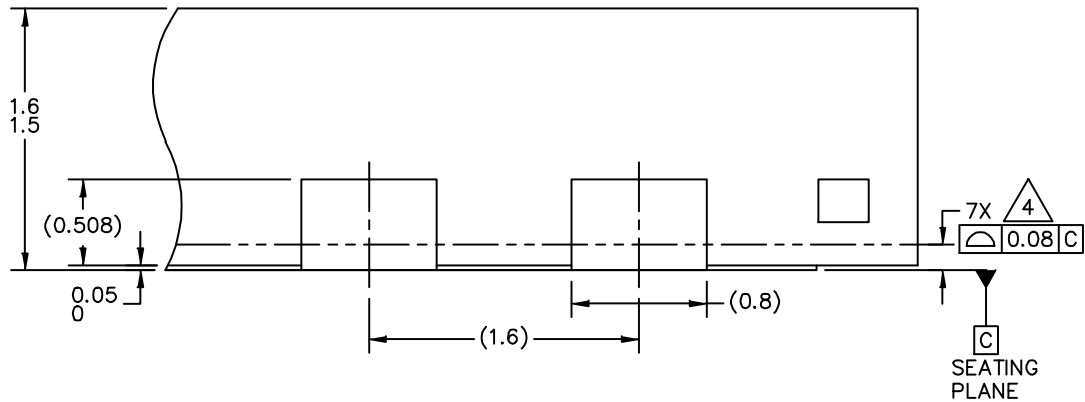
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H-PDFN-6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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DETAIL E
VIEW ROTATED 90°CW

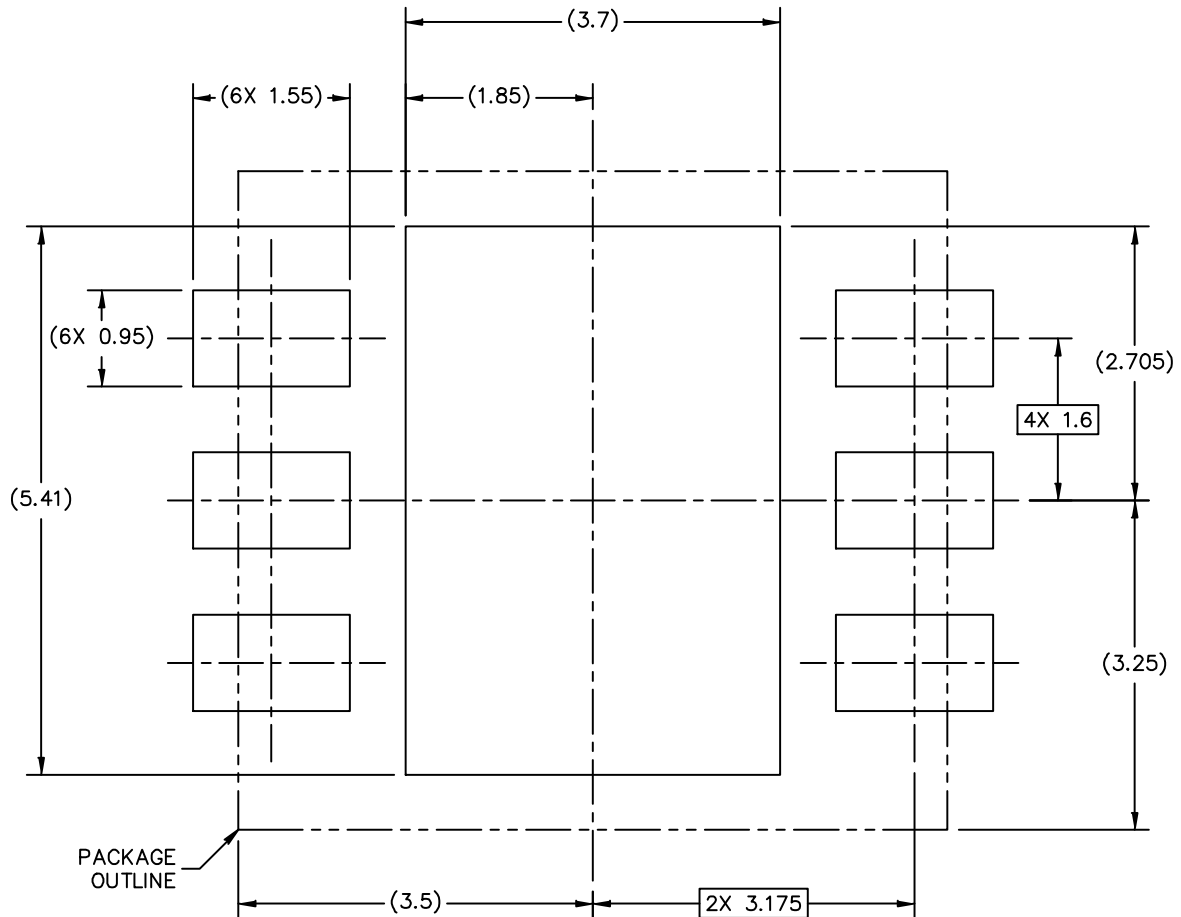
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H-PDFN-6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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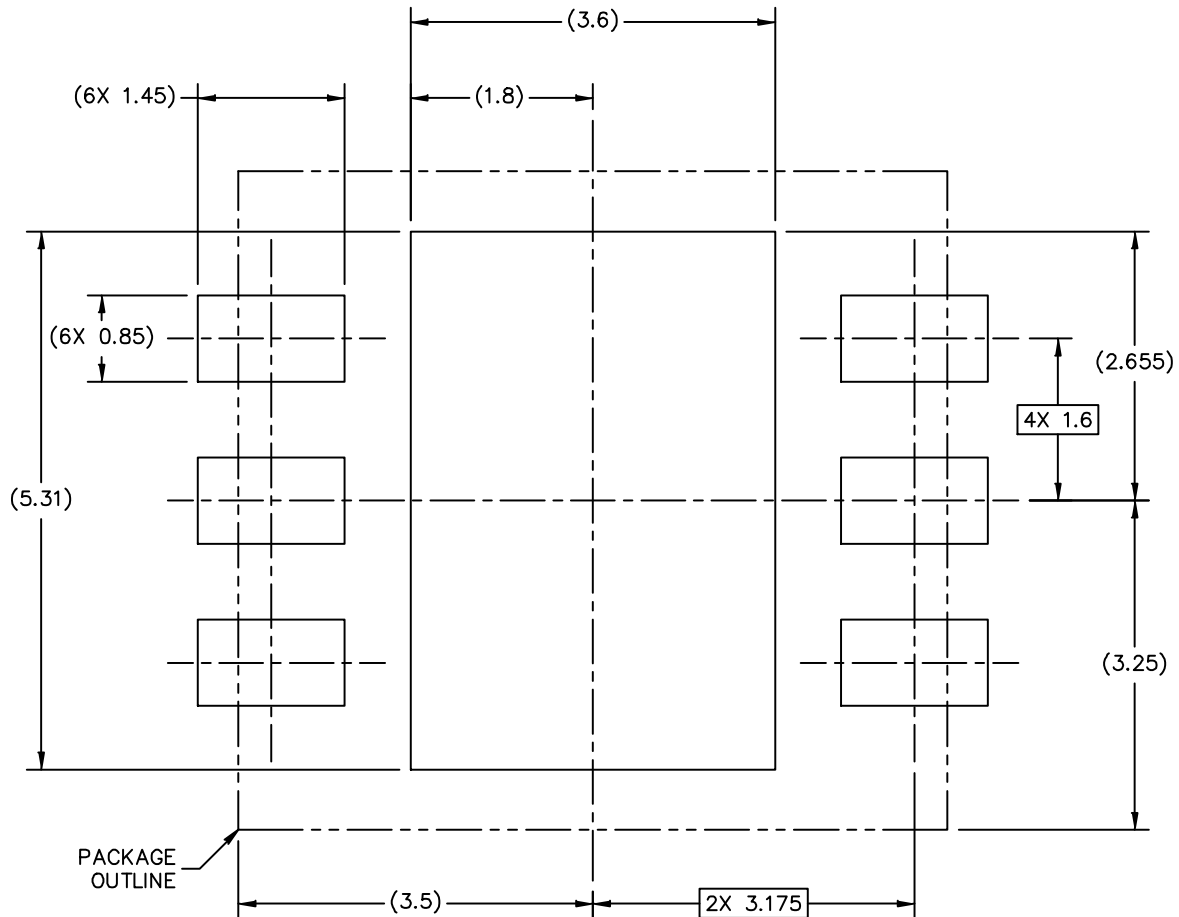
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H-PDFN-6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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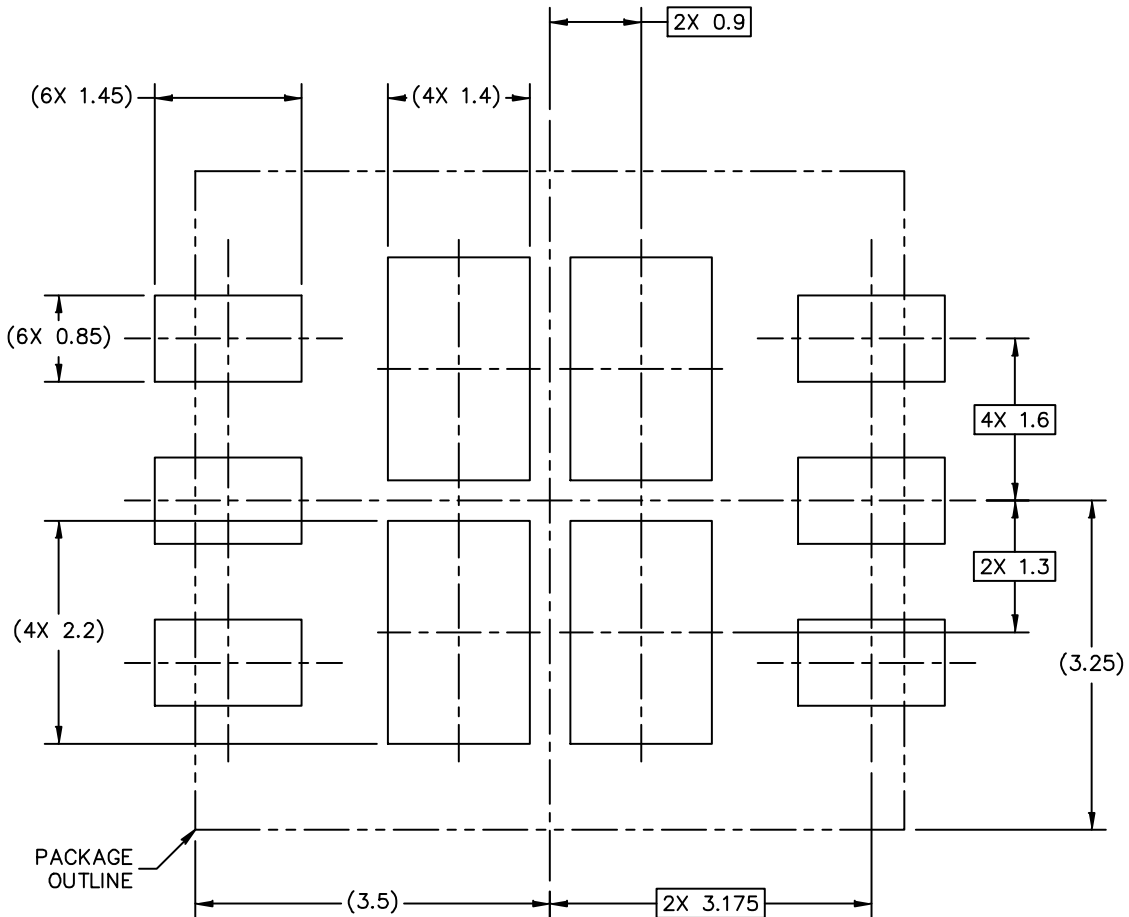
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H-PDFN-6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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H-PDFN-6 I/O
7 X 6.5 X 1.55 PKG, 1.6 PITCH

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. RADIUS ON LEAD AND DIE ATTACH FLAG IS OPTIONAL.

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Product Documentation and Software

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Software

- .s2p File

Revision History

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|--|
| 0 | Dec. 2021 | <ul style="list-style-type: none">• Initial release of data sheet |
| 1 | Nov. 2022 | <ul style="list-style-type: none">• Table 1, Maximum Ratings: Gate–Source Voltage: updated –8, 0 to –16, 0 Vdc, p. 2• Table 4, ESD Protection Characteristics, Human Body Model: updated to reflect test data, p. 2• Table 6, Electrical Characteristics, Off Characteristics: added Off–State Gate Leakage, p. 2• General updates made to align data sheet to current standard |

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