NXP Semiconductors
Technical Data

Document Number: A3I25D080N
Rev. 0, 03/2021

RoHS

RF LDMOS Wideband Integrated Power Amplifiers

A3I25D080N
A3I25D080GN

2300–2690 MHz, 8.3 W Avg., 28 V
AIRFAST RF LDMOS
INTEGRATED POWER AMPLIFIERS

The A3I25D080N integrated Doherty circuit is designed with on-chip matching that makes it usable from 2300 to 2690 MHz. This multi-stage structure is rated for 20 to 32 V operation and covers all typical cellular base station modulation formats.

TO-270WB-17
PLASTIC
A3I25D080N

TO-270WBG-17
PLASTIC
A3I25D080GN

2600 MHz

- Typical Doherty Single-Carrier W-CDMA Characterization Performance: V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 175 mA, $V_{GS(Peaking)}$ = 1.85 Vdc, P_{out} = 8.5 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2496 MHz	29.7	36.7	–37.9
2590 MHz	29.6	37.0	–37.5
2690 MHz	29.4	36.1	–36.2

2300 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 182 mA, $V_{GS(Peaking)}$ = 2.42 Vdc, P_{out} = 8.9 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. (1)

Frequency	G_{ps} (dB)	PAE (%)	ACPR (dBc)
2300 MHz	30.3	36.1	–36.2
2350 MHz	30.2	35.5	–38.7
2400 MHz	30.2	35.2	–39.5

Features

- Integrated Doherty splitter and combiner
- RF decoupled drain pins reduce overall board space
- On-chip matching (50 ohm input, DC blocked)
- Integrated quiescent current temperature compensation with enable/disable function (2)

1. All data measured in fixture with device soldered to heatsink.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.

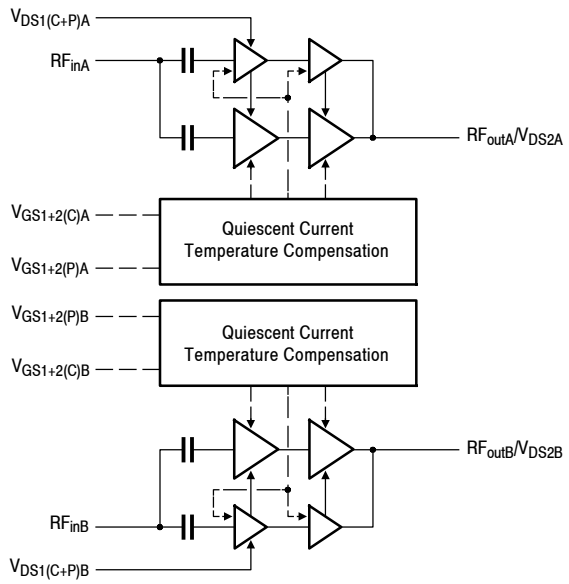
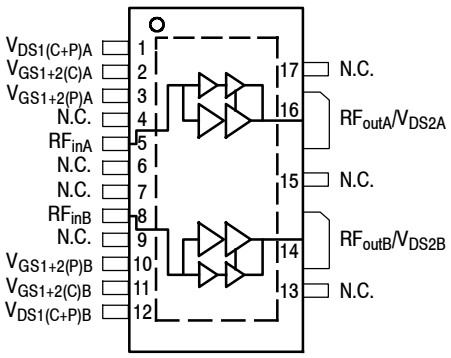


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 2. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–0.5, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1)	T_J	–40 to +225	°C
Input Power	P_{in}	23	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 85°C, 8.3 W, 2590 MHz Stage 1, 28 Vdc, $I_{DQ(Carrier)}$ = 175 mA Stage 2, 28 Vdc, $V_{GS(Peaking)}$ = 1.92 Vdc	$R_{\theta JC}$	 5.6 1.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	1B
Charge Device Model (per JS-002-2014)	C2

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

1. Continuous use at maximum temperature will affect MTTF.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Carrier Stage 1 and Stage 2 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	$I_{DSS(TOTAL)}$	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	$I_{DSS(TOTAL)}$	—	—	1	μAdc
Carrier Stage 1 and Stage 2 — On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 16 μAdc)	$V_{GSC(th)}$	0.9	1.3	1.9	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, $I_{DQ(Carrier)}$ = 175 mAdc)	$V_{GSC(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage (V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 175 mAdc, Measured in Functional Test)	$V_{GGC(Q)}$	4.2	4.9	5.7	Vdc
Peaking Stage 1 and Stage 2 — On Characteristics					
Gate Threshold Voltage (1) (V_{DS} = 10 Vdc, I_D = 31 μAdc)	$V_{GSP(th)}$	0.9	1.4	2.1	Vdc

1. Each side of device measured separately.

(continued)

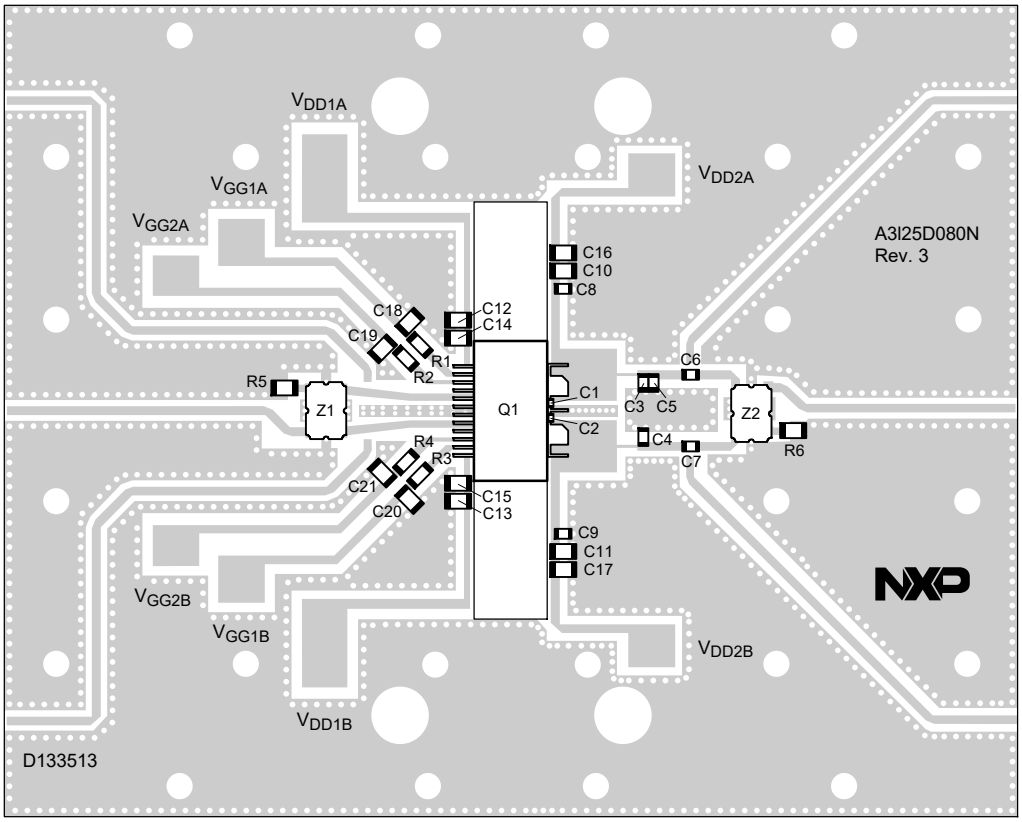
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2] (In NXP Production Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 175 mA, $V_{GS(Peaking)}$ = 1.92 Vdc, P_{out} = 8.3 W Avg., f = 2690 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	27.2	29.2	32.0	dB
Power Added Efficiency	PAE	34.0	35.6	—	%
Adjacent Channel Power Ratio	ACPR	—	–35.5	–33.0	dBc
P_{out} @ 3 dB Compression Point, CW	P3dB	56.2	71.6	—	W
Wideband Ruggedness [3] (In NXP Characterization Test Fixture, 50 ohm system) $I_{DQ(Carrier)}$ = 175 mA, $V_{GS(Peaking)}$ = 1.85 Vdc, f = 2600 MHz, Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 30 Vdc, 16.6 W Avg. Modulated Output Power (3 dB Input Overdrive from 8.3 W Avg. Modulated Output Power)	No Device Degradation				
Typical Performance [3] (In NXP Characterization Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, $I_{DQ(Carrier)}$ = 175 mA, $V_{GS(Peaking)}$ = 1.85 Vdc, 2496–2690 MHz Bandwidth					
P_{out} @ 3 dB Compression Point [4]	P3dB	—	85.0	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2496–2690 MHz frequency range.)	Φ	—	–14	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	260	—	MHz
Quiescent Current Accuracy over Temperature [5] with 2.4 kΩ Gate Feed Resistors (-40°C to +85°C) Stage 1 with 2.4 kΩ Gate Feed Resistors (-40°C to +85°C) Stage 2	ΔI_{QT}	 — —	 9.52 12.79	 — —	%
Gain Flatness in 194 MHz Bandwidth @ P_{out} = 8.5 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–40°C to +85°C)	ΔG	—	0.032	—	dB/°C
Output Power Variation over Temperature (–40°C to +85°C)	ΔP3dB	—	0.013	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A3I25D080NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-inch Reel	TO-270WB-17
A3I25D080GNR1		TO-270WBG-17

1. Part internally input and output matched.
2. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.
3. All data measured in fixture with device soldered to heatsink.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family.* Go to http://www.nxp.com/RF and search for AN1977 or AN1987.



Note: All data measured in fixture with device soldered to heatsink. aaa-039007

Figure 3. A3I25D080N Characterization Test Circuit Component Layout — 2496–2690 MHz

Table 7. A3I25D080N Characterization Test Circuit Component Designations and Values — 2496–2690 MHz

Part	Description	Part Number	Manufacturer
C1, C2	2.4 pF Chip Capacitor	600L2R4AT200T	ATC
C3, C4	1.2 pF Chip Capacitor	600F1R2BT250XT	ATC
C5	0.2 pF Chip Capacitor	600F0R2BT250XT	ATC
C6, C7, C8, C9	20 pF Chip Capacitor	600F200JT250XT	ATC
C10, C11, C12, C13, C14, C15, C16, C17	10 μF Chip Capacitor	GRM32EC72A106KE05L	Murata
C18, C19, C20, C21	4.7 μF Chip Capacitor	GRM31CR71H475KA12L	Murata
Q1	RF Power LDMOS Transistor	A3I25D080N	NXP
R1, R2, R3, R4	2.4 kΩ, 1/4 W Chip Resistor	CRCW12062K40FKEA	Vishay
R5, R6	50 Ω, 8 W Termination Chip Resistor	C8A50Z4B	Anaren
Z1, Z2	2300–2900 MHz, 90°, 3 dB Hybrid Coupler	X3C26P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D133513	MTL

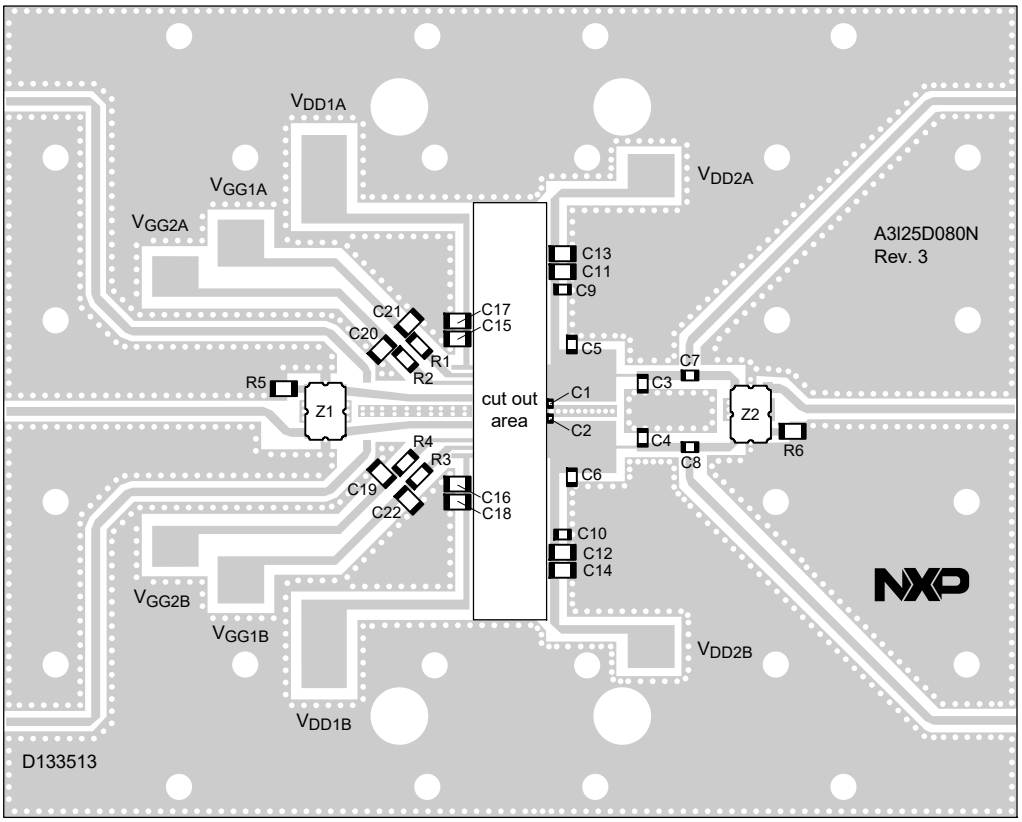
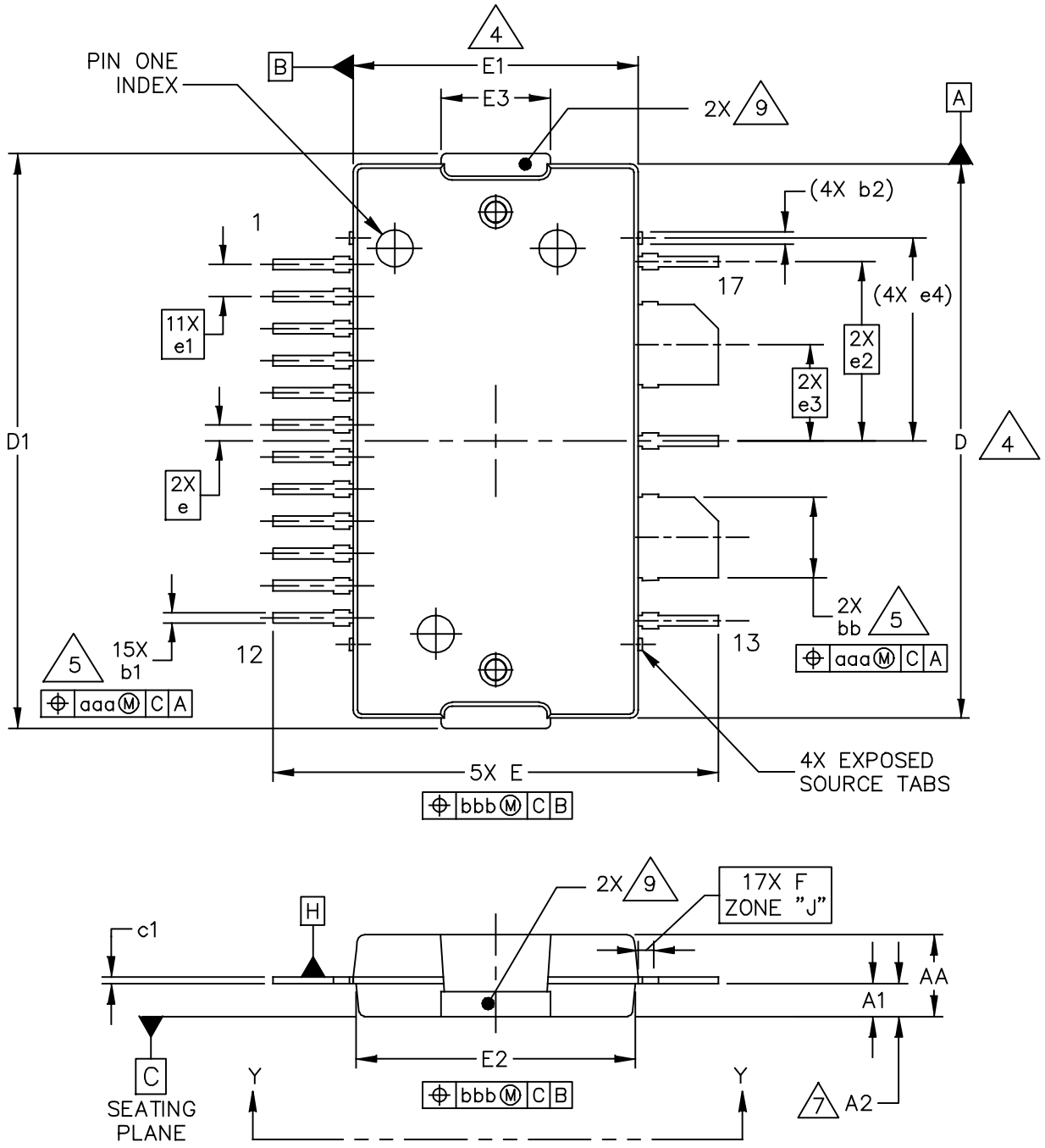


Figure 4. A3I25D080N Test Circuit Component Layout — 2300–2400 MHz

Table 8. A3I25D080N Test Circuit Component Designations and Values — 2300–2400 MHz

Part	Description	Part Number	Manufacturer
C1, C2	2.4 pF Chip Capacitor	600L2R4AT200T	ATC
C3, C4	1.1 pF Chip Capacitor	600F1R1BT250XT	ATC
C5, C6	0.8 pF Chip Capacitor	600F0R8BT250XT	ATC
C7, C8, C9, C10	20 pF Chip Capacitor	600F200JT250XT	ATC
C11, C12, C13, C14, C15, C16, C17, C18	10 μF Chip Capacitor	GRM32EC72A106KE05L	Murata
C19, C20, C21, C22	4.7 μF Chip Capacitor	GRM31CR71H475KA12L	Murata
R1, R2, R3, R4	2.4 kΩ, 1/4 W Chip Resistor	CRCW12062K40FKEA	Vishay
R5, R6	50 Ω, 8 W Termination Chip Resistor	C8A50Z4B	Anaren
Z1, Z2	2300–2900 MHz, 90°, 3 dB Hybrid Coupler	X3C26P1-03S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D133513	MTL

PACKAGE INFORMATION



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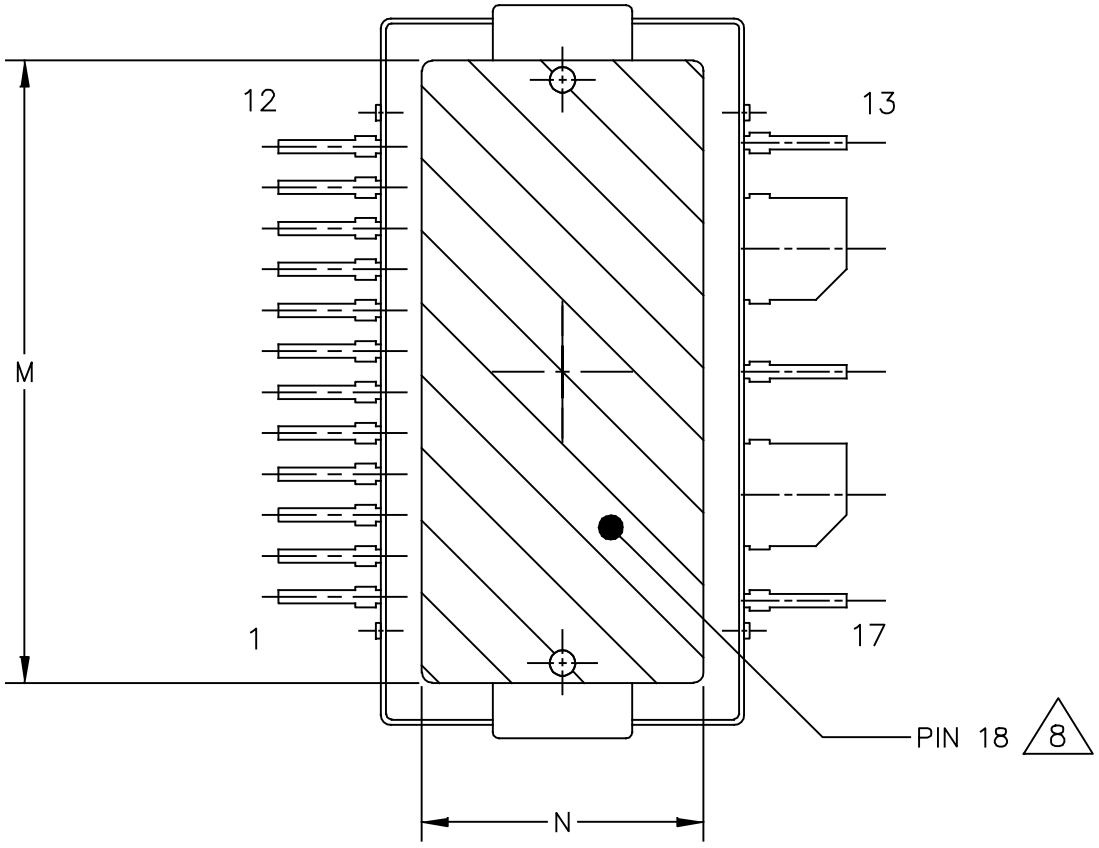
	SOT1730−1	21 JAN 2016



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	SOT1730–1	21 JAN 2016

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.551	.559	14.00	14.20	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

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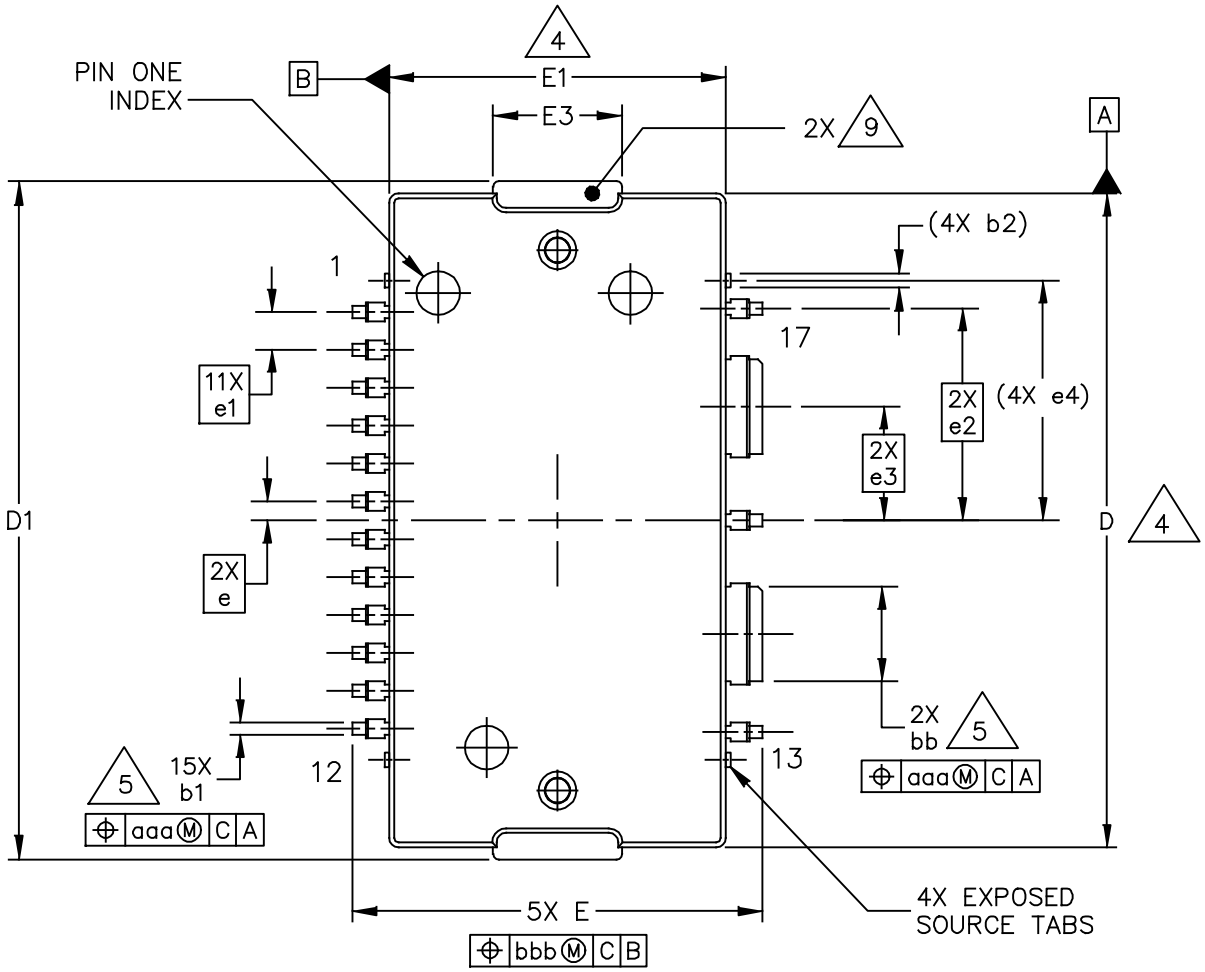

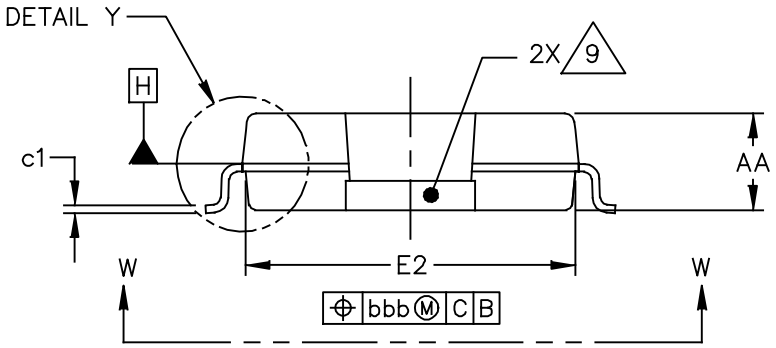

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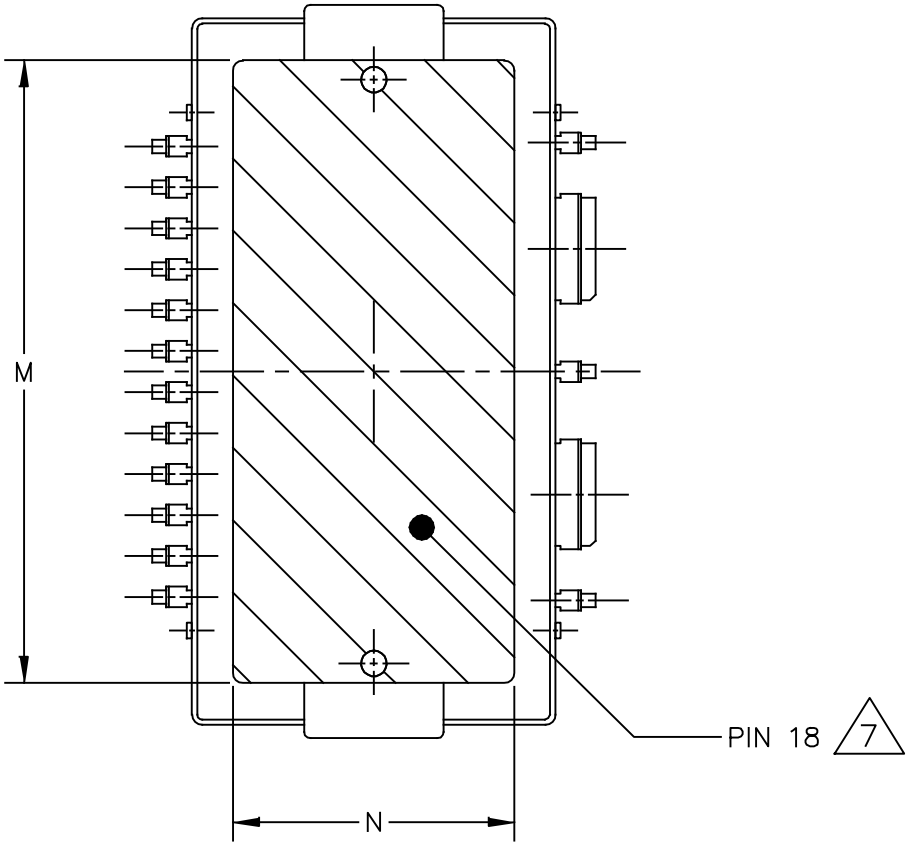

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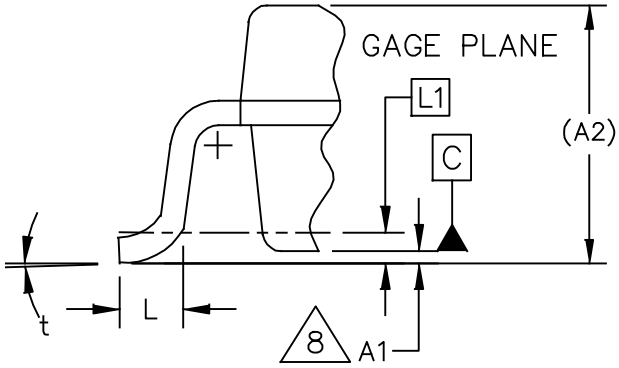

DETAIL "Y"

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NOTES:

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6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.001	.004	0.03	0.10	b1	.010	.016	0.25	0.41
A2	(.105)		(2.67)		b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.429	.437	10.90	11.10	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
L	.018	.024	0.46	0.61	t	2°	8°	2°	8°
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Software

- .s2p File

Development Tools

- Printed Circuit Boards

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2021	• Initial release of data sheet

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