



RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 79 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 720 to 960 MHz.

900 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 48$ Vdc, $I_{DQA} = 400$ mA, $V_{GSB} = 1.2$ Vdc, $P_{out} = 79$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	19.8	55.1	7.2	-32.7
940 MHz	19.7	55.9	7.1	-33.4
960 MHz	19.5	56.1	6.7	-33.9

800 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 48$ Vdc, $I_{DQA} = 400$ mA, $V_{GSB} = 1.0$ Vdc, $P_{out} = 79$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

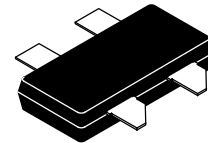
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
790 MHz	18.4	55.0	7.6	-25.0
806 MHz	18.9	56.0	8.0	-28.0
821 MHz	18.1	53.0	8.0	-32.0

Features

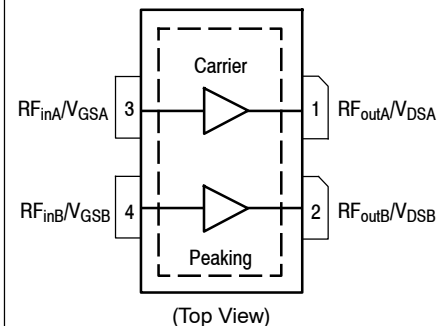
- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

A2V09H300-04NR3

**720-960 MHz, 79 W AVG., 48 V
 AIRFAST RF POWER LDMOS
 TRANSISTOR**



**OM-780-4L
 PLASTIC**



Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections



Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 76°C, 79 W Avg., W-CDMA, 48 Vdc, $I_{DQA} = 400$ mA, $V_{GSB} = 1.2$ Vdc, 940 MHz	$R_{\theta JC}$	0.34	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Off Characteristics (4)

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 105$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 48$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	1	μAdc

On Characteristics - Side A, Carrier

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 90$ μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Gate Quiescent Voltage ($V_{DD} = 48$ Vdc, $I_D = 400$ mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.0	2.4	3.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 0.9$ Adc)	$V_{DS(on)}$	0.1	0.21	0.3	Vdc

On Characteristics - Side B, Peaking

Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 140$ μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Drain-Source On-Voltage ($V_{GS} = 10$ Vdc, $I_D = 1.3$ Adc)	$V_{DS(on)}$	0.1	0.21	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.nxp.com/RF/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ^(1,2) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 48\text{ Vdc}$, $I_{DQA} = 400\text{ mA}$, $V_{GSB} = 1.2\text{ Vdc}$, $P_{out} = 79\text{ W Avg.}$, $f = 940\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	19.1	19.7	21.1	dB
Drain Efficiency	η_D	50.0	55.9	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.5	7.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33.4	-30.0	dBc

Load Mismatch ⁽²⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $I_{DQA} = 400\text{ mA}$, $V_{GSB} = 1.2\text{ Vdc}$, $f = 940\text{ MHz}$, 12 μsec (on), 10% Duty Cycle

VSWR 10:1 at 50 Vdc, 319 W Pulsed CW Output Power (3 dB Input Overdrive from 223 W Pulsed CW Rated Power)	No Device Degradation
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Typical Performance ⁽²⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 48\text{ Vdc}$, $I_{DQA} = 400\text{ mA}$, $V_{GSB} = 1.2\text{ Vdc}$, 920–960 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	223	—	W
P_{out} @ 3 dB Compression Point ⁽³⁾	P3dB	—	400	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range)	Φ	—	-12.3	—	$^\circ$
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 79\text{ W Avg.}$	G_F	—	0.3	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.004	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.012	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2V09H300-04NR3	R3 Suffix = 250 Units, 32 mm Tape Width, 13-inch Reel	OM-780-4L

- Part internally input matched.
- Measurement made with device in an asymmetrical Doherty configuration.
- $P3dB = P_{avg} + 7.0\text{ dB}$ where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

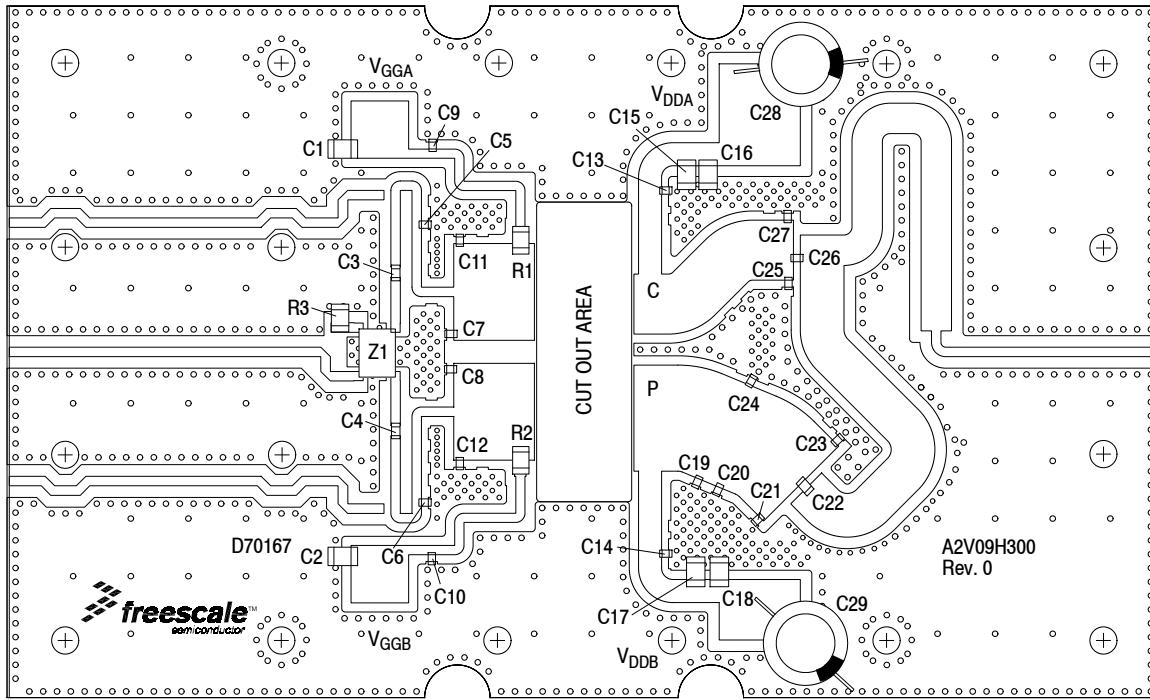


Figure 2. A2V09H300-04NR3 Test Circuit Component Layout

Table 7. A2V09H300-04NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C15, C16, C17, C18	10 μ F Chip Capacitors	GRM32ER61H106KA12L	Murata
C3, C9, C10, C13, C14, C22	100 pF Chip Capacitors	ATC600F101JT250XT	ATC
C4, C26	20 pF Chip Capacitors	ATC600F200JT250XT	ATC
C5, C25, C27	5.1 pF Chip Capacitors	ATC600F5R1BT250XT	ATC
C6	4.3 pF Chip Capacitor	ATC600F4R3BT250XT	ATC
C7, C8, C11, C12	8.2 pF Chip Capacitors	ATC600F8R2BT250XT	ATC
C19, C20, C24	2.2 pF Chip Capacitors	ATC600F2R2BT250XT	ATC
C21	5.6 pF Chip Capacitor	ATC600F5R6BT250XT	ATC
C23	4.7 pF Chip Capacitor	ATC600F4R7BT250XT	ATC
C28, C29	330 μ F, 63 V Electrolytic Capacitors	MCRH63V337M13X21-RH	Multicomp
R1, R2	2.2 Ω , 1/4 W Chip Resistors	CRCW12062R20JNEA	Vishay
R3	50 Ω , 8 W Termination Resistor	C8A50Z4A	Anaren
Z1	800–1000 MHz Band, 90°, 3 dB Hybrid Coupler	X3C09P1-03S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D70167	MTL

TYPICAL CHARACTERISTICS — 920–960 MHz

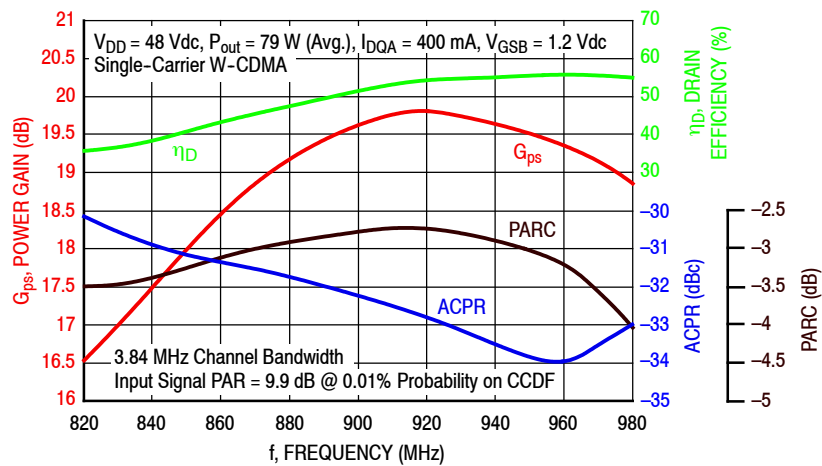


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 79$ Watts Avg.

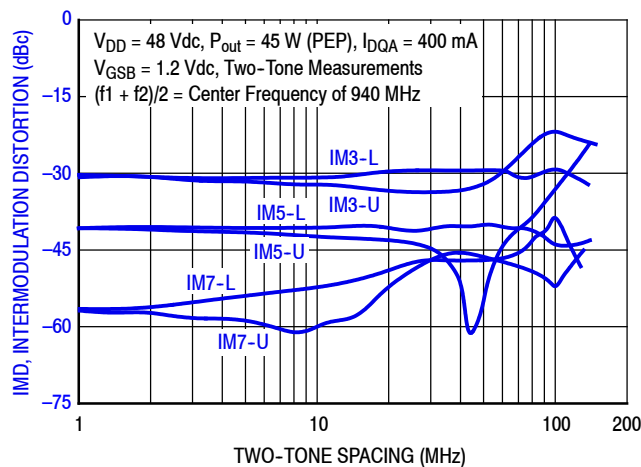


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

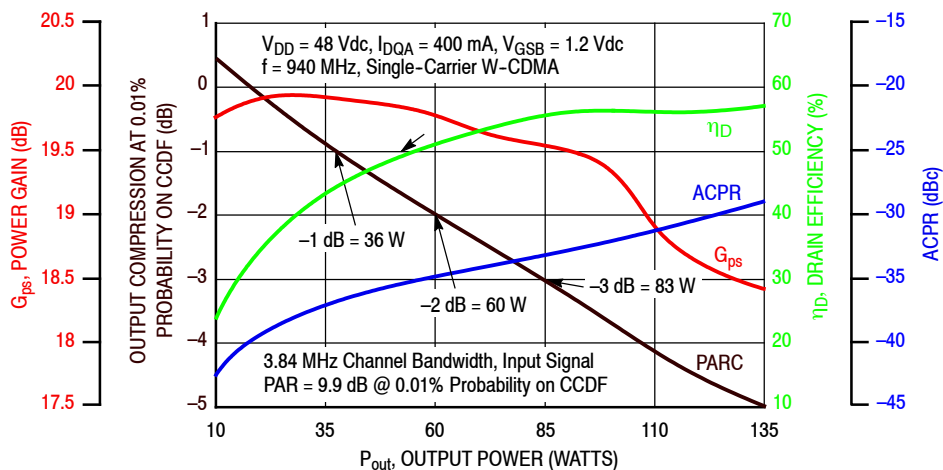


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 920–960 MHz

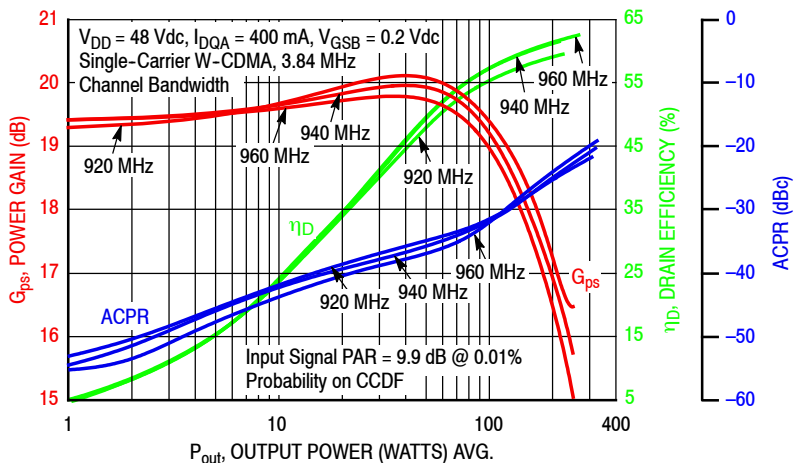


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

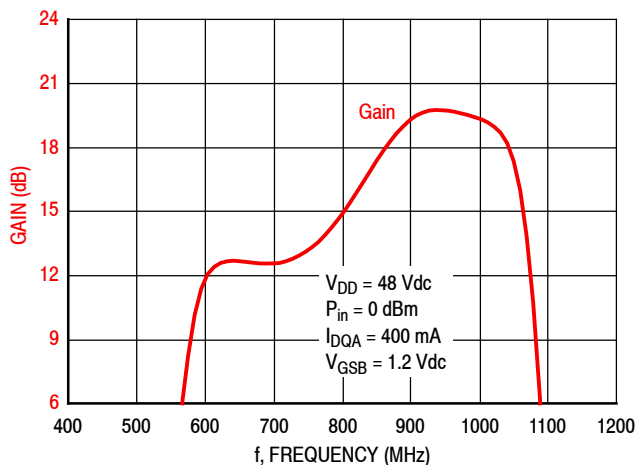
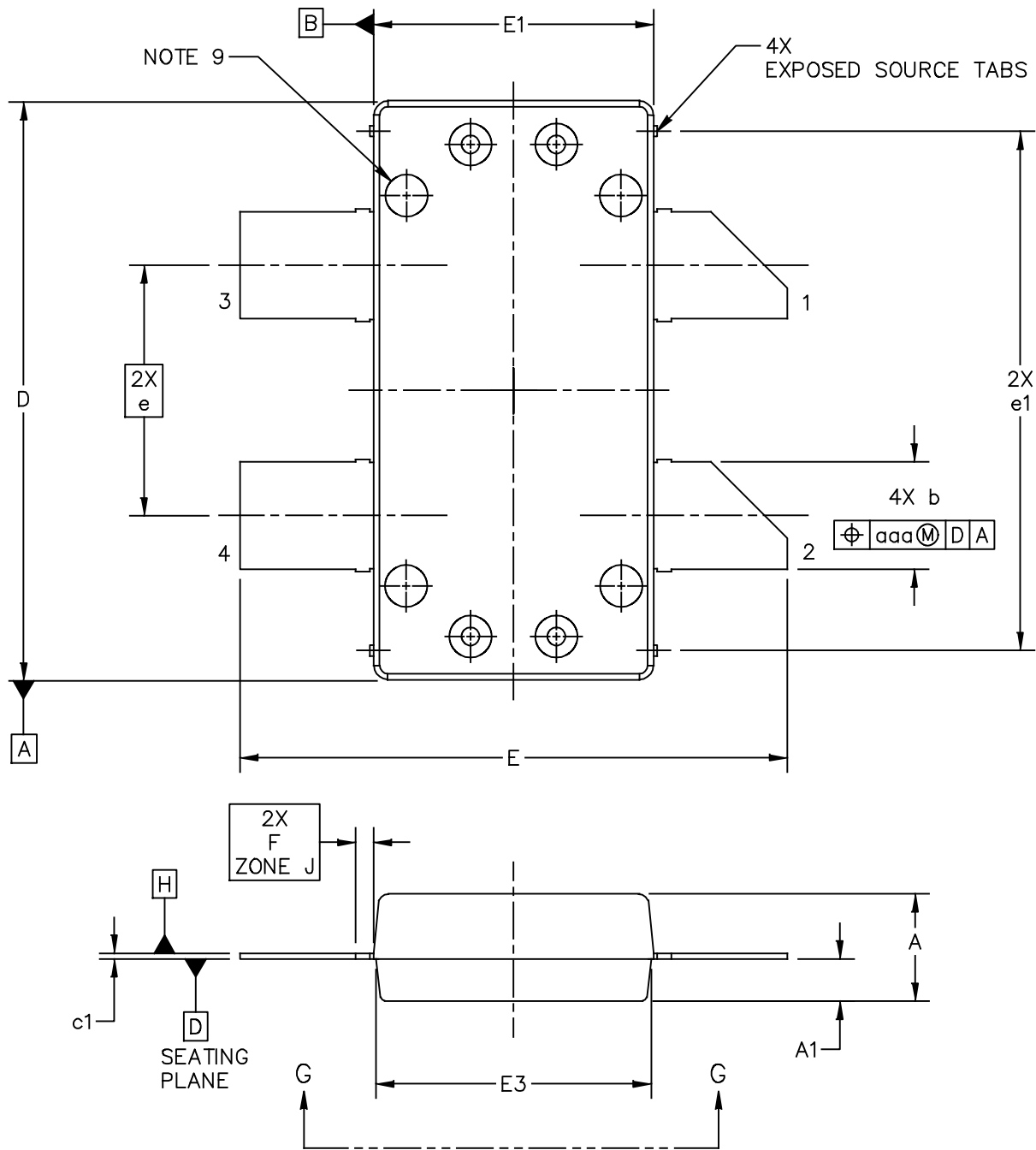


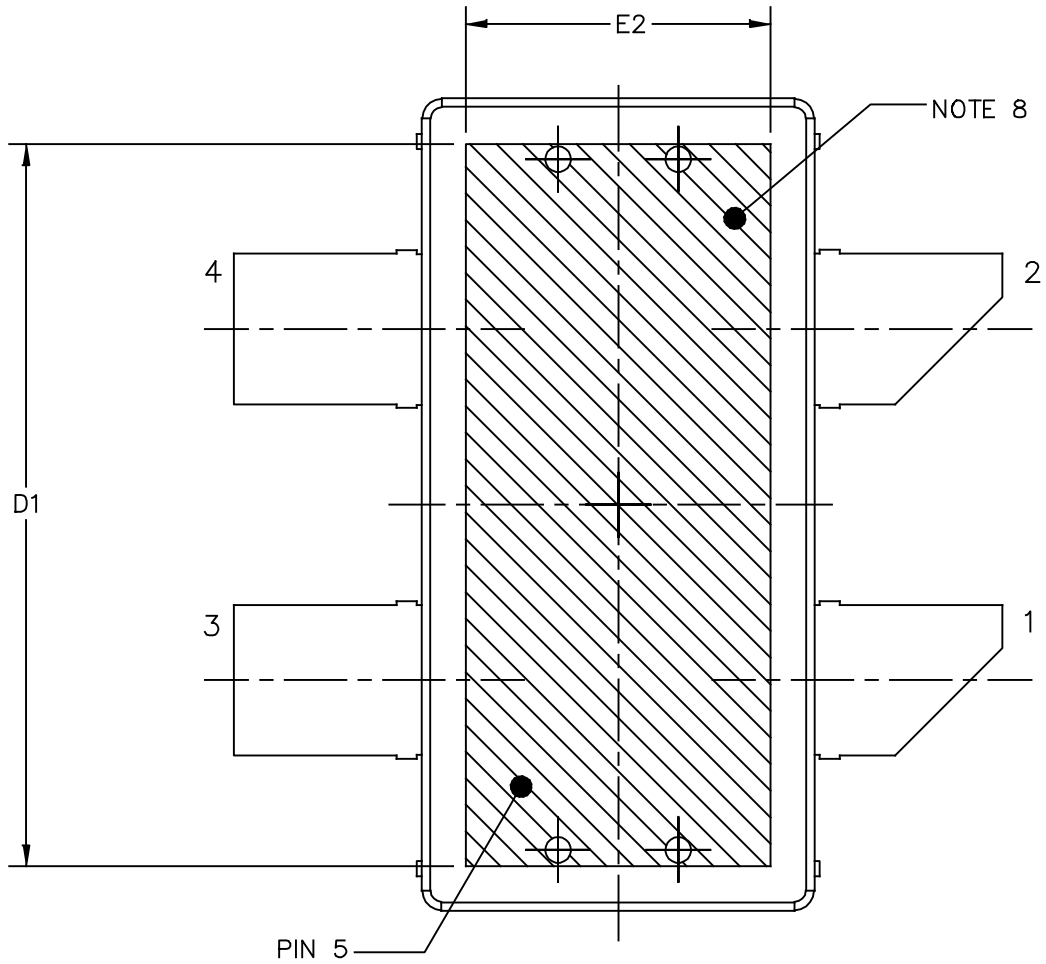
Figure 7. Broadband Frequency Response

PACKAGE DIMENSIONS



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		CASE NUMBER: 2023-02		10 FEB 2010	
		STANDARD: NON-JEDEC			

A2V09H300-04NR3



BOTTOM VIEW
VIEW G-G

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NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.148	.152	3.76	3.86	b	.147	.153	3.73	3.89
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e	.350 BSC		8.89 BSC	
D1	.720	----	18.29	----	e1	.721	.729	18.31	18.52
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.72	9.83					
F	.025 BSC		0.635 BSC						
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					CASE NUMBER: 2023-02			10 FEB 2010	
					STANDARD: NON-JEDEC				

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2016	• Initial release of data sheet

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