Description

The ICS9173B provide the analog PLL circuit blocks to implement a frequency multiplier. Because the device is configured to use an external divider in the PLL clock feedback path, a large divider can be used to result in a large frequency multiplication ratio. This is useful when using a low frequency input clock to generate a high frequency output clock. The ICS9173B contains a phase detector, charge pump, loop filter, and voltage-controlled oscillator (VCO). The ICS674-01 can be used as the external feedback divider.

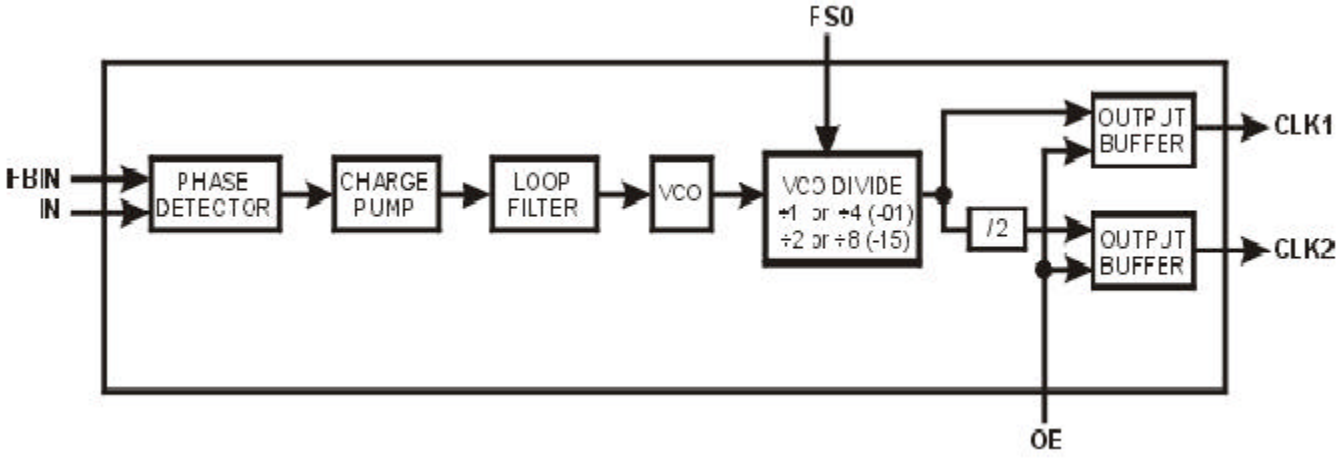
A common application of the ICS9173B is the implementation of a video genlock circuit. Because of this, the ICS9173B inputs operate on the negative-going clock edge.

The ICS9173B is pin and function compatible to the AV9173-01/15.

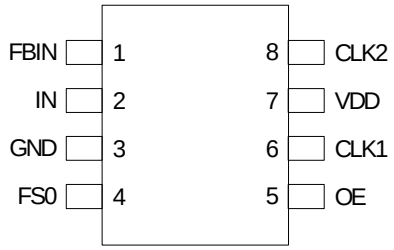
Features

- Phase-detector/VCO circuit block
- Ideal for genlock system
- Reference clock range 12 kHz to 1 MHz for full output clock range
- Output clock range of 1.25 to 75 MHz (-01), and 0.625 to 37.5 MHz (-15). See “Allowable Input Frequency to Output Frequency” table for conditions
- On-chip loop filter
- Single 5 V power supply
- Low power CMOS technology
- 8-pin SOIC package

Block Diagram



Pin Assignment



8 pin SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	FBIN	Input	Feedback input.
2	IN	Input	Input for reference sync pulse.
3	GND	Power	Ground.
4	FS0	Input	Frequency select 0 input.
5	OE	Input	Output enable.
6	CLK1	Output	Clock output 1.
7	VDD	Power	Power supply (+5 V).
8	CLK2	Output	Clock output 2 (divided-by-2 from Clock 1).

Allowable Input Frequency to Output Frequency for ICS9173B-01 (in MHz)

(ICS9173B-15 outputs run at exactly half of the ICS9173B-01 frequencies)

	f_{OUT} for FS = 0		f_{OUT} for FS = 1	
f_{IN} (kHz)	CLK1 Output	CLK2 Output	CLK1 Output	CLK2 Output
$12 \le f_{IN} \le 14$ kHz	44.0 to 75	22.0 to 37.5	11.0 to 18.75	5.5 to 9.375
$14 < f_{IN} \le 17$ kHz	30.0 to 75	15.0 to 37.5	7.5 to 18.75	3.75 to 9.375
$17 < f_{IN} \le 30$ kHz	25.0 to 75	12.5 to 37.5	6.25 to 18.75	3.125 to 9.375
$30 < f_{IN} \le 35$ kHz	15.0 to 75	7.5 to 37.5	3.75 to 18.75	1.875 to 9.375
$35 < f_{IN} \le 1000$ kHz	10.0 to 75	5.0 to 37.5	2.5 to 18.75	1.25 to 9.375

Using the ICS9173B in Genlock Applications

Most video sources, such as video cameras, are asynchronous, free-running devices. To digitize video or synchronize one video source to another free-running reference video source, a video “genlock” (generator lock) circuit is required. The ICS9173B integrates the analog blocks which make the task much easier.

In the complete video genlock circuit, the primary function of the ICS9173B is to provide the analog circuitry required to generate the video dot clock within a PLL. This application is illustrated in Figure 1. The input reference signal for this circuit is the horizontal synchronization (H-SYNC) signal. If a composite video reference source is being used, the h-sync pulses must be separated from the composite signal. A video sync separator circuit, such as the National Semiconductor LM1881, can be used for this purpose.

The clock feedback divider shown in Figure 1 is a digital divider used within the PLL to multiply the reference frequency. Its divide ratio establishes how many video dot clock cycles occur per h-sync pulse. For example, if 880 pixel clocks are desired per h-sync pulse, then the divider ratio is set to 880. Hence, together the h-sync frequency and external divider ratio establish the dot clock frequency:

$f_{OUT} = f_{IN}$ x N where N is external divide ratio

Both input pins IN and FBIN respond only to negative-going clock edges of the input signal. The H-SYNC signal must be constant frequency in the 12 kHz to 1 MHz range and stable (low clock jitter) for creation of a stable output clock.

The output hook-ups of the ICS9173B are dictated by the desired dot clock frequency. The primary consideration is the internal VCO which operates over a frequency range of 10 MHz to 75 MHz. Because of the selectable VCO output divider and the additional divider on output CLK2, four distinct output frequency ranges can be achieved. The following Table lists these ranges and the corresponding device configuration.

FS0 State	Output Used	Frequency/Range ICS9173B-01	Frequency/Range IcS9173B-15
0	CLK1	10 to 75 MHz	5 to 37.5 MHz
0	CLK2	5 to 37.5 MHz	2.5 to 18.75 MHz
1	CLK1	2.5 to 18.75 MHz	1.25 to 9.375 MHz
1	CLK2	1.25 to 9.375 MHz	0.625 to 4.6875 MHz

Note that both outputs, CLK1 and CLK2, are available during operation even though only one is fed back via the external clock divider.

Pin 5, OE, tristates both CLK1 and CLK2 upon logic low input. This feature can be used to revert dot clock control to the system clock when not in genlock mode (hence, when in genlock mode the system dot clock must be tristated).

When unused, inputs FS0 and OE must be tied to either GND (logic low) or VDD (logic high).

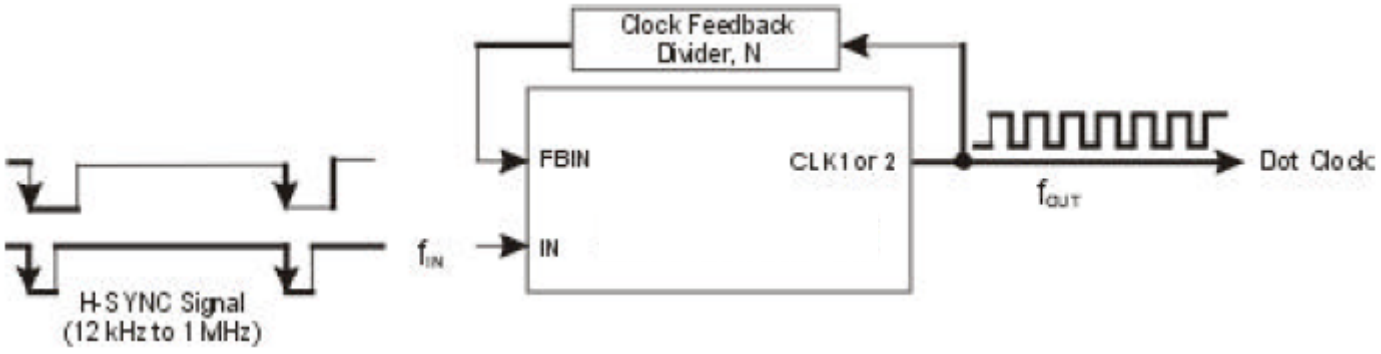


Figure 1: Typical Application of ICS9173B in a Video Genlock System

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS9173B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
Storage Temperature	-65 to +150°C
Voltage on I/O Pins referenced to GND	GND - 0.5 V to VDD + 0.5 V
Junction Temperature	125°C
Soldering Temperature	260°C
Power Dissipation	0.5 Watts

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Temperature under Bias	-0		+70	°C
Power Supply Voltage (measured with respect to GND)	+4.75	+5 V	+5.25	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 5 V ±5%**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Supply Current	IDD	No load,50 MHz		20	50	mA
Input Low Voltage	V_{IH}	VDD = 5 V			0.8	V
Input High Voltage	V_{IL}	VDD = 5 V	2.0			V
Input Low Current	I_{IL}	VIN = 0V	-5			µA
Input High Current	I_{IH}	VIN = VDD	-5		5	µA
Output Low Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Output High Voltage [1]	V_{OH1}	I_{OH} = -1 mA	VDD-0.4			V
Output High Voltage [1]	V_{OH2}	I_{OH} = -4 mA	VDD-0.8			V
Output High Voltage [1]	V_{OH3}	I_{OH} = -8 mA	2.4			V

Notes:
1. Duty cycle measured at 1.4 V.
2. Input Reference Frequency = 25 kHz, Output Frequency = 25 MHz. Jitter measured between adjacent vertical pixels.
3. CLK1 frequency applies for FS = 0. For FS = 1 condition, divide allowable CLK1 range by the factor of 4.

AC Electrical Characteristics

Unless stated otherwise, **VDD = 5 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Clock Rise Time [1]	$ICLK_r$				10	ns
Output Clock Fall Time [1]	$ICLK_f$				10	ns
Output Rise Time [1]	t_{r1}	15 pF load, 0.8 to 2.0V		0.6	1.5	ns
Output Rise Time [1]	t_{r2}	15 pF load, 20% to 80% VDD		1.3	3.0	ns
Output Fall Time [1]	t_{f1}	15 pF load, 0.8 to 2.0V		0.6	1.5	ns
Output Fall Time [1]	t_{f2}	15 pF load, 80% to 20% VDD		0.7	2.0	ns
Output Duty Cycle [1]		15 pF load	40	47	55	%
One-Sigma Jitter [1, 5]	$T1_S1$	CLK1 frequency [3], 25 MHz		120	250	ps
Jitter, Absolute [1, 5]	$T_{ABS}1$	CLK1 frequency [3], 25 MHz	-400	±250	400	ps
One-Sigma Jitter [1, 5]	$T1_S2$	CLK1 frequency < 25 MHz			1	%
Jitter, Absolute [1, 5]	$T_{ABS}2$	CLK1 frequency < 25 MHz			2	%
Line-to-Line Jitter [1], Absolute [2]	T_{LABS}			±4		ns
Input Frequency [1], IN or FBIN	f_{IN}	see allowable fi below	12		1000	kHz
CLK1 Frequency, -01 [1, 3, 4]	f_{CLK1}	$12 \le f_{IN} \le 14$ kHz	44		75	MHz
		$14 < f_{IN} \le 17$ kHz	30		75	
		$17 < f_{IN} \le 30$ kHz	25		75	
		$30 < f_{IN} \le 35$ kHz	15		75	
		$35 < f_{IN} \le 1000$ kHz	10		75	
CLK1 Frequency, -15 [1, 3, 4]	f_{CLK1}	$12 \le f_{IN} \le 14$ kHz	22		37.5	MHz
		$14 < f_{IN} \le 17$ kHz	15		37.5	
		$17 < f_{IN} \le 30$ kHz	12.5		37.5	
		$30 < f_{IN} \le 35$ kHz	7.5		37.5	
		$35 < f_{IN} \le 1000$ kHz	5		37.5	

Notes:

1. Parameter is guaranteed by design and characterization. Not 100% tested in production.

2. Input Reference Frequency = 25 kHz, Output Frequency = 25 MHz. Jitter measured between adjacent vertical pixels.

3. CLK1 frequency applies for FS = 0. For FS = 1 condition, divide allowable CLK1 range by the factor of 4.

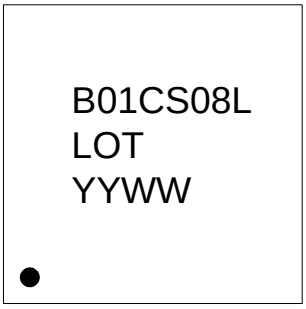
4. An Application Brief (AB01) documents the operation of the AV9173 for low input frequencies. This provides guidelines for usable output frequencies and feedback ratios required to use inputs below 25 kHz. By following these guidelines, the ICS9173B will operate down to 12 kHz inputs across temperature, voltage and lot-to-lot variation.

5. Jitter values are measured at frequencies $\geq$ 25 MHz for IDT9173B-01, for ICS9173B-15, jitter is measured at frequency $\geq$ 12.5 MHz.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W
Thermal Resistance Junction to Top of Case	Ψ_{JT}	Still air		20		°C/W

Marking Diagram

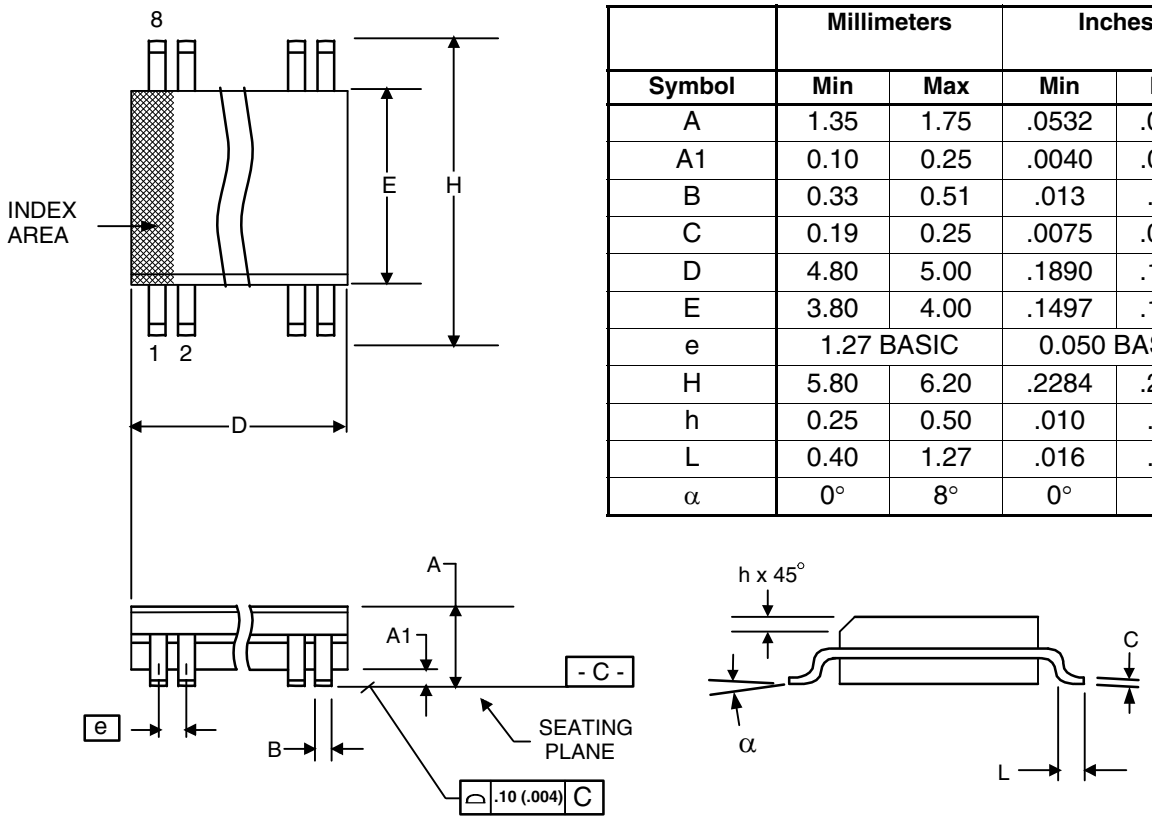


Notes:

1. Line 1: truncated part number
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “LOT” denotes the lot number.
4. “L” suffix designates RoHS compliant package.
5. Bottom mark: country of origin.

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9173B-01CS08LF	Tubes	8-pin SOIC	0 to +70° C
9173B-01CS08LFT	Tape and Reel	8-pin SOIC	0 to +70° C
9173B-15CS08LF	Tubes	8-pin SOIC	0 to +70° C
9173B-15CS08LFT	Tape and Reel	8-pin SOIC	0 to +70° C

"LF" suffix to the part number denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	R.Willner	09/23/08	New datasheet.
B	RDW	11/12/09	Released to final.
C	RDW	07/29/11	Corrected typographical errors on page 5 for rise/fall times
D	LPL	01/29/13	Added top-side device marking

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