Low Voltage 1:20 Differential PECL/HSTL Clock Fanout Buffer

8T33FS6221

DATASHEET

Description

The 8T33FS6221 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the 8T33FS6221 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

The 8T33FS6221 is designed for low skew clock distribution systems and supports clock frequencies up to 2GHz. The device accepts two clock sources. The CLK0 input can be driven by PECL compatible signals, the CLK1 input accepts HSTL compatible signals. The selected input signal is distributed to 20 identical, differential PECL outputs. If V_{BB} is connected to the nCLK0 or nCLK1 input and bypassed to GND by a 10nF capacitor, the 8T33FS6221 can be driven by single-ended PECL signals utilizing the V_{BB} bias voltage output.

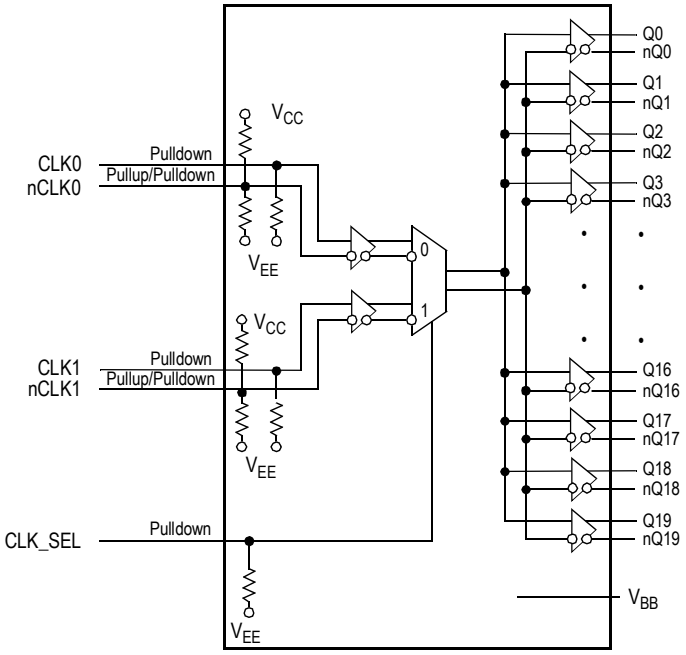
In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The 8T33FS6221 can be operated from a single 3.3V or 2.5V supply.

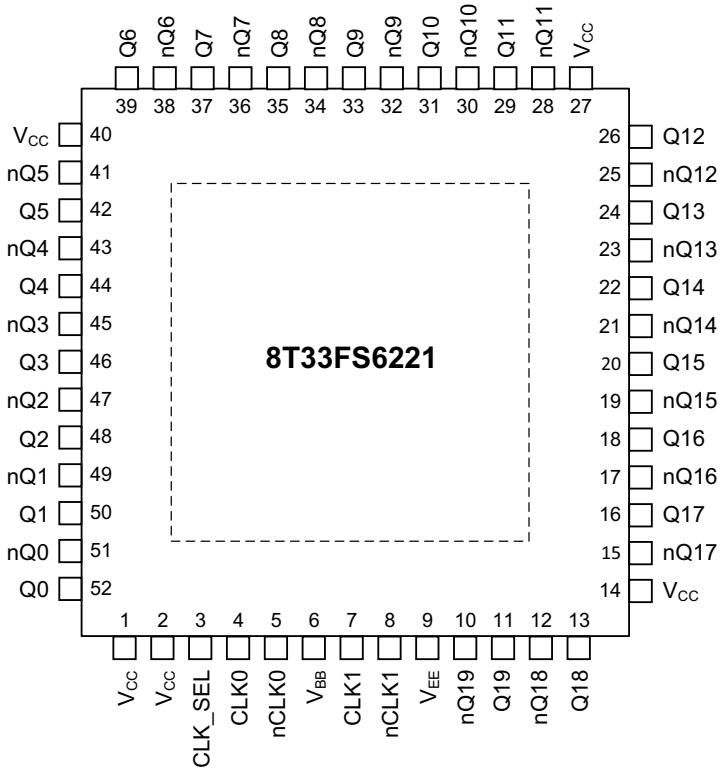
Features

- 1:20 differential clock fanout buffer
- 50ps typical device skew
- SiGe technology
- Maximum output frequency: 2GHz
- PECL compatible differential clock outputs
- PECL/ HSTL compatible differential clock inputs
- Single 3.3V or 2.5V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Lead-free Packaging

Block Diagram



Pin Assignment



52-pin, 10mm x 10mm LQFP Package, exposed pad

Pin Description

Table 1. Pin Description Table

Number	Name	Type		Description
1	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
2	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
3	CLK_SEL	Input	Pull-down	Clock reference select input.
4	CLK0	Input	Pull-down	Differential reference clock signal input.
5	nCLK0	Input	Pull-up/ Pull-down	Differential reference clock signal input.
6	V_{BB}	Output		Reference voltage output for single ended PECL operation.
7	CLK1	Input	Pull-down	Differential reference clock signal input.
8	nCLK1	Input	Pull-up/ Pull-down	Differential reference clock signal input.
9	V_{EE}[1]	Power		Negative power supply.
10	nQ19	Output	PECL	Differential clock output.
11	Q19	Output	PECL	Differential clock output.
12	nQ18	Output	PECL	Differential clock output.
13	Q18	Output	PECL	Differential clock output.
14	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
15	nQ17	Output	PECL	Differential clock output.
16	Q17	Output	PECL	Differential clock output.
17	nQ16	Output	PECL	Differential clock output.
18	Q16	Output	PECL	Differential clock output.
19	nQ15	Output	PECL	Differential clock output.
20	Q15	Output	PECL	Differential clock output.
21	nQ14	Output	PECL	Differential clock output.
22	Q14	Output	PECL	Differential clock output.
23	nQ13	Output	PECL	Differential clock output.
24	Q13	Output	PECL	Differential clock output.
25	nQ12	Output	PECL	Differential clock output.
26	Q12	Output	PECL	Differential clock output.
27	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
28	nQ11	Output	PECL	Differential clock output.
29	Q11	Output	PECL	Differential clock output.
30	nQ10	Output	PECL	Differential clock output.
31	Q10	Output	PECL	Differential clock output.
32	nQ9	Output	PECL	Differential clock output.

Table 1. Pin Description Table

Number	Name	Type		Description
33	Q9	Output	PECL	Differential clock output.
34	nQ8	Output	PECL	Differential clock output.
35	Q8	Output	PECL	Differential clock output.
36	nQ7	Output	PECL	Differential clock output.
37	Q7	Output	PECL	Differential clock output.
38	nQ6	Output	PECL	Differential clock output.
39	Q6	Output	PECL	Differential clock output.
40	V_{CC}	Power		Power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
41	nQ5	Output	PECL	Differential clock output.
42	Q5	Output	PECL	Differential clock output.
43	nQ4	Output	PECL	Differential clock output.
44	Q4	Output	PECL	Differential clock output.
45	nQ3	Output	PECL	Differential clock output.
46	Q3	Output	PECL	Differential clock output.
47	nQ2	Output	PECL	Differential clock output.
48	Q2	Output	PECL	Differential clock output.
49	nQ1	Output	PECL	Differential clock output.
50	Q1	Output	PECL	Differential clock output.
51	nQ0	Output	PECL	Differential clock output.
52	Q0	Output	PECL	Differential clock output.
ePAD	V_{EE_EP}	Power		Exposed pad of package. Connect to ground.

NOTE 1. In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3 V or +2.5 V. The input and output levels are referenced to the most positive supply (V_{CC}).

Table 2. Function Table

Control Pin	0 (Default)	1
CLK_SEL	CLK0, nCLK0 input pair is the reference clock. CLK0 can be driven by PECL compatible signals.	CLK1, nCLK1 input pair is the reference clock. CLK1 can be driven by HSTL compatible signals.

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings Table[1]

Symbol	Characteristics	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Supply Voltage		–0.3		3.6	V
V_{IN}	DC Input Voltage		–0.3		V_{CC} + 0.3	V
V_{OUT}	DC Output Voltage		–0.3		V_{CC} + 0.3	V
I_{IN}	DC Input Current				±20	mA
I_{OUT}	DC Output Current				±50	mA
T_S	Storage Temperature		–65		125	°C
T_J	Operating Junction Temperature				125	°C

NOTE 1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

DC Electrical Characteristics

Table 4. General Specifications

Symbol	Characteristics	Condition	Minimum	Typical	Maximum	Unit
V_{TT}	Output Termination Voltage[1]			V_{CC} – 2		V
MM	ESD Protection (Machine Model)[2]		200			V
HBM	ESD Protection (Human Body Model)[2]		4000			V
CDM	ESD Protection (Charged Device Model)[2]		2000			V
LU	Latch-Up Immunity		200			mA
C_{IN}	Input Capacitance	Inputs		4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
R_{PULLUP}	Input Pullup Resistor			75		kΩ

NOTE 1. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.

NOTE 2. According to JEDEC/JS-001-2012/JESD22-C101E.

Table 5. PECL DC Characteristics, V_{CC} = 2.5V ±5% or V_{CC} = 3.3V ±5%, V_{EE} = GND, T_A = -40°C to +85°C

Symbol	Characteristics	Condition	Minimum	Typical	Maximum	Unit
Clock Input Pair CLK0, nCLK0 (PECL Differential Signals)[1]						
V_{PP}	Differential Input Voltage[2]	Differential Operation	0.2		1.3	V
V_{CMR}	Differential Crosspoint Voltage[3]	Differential Operation	1.0		$V_{CC} – V_{PP}/2$	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			±100	µA
Clock Input Pair CLK1, nCLK1 (HSTL Differential Signals)[4]						
V_{DIF}	Differential Input Voltage (peak-to-peak)[5]		0.2		1.4	V
V_X	Differential Crosspoint Voltage[6]		0.1	0.68 - 0.9	$V_{CC} – 1.0$	V
I_{IN}	Input Current	$V_{IN} = V_X$ ± 0.2V			±100	µA
Control Input CLK_SEL						
V_{IH}	Input Voltage High		$V_{CC} – 1.165$		V_{CC}	V
V_{IL}	Input Voltage Low		V_{EE}		$V_{CC} – 1.475$	V
I_{IN}	Input Current[7]	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			±100	µA
PECL Clock Outputs (Q[0:19], nQ[0:19]						
V_{OH}	Output High Voltage	I_{OH} = –30mA[8]	$V_{CC} – 1.1$		$V_{CC} – 0.7$	V
V_{OL}	Output Low Voltage	I_{OL} = –5mA[8]	$V_{CC} – 1.9$		$V_{CC} – 1.4$	V
Supply Current and V_{BB}						
I_{EE}[9]	Maximum Quiescent Supply Current without Output Termination Current	V_{EE} pins			160	mA
V_{BB}	Output Reference Voltage (f_{REF} < 1.0GHz)[10]	I_{BB} = 0.4mA	$V_{CC} – 1.4$		$V_{CC} – 1.2$	V

NOTE 1. The input pairs CLK0, CLK1 are compatible to differential signaling standards. CLK0 is compatible to LVPECL signals and CLK1 meets both HSTL differential signal specifications. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).

NOTE 2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality. V_{IL} should not be less than -0.3V. V_{IH} should not be greater than V_{CC}.

NOTE 3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

NOTE 4. Clock inputs driven by differential HSTL compatible signals. Only applicable to CLK1, nCLK1.

NOTE 5. V_{DIF} (DC) is the minimum differential HSTL input voltage swing is required for device functionality. V_{IL} should not be less than -0.3V. V_{IH} should not be greater than V_{CC}.

NOTE 6. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.

NOTE 7. Input have internal pullup/pulldown resistors which affect the input current.

NOTE 8. Equivalent to a termination of 50Ω to V_{TT}.

NOTE 9. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}.
I_{CC} = (number of differential output used) x ($V_{OH} – V_{TT}$)/R_{load} + ($V_{OL} – V_{TT}$)/R_{load} + I_{EE}.

NOTE 10. Using V_{BB} to bias unused single-ended inputs is recommended only up to a clock reference frequency of 1GHz. Above 1GHz, only differential input signals should be used with the 8T33FS6221.

AC Electrical Characteristics

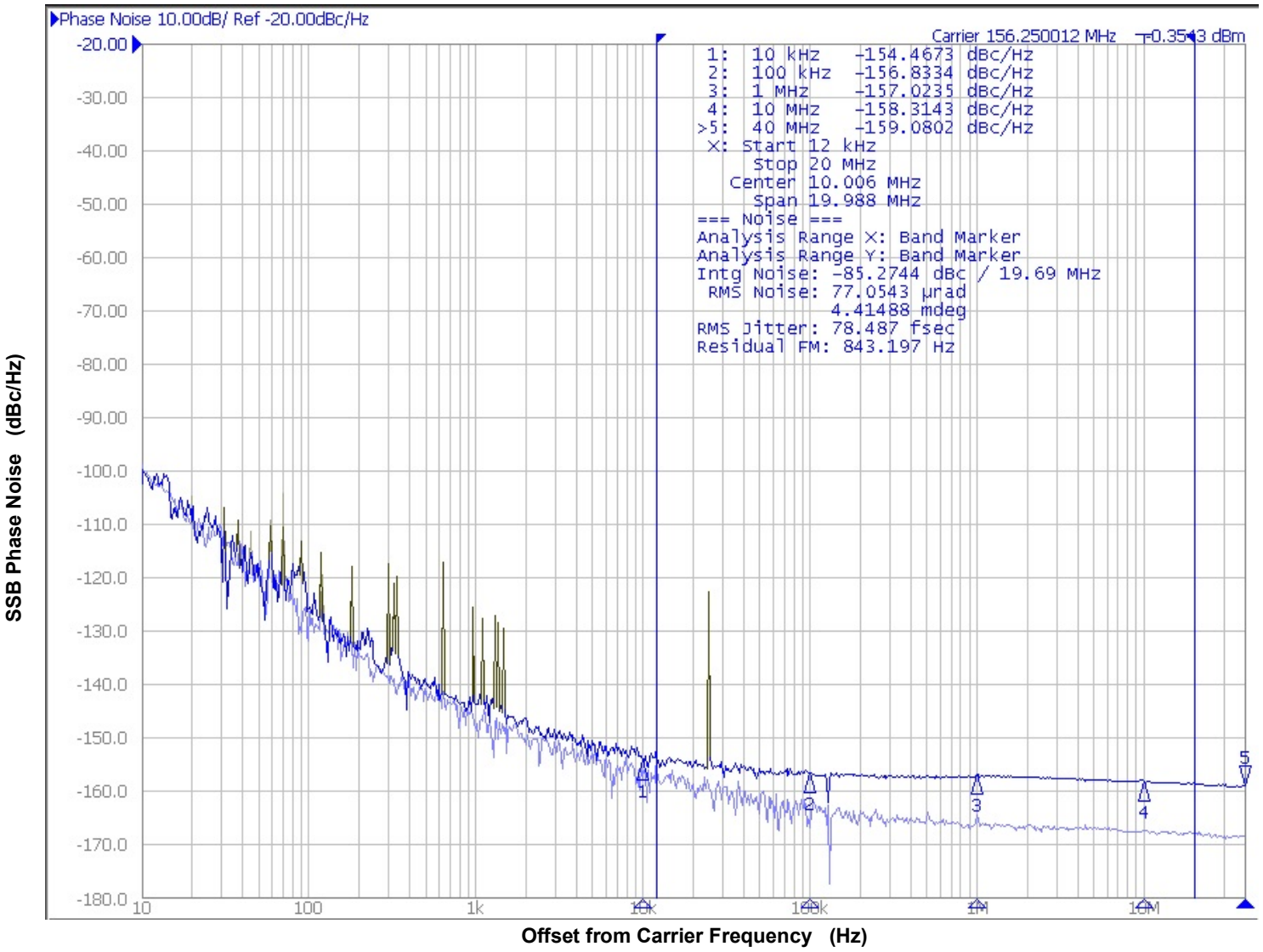
Table 6. AC Characteristics, V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, V_{EE} = GND, T_A = –40°C to +85°C[1]

Symbol	Characteristics		Condition	Min	Typ	Max	Unit
Clock Input Pair CLK0, nCLK0 (PECL Differential Signals)							
f_{CLK}	Input Frequency		Differential			2000	MHz
t_{PD}	Propagation Delay	CLK0 to Q[0:19]	Differential	300	450	670	ps
Clock Input Pair CLK1, nCLK1 (HSTL Differential Signals)							
f_{CLK}	Input Frequency		Differential			1000	MHz
t_{PD}	Propagation Delay	CLK1 to Q[0:19]	Differential	330	600	800	ps
PECL Clock Outputs (Q[0:19], nQ[0:19])							
$V_{O(P-P)}$	Output Voltage (peak-to-peak)	f_O < 1.0 GHz			0.7		V
		f_O < 2.0 GHz			0.7		V
$t_{sk(O)}$	Output-to-Output Skew		Differential		50	100	ps
$t_{sk(PP)}$	Part-to-Part Skew	using CLK0	Differential			270	ps
		using CLK1				300	ps
		parts at one given T_J, V_{CC}, f_{ref}				250	ps
t_{JIT}	Buffer Additive Phase Jitter, RMS		f_{OUT} = 156.25MHz, Integration Range: 12kHz - 20MHz		78	125	fs
odc	Output Duty Cycle	f_{REF} < 0.1GHz	DC_{REF} = 50%	49		51	%
		f_{REF} < 1.0GHz	DC_{REF} = 50%	45		55	%
t_r, t_f	Output Rise/Fall Time		20% to 80%	50		350	ps

NOTE 1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

Additive Phase Jitter

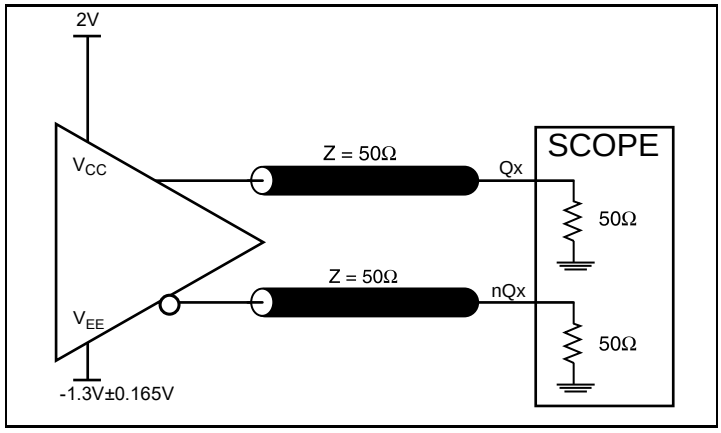
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



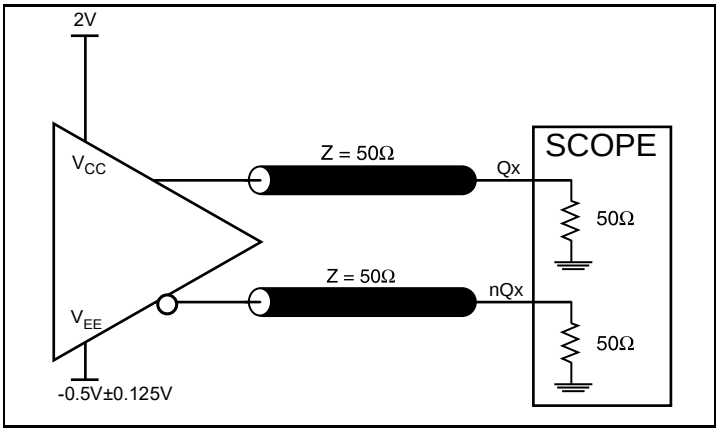
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

Measured using a Wenzel, 156.25MHz Oscillator as the input source.

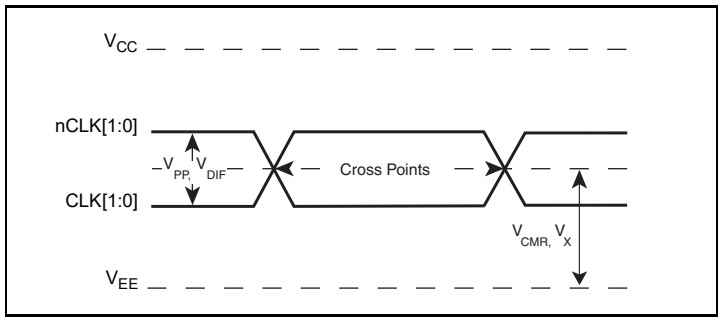
Parameter Measurement Information



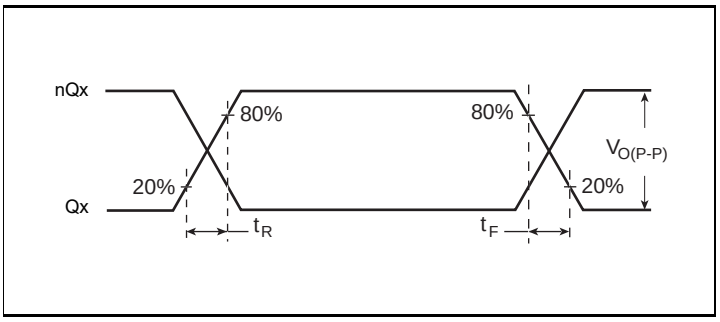
3.3V LVPECL Output Load AC Test Circuit



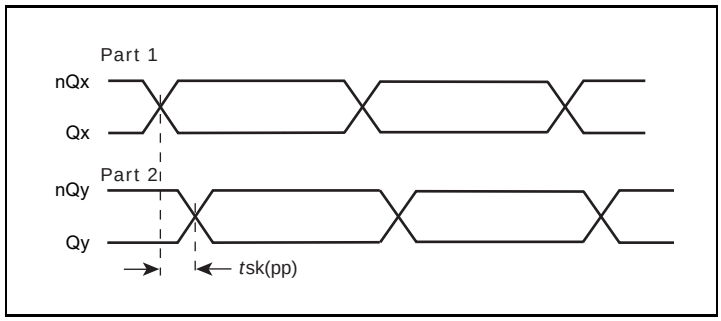
2.5V LVPECL Output Load AC Test Circuit



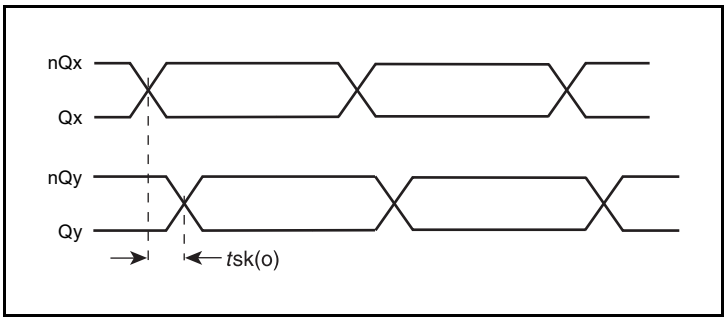
Differential Input Level



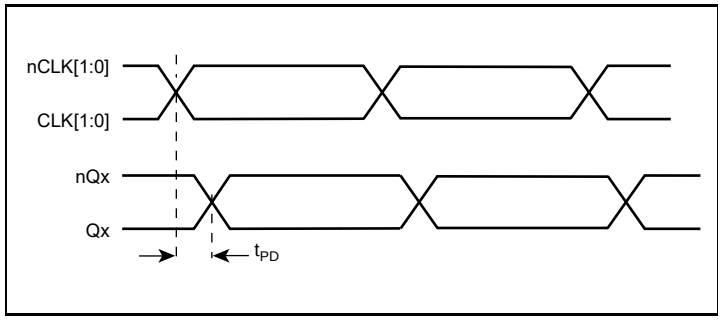
Output Rise/Fall Time



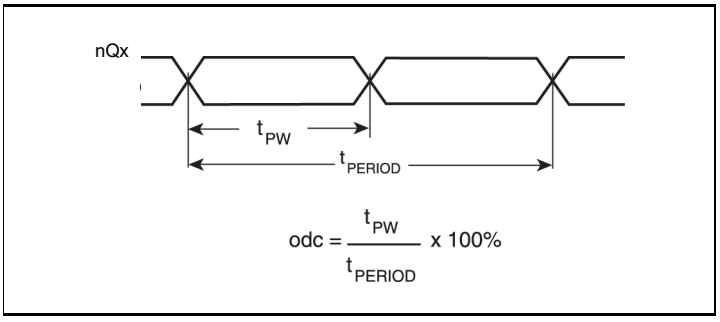
Part-to-Part Skew



Output Skew



Propagation Delay



Output Duty Cycle/Pulse Width

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLKx/nCLKx Inputs

For applications not requiring the use of a differential input, both the CLKx and nCLKx pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLKx to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

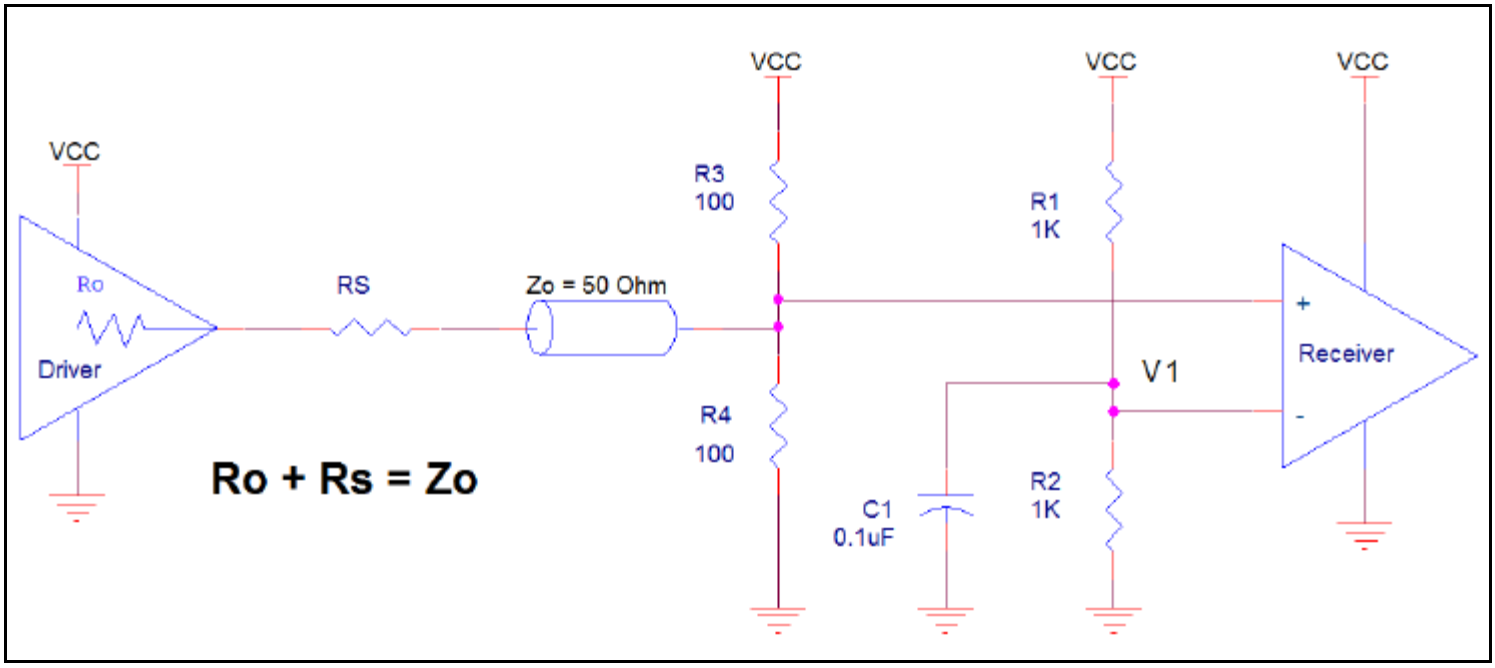


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V LVPECL Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 2A to* Figure 2E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 2A*, the input termination applies for IDT open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

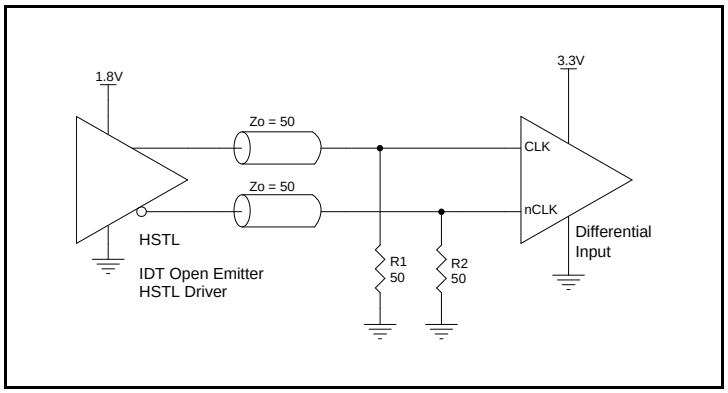


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter HSTL Driver

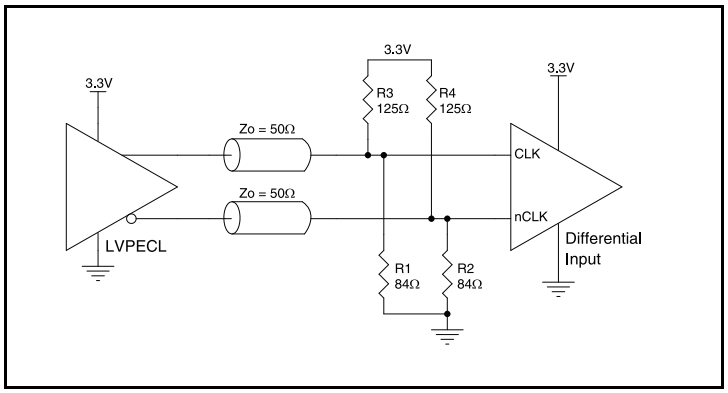


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

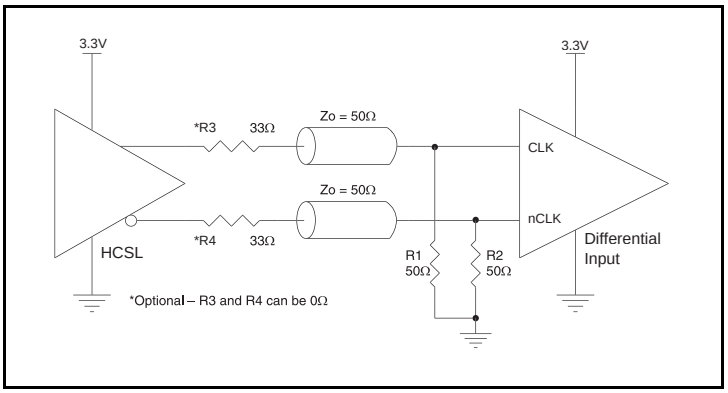


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

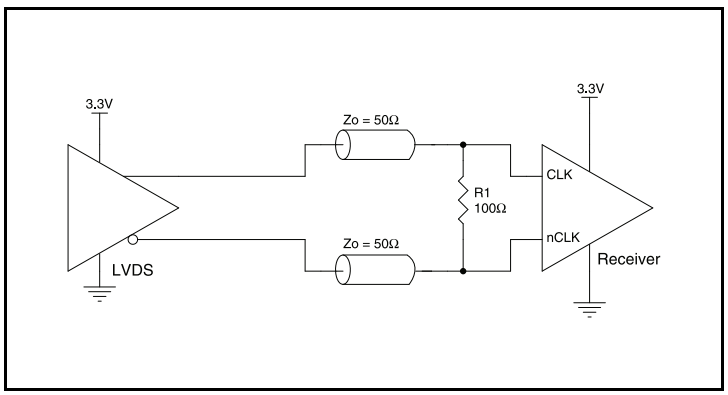


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V LVPECL Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, HSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 3A to Figure 3E* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter HSTL drivers. If you are using an HSTL driver from another vendor, use their termination recommendation.

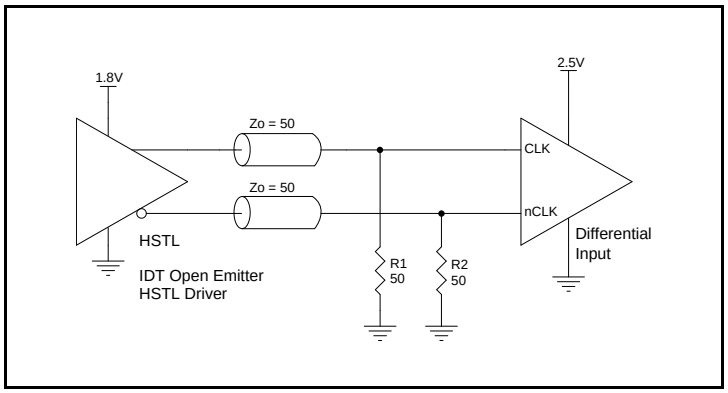


Figure 3A. CLKx/nCLKx Input Driven by an IDT Open Emitter HSTL Driver

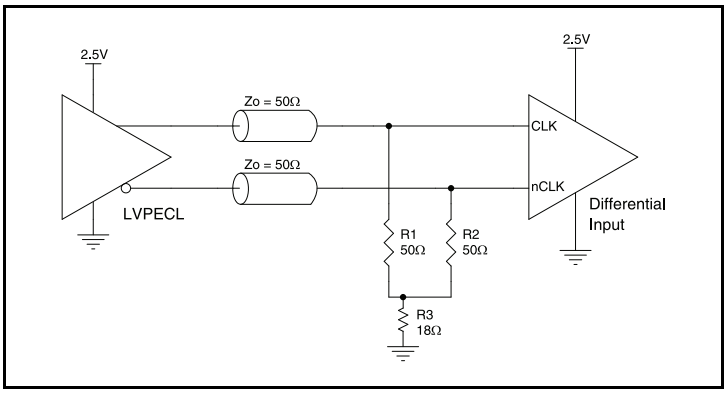


Figure 3D. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

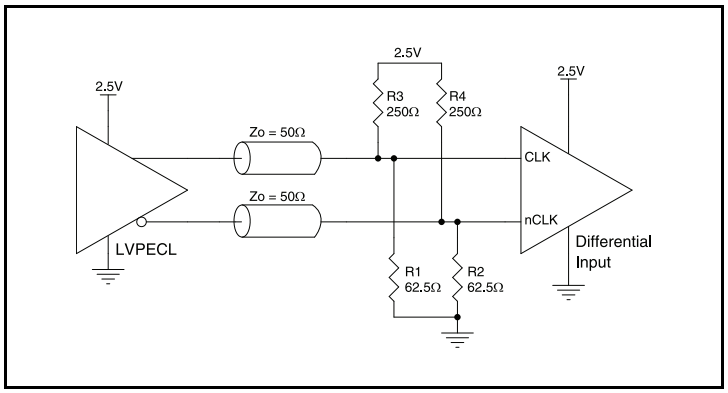


Figure 3B. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

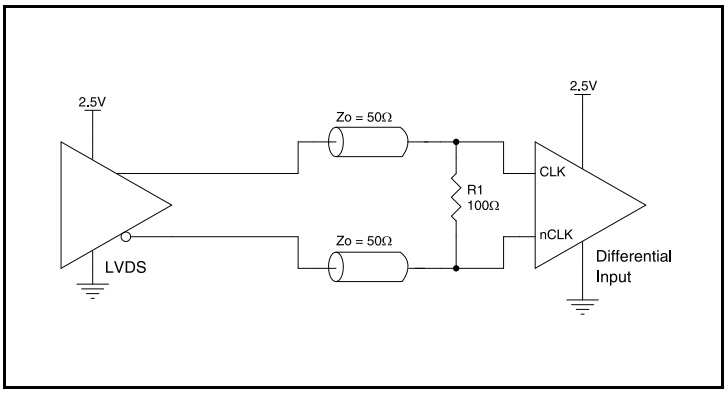


Figure 3E. CLKx/nCLKx Input Driven by a 2.5V LVDS Driver

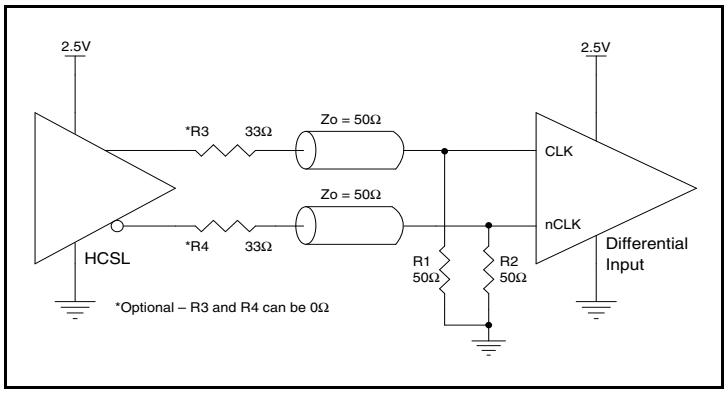


Figure 3C. CLKx/nCLKx Input Driven by a 2.5V HCSL Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 4A and Figure 4B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

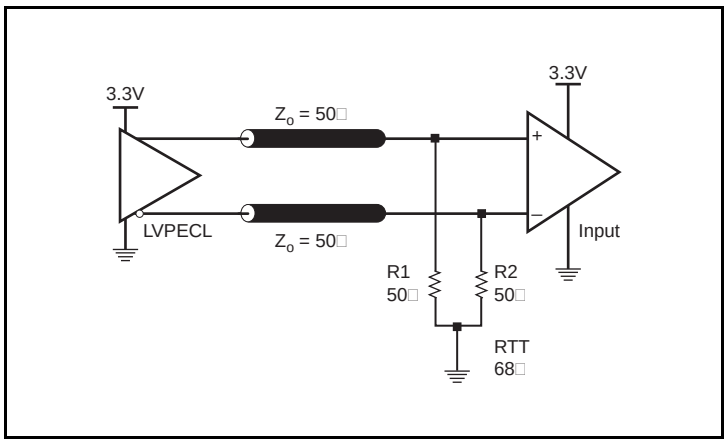


Figure 4A. 3.3V LVPECL Output Termination

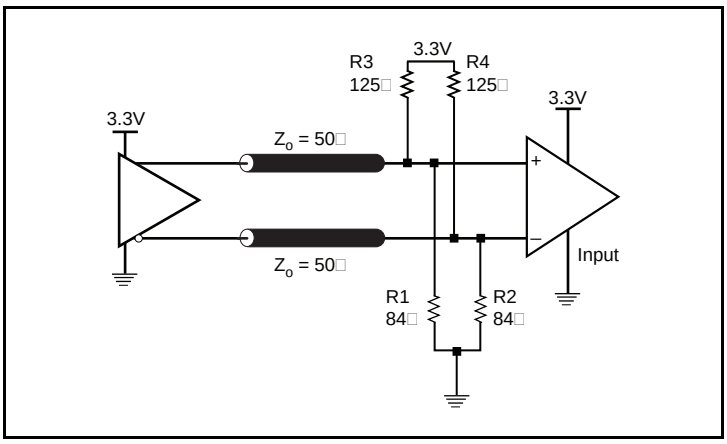


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C*.

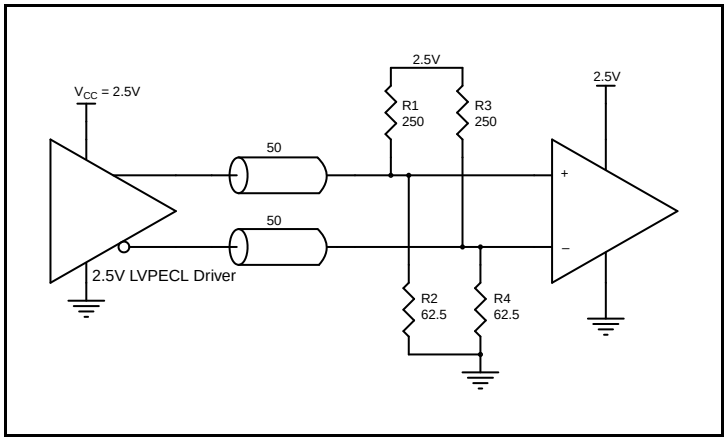


Figure 5A. 2.5V LVPECL Driver Termination Example

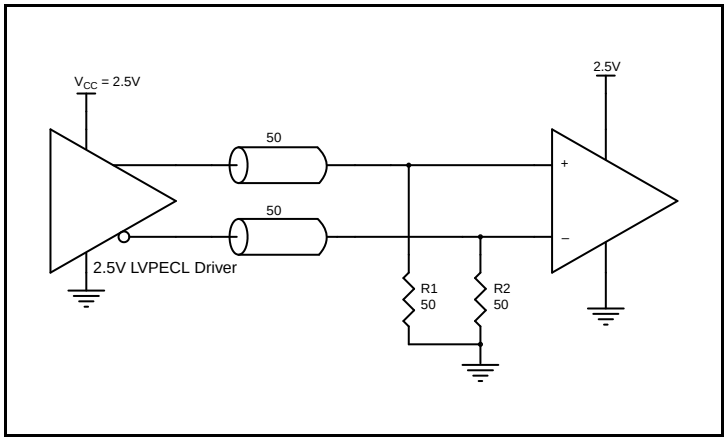


Figure 5B. 2.5V LVPECL Driver Termination Example

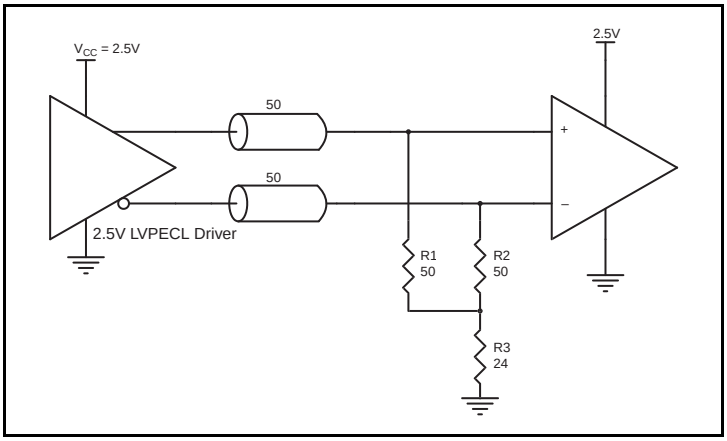


Figure 5C. 2.5V LVPECL Driver Termination Example

EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Lead-frame Base Package, Amkor Technology.

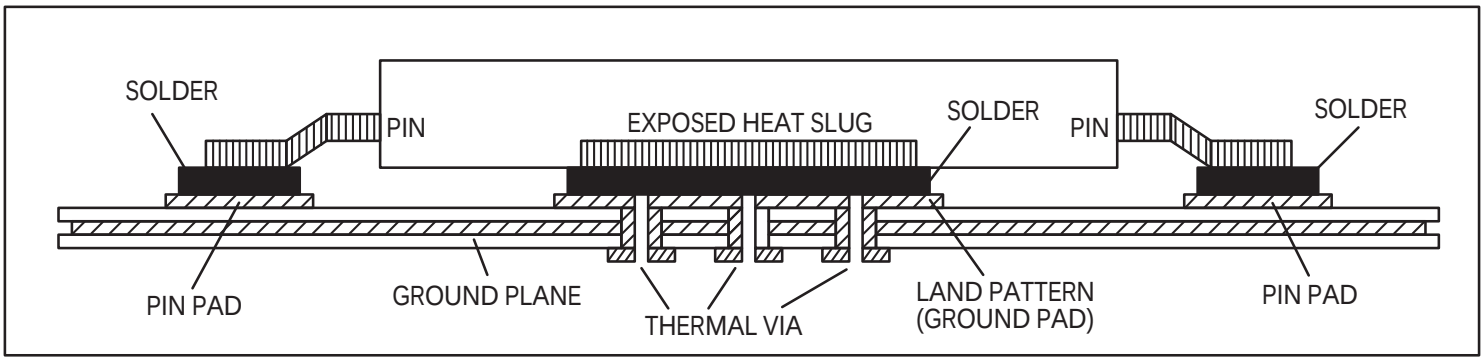


Figure 6. Assembly for Exposed Pad Thermal Release Path - Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the 8T33FS6221.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8T33FS6221 is the sum of the core power plus the power dissipated due to the load.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- The maximum current at 85C is: I_{EE_max} = **160mA**
- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 160mA = **554.4mW**
- Power $(outputs)_{MAX}$ = **35mW/Loaded Output pair**
  If all outputs are loaded, the total power is 20 * 35mW = **700mW**

  Total Power$_{MAX}$ (3.465V, with all outputs switching) = 554.4mW + 700mW = **1254mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 26.84°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.254W * 26.84°C/W = 118.7°C. This is within the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 52-Lead LQFP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	26.84°C/W	22.08°C/W	20.54°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 7*.

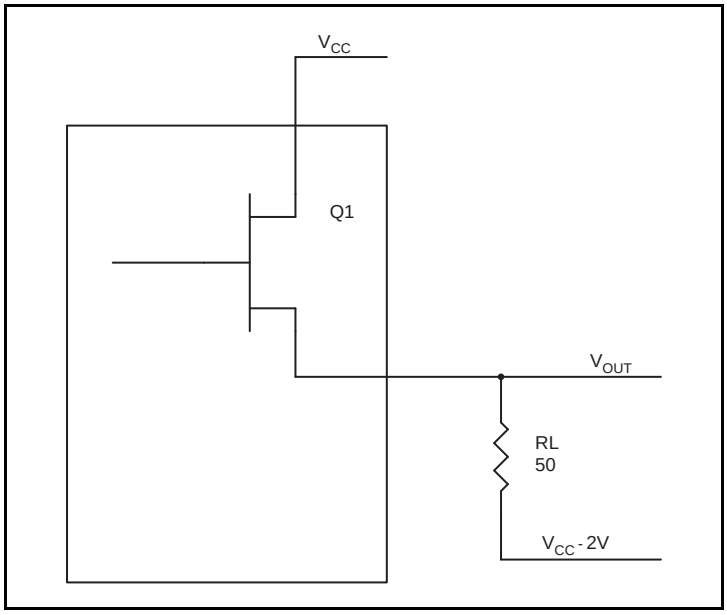


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CC_MAX} – 0.7V**
  ($V_{CC\_MAX} - V_{OH\_MAX}$) = **0.7V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CC_MAX} – 1.4V**
  ($V_{CC\_MAX} - V_{OL\_MAX}$) = **1.4V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.7V)/50\Omega] * 0.7V =$ **18.2mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.4V)/50\Omega] * 1.4V =$ **16.8mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **35mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 52 Lead LQFP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	26.84°C/W	22.08°C/W	20.5°C/W

Transistor Count

The transistor count for 8T33FS6221 is: 1689

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T33FS6221ETGI	IDT8T33FS6221ETGI	10.0 x 10.0 x 1.0 mm TQFP	Tray	-40°C to +85°C
8T33FS6221ETGI8	IDT8T33FS6221ETGI	10.0 x 10.0 x 1.0 mm TQFP	Tape & Reel	-40°C to +85°C

NOTE: Parts that are ordered with an “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

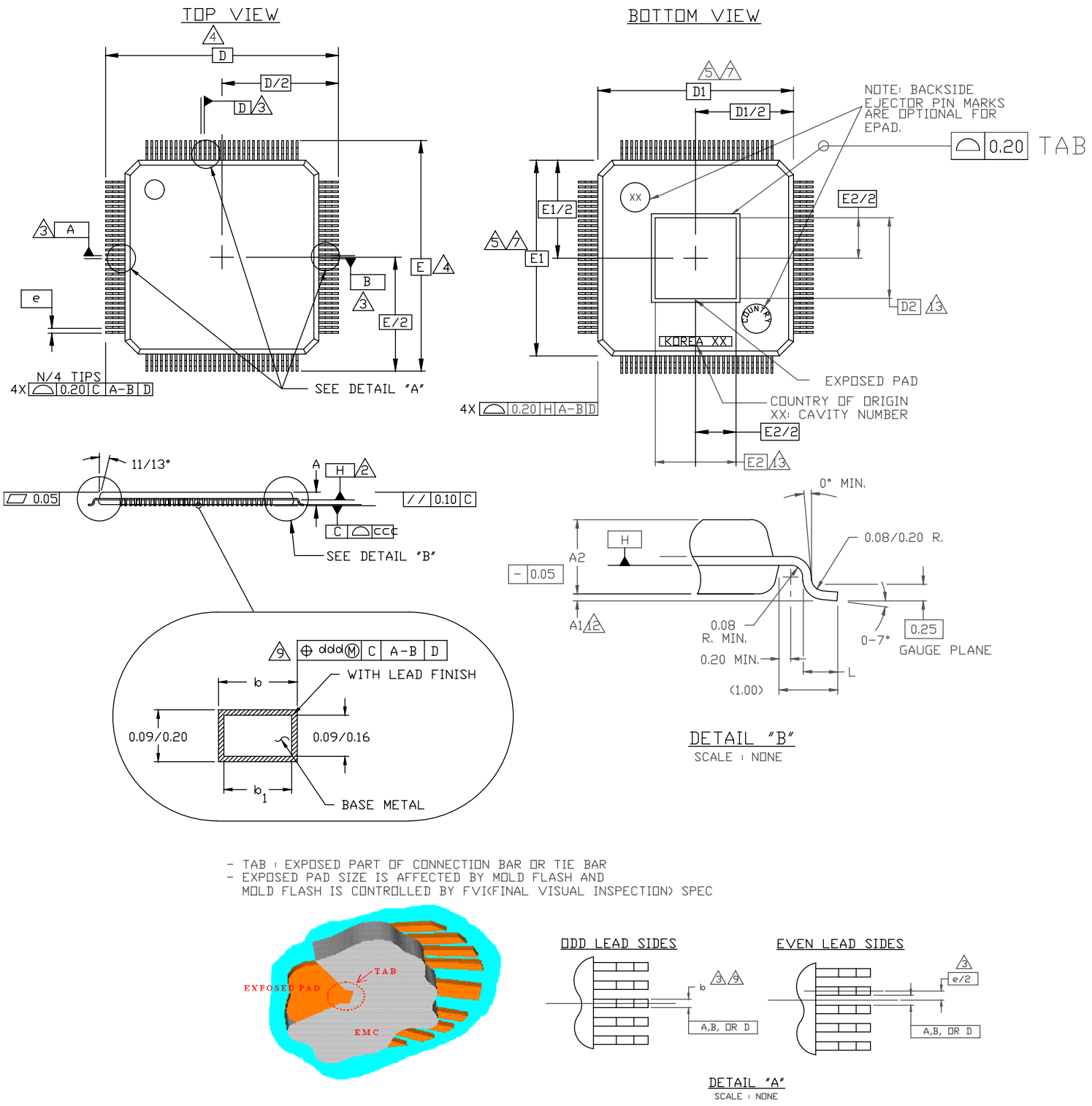
Revision History

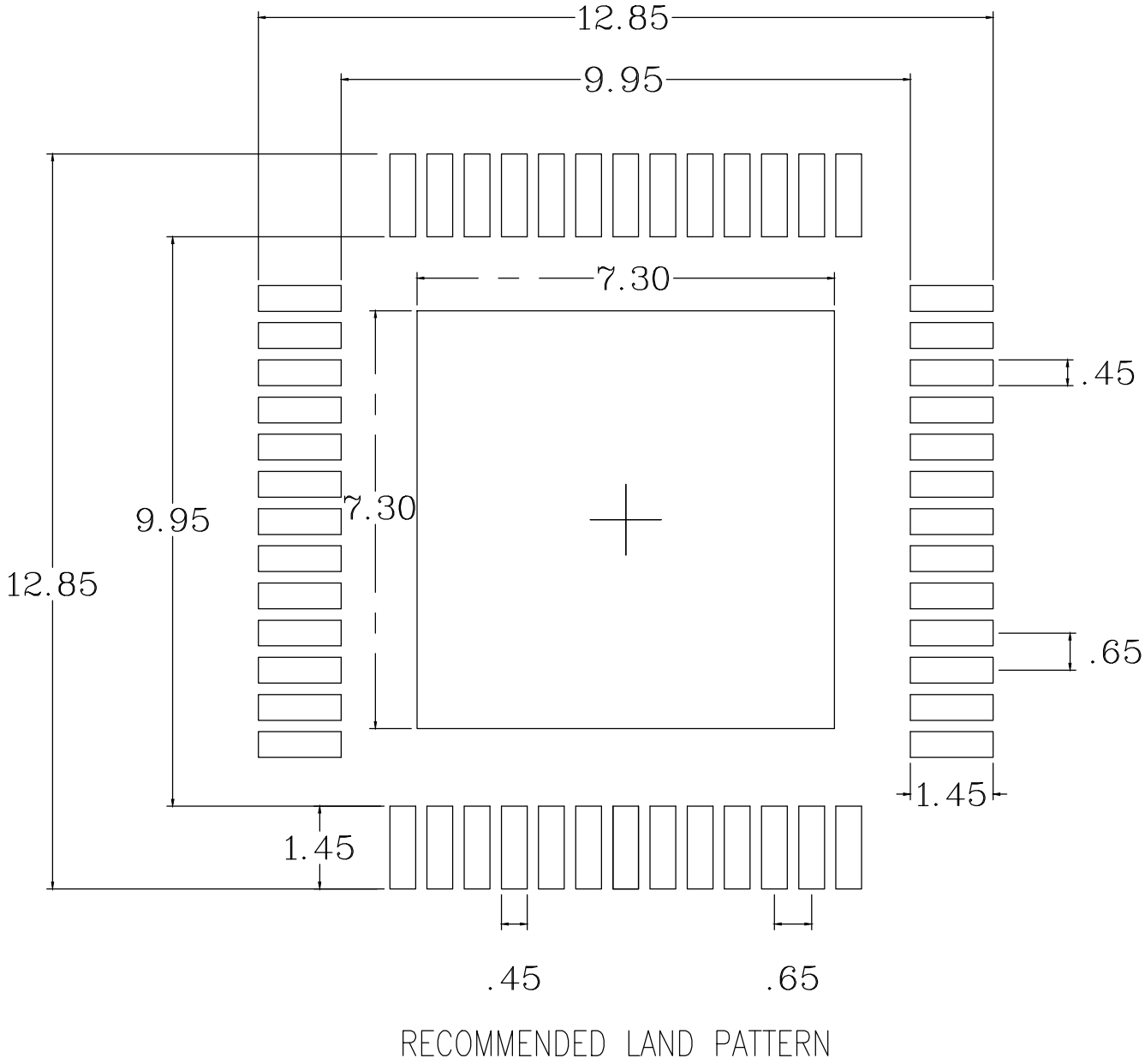
Revision	Revision Date	Description of Change
1.1	Apr 8, 2021	• Updated Package Outline Drawings section. • Updated Part/Order Number suffix from EPGI to ETGI. • Updated Marking suffix from EPGI to ETGI. • Added links to package outline drawings in Ordering Information. • Rebranded document to Renesas.
1.0	Jun 25, 2015	Initial release.

52-TQFP, Package Outline Drawing

10.0 x 10.0 x 1.0 mm Body, 0.65mm Pitch

ETG52P1, PSC-4863-01, Rev 01, Page 1





RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE [H] LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS [A-B] AND [D] TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE [H].
4. TO BE DETERMINED AT SEATING PLANE [C].
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE [H].
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATIONS ACB, ACC, ACD & ACE.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
13. DIMENSION D2 AND E2 REPRESENT THE SIZE OF THE EXPOSED PAD. THE ACTUAL DIMENSIONS ARE SPECIFIED ON THE BONDING DIAGRAM, AND IS DEPENDENT ON THE DIE SIZE.
14. EXPOSED PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE.

SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
	ACC			NOTE
	MIN.	NOR.	MAX.	
A	~	~	1.20	
A_1	0.05	~	0.15	12
A_2	0.95	1.00	1.05	
D	12.00 BSC.			4
D_1	10.00 BSC.			7,8
E	12.00 BSC.			4
E_1	10.00 BSC.			7,8
L	0.45	0.60	0.75	
D2	7.20	7.30	7.40	13
E2	7.20	7.30	7.40	13
N	52			9
e	0.65 BSC			
b	0.22	0.32	0.38	
b1	0.22	0.30	0.33	
ccc	~	~	0.10	
ddd	~	~	0.13	

		Package Revision History
Date Created	Rev No.	Description
May 8, 2020	00	Initial release
May 12, 2021	01	Add land pattern

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