

## GENERAL DESCRIPTION

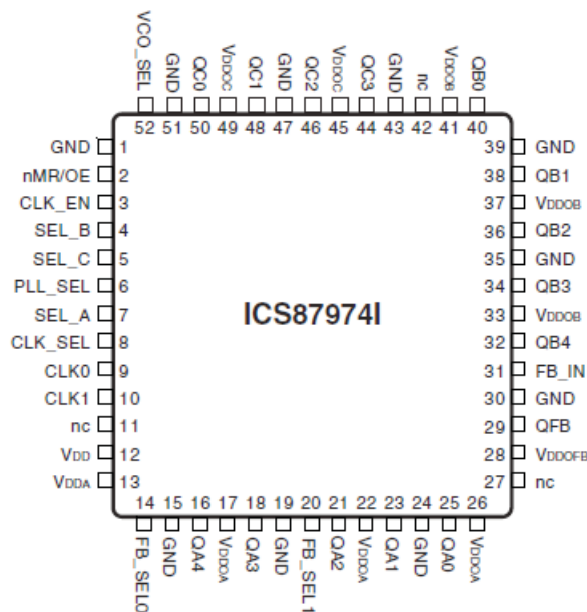
The 87974I is a low skew, low jitter 1-to-15 LVCMOS/LVTTL Clock Generator/Zero Delay Buffer. The device has a fully integrated PLL and three banks whose divider ratios can be independently controlled, providing output frequency relationships of 1:1, 2:1, 3:1, 3:2, 3:2:1. In addition, the external feedback connection provides for a wide selection of output-to-input frequency ratios. The CLK0 and CLK1 pins allow for redundant clocking on the input and dynamically switching the PLL between two clock sources.

Guaranteed low jitter and output skew characteristics make the 87974I ideal for those applications demanding well defined performance and repeatability.

## FEATURES

- Fully integrated PLL
- Fifteen single ended 3.3V LVCMOS/LVTTL outputs
- Two LVCMOS/LVTTL clock inputs for redundant clock applications
- CLK0 and CLK1 accepts the following input levels: LVCMOS/LVTTL
- Output frequency range: 8.33MHz to 125MHz
- VCO range: 200MHz to 500MHz
- External feedback for "zero delay" clock regeneration
- Cycle-to-cycle jitter:  $\pm 100\text{ps}$  (typical)
- Output skew: 350ps (maximum)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free RoHS-compliant package

## PIN ASSIGNMENT



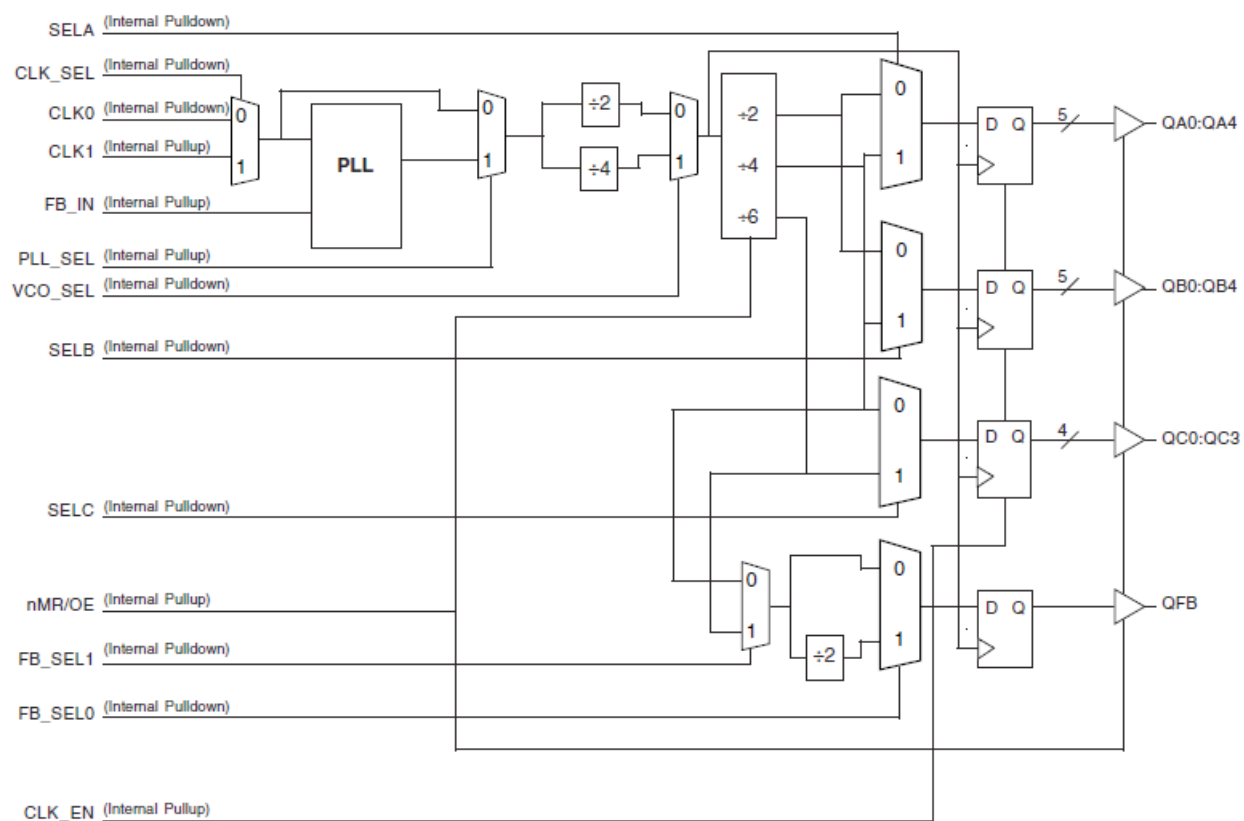
### 52-Lead LQFP

10mm x 10mm x 1.4mm package body

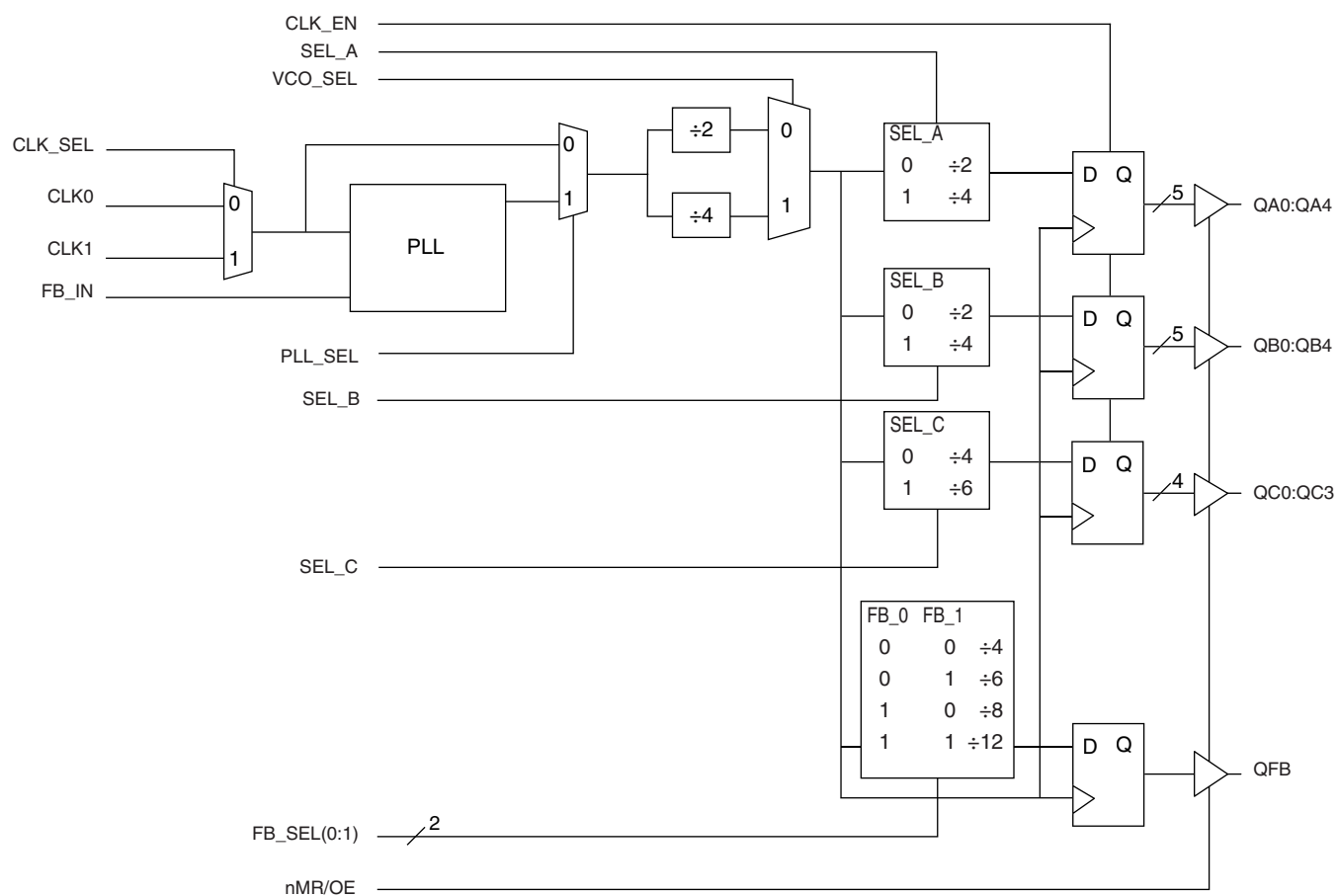
**Y package**

Top View

## BLOCK DIAGRAM



# SIMPLIFIED BLOCK DIAGRAM



**TABLE 1. PIN DESCRIPTIONS**

| Number                                      | Name                       | Type   |          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------------------------------------------|----------------------------|--------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 15, 19,<br>24, 30, 35, 39,<br>43, 47, 51 | GND                        | Power  |          | Power supply ground.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 2                                           | nMR/OE                     | Input  | Pullup   | Active HIGH outputs enabled (active). When LOW, outputs are disabled (High-impedance state) and reset of the device. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The 87974I requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CLKx) |
| 3                                           | CLK_EN                     | Input  | Pullup   | Synchronizing clock enable. When HIGH, clock outputs QAx:QCx are enabled. When LOW, clock outputs QAx:QCx are low. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                        |
| 4                                           | SEL_B                      | Input  | Pulldown | Selects divide value for Bank B output as described in Table 3D. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                          |
| 5                                           | SEL_C                      | Input  | Pulldown | Selects divide value for Bank C output as described in Table 3D. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                          |
| 6                                           | PLL_SEL                    | Input  | Pullup   | Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects the reference clock. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                              |
| 7                                           | SEL_A                      | Input  | Pulldown | Selects divide value for Bank A output as described in Table 3D. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                          |
| 8                                           | CLK_SEL                    | Input  | Pulldown | Clock select input. When HIGH, selects CLK1. When LOW, selects CLK0. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                      |
| 9                                           | CLK0                       | Input  | Pulldown | Reference clock input. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                                                                    |
| 10                                          | CLK1                       | Input  | Pullup   | Reference clock input. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                                                                    |
| 11, 27, 42                                  | nc                         | Unused |          | No connect.                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 12                                          | V <sub>DD</sub>            | Power  |          | Core supply pin.                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 13                                          | V <sub>DDA</sub>           | Power  |          | Analog supply pin.                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 14, 20                                      | FB_SEL0, FB_SEL1           | Input  | Pulldown | Selects divide value for Bank feedback output as described in Table 3E. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                   |
| 16, 18,<br>21, 23, 25                       | QA4, QA3,<br>QA2, QA1, QA0 | Output |          | Bank A clock outputs. 7Ω typical output impedance. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                                        |
| 17, 22, 26                                  | V <sub>DDOA</sub>          | Power  |          | Output supply pins for Bank A clock outputs.                                                                                                                                                                                                                                                                                                                                                                                                                |
| 28                                          | V <sub>DDOFB</sub>         | Power  |          | Output supply pin for QFB clock output.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 29                                          | QFB                        | Output |          | Clock output. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                                                                             |
| 31                                          | FB_IN                      | Input  | Pullup   | Feedback input to phase detector for generating clocks with “zero delay”. Connect to pin 29. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                              |
| 32, 34,<br>36, 38, 40                       | QB4, QB3,<br>QB2, QB1, QB0 | Output |          | Bank B clock outputs. 7Ω typical output impedance. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                                        |
| 33, 37, 41                                  | V <sub>DDOB</sub>          | Power  |          | Output supply pins for Bank B clock outputs.                                                                                                                                                                                                                                                                                                                                                                                                                |
| 44, 46,<br>48, 50                           | QC3, QC2, QC1,<br>QC0      | Output |          | Bank C clock outputs. 7Ω typical output impedance. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                                        |
| 45, 49                                      | V <sub>DDOC</sub>          | Power  |          | Output supply pins for Bank C clock outputs.                                                                                                                                                                                                                                                                                                                                                                                                                |
| 52                                          | VCO_SEL                    | Input  | Pulldown | Selects VCO ÷ 4 when HIGH. Selects VCO ÷ 2 when LOW. LVCMOS / LVTTTL interface levels.                                                                                                                                                                                                                                                                                                                                                                      |

NOTE: and refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

| Symbol         | Parameter                                          | Test Conditions                      | Minimum | Typical | Maximum | Units      |
|----------------|----------------------------------------------------|--------------------------------------|---------|---------|---------|------------|
| $C_{IN}$       | Input Capacitance                                  |                                      |         | 4       |         | pF         |
| $R_{PULLUP}$   | Input Pullup Resistor                              |                                      |         | 51      |         | K $\Omega$ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor                            |                                      |         | 51      |         | K $\Omega$ |
| $C_{PD}$       | Power Dissipation Capacitance (per output); Note 1 | $V_{DD}, V_{DDA}, V_{DDOx} = 3.465V$ |         |         | 15      | pF         |
| $R_{OUT}$      | Output Impedance                                   |                                      | 5       | 7       | 12      | $\Omega$   |

NOTE 1:  $V_{DDOx}$  denotes  $V_{DDOx}, V_{DDOB}, V_{DDOC}, V_{DDOFB}$ .

**TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE**

| Inputs |        | Outputs |         |         |        |
|--------|--------|---------|---------|---------|--------|
| nMR/OE | CLK_EN | QA0:QA4 | QB0:QB4 | QC0:QC3 | QFB    |
| 0      | X      | HiZ     | HiZ     | HiZ     | HiZ    |
| 1      | 0      | LOW     | LOW     | LOW     | Enable |
| 1      | 1      | Enable  | Enable  | Enable  | Enable |

**TABLE 3B. OPERATING MODE FUNCTION TABLE**

| Inputs  | Operating Mode |
|---------|----------------|
| PLL_SEL |                |
| 0       | Bypass         |
| 1       | PLL            |

**TABLE 3C. PLL INPUT FUNCTION TABLE**

| Inputs  |           |
|---------|-----------|
| CLK_SEL | PLL Input |
| 0       | CLK0      |
| 1       | CLK1      |

**TABLE 3D. SELECT PIN FUNCTION TABLE**

| SEL_A | QA <sub>x</sub> | SEL_B | QB <sub>x</sub> | SEL_C | QC <sub>x</sub> |
|-------|-----------------|-------|-----------------|-------|-----------------|
| 0     | ÷ 2             | 0     | ÷ 2             | 0     | ÷ 4             |
| 1     | ÷ 4             | 1     | ÷ 4             | 1     | ÷ 6             |

**TABLE 3E. FB SELECT FUNCTION TABLE**

| Inputs  |         | Outputs |
|---------|---------|---------|
| FB_SEL1 | FB_SEL0 | QFB     |
| 0       | 0       | ÷ 4     |
| 1       | 0       | ÷ 6     |
| 0       | 1       | ÷ 8     |
| 1       | 1       | ÷ 12    |

**TABLE 3F. VCO SELECT FUNCTION TABLE**

| Inputs  |       |
|---------|-------|
| VCO_SEL | fVCO  |
| 0       | VCO/2 |
| 1       | VCO/4 |

**ABSOLUTE MAXIMUM RATINGS**

|                                          |                           |
|------------------------------------------|---------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                      |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $V_O$                           | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm)         |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C            |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol     | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$   | Core Supply Voltage           |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDA}$  | Analog Supply Voltage         |                 | 2.935   | 3.3     | 3.465   | V     |
| $V_{DDOx}$ | Output Supply Voltage; NOTE 1 |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$   | Power Supply Current          |                 |         |         | 121     | mA    |
| $I_{DDA}$  | Analog Supply Current         |                 |         |         | 15      | mA    |
| $I_{DDOx}$ | Output Supply Current; NOTE 2 |                 |         |         | 24      | mA    |

NOTE 1:  $V_{DDOx}$  denotes  $V_{DDOA}$ ,  $V_{DDOB}$ ,  $V_{DDOC}$ ,  $V_{DDOFB}$

NOTE 2:  $I_{DDOx}$  denotes  $I_{DDOA}$ ,  $I_{DDOB}$ ,  $I_{DDOC}$ ,  $I_{DDOFB}$

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

| Symbol   | Parameter                   | Test Conditions                                                                 | Minimum                        | Typical | Maximum  | Units         |
|----------|-----------------------------|---------------------------------------------------------------------------------|--------------------------------|---------|----------|---------------|
| $V_{IH}$ | Input High Voltage          | SEL_A:SEL_C, nMR/OE, VCO_SEL, PLL_SEL, CLK_SEL, CLK_EN, FB_SEL0, FB_SEL1, FB_IN | 2                              |         | $V_{DD}$ | V             |
|          |                             | CLK0, CLK1                                                                      | 2                              |         | $V_{DD}$ | V             |
| $V_{IL}$ | Input Low Voltage           | SEL_A:SEL_C, nMR/OE, VCO_SEL, PLL_SEL, CLK_SEL, CLK_EN, FB_SEL0, FB_SEL1, FB_IN |                                |         | 0.8      | V             |
|          |                             | CLK0, CLK1                                                                      |                                |         | 0.8      | V             |
| $I_{IH}$ | Input High Current          | FB_SEL0, FB_SEL1, SEL_A:SEL_C, CLK0, VCO_SEL, CLK_SEL                           | $V_{DD} = V_{IN} = 3.465V$     |         | 100      | $\mu\text{A}$ |
|          |                             | CLK1, FB_IN, nMR/OE, PLL_SEL, CLK_EN                                            | $V_{DD} = V_{IN} = 3.465V$     |         | 5        | $\mu\text{A}$ |
| $I_{IL}$ | Input Low Current           | FB_SEL0, FB_SEL1, SEL_A:SEL_C, CLK0, VCO_SEL, CLK_SEL                           | $V_{IN} = 0V, V_{DD} = 3.465V$ | -5      |          | $\mu\text{A}$ |
|          |                             | CLK1, FB_IN, nMR/OE, PLL_SEL, CLK_EN                                            | $V_{IN} = 0V, V_{DD} = 3.465V$ | -100    |          | $\mu\text{A}$ |
| $V_{OH}$ | Output High Voltage; NOTE 1 |                                                                                 | 2.4                            |         |          | V             |
| $V_{OL}$ | Output Low Voltage; NOTE 1  |                                                                                 |                                |         | 0.5      | V             |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDOx}/2$ .

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$** 

| Symbol        | Parameter                                     | Test Conditions                        | Minimum              | Typical                | Maximum              | Units |
|---------------|-----------------------------------------------|----------------------------------------|----------------------|------------------------|----------------------|-------|
| $f_{MAX}$     | Output Frequency                              | $Qx_{\div 2}, VCO_{\div 2}$            |                      |                        | 125                  | MHz   |
|               |                                               | $Qx_{\div 4}, VCO_{\div 2}$            |                      |                        | 63                   | MHz   |
|               |                                               | $Qx_{\div 6}, VCO_{\div 2}$            |                      |                        | 42                   | MHz   |
| $f_{VCO}$     | PLL VCO Lock Range; NOTE 5                    |                                        | 200                  |                        | 500                  | MHz   |
| $t_{PD}$      | SYNC to Feedback Propagation Delay; NOTE 2, 5 | PLL_SEL = 3.3V, $f_{REF} = 50MHz$      | -250                 |                        | 100                  | ps    |
| $t_{sk(o)}$   | Output Skew; NOTE 4, 5                        | Measured on rising edge at $V_{DDO}/2$ |                      |                        | 350                  | ps    |
| $t_{jit(cc)}$ | Cycle-to-Cycle Jitter; NOTE 5, 6              |                                        |                      | $\pm 100$              |                      | ps    |
| $t_L$         | PLL Lock Time                                 |                                        |                      |                        | 10                   | mS    |
| $t_R / t_F$   | Output Rise/Fall Time                         | 0.8V to 2.0V                           | 0.15                 |                        | 1.5                  | ns    |
| $t_{PW}$      | Output Pulse Width                            |                                        | $t_{Period}/2 - 800$ | $t_{Period}/2 \pm 500$ | $t_{Period}/2 + 800$ | ps    |
| $t_{EN}$      | Output Enable Time                            |                                        | 2                    |                        | 10                   | ns    |
| $t_{DIS}$     | Output Disable Time                           |                                        | 2                    |                        | 10                   | ns    |

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}/2$  point of the input to the  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

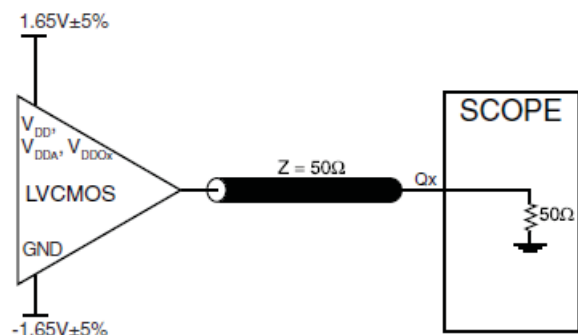
NOTE 3: Defined as skew within a bank with equal load conditions.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDOX}/2$ .

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Measured as peak-to-peak.

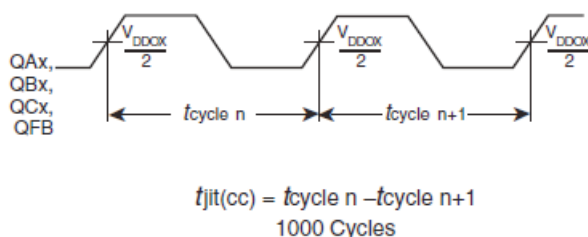
# PARAMETER MEASUREMENT INFORMATION



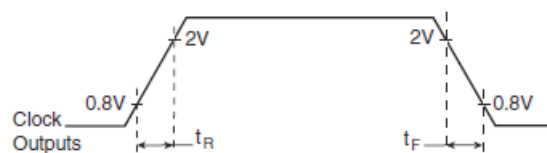
3.3V OUTPUT LOAD AC TEST CIRCUIT



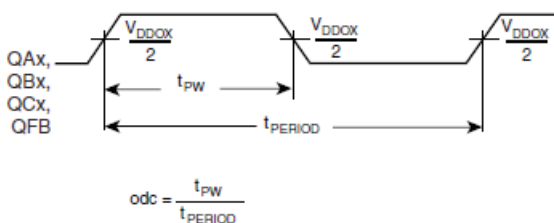
OUTPUT SKEW



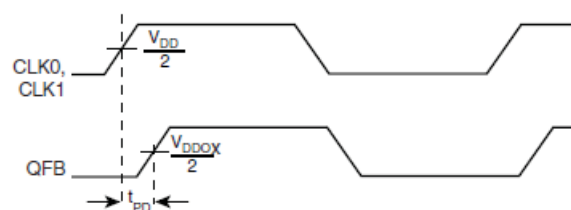
CYCLE-TO-CYCLE JITTER



OUTPUT RISE/FALL TIME



OUTPUT PULSE WIDTH/PULSE WIDTH PERIOD



SYNC TO FEEDBACK PROPAGATION DELAY



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 87974I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDOX}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{DDA}$  pin. The  $10\Omega$  resistor can also be replaced by a ferrite bead.

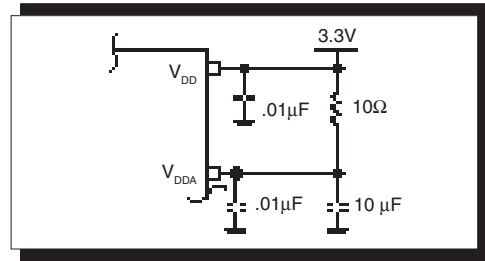


FIGURE 1. POWER SUPPLY FILTERING

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CLK INPUT:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a  $1k\Omega$  resistor can be tied from the CLK input to ground.

##### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1k\Omega$  resistor can be used.

#### OUTPUTS:

##### LVC MOS OUTPUT:

All unused LVC MOS output can be left floating. We recommend that there is no trace attached.



The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

### POWER AND GROUNDING

Place the decoupling capacitors as close as possible to the power pins. If space allows, placement of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin caused by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R7, C11, and C16 should be placed as close to the  $V_{DDA}$  pin as possible.

### CLOCK TRACES AND TERMINATION

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the

trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The series termination resistors should be located as close to the driver pins as possible.

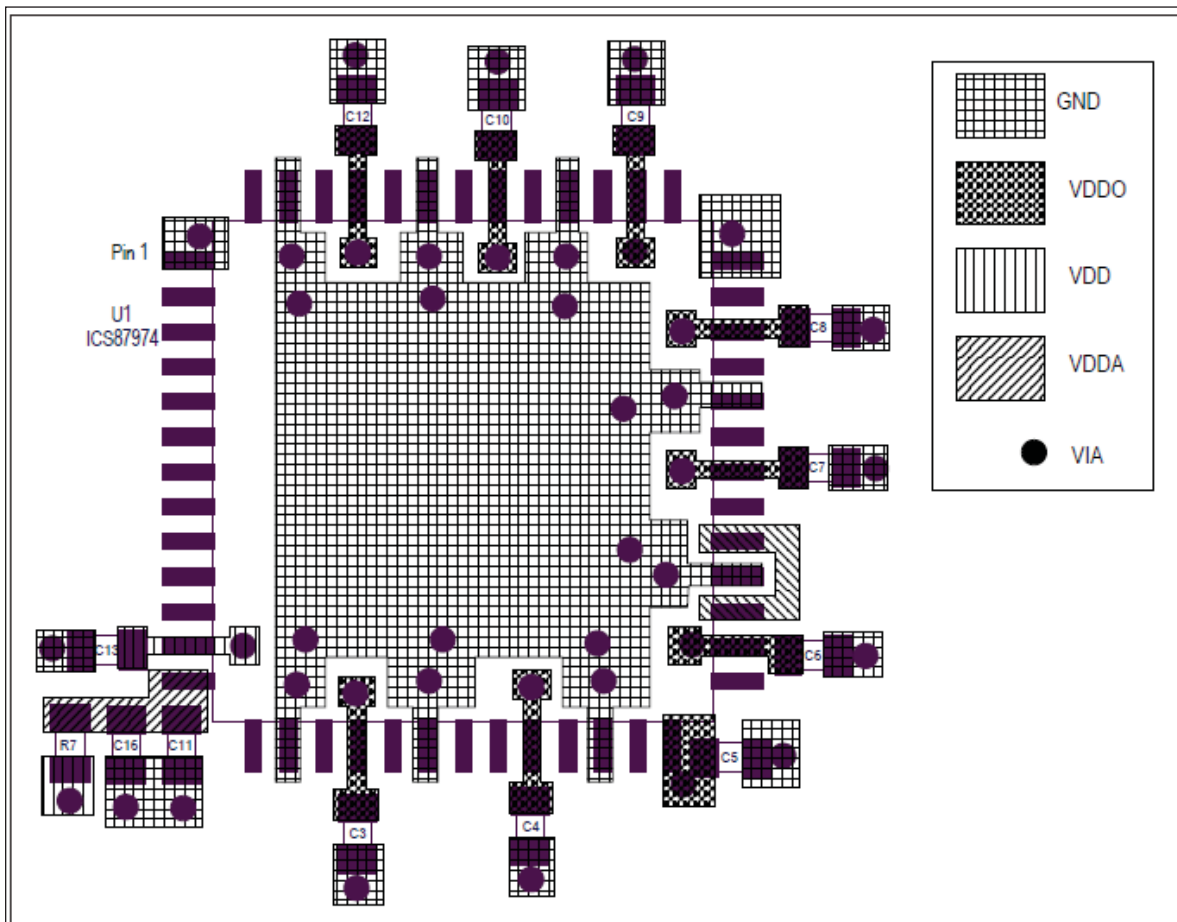


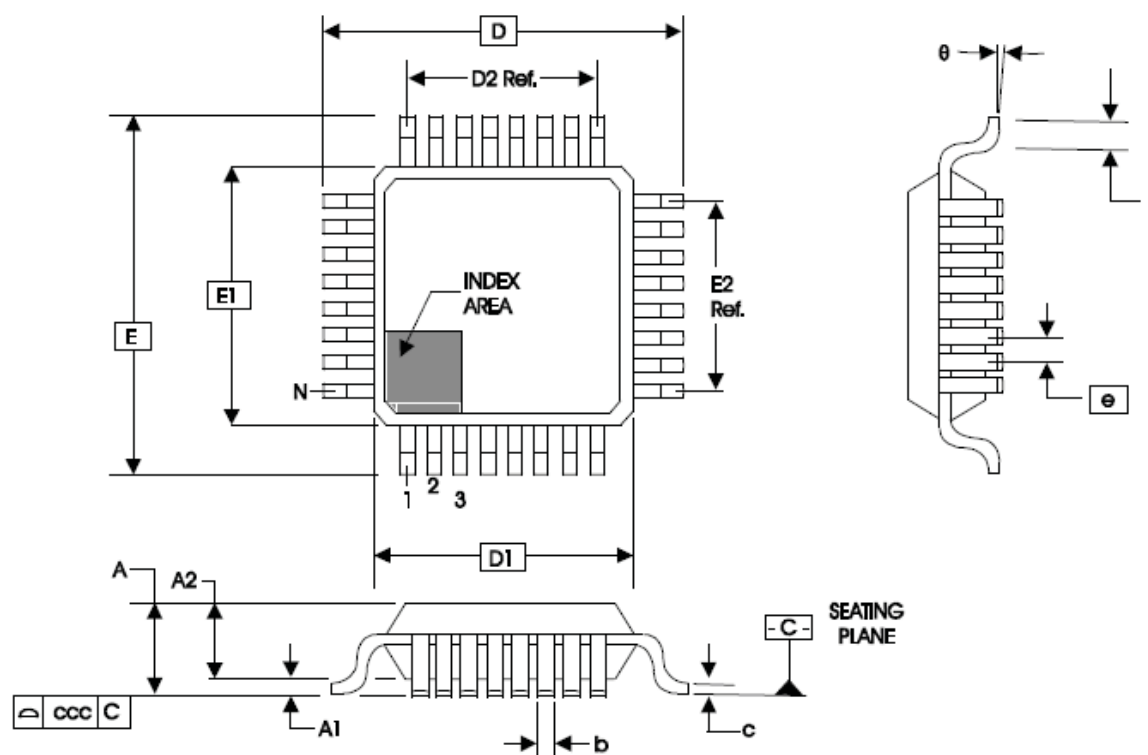
FIGURE 2B. PCB BOARD LAYOUT FOR 87974I

RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 52 LEAD LQFP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute)                                                                  |          |          |          |
|---------------------------------------------------------------------------------------------------------------------|----------|----------|----------|
|                                                                                                                     | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards                                                                        | 58.0°C/W | 47.1°C/W | 42.0°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards                                                                         | 42.3°C/W | 36.4°C/W | 34.0°C/W |
| <b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs. |          |          |          |

**TRANSISTOR COUNT**  
The transistor count for 87974I is: 4225

**PACKAGE OUTLINE - Y SUFFIX FOR 52 LEAD LQFP**

**TABLE 7. PACKAGE DIMENSIONS**

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |             |         |         |
|--------------------------------------------------|-------------|---------|---------|
| SYMBOL                                           | BCC         |         |         |
|                                                  | MINIMUM     | NOMINAL | MAXIMUM |
| N                                                | 52          |         |         |
| A                                                | --          | --      | 1.60    |
| A1                                               | 0.05        | --      | 0.15    |
| A2                                               | 1.35        | 1.40    | 1.45    |
| b                                                | 0.22        | 0.32    | 0.38    |
| c                                                | 0.09        | --      | 0.20    |
| D                                                | 12.00 BASIC |         |         |
| D1                                               | 10.00 BASIC |         |         |
| E                                                | 12.00 BASIC |         |         |
| E1                                               | 10.00 BASIC |         |         |
| e                                                | 0.65 BASIC  |         |         |
| L                                                | 0.45        | --      | 0.75    |
| θ                                                | 0°          | --      | 7°      |
| ccc                                              | --          | --      | 0.08    |

Reference Document: JEDEC Publication 95, MS-026

**TABLE 8. ORDERING INFORMATION**

| Part/Order Number | Marking       | Package                  | Shipping Packaging | Temperature    |
|-------------------|---------------|--------------------------|--------------------|----------------|
| 87974CYILF        | ICS87974CYILF | 52 lead "Lead Free" LQFP | Tray               | -40°C to +85°C |
| 87974CYILFT       | ICS87974CYILF | 52 lead "Lead Free" LQFP | Tape and Reel      | -40°C to +85°C |

| REVISION HISTORY SHEET |           |         |                                                                                                                                                                                                                                                                    |          |
|------------------------|-----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|
| Rev                    | Table     | Page    | Description of Change                                                                                                                                                                                                                                              | Date     |
| A                      |           | 10 & 11 | Added Layout Guideline and PCB Board Layout.                                                                                                                                                                                                                       | 4/2/02   |
| A                      |           | 3       | Added simplified block diagram.                                                                                                                                                                                                                                    | 4/4/02   |
| A                      | T7        | 12      | Revised Package Outline drawing. Corrected Package Dimensions table to correspond with the Package Outline drawing.<br>Update format throughout datasheet.                                                                                                         | 11/15/02 |
| B                      | T1<br>T4A | 4       | Pin Description table - updated nMR/OE and $V_{DDOX}$ pin descriptions.                                                                                                                                                                                            | 3/20/03  |
|                        |           | 6       | 3V Power Supply table - changed $V_{DD}$ parameter to "Core..." from "Positive...".<br>Changed $I_{DD}$ max. limit from 105mA max. to 118mA max.,<br>and $I_{DDOX}$ from 20mA max. to 22mA max.                                                                    |          |
| B                      | T2<br>T3E | 5       | Pin Characteristics Table - changed $C_{IN}$ 8pF max. to 4pF typical.                                                                                                                                                                                              | 5/15/03  |
|                        |           | 5       | FB Select Function Table - switched FB_SELx headings,<br>FB_SEL1 heading is in column 1, FB_SEL0 heading is in column 2.                                                                                                                                           |          |
| B                      | T2        | 5       | Pin Characteristics Table - added $R_{OUT}$ , Output Impedance row.                                                                                                                                                                                                | 7/9/03   |
|                        |           | 12      | Revised Package Outline.                                                                                                                                                                                                                                           |          |
| C                      | T4A       | 6       | Change from die rev. A to B on part marking throughout data sheet.                                                                                                                                                                                                 | 7/23/03  |
|                        |           |         | Change max. temperature to 70°C down from 85°C throughout data sheet.<br>Power Supply DC Characteristics table - adjusted:<br>$V_{DDA}$ from 3.135V min. to 2.9375V min.,<br>$I_{DD}$ from 118mA max. to 125mA max., and<br>$I_{DDOX}$ from 22mA max. to 25mA max. |          |
| D                      | T4A       | 6       | Through out the data sheet the maximum temperature was changed from 70°C to 85°C.<br>Power Supply DC Characteristics Table - $I_{DD}$ changed from 125mA max. to 121mA max. and $I_{DDOX}$ changed from 25mA max. to 24mA max.                                     | 8/4/03   |
| D                      |           | 2 & 3   | Swaped labels for FB_SEL0 and FB_SEL1 in the Block Diagram and Simplified Block Diagram.                                                                                                                                                                           | 2/9/04   |
| D                      | T3E       | 5       | Corrected FB Select Function Table.                                                                                                                                                                                                                                | 6/9/04   |
| D                      | T8        | 13      | Ordering Information Table - added Lead-Free part number.                                                                                                                                                                                                          | 10/11/04 |
| D                      | T8        | 9       | Added <i>Recommendations for Unused Input and Output Pins</i> .                                                                                                                                                                                                    | 1/19/06  |
|                        |           | 14      | Ordering Information Table - part number and order number is now a revision C. Corrected lead-free part number and marking, and added lead-free note.                                                                                                              |          |
| E                      | T8        | 14      | Updated datasheet's header/footer with IDT from ICS.                                                                                                                                                                                                               | 7/26/10  |
|                        |           | 16      | Removed ICS prefix from Part/Order Number column.                                                                                                                                                                                                                  |          |
| E                      | T1        | 4       | Added Contact Page.                                                                                                                                                                                                                                                | 04/18/13 |
|                        |           |         | Updated description of nMR/OE pin                                                                                                                                                                                                                                  |          |
| E                      | T8        | 1<br>14 | Removed ICS from part numbers where needed.<br>Features section - removed reference to leaded packages.<br>Ordering Information - removed quantity from tape and reel. Deleted LF note below the table.<br>Updated header and footer.                              | 1/26/16  |





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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
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