General Description

The 874005-04 is a high performance Differential-to-LVDS Jitter Attenuator designed for use in PCI Express systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The 874005-04 has 2 PLL bandwidth modes: 300kHz and 2MHz. The 300kHz mode will provide maximum jitter attenuation, but higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 2MHz bandwidth provides the best tracking skew and will pass most spread profiles. The 874005-04 supports Serdes reference clock frequencies of 100MHz, 125MHz and 250MHz.

The 874005-04 uses IDT's 3rd Generation FemtoClock™ PLL technology to achive the lowest possible phase noise. The device is packaged in a 24 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

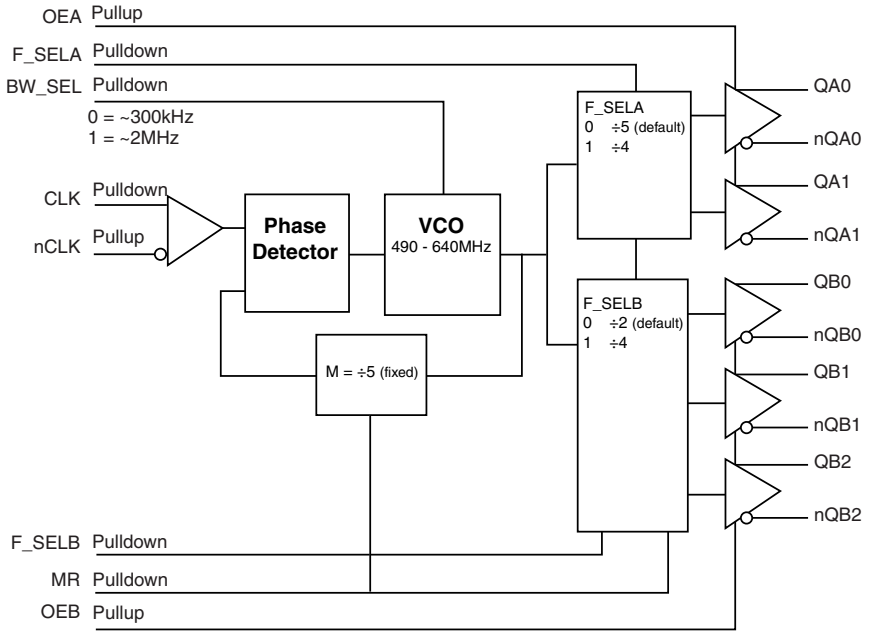
Features

- Five differential LVDS output pairs
- One differential clock input
- Supports 100MHz, 125MHz, and 250MHz Serdes reference clocks
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 320MHz
- Input frequency range: 98MHz - 128MHz
- PCI Express (2.5 Gb/S) and Gen 2 (5 Gb/s) jitter compliant
- RMS phase jitter @ 100MHz (1.875MHz – 20MHz): 0.88ps (typical)
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 35ps (maximum) QA = QB = ÷4
- 3.3V operating supply
- Two bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

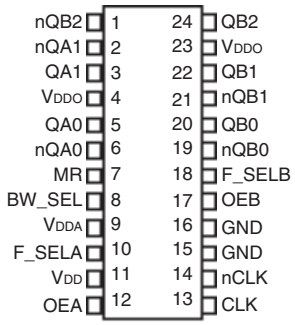
PLL Bandwidth

BW_SEL
0 = PLL Bandwidth: ~300kHz (default)
1 = PLL Bandwidth: ~2MHz

Block Diagram



Pin Assignment



874005-04
24-Lead TSSOP
4.40mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 24	nQB2, QB2	Output		Differential output pair. LVDS interface levels.
2, 3	nQA1, QA1	Output		Differential output pair. LVDS interface levels.
4, 23	V_{DDO}	Power		Output supply pins.
5, 6	QA0, nQA0	Output		Differential output pair. LVDS interface levels.
7	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx) to go low and the inverted outputs (nQx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
8	BW_SEL	Input	Pulldown	PLL bandwidth input. See Table 3B. LVCMOS/LVTTL interface levels.
9	V_{DDA}	Power		Analog supply pin.
10	F_SELA	Input	Pulldown	Frequency select pin for QAx/nQAx outputs. See Table 3C. LVCMOS/LVTTL interface levels.
11	V_{DD}	Power		Core supply pin.
12	OEA	Input	Pullup	Output enable pin for QA pins. When HIGH, the QAx/nQAx outputs are active. When LOW, the QAx/nQAx outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
13	CLK	Input	Pulldown	Non-inverting differential clock input.
14	nCLK	Input	Pullup	Inverting differential clock input.
15, 16	GND	Power		Power supply ground.
17	OEB	Input	Pullup	Output enable pin for QB pins. When HIGH, the QBx/nQBx outputs are active. When LOW, the QBx/nQBx outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
18	F_SELB	Input	Pulldown	Frequency select pin for QBx/nQBx outputs. See Table 3C. LVCMOS/LVTTL interface levels.
19, 20	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
21, 22	nQB1, QB1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Table 3A. Output Enable Function Table

Inputs	Outputs	
OEA/OEB	QAx/nQAx	QBx/nQBx
0	High Impedance	High Impedance
1	Enabled	Enabled

Table 3B. PLL Bandwidth Control, f_{REF} = 100MHz

Inputs	
BW_SEL	PLL Bandwidth
0	~300kHz (default)
1	~2MHz

Table 3C. Output Frequency for Input Frequency = 100MHz

Inputs		Outputs	
F_SELA	F_SELB	QAx/nQAx	QBx/nQBx
0 (default)	0 (default)	VCO/5, 100MHz	VCO/2, 250MHz
0	1	VCO/5, 100MHz	VCO/4, 125MHz
1	0	VCO/4, 125MHz	VCO/2, 250MHz
1	1	VCO/4, 125MHz	VCO/4, 125MHz

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	82.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.10	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				80	mA
I_{DDA}	Analog Supply Current				10	mA
I_{DDO}	Output Supply Current				75	mA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V			150	µA
		nCLK	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = V_{IN} = 3.465V	-5			µA
		nCLK	V_{DD} = V_{IN} = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVDS DC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V±5%, TA = 0°C TO 70°C

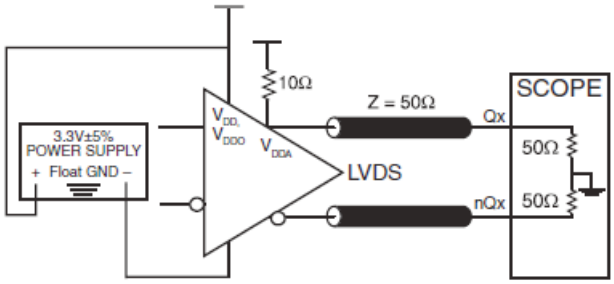
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 5. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V±5%, TA = 0°C TO 70°C

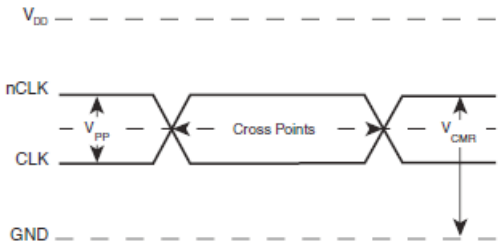
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			98		320	MHz
*t*jit(θ)	RMS Phase Jitter (Random); NOTE 1		100MHz, Integration Range: (1.875MHz – 20MHz)		0.88		ps
*t*jit(cc)	Cycle-to-Cycle Jitter, NOTE 2		QA, QB = ÷4			35	ps
			QA = ÷5			75	ps
*t*sk(o)	Output Skew; NOTE 3					90	ps
*t*sk(b)	Bank Skew: NOTE 4	QAx				15	ps
		QBx				68	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		500	ps
odc	Output Duty Cycle			48		52	%

NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and frequency, and with equal load conditions. Measured at the differential cross points.
NOTE 4: Defined as skew within a bank of outputs at the same supply voltage and frequency, and with equal load conditions.

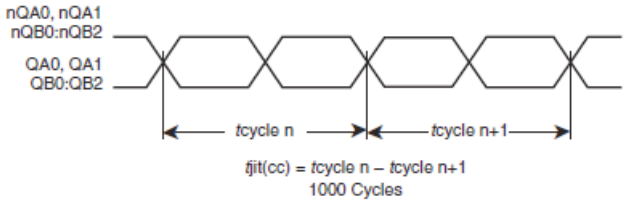
Parameter Measurement Information



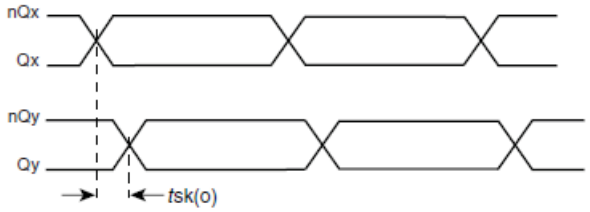
3.3V LVDS Output Load AC Test Circuit



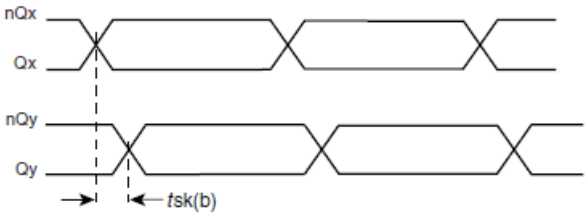
Differential Input Level



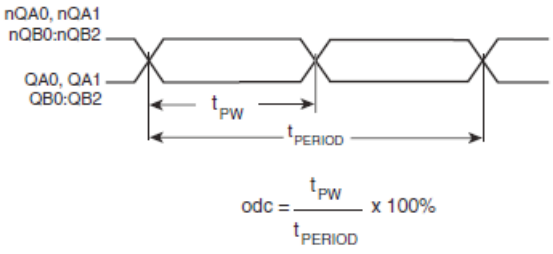
Cycle-to-Cycle Jitter



Output Skew

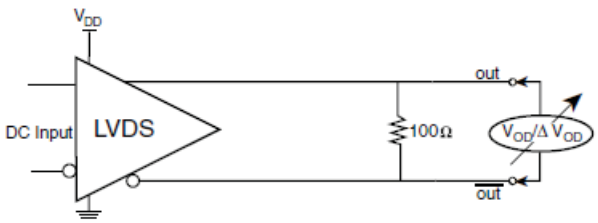


Bank Skew

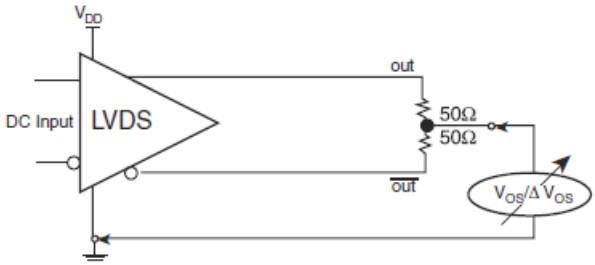


Output Duty Cycle/Pulse Width/Period

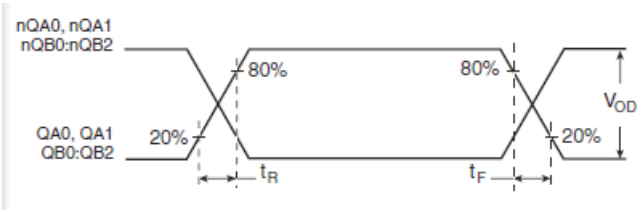
PARAMETER MEASUREMENT INFORMATION, CONTINUED



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP



OUTPUT RISE/FALL TIME

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 874005-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

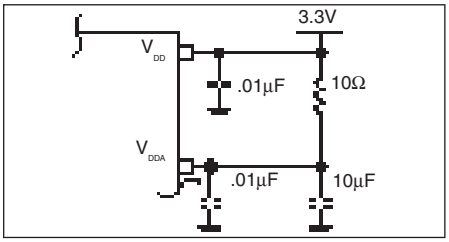


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

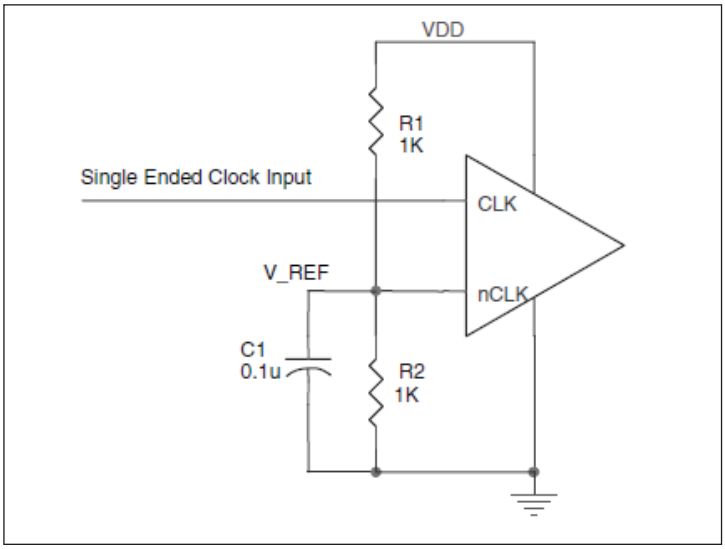


Figure 2. Single Ended Signal Driving Differential Input

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and LVHSTL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

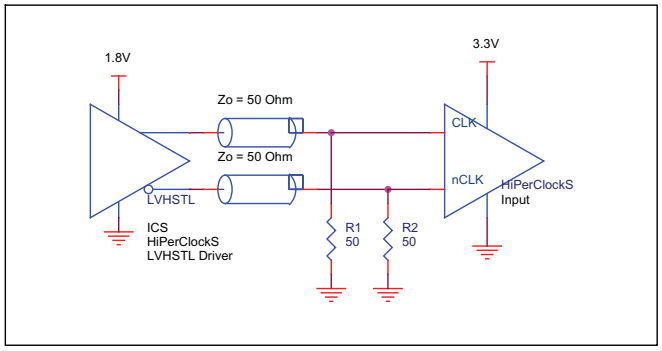


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

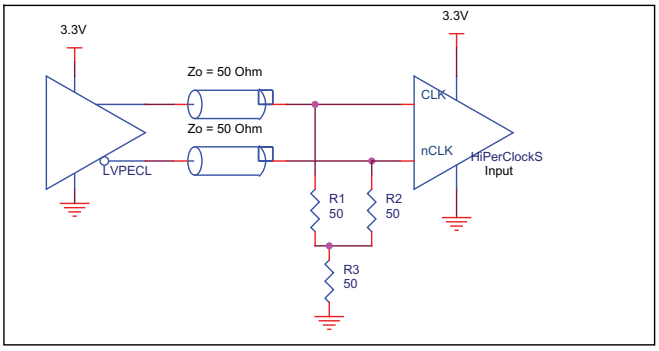


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

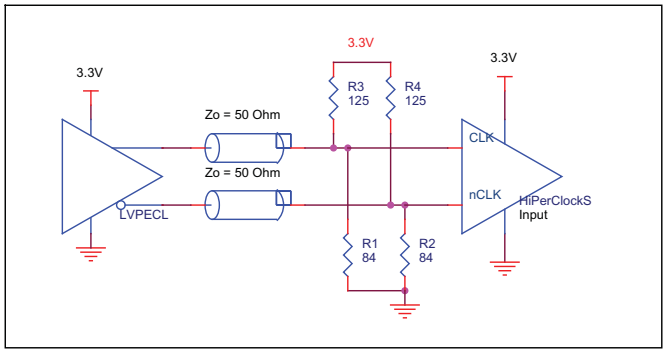


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

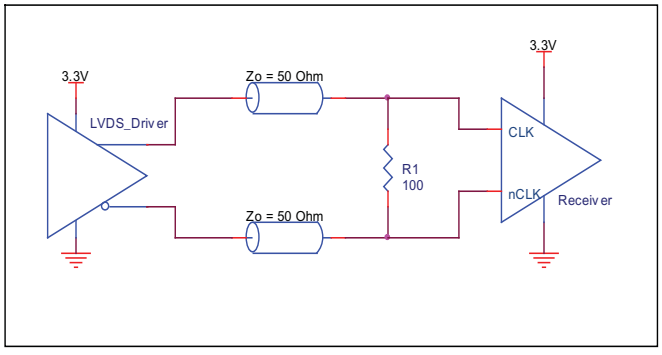


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

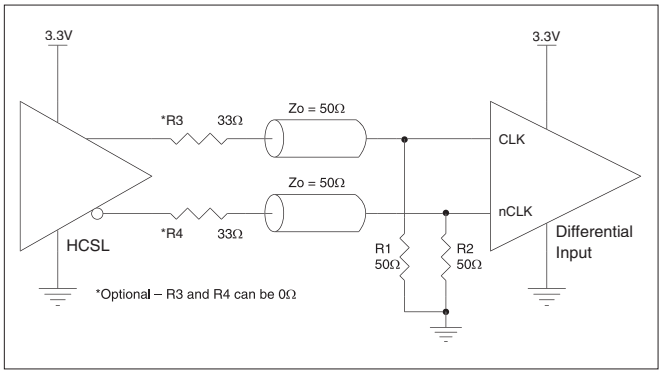


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

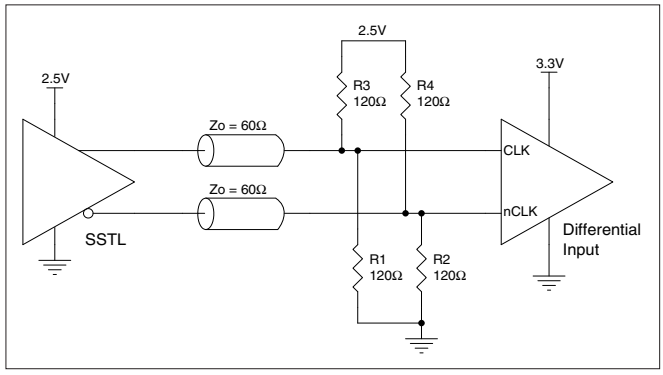


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS output buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

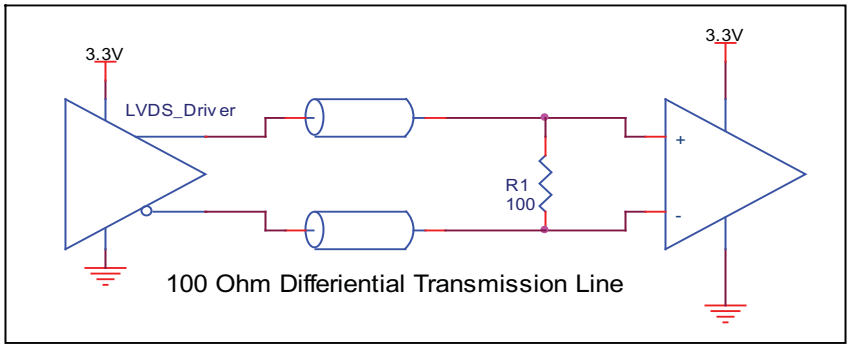


Figure 4. Typical LVDS Driver Termination

Schematic Example

Figure 5 shows an example of 874005-04 application schematic. In this example, the device is operated at V_{DD}= 3.3V. The decoupling capacitor should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver.

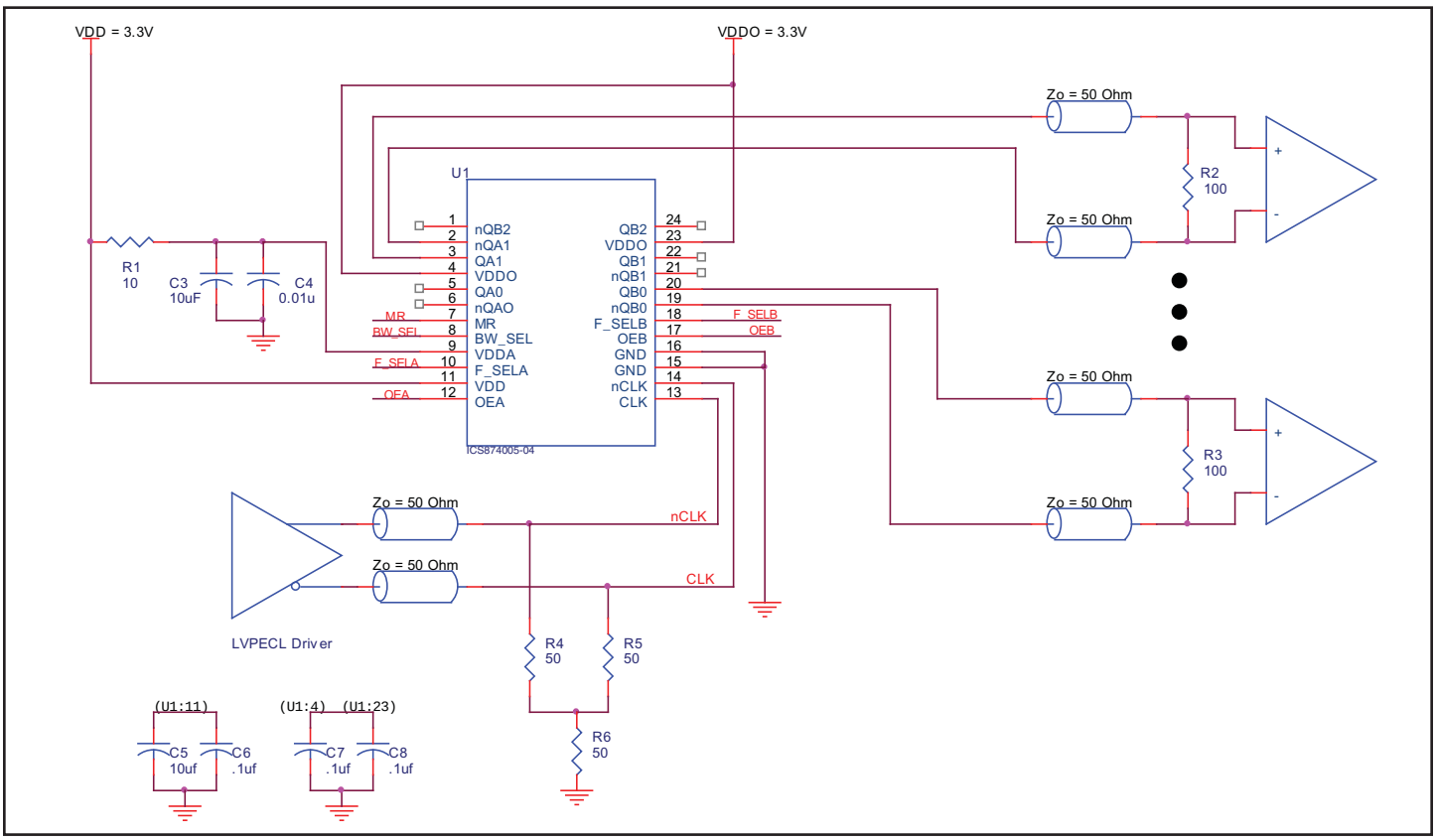


Figure 5. 874005-04 Schematic Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 874005-04.
Equations and example calculations are also provided.

1. Power Dissipation (typical).

The total power dissipation for the 874005-04 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V * (80mA + 10mA) = **311.85mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX} * I_{DDO_MAX} = 3.465V * 75mA = **259.875mW**

Total Power$_{_MAX}$ = 311.85mW + 259.875mW = **571.725mW**

2. Junction Temperature (typical).

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 82.3°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.572W * 82.3°C/W = 117.1°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board.

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24-LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 24 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78.0°C/W	75.9°C/W

Transistor Count

The transistor count for 874005-04 is: 1428

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

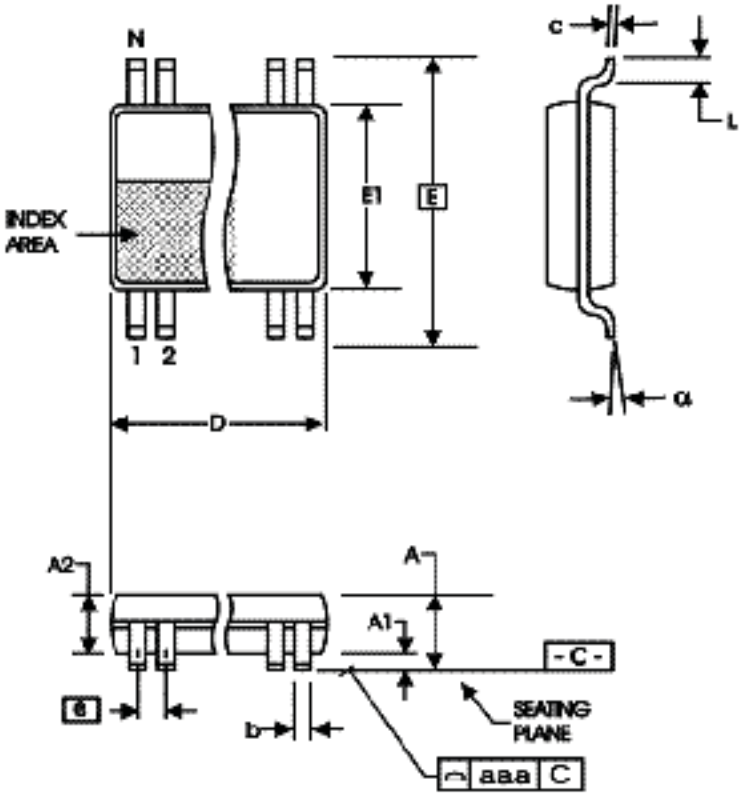


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
874005AG-04LF	ICS874005A04L	24 Lead “Lead-Free” TSSOP	tube	0°C to 70°C
874005AG-04LFT	ICS874005A04L	24 Lead “Lead-Free” TSSOP	tape & reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
			Removed ICS from part numbers where needed.	
		1	General Description - Deleted ICS chip.	
	T9	12	Ordering Information - removed quantity from tape and reel. Deleted LF note below table.	1/26/16
			Updated header and footer.	

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