

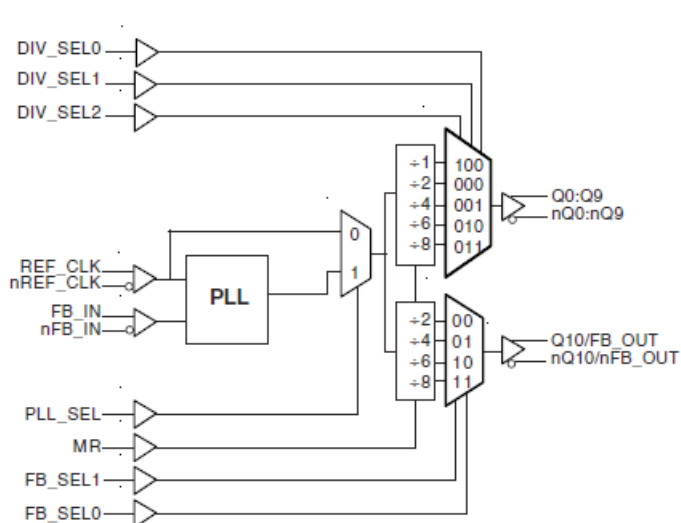
GENERAL DESCRIPTION

The 8731-01 is a low voltage, low skew, 1-to-11 Differential-to-3.3V LVPECL Clock Multiplier/Zero Delay Buffer. With output frequencies up to 700MHz the 8731-01 is targeted at high performance clock applications. Along with a fully integrated PLL the 8731-01 contains frequency configurable, differential outputs and external feedback inputs for multiplying clock frequencies and regenerating clocks with “zero delay”. Frequency multiplication is achieved by utilizing the separate feedback and clock output dividers. The value of the multiplier is determined by the ratio of the feedback divider, M, to the output divider, N. For multiplier values greater than 1, M must be greater than N. For multiplier values less than 1, M must be less than N. The zero delay mode is achieved with M and N at equal values. The divide values of the clock and feedback outputs are controlled by the DIV_SEL0:2 and FB_SEL0:1 inputs, respectively. The 8731-01 accepts any differential signal and translates it to differential 3.3V LVPECL output levels.

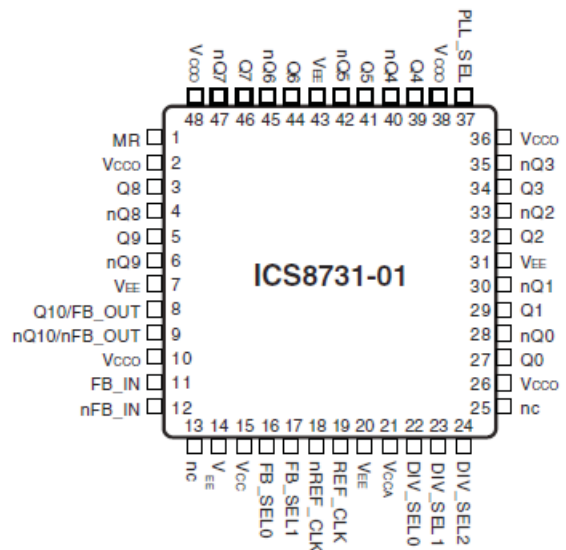
FEATURES

- Eleven differential 3.3V LVPECL outputs
- Differential reference clock input pair
- REF_CLK, nREF_CLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Maximum reference clock input frequency: 200MHz
- VCO range: 250MHz - 700MHz
- Accepts any single-ended input signal with a resistor bias on nCLK input
- External feedback for zero delay capability
- Output skew: 70ps (maximum)
- Cycle-to-cycle jitter: 65ps (maximum)
- Full 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free RoHS compliant package

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Lead LQFP

7mm x 7mm x 1.4mm package body

Y Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs, Qx, to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
2, 10, 26, 36, 38, 48	V _{CCO}	Power		Output supply pins.
3, 4, 5, 6	Q8, nQ8, Q9, nQ9	Output		Differential output pairs.
7, 14, 20, 31, 43	V _{EE}	Power		Negative supply pins.
8, 9	Q10/FB_OUT, nQ10/nFB_OUT	Output		Differential clock outputs.
11, 12	FB_IN, nFB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with “zero delay”.
15	V _{CC}	Power		Core supply pin.
16	FB_SEL0	Input	Pulldown	Determines output divider for Q10/FB outputs (see Table 3). LVCMOS / LVTTTL interface levels.
17	FB_SEL1	Input	Pulldown	Determines output divider for Q10/FB outputs (see Table 3). LVCMOS / LVTTTL interface levels.
18	nREF_CLK	Input	Pullup	Inverting differential clock input.
19	REF_CLK	Input	Pulldown	Non-inverting differential clock input.
21	V _{CCA}	Power		Analog supply pin.
22	DIV_SEL0,	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
23	DIV_SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
24	DIV_SEL2	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
13, 25	nc	Unused		No connect.
27, 28 29, 30	Q0, nQ0, Q1, nQ1	Output		Differential output pairs.
32, 33, 34, 35	Q2, nQ2, Q3, nQ3	Output		Differential output pairs.
37	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS / LVTTTL interface levels.
39, 40, 41, 42	Q4, nQ4, Q5, nQ5	Output		Differential output pairs.
44, 45, 46, 47	Q6, nQ6, Q7, nQ7	Output		Differential output pairs.

NOTE: and refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE FOR Q0:Q9 OUTPUTS

Inputs					Outputs
MR	PLL_SEL	DIV_SEL2	DIV_SEL1	DIV_SEL0	Q0:Q9, nQ0:nQ9
1	X	X	X	X	Low
0	1	1	0	0	fVCO/1
0	1	0	0	0	fVCO/2
0	1	0	0	1	fVCO/4
0	1	0	1	0	fVCO/6
0	1	0	1	1	fVCO/8
0	0	1	0	0	fREF_CLK/1
0	0	0	0	0	fREF_CLK/2
0	0	0	0	1	fREF_CLK/4
0	0	0	1	0	fREF_CLK/6
0	0	0	1	1	fREF_CLK/8

TABLE 3B. CONTROL INPUT FUNCTION TABLE FOR Q10/FB

Inputs				Outputs
MR	PLL_SEL	FB_SEL1	FB_SEL0	Q10/FB, nQ10/FB
1	X	X	X	Low
0	1	0	0	fVCO/2
0	1	0	1	fVCO/4
0	1	1	0	fVCO/6
0	1	1	1	fVCO/8
0	0	0	0	fREF_CLK/2
0	0	0	1	fREF_CLK/4
0	0	1	0	fREF_CLK/6
0	0	1	1	fREF_CLK/8

TABLE 3C. Qx OUTPUT FREQUENCY W/FB_IN = Q10/FB

Inputs						fVCO
FB_IN	FB_SEL1	FB_SEL0	Q10/FB Output Divider Mode	REF_CLK (MHz)		(NOTE 1)
				Minimum	Maximum	
Q10/FB	0	0	÷2	125	200 (NOTE 2)	fREF_CLK x 2
Q10/FB	0	1	÷4	62.5	175	fREF_CLK x 4
Q10/FB	1	0	÷6	41.67	116.67	fREF_CLK x 6
Q10/FB	1	1	÷8	31.25	87.5	fREF_CLK x 8

NOTE 1: VCO frequency range is 250MHz to 700MHz.

NOTE 2: The maximum input frequency that the phase defector can accept is 200MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to $V_{CC} + 0.5V$
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				195	mA
I_{CCA}	Analog Supply Current				15	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	PLL_SEL, DIV_SEL0, DIV_SEL1, DIV_SEL2, FB_SEL0, FB_SEL1, MR	2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	PLL_SEL, DIV_SEL0, DIV_SEL1, DIV_SEL2, FB_SEL0, FB_SEL1, MR	-0.3		0.8	V
I_{IH}	Input High Current	DIV_SEL0, DIV_SEL1, DIV_SEL2, MR, FB_SEL0, FB_SEL1	$V_{CC} = V_{IN} = 3.465V$		150	μA
		PLL_SEL	$V_{CC} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	DIV_SEL0, DIV_SEL1, DIV_SEL2, MR, FB_SEL0, FB_SEL1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5		μA
		PLL_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150		μA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	REF_CLK, FB_IN $V_{CC} = V_{IN} = 3.465V$			150	μA
		nREF_CLK, nFB_IN $V_{CC} = V_{IN} = 3.465V$			5	μA
I_{IL}	Input Low Current	REF_CLK, FB_IN $V_{CC} = 3.465V, V_{IN} = 0V$	-5			μA
		nREF_CLK, nFB_IN $V_{CC} = 3.465V, V_{IN} = 0V$	-150			μA
V_{PP}	Peak-to-Peak Input Voltage		0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for REF_CLK, nREF_CLK and FB_IN, nFB_IN is $V_{CC} + 0.3V$.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

TABLE 5. PLL INPUT REFERENCE CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Input Reference Frequency				200	MHz

TABLE 6. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V, $f \leq 450\text{MHz}$	4.0		5.5	ns
$t(\emptyset)$	Static Phase Offset; NOTE 2	PLL_SEL = 3.3V, DIV_SEL[2:0] = 000, FB_SEL[1:0] = 00	50		150	ps
tsk(o)	Output Skew; NOTE 3, 4				70	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 4				65	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle	$f \leq 300\text{MHz}$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.

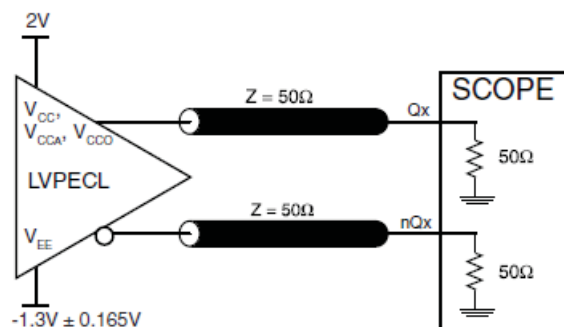
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

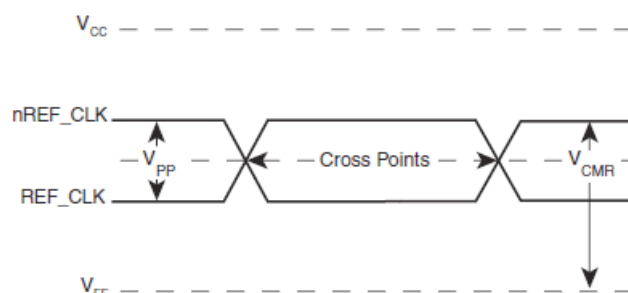
NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

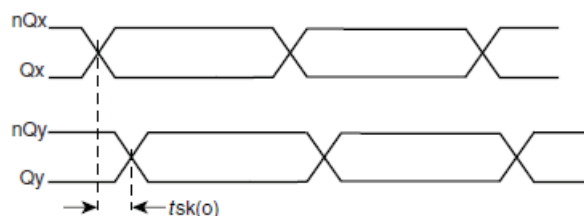
PARAMETER MEASUREMENT INFORMATION



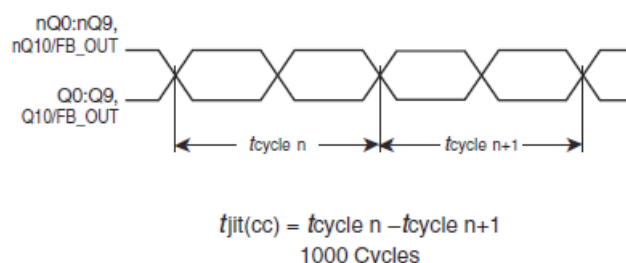
3.3V OUTPUT LOAD AC TEST CIRCUIT



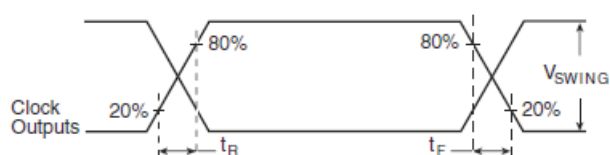
DIFFERENTIAL INPUT LEVEL



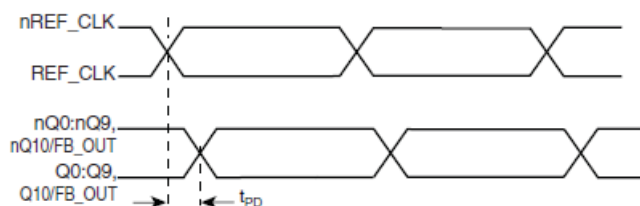
OUTPUT SKEW



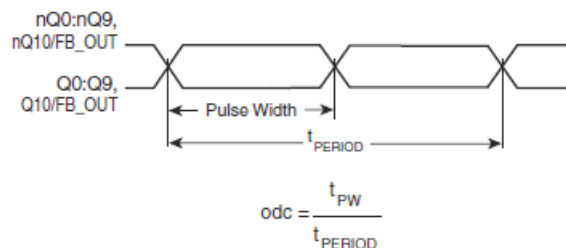
CYCLE-TO-CYCLE JITTER



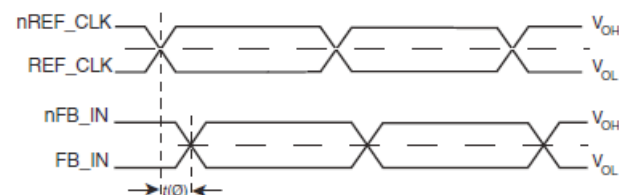
OUTPUT RISE/FALL TIME



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



STATIC PHASE OFFSET

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 8731-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} , and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu F$ and a $.01\mu F$ bypass capacitor should be connected to each V_{CCA} pin.

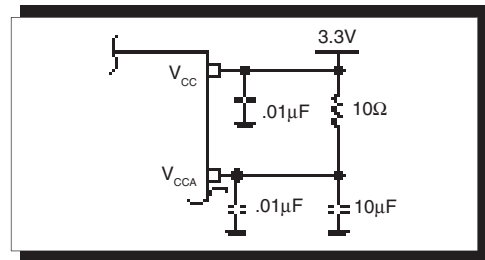


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors $R1$, $R2$ and $C1$. This bias circuit should be located as close as possible to the input pin. The ratio

of $R1$ and $R2$ might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only $2.5V$ and $V_{CC} = 3.3V$, V_{REF} should be $1.25V$ and $R2/R1 = 0.609$.

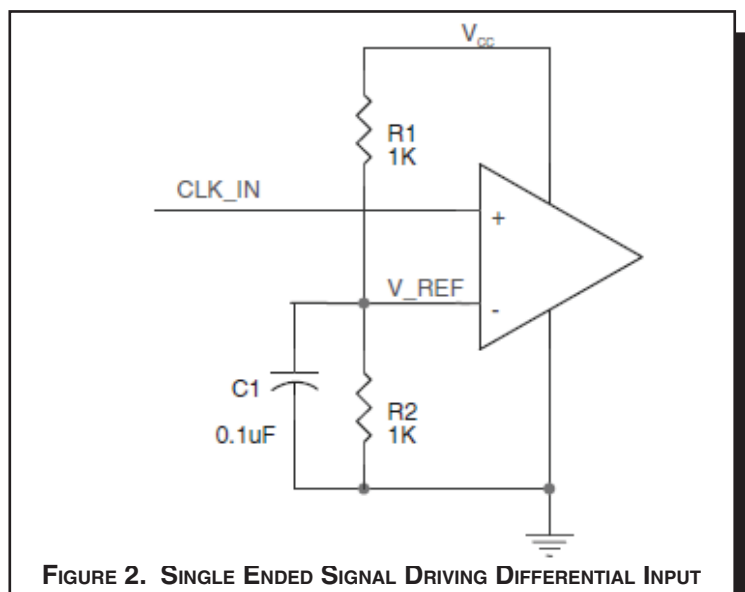


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The REF_CLK /nREF_CLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals.

Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the REF_CLK/nREF_CLK input driven by the most common driver types. The input interfaces suggested here are examples

only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

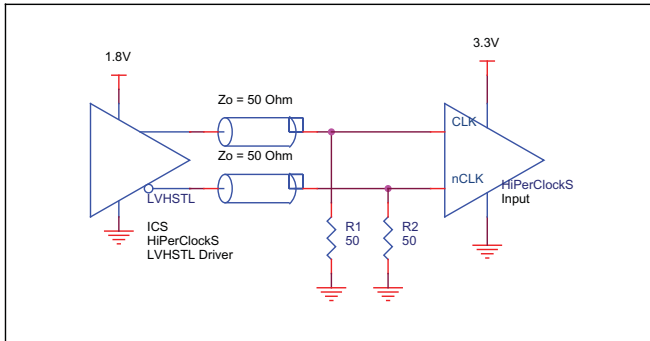


FIGURE 3A. REF_CLK/nREF_CLK INPUT DRIVEN BY LVHSTL DRIVER

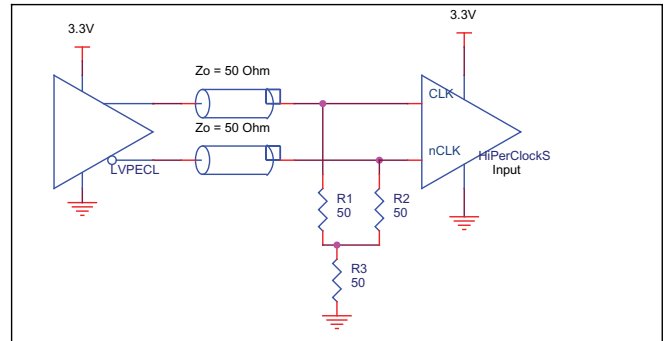


FIGURE 3B. REF_CLK/nREF_CLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

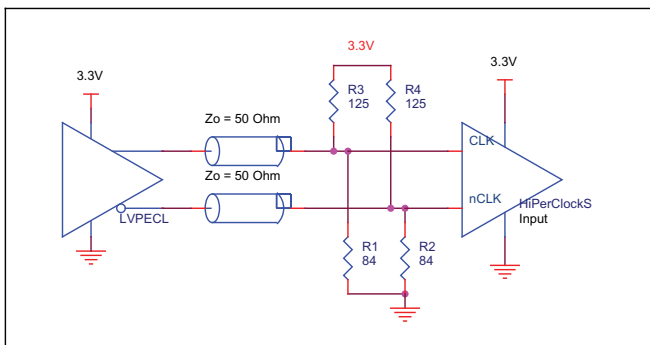


FIGURE 3C. REF_CLK/nREF_CLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

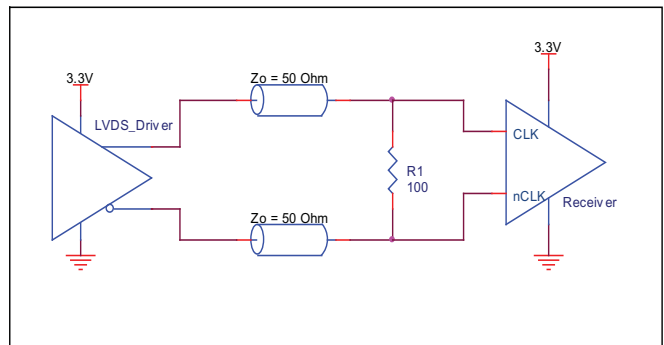


FIGURE 3D. REF_CLK/nREF_CLK INPUT DRIVEN BY 3.3V LVDS DRIVER

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

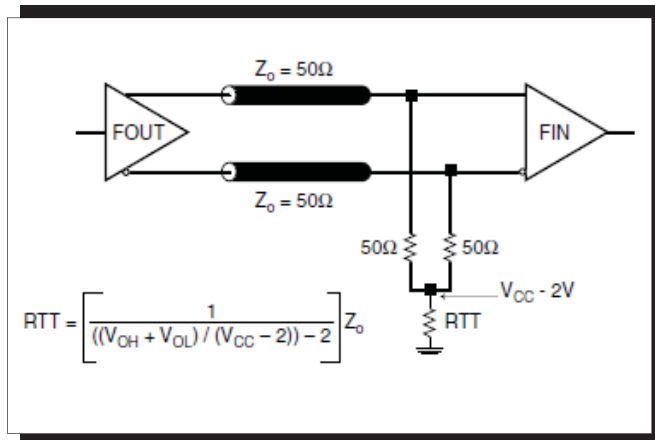


FIGURE 4A. LVPECL OUTPUT TERMINATION

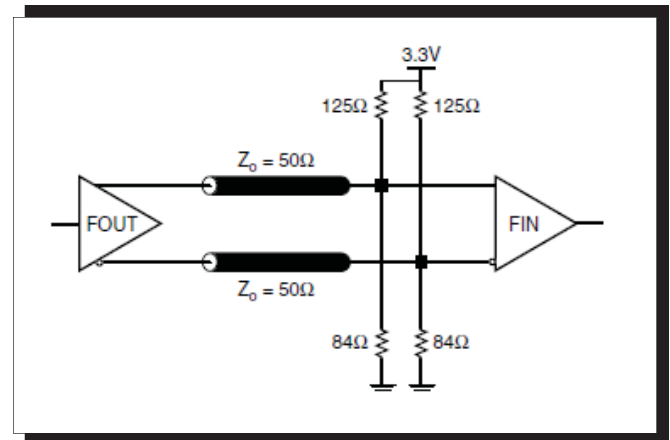


FIGURE 4B. LVPECL OUTPUT TERMINATION

SCHEMATIC EXAMPLE

Figure 5 shows an application schematic example of the 8731-01. This schematic provides examples of input and output handling. The input can accept various types of differential signal. This example shows the 8731-01 input driven by a 3.3V LVPECL driver. Additional examples for the input driven by other types of drivers are shown in the application section of

this data sheet. The 8731-01 outputs are LVPECL driver. In this example, we assume the traces are long transmission line and the receiver is high input impedance without built-in matched load. An example of 3.3V LVPECL termination is shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

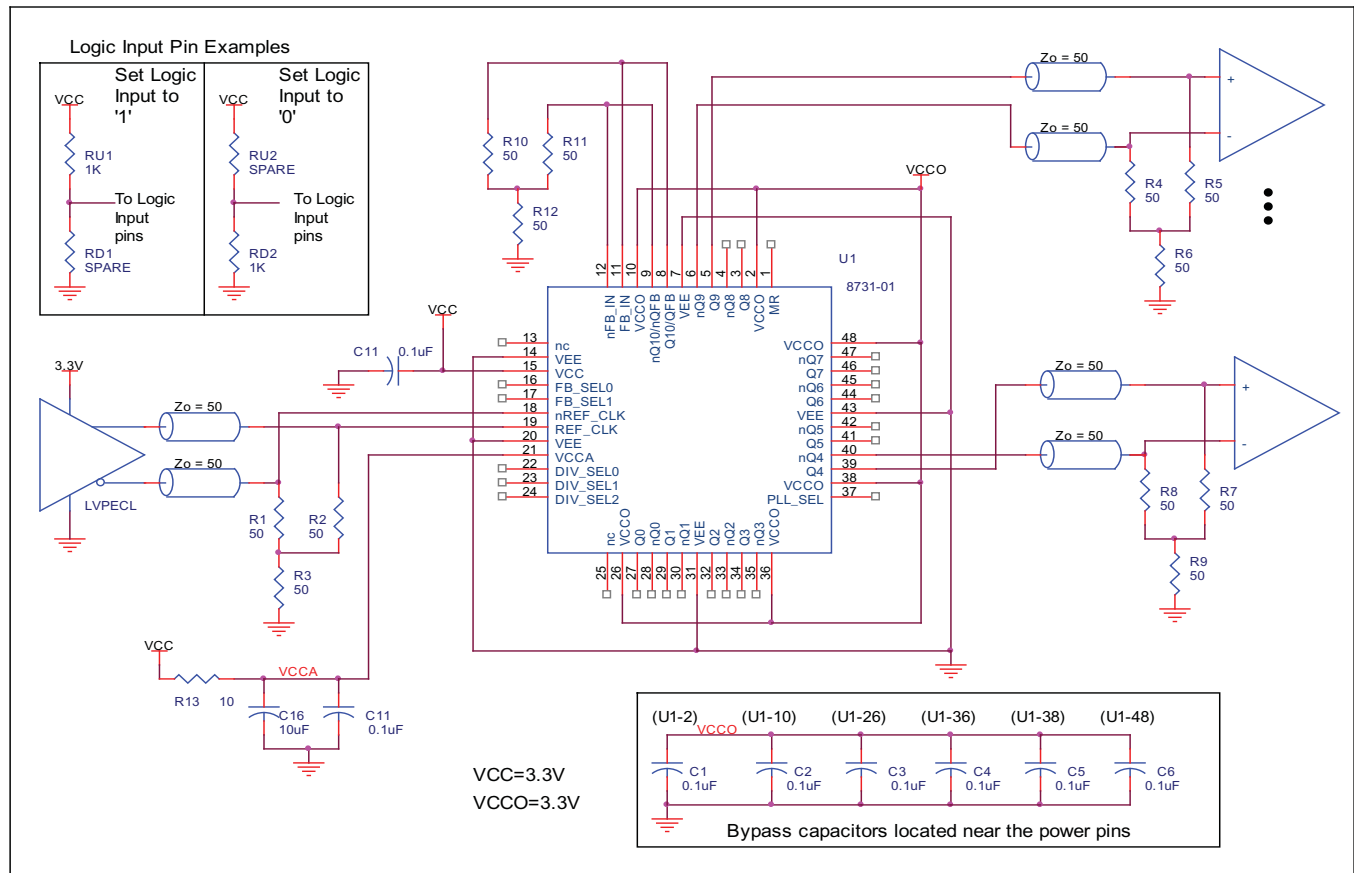


FIGURE 5. APPLICATION SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8731-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8731-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 195mA = 675.67mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $11 * 30mW = 330mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 675.67mW + 330mW = 1005.67mW$$

2. Junction Temperature.

Junction temperature, T_J , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for T_J is as follows: $T_J = \theta_{JA} * Pd_total + T_A$

T_J = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 42.1°C/W per Table 7 below.

Therefore, T_J for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 1.006W * 42.1^\circ C/W = 112.4^\circ C. \text{ This is below the limit of } 125^\circ C.$$

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

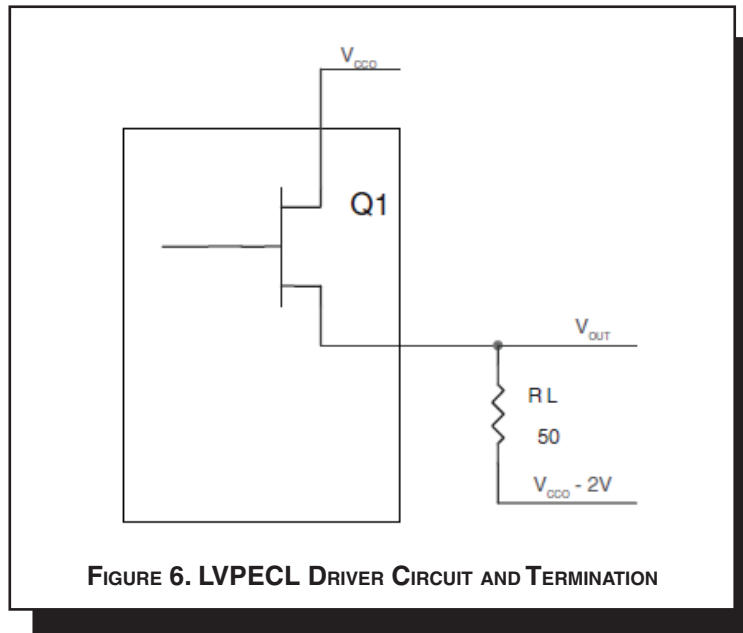
TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LQFP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$

$$(V_{CCO_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.
 Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC} - V_{OH_MAX}))/R_L] * (V_{CC} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC} - V_{OL_MAX}))/R_L] * (V_{CC} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = \mathbf{30mW}$$

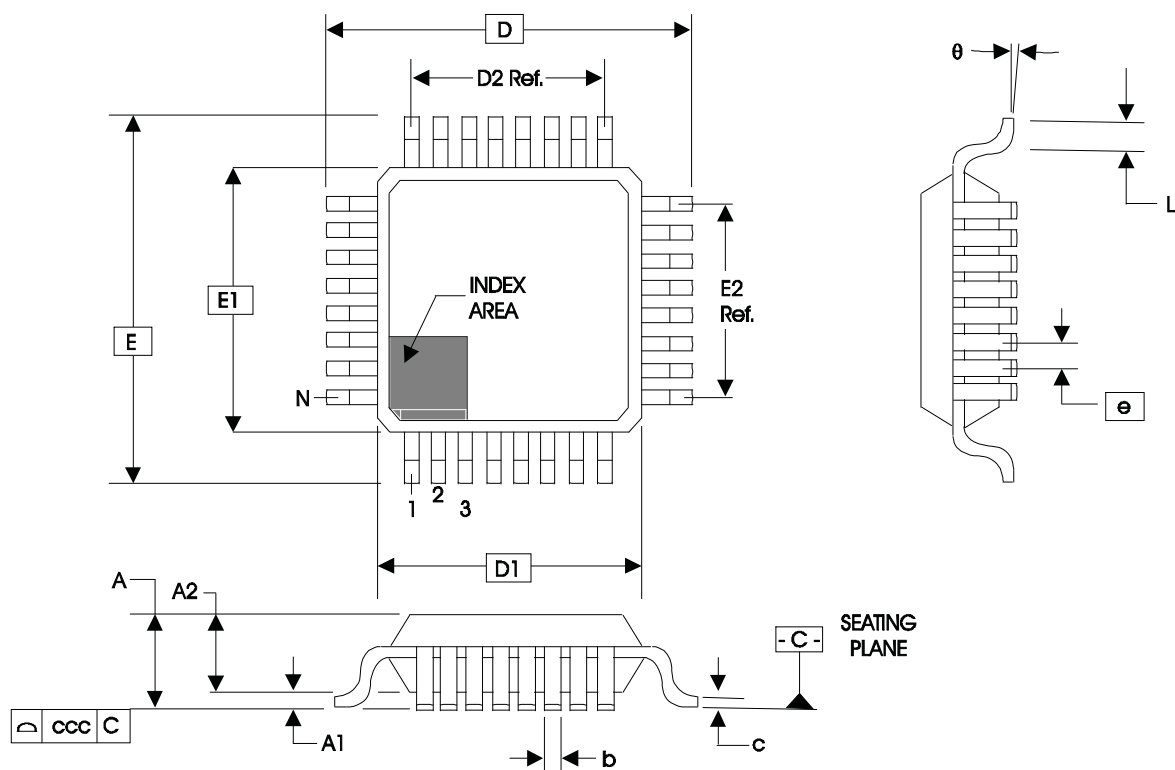
RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for 8731-01 is: 2883

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8731CY-01LF	ICS8731CY01L	48 Lead "Lead-Free" LQFP	tray	0°C to 70°C
8731CY-01LFT	ICS8731CY01L	48 Lead "Lead-Free" LQFP	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T10	1	Features Section - added Lead-Free bullet .	6/6/06
		15	Ordering Information Table - added Lead-Free part number, marking and note.	
B	T10	15	Updated datasheet's header/footer with IDT from ICS.	7/27/10
		17	Removed ICS prefix from Part/Order Number column. Added Contact Page.	
B	T10	15	Ordering Information - removed leaded devices. Updated data sheet format.	7/14/15

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.