

## General Description

The 870931I-01 is an LVC MOS clock generator that uses an internal phase lock loop (PLL) for frequency multiplication and to lock the low-skew outputs to the reference clock. The device offers six outputs. The PLL loop filter is completely internal and does not require external components. Several combinations of the PLL feedback and a divide-by-2 (controlled by `FREQ_SEL`) allow applications to optimize frequency generation over a wide range of input reference frequencies. The PLL can also be disabled by the `PLL_EN` control signal to allow for low frequency or DC testing. The 870931I-01 device is a member of the family of high performance clock solutions from IDT.

## Features

- Single-ended input reference clock
- Six single-ended clock outputs
- Internal PLL does not require external loop filter components
- 5V tolerant inputs
- Maximum output frequency: 80MHz, (Q0:Q4 outputs)
- Maximum output frequency: 40MHz, (Q/2 output)
- LVC MOS interface levels for all inputs and outputs
- PLL disable feature for low-frequency testing
- Output drive capability:  $\pm 24\text{mA}$
- Output skew: 300ps (maximum), Q0:Q4 and Q/2
- Full 3.3V supply voltage
- Available in lead-free packages
- $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  ambient operating temperature
- Fully pin and function compatible with the IDTQS5LV931 (including 50, 66 and 80MHz options)

## Pin Assignment

GND	1	20	Q4
OE/nRST	2	19	Q/2
FEEDBACK	3	18	GND
AVDD	4	17	Q3
VDD	5	16	VDD
AGND	6	15	Q2
SYNC	7	14	GND
FREQ_SEL	8	13	PLL_EN
GND	9	12	GND
Q0	10	11	Q1

**870931I-01**

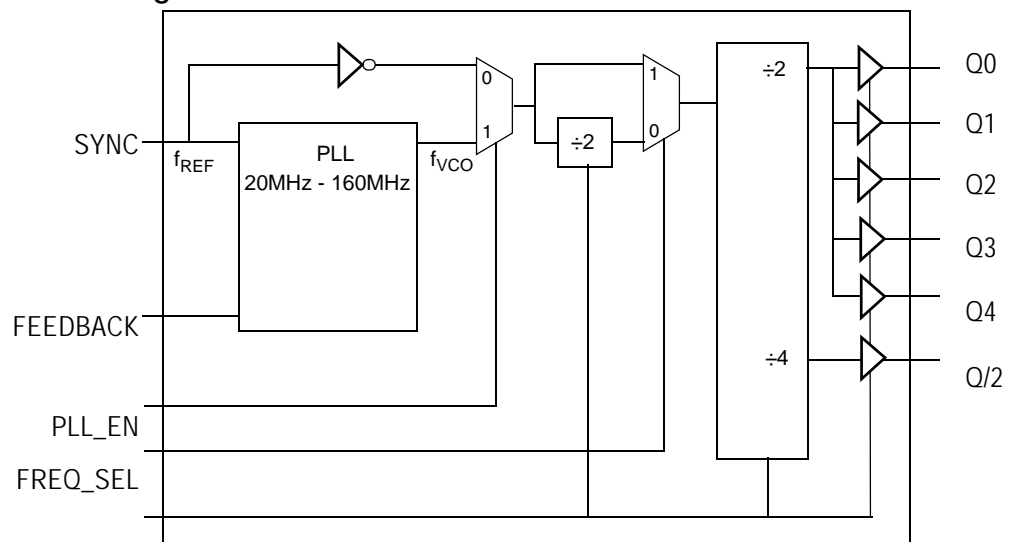
**20-Lead QSOP, 150Mil**

**3.9mm x 8.65mm x 1.5mm package body**

**R Package**

**Top View**

## Block Diagram



**Table 1. Pin Descriptions**

Number	Name	Type	Description
1, 9, 12, 14, 18	GND	Power	Power supply ground.
2	OE/nRST	Input	Output enable and asynchronous reset. Resets all outputs. Logic LOW, the outputs are in high-impedance state. Logic HIGH enables all outputs. LVCMOS/LVTTL interface levels.
3	FEEDBACK	Input	PLL feedback input which is connected to one of the clock outputs to close the PLL feedback loop. LVCMOS/LVTTL interface levels.
4	AV <sub>DD</sub>	Power	Positive power supply for the PLL.
5, 16	V <sub>DD</sub>	Power	Positive power supply pins.
6	AGND	Power	Power supply ground for the PLL.
7	SYNC	Input	Single-ended reference clock input. LVCMOS/LVTTL interface levels.
8	FREQ_SEL	Input	Frequency select. Logic LOW level inserts a divide-by-2 into the PLL output and feedback path. Logic HIGH inserts a divide-by-1 into the PLL output and feedback path. LVCMOS/LVTTL interface levels.
10, 11, 15, 17, 20	Q0, Q1, Q2, Q3, Q4	Output	Single-ended clock outputs. LVCMOS/LVTTL interface levels.
13	PLL_EN	Input	PLL enable. Enable and disables the PLL. Logic HIGH enables the PLL. Logic LOW disables the PLL and the input reference signal is routed to the output dividers (PLL bypass). LVCMOS/LVTTL interface levels.
19	Q/2	Output	Single-ended clock output. LVCMOS/LVTTL interface levels.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>DD</sub> = AV <sub>DD</sub> = 3.6V		330		pF
R <sub>OUT</sub>	Output Impedance			11		Ω

## Device Configuration

The 870931I-01 requires a connection to one of the clock outputs to the FEEDBACK input to close the PLL feedback path. The selection of the output (output divider) for PLL feedback will impact the device configuration and input to output frequency ratio and frequency ranges. See [Table 3D](#) for details.

## Function Tables

**Table 3A. OE/nRST Mode Configuration Table**

Input	Operation
OE/nRST	
0	Device is reset and the outputs Q0:Q4 and Q/2 are in high-impedance state. This control is asynchronous.
1	Outputs are enabled.

**Table 3B. FREQ\_SEL Mode Configuration Table**

Input	Operation
FREQ_SEL	
0	The VCO output is frequency-divided by 2. This setting allows for a lower input frequency range. See also table 3D for available frequency ranges.
1	The VCO output is frequency-divided by 1. This setting allows for a higher input frequency range. See also table 3D for available frequency ranges.

**Table 3C. PLL\_EN Mode Configuration Table**

Input	Operation
PLL_EN	
0	The PLL is bypassed. The input reference clock is routed to the output dividers for low-frequency board test purpose. The PLL-related AC specifications do not apply in PLL bypass mode.
1	The PLL is enabled and locks to the input reference signal.

**Table 3D. Frequency Configuration Table**

Outputs Used for PLL Feedback	FREQ_SEL	Input Frequency Range (MHz)	Output Frequency Range (MHz) and Output-to-Input Frequency Multiplication Factor	
		SYNC	Q[0:4]	Q/2
Q0, Q1, Q2, Q3 or Q4	0	5 - 40	5 - 40 (1x)	2.5 - 20 (0.5x)
	1	10 - 80	10 - 80 (1x)	5 - 40 (0.5x)
Q/2	0	2.5 - 20	5 - 40 (2x)	2.5 - 20 (1x)
	1	5 - 40	10 - 80 (2x)	5 - 40 (1x)

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	72.3°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = AV_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}, AV_{DD}$	Positive Supply Voltage		3.0	3.3	3.6	V
$I_{DDQ}$	Quiescent Power Supply Current	$V_{DD} = AV_{DD} = \text{Max.}$ , OE/nRST = 0, SYNC = 0, All Outputs Open			5	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = AV_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	SYNC, OE/nRST, FEEDBACK, PLL_EN, FREQ_SEL $V_{DD} = V_{IN} = 3.3V$			5	$\mu A$
$I_{IL}$	Input Low Current	SYNC, OE/nRST, FEEDBACK, PLL_EN, FREQ_SEL $V_{DD} = 3.3V$ , $V_{IN} = 0V$	-5			$\mu A$
$V_{OH}$	Output High Voltage:	Q0:Q4, Q/2 $I_{OH} = -24 \text{ mA}$	2.6			V
$V_{OL}$	Output Low Voltage	Q0:Q4, Q/2 $I_{OL} = 24 \text{ mA}$			0.5	V
$I_{OZ}$	Output Leakage Current	Q0:Q4, Q/2 OE/nRST = 0, $V_{OUT} = 0V$ or $V_{DD}$ , $V_{DD} = 3.6V$			$\pm 5$	$\mu A$

**Table 5. AC Electrical Characteristics,  $V_{DD} = AV_{DD} = 3.3V \pm 0.3V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$f_{REF}$	SYNC Input Reference Frequency		Feedback of Q0:Q4, FREQ_SEL = 0	5		40	MHz
			Feedback of Q0:Q4, FREQ_SEL = 1	10		80	MHz
			Feedback of Q/2, FREQ_SEL = 0	2.5		20	MHz
			Feedback of Q/2, FREQ_SEL = 1	5		40	MHz
$f_{OUT}$	Output Frequency		Q0-Q4			80	MHz
			Q/2			40	MHz
$idc$	Input Duty Cycle		SYNC	25		75	%
$t_R / t_F$	Input Rise/ Fall Time		SYNC			3	ns
$tsk(o)$	Output Skew; NOTE 1, 2, 3		Rising edges of Q0:Q4 and Q/2			300	ps
	Output Skew; NOTE 1, 2, 3		Falling edges of Q0:Q4			300	ps
$t_{PW}$	Output Pulse Width	Q0:Q4	80MHz	$t_{PERIOD}/2 - 0.5$		$t_{PERIOD}/2 + 0.5$	ns
		Q/2	40MHz	$t_{PERIOD}/2 - 0.4$		$t_{PERIOD}/2 + 0.4$	ns
$t_{jit(cc)}$	Cycle-to-Cycle Jitter		Feedback = Q			320	ps
			Feedback = Q/2			530	ps
$t(\phi)$	Static Phase Offset, (SYNC to FEEDBACK delay); NOTE 2, 4	Q0:Q4	80MHz	-500		500	ps
$t_{PZL}$	Output Enable Time; NOTE 5	OE/nRST	Low-to-High			14	ns
$t_{PHZ}, t_{PLZ}$	Output Disable Time; NOTE 5	OE/nRST	High-to-Low			14	ns
$t_R / t_F$	Output Rise/ Fall Time	Q0:Q4, Q/2	0.8V – 2.0V	0.2		2	ns
$t_{LOCK}$	PLL Lock Time					10	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DD}/2$ .

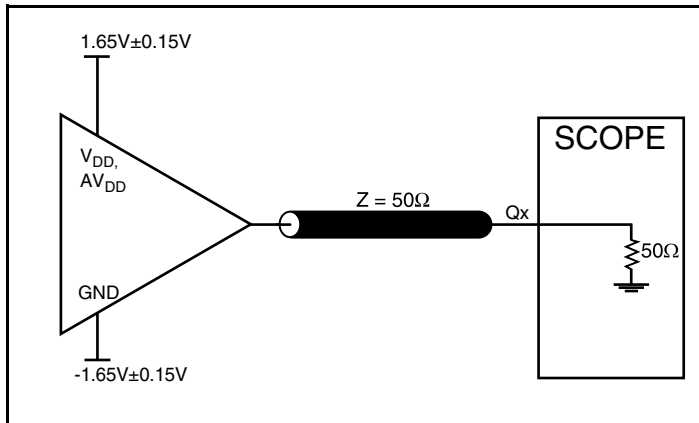
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Measured between coincident rising output edges of Q0:Q4 and Q/2.

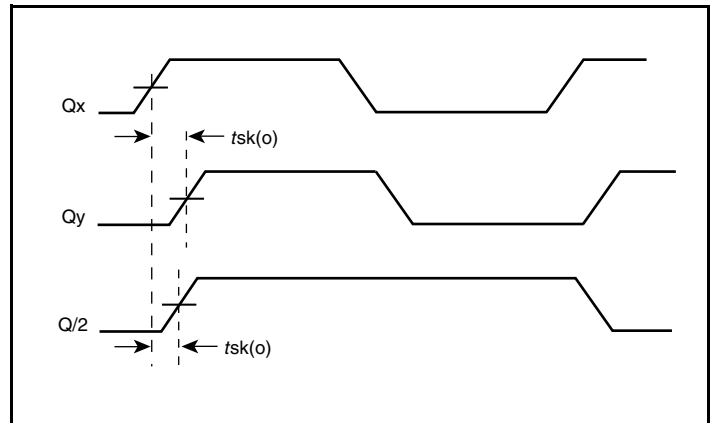
NOTE 4: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

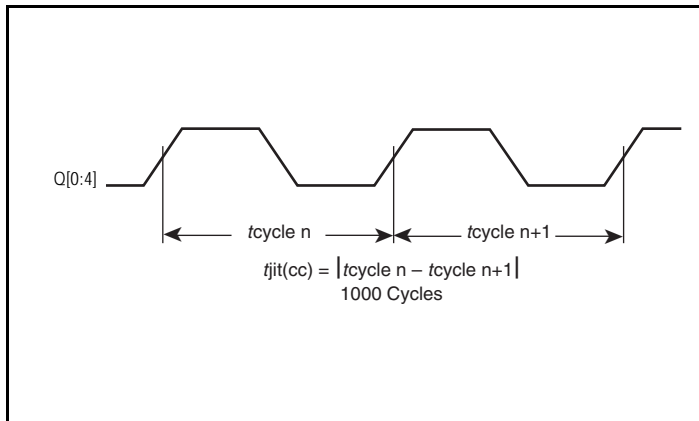
## Parameter Measurement Information



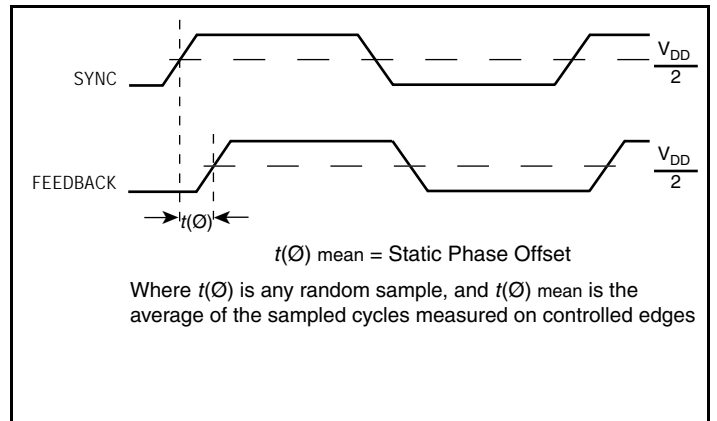
3.3V Output Load AC Test Circuit



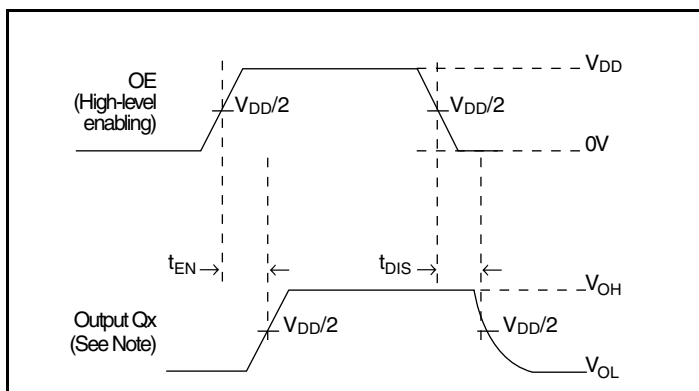
Output Skew



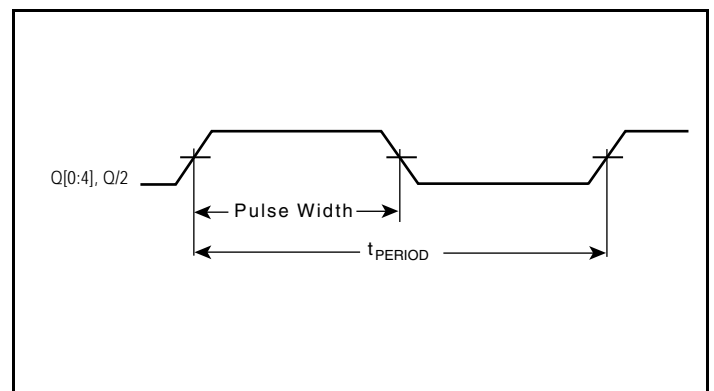
Cycle-to-Cycle Jitter



Static Phase Offset

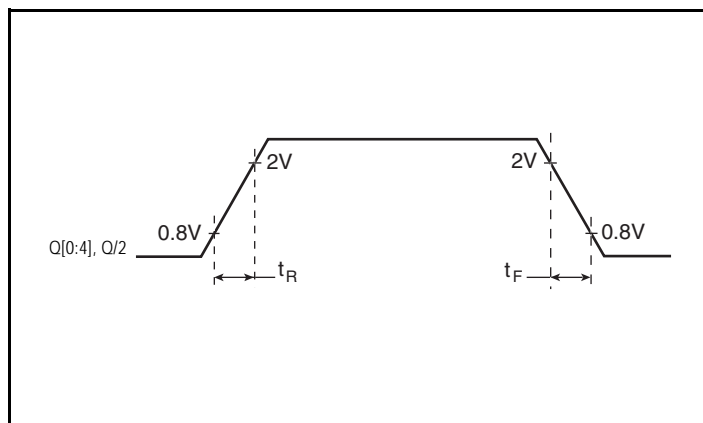


Output Enable/Disable



Output Pulse Width

## Parameter Measurement Information, continued



**Output Rise/Fall Time**

## Application Information

### Recommendations for Unused Output Pins

#### Outputs:

##### LVC MOS Outputs

All unused LVC MOS output can be left floating. There should be no trace attached.

## Schematic Example

Figure 1 shows an example of an 870931I-01 application schematic. In this example, the device is operated at  $V_{DD} = 3.3V$ . The decoupling capacitors should be located as close as possible to the

power pin. The input is driven by a 3.3V LVCMOS driver. An example of LVCMOS termination is shown in this schematic.

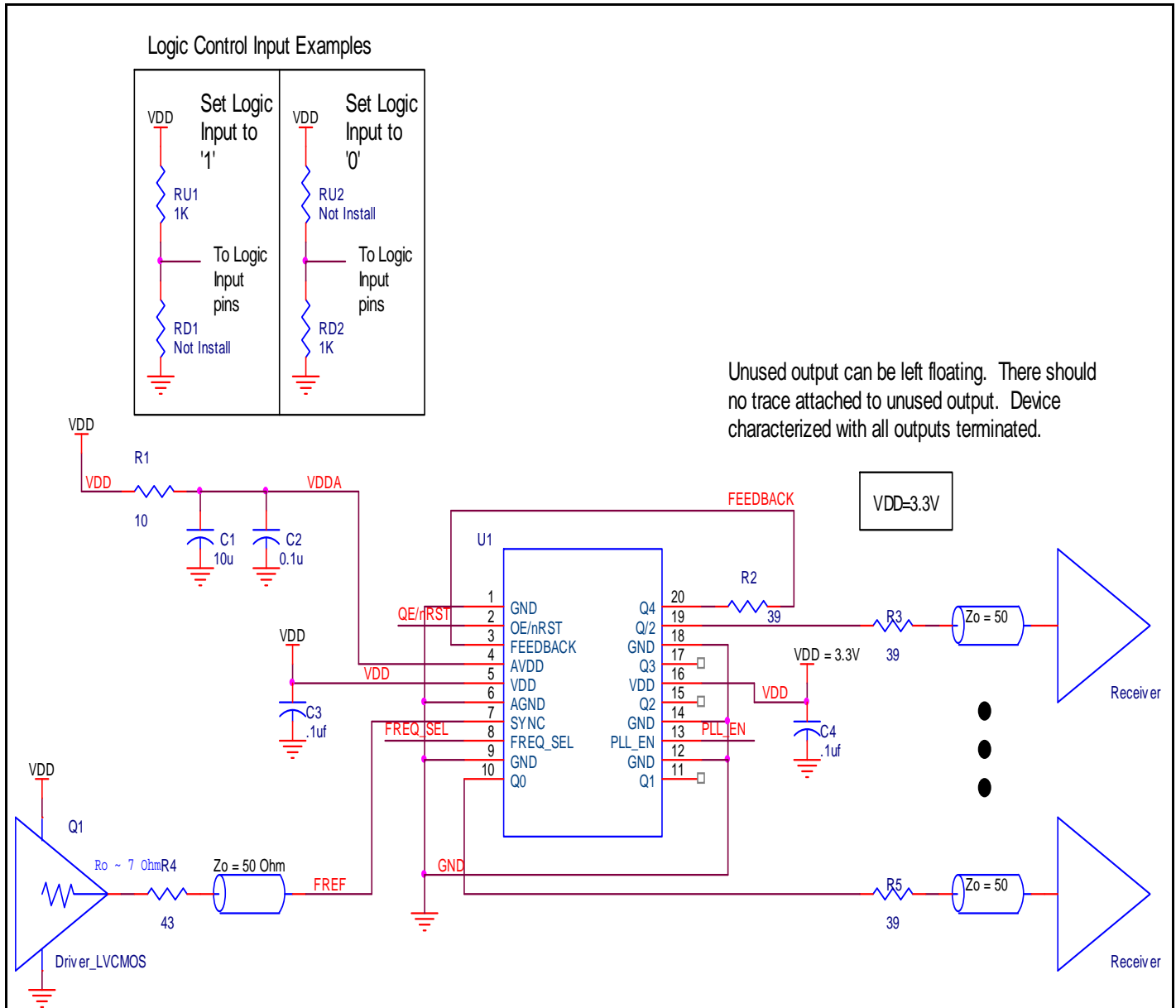


Figure 1. 870931I-01 Schematic Layout Example



## Power Considerations

This section provides information on power dissipation and junction temperature for the 870931I-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 870931I-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 0.3V = 3.6V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{DD\_MAX} = 3.6V * 5mA = 18mW$
- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DD}/2$   
Output Current  $I_{OUT} = V_{DD\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.6V / [2 * (50\Omega + 11\Omega)] = 29.5mA$
- Power Dissipation on the  $R_{OUT}$  per LVCMOS output  
Power ( $R_{OUT}$ ) =  $R_{OUT} * (I_{OUT})^2 = 11\Omega * (29.5mA)^2 = 9.57mW$  per output
- Total Power ( $R_{OUT}$ ) =  $R_{OUT}$  (per output) \* number of outputs =  $9.57mW * 6$  outputs = **57.42mW**

### Dynamic Power Dissipation at 80MHz

$$\text{Power (80MHz)} = C_{PD} * \text{Frequency} * (V_{DD})^2 = 330pF * 80MHz * (3.6V)^2 = 342mW$$

### Total Power

$$\begin{aligned} &= \text{Power (core)}_{MAX} + \text{Total Power (} R_{OUT} \text{)} + \text{Power (80MHz)} \\ &= 18mW + 57.42mW + 342mW \\ &= \mathbf{417.42mW} \end{aligned}$$

### 2. Junction Temperature.

Junction temperature,  $T_J$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is  $125^\circ C$ .

The equation for  $T_J$  is as follows:  $T_J = \theta_{JA} * Pd\_total + T_A$

$T_J$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is  $72.3^\circ C/W$  per Table 6 below.

Therefore,  $T_J$  for an ambient temperature of  $85^\circ C$  with all outputs switching is:

$$85^\circ C + 0.417W * 72.3^\circ C/W = 115.1^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_J$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for a 20 Lead QSOP, Forced Convection**

$\theta_{JA}$ by Velocity			
Linear Feet per Minute	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	$72.3^\circ C/W$	$64.4^\circ C/W$	$61.0^\circ C/W$

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead QSOP

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	72.3°C/W	64.4°C/W	61.0°C/W

## Transistor Count

The transistor count for 870931I-01: 1489

## Package Outline and Package Dimensions

Package Outline - R Suffix for 20 Lead QSOP, 150MIL

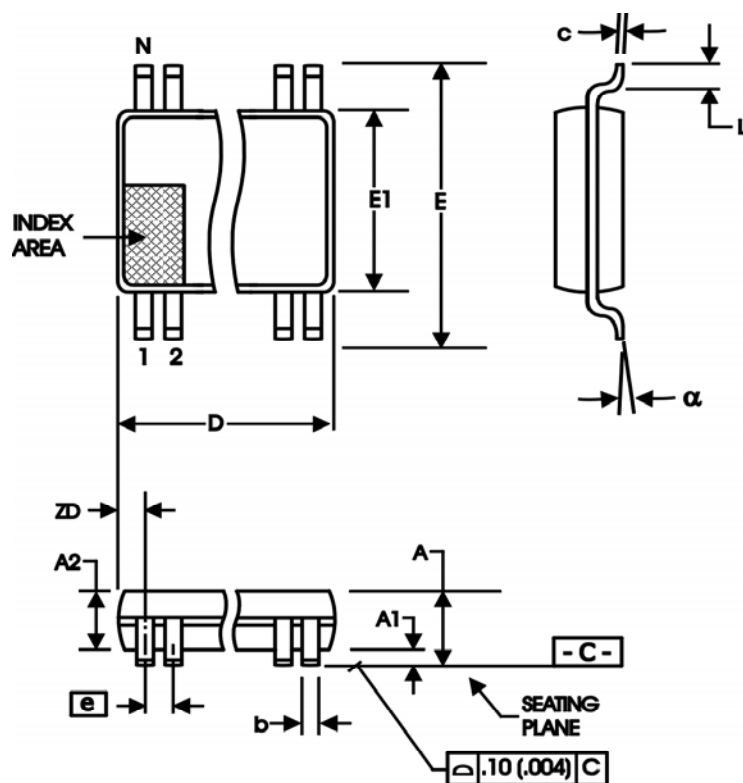


Table 8. Package Dimensions for 20 Lead QSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A	1.35	1.75
A1	0.10	0.25
A2		1.50
b	0.20	0.30
c	0.18	0.25
D	8.55	8.750
E	5.80	6.20
E1	3.80	4.00
e	0.635 Basic	
L	0.40	1.27
$\alpha$	0°	8°
ZD	1.47 Ref	

Reference Document: JEDEC Publication 95, MO-137

## Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
870931ARI-01LF	870931AI01L	"Lead-Free" 20 Lead QSOP	Tube	-40°C to 85°C
870931ARI-01LFT	870931AI01L	"Lead-Free" 20 Lead QSOP	Tape & Reel	-40°C to 85°C

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		8	Added Layout Schematic.	6/10/09
A	T9	11	Removed leaded orderable parts from the Ordering Information table	11/15/12
A	T9	1 11	Removed ICS from part number were needed. General Description - Deleted ICS Chip and HiperClocks. Ordering Information - Deleted LF note below table. Removed quantity for tape and reel. Updated header and footer.	1/27/16
B		1	Corrected header title.	4/25/16



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