

## GENERAL DESCRIPTION

The 8701I is a low skew,  $\div 1$ ,  $\div 2$  Clock Generator. The low impedance LVCMOS outputs are designed to drive 50 $\Omega$  series or parallel terminated transmission lines. The effective fanout can be increased from 20 to 40 by utilizing the ability of the outputs to drive two series terminated lines.

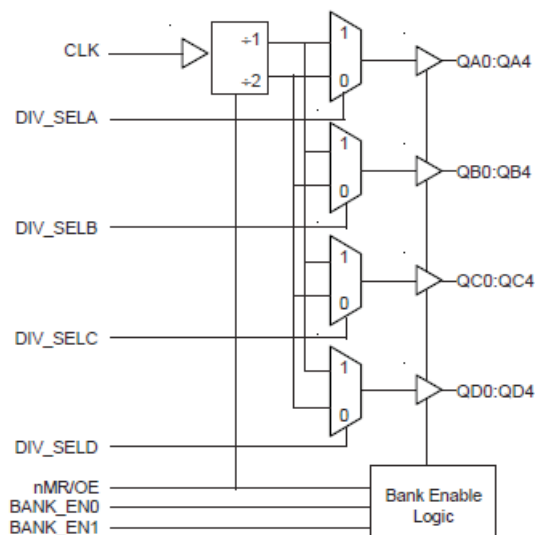
The divide select inputs, DIV\_SELx, control the output frequency of each bank. The outputs can be utilized in the  $\div 1$ ,  $\div 2$  or a combination of  $\div 1$  and  $\div 2$  modes. The bank enable inputs, BANK\_EN0:1, support enabling and disabling each bank of outputs individually. The master reset input, nMR/OE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The 8701I is characterized at 3.3V and mixed 3.3V input supply, and 2.5V output supply operating modes. Guaranteed bank, output and part-to-part skew characteristics make the 8701I ideal for those clock distribution applications demanding well defined performance and repeatability.

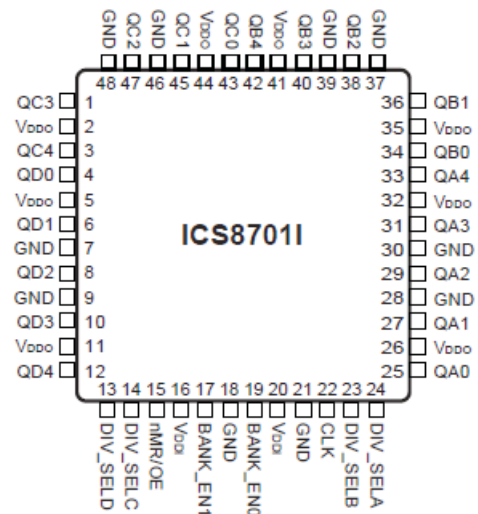
## FEATURES

- Twenty LVCMOS outputs, 7 $\Omega$  typical output impedance
- LVCMOS / LVTTTL clock input
- Maximum input frequency: 250MHz
- Bank enable logic allows unused banks to be disabled in reduced fanout applications
- Bank skew: 200ps
- Output skew: 250ps
- Multiple frequency skew: 300ps
- Part-to-part skew: 600ps
- 3.3V or mixed 3.3V input, 2.5V output operating supply
- -40°C to 85°C ambient operating temperature
- Other divide values available on request
- Available in lead-free RoHS compliant package

## BLOCK DIAGRAM



## PIN ASSIGNMENT



### 48-Pin LQFP

7mm x 7mm x 1.4mm package body

### Y Package

Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
2, 5, 11, 26, 32, 35, 41, 44	V <sub>DDO</sub>	Power		Output supply pins.
7, 9, 18, 21, 28, 30, 37, 39, 46, 48	GND	Power		Power supply ground.
16, 20	V <sub>DD</sub>	Power		Positive supply pins.
25, 27, 29, 31, 33	QA0, QA1, QA2, QA3, QA4	Output		Bank A outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
34, 36, 38, 40, 42	QB0, QB1, QB2, QB3, QB4	Output		Bank B outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
43, 45, 47, 1, 3	QC0, QC1, QC2, QC3, QC4	Output		Bank C outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
4, 6, 8, 10, 12	QD0, QD1, QD2, QD3, QD4	Output		Bank D outputs. LVCMOS / LVTTL interface levels. 7Ω typical output impedance.
22	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
13	DIV_SELD	Input	Pullup	Controls frequency division for Bank D outputs. LVCMOS / LVTTL interface levels.
14	DIV_SEL C	Input	Pullup	Controls frequency division for Bank C outputs. LVCMOS / LVTTL interface levels.
23	DIV_SEL B	Input	Pullup	Controls frequency division for Bank B outputs. LVCMOS / LVTTL interface levels.
24	DIV_SEL A	Input	Pullup	Controls frequency division for Bank A outputs. LVCMOS / LVTTL interface levels.
17, 19	BANK_EN1, BANK_EN0	Input	Pullup	Enables and disables outputs by banks. LVCMOS / LVTTL interface levels.
15	nMR/OE	Input	Pullup	Master Reset and output enable. When HIGH, output drivers are enabled. When LOW, output drivers are in HiZ and dividers are reset. LVCMOS / LVTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance			4		pF
$R_{PULLUP}$	Input Pullup Resistor			51		k $\Omega$
$R_{PULLDOWN}$	Input Pulldown Resistor			51		k $\Omega$
$C_{PD}$	Power Dissipation Capacitance (per output)	$V_{DD}, V_{DDO} = 3.465V$			15	pF
$R_{OUT}$	Output Impedance			7		$\Omega$

**TABLE 3. FUNCTION TABLE**

Inputs				Outputs				
nMR/OE	BANK_EN1	BANK_EN0	DIV_SELx	QA0:QA4	QB0:QB4	QC0:QC4	QD0:QD4	Qx frequency
0	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	zero
1	0	0	0	Active	Hi Z	Hi Z	Hi Z	fIN/2
1	1	0	0	Active	Active	Hi Z	Hi Z	fIN/2
1	0	1	0	Active	Active	Active	Hi Z	fIN/2
1	1	1	0	Active	Active	Active	Active	fIN/2
1	0	0	1	Active	Hi Z	Hi Z	Hi Z	fIN
1	1	0	1	Active	Active	Hi Z	Hi Z	fIN
1	0	1	1	Active	Active	Active	Hi Z	fIN
1	1	1	1	Active	Active	Active	Active	fIN

# **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5\text{ V}$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5\text{ V}$
Package Thermal Impedance, $\theta_{JA}$	47.9°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3\text{V} \pm 5\%$ ,  $V_{DDO} = 3.3\text{V} \pm 5\%$  OR  $2.5\text{V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				100	mA

**TABLE 4B. LVCMOS DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = 0^\circ\text{C}$  TO  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SEL, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	2		$V_{DD} + 0.3$	V
		CLK	2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SEL, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	-0.3		0.8	V
		CLK	-0.3		1.3	V
$I_{IH}$	Input High Current	DIV_SELA, DIV_SELB, DIV_SEL, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	$V_{DD} = V_{IN} = 3.465V$		5	$\mu\text{A}$
		CLK	$V_{DD} = V_{IN} = 3.465V$		150	$\mu\text{A}$
$I_{IL}$	Input Low Current	DIV_SELA, DIV_SELB, DIV_SEL, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu\text{A}$
		CLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu\text{A}$
$V_{OH}$	Output High Voltage	$V_{DD} = V_{DDO} = 3.135V$ $I_{OH} = -36\text{mA}$	2.6			V
		$V_{DD} = 3.135V$ , $V_{DDO} = 2.375V$ $I_{OH} = -27\text{mA}$	1.8			V
$V_{OL}$	Output Low Voltage	$V_{DD} = V_{DDO} = 3.135V$ $I_{OL} = 36\text{mA}$			0.5	V
		$V_{DD} = 3.135V$ , $V_{DDO} = 2.375V$ $I_{OL} = 27\text{mA}$			0.5	V

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Input Frequency				250	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1	$0\text{MHz} \leq f \leq 200\text{MHz}$	2.2		3.6	ns
$t_{p_{HL}}$	Propagation Delay, High-to-Low; NOTE 1	$0\text{MHz} \leq f \leq 200\text{MHz}$	2.2		3.6	ns
$t_{sk(b)}$	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDO}/2$			200	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDO}/2$			250	ps
$t_{sk(w)}$	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDO}/2$			300	ps
$t_{sk(pp)}$	Part to Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDO}/2$			600	ps
$t_R$	Output Rise Time; NOTE 6	30% to 70%	200		900	ps
$t_F$	Output Fall Time; NOTE 6	30% to 70%	200		900	ps
$t_{PW}$	Output Pulse Width	$0\text{MHz} \leq f \leq 200\text{MHz}$	$t_{CYCLE}/2 - 0.6$	$t_{CYCLE}/2$	$t_{CYCLE}/2 + 0.6$	ns
		$f = 200\text{MHz}$	1.9	2.5	3.1	ns
$t_{EN}$	Output Enable Time; NOTE 6	$f = 10\text{MHz}$			6	ns
$t_{DIS}$	Output Disable Time; NOTE 6	$f = 10\text{MHz}$			6	ns

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}$  input crossing point to the output at  $V_{DDO}/2$ .

NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Input Frequency				250	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1	$0\text{MHz} \leq f \leq 200\text{MHz}$	2.4		3.7	ns
$t_{p_{HL}}$	Propagation Delay, High-to-Low; NOTE 1	$0\text{MHz} \leq f \leq 200\text{MHz}$	2.4		3.7	ns
$t_{sk(b)}$	Bank Skew; NOTE 2, 7	Measured on rising edge at $V_{DDO}/2$			225	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 7	Measured on rising edge at $V_{DDO}/2$			250	ps
$t_{sk(w)}$	Multiple Frequency Skew; NOTE 4, 7	Measured on rising edge at $V_{DDO}/2$			300	ps
$t_{sk(pp)}$	Part to Part Skew; NOTE 5, 7	Measured on rising edge at $V_{DDO}/2$			650	ps
$t_R$	Output Rise Time; NOTE 6	30% to 70%	200		900	ps
$t_F$	Output Fall Time; NOTE 6	30% to 70%	200		900	ps
$t_{PW}$	Output Pulse Width	$0\text{MHz} \leq f \leq 200\text{MHz}$	$t_{CYCLE}/2 - 0.6$	$t_{CYCLE}/2$	$t_{CYCLE}/2 + 0.6$	ns
		$f = 200\text{MHz}$	1.9	2.5	3.1	ns
$t_{EN}$	Output Enable Time; NOTE 6	$f = 10\text{MHz}$			6	ns
$t_{DIS}$	Output Disable Time; NOTE 6	$f = 10\text{MHz}$			6	ns

All parameters measured at 200MHz unless noted otherwise.

NOTE 1: Measured from the  $V_{DD}$  input crossing point to the output at  $V_{DDO}/2$ .

NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions.

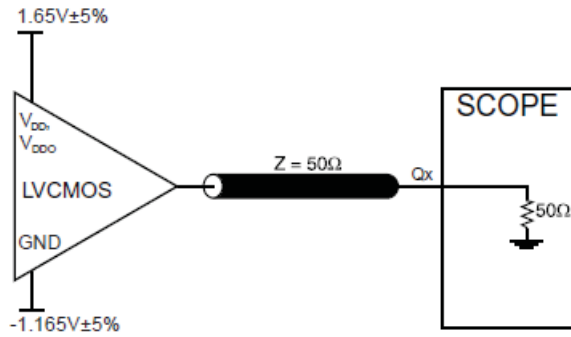
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.

NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at  $V_{DDO}/2$ .

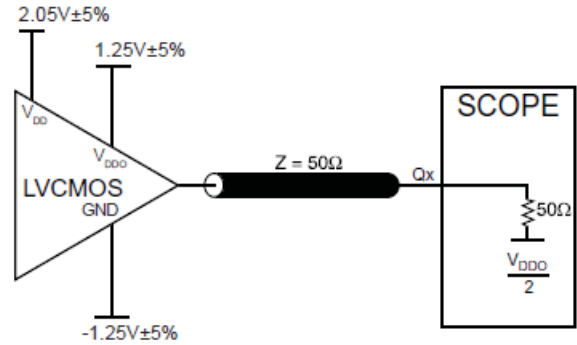
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

NOTE 7: This parameter is defined in accordance with JEDEC Standard 65.

## PARAMETER MEASUREMENT INFORMATION



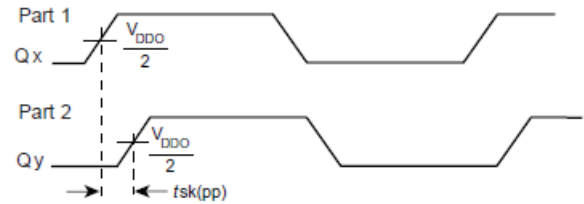
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



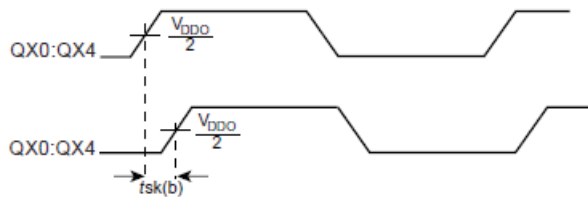
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



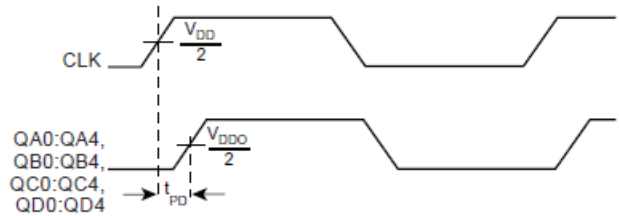
OUTPUT SKEW



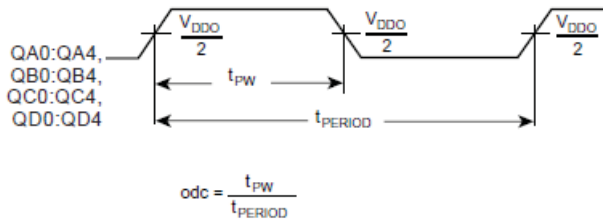
PART-TO-PART SKEW



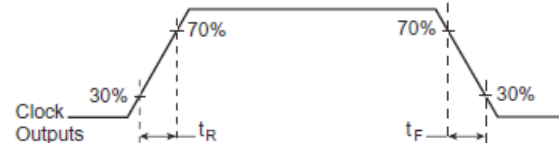
BANK SKEW (where X denotes outputs in the same bank)



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



## APPLICATION INFORMATION

### Driver Termination

For LVCMOS Output Termination, please refer to a separate Application Note: *LVCMOS Driver Termination*.

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### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### OUTPUTS:

##### LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

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## POWER CONSIDERATIONS

For Power Dissipation, please refer to a separate Application Note: *Power Dissipation for LVCMOS Buffer*.

RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 48 LEAD LQFP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W
<b>NOTE:</b> Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.			

TRANSISTOR COUNT

The transistor count for 8701I is: 1743

PACKAGE OUTLINE -Y SUFFIX FOR 48 LEAD LQFP

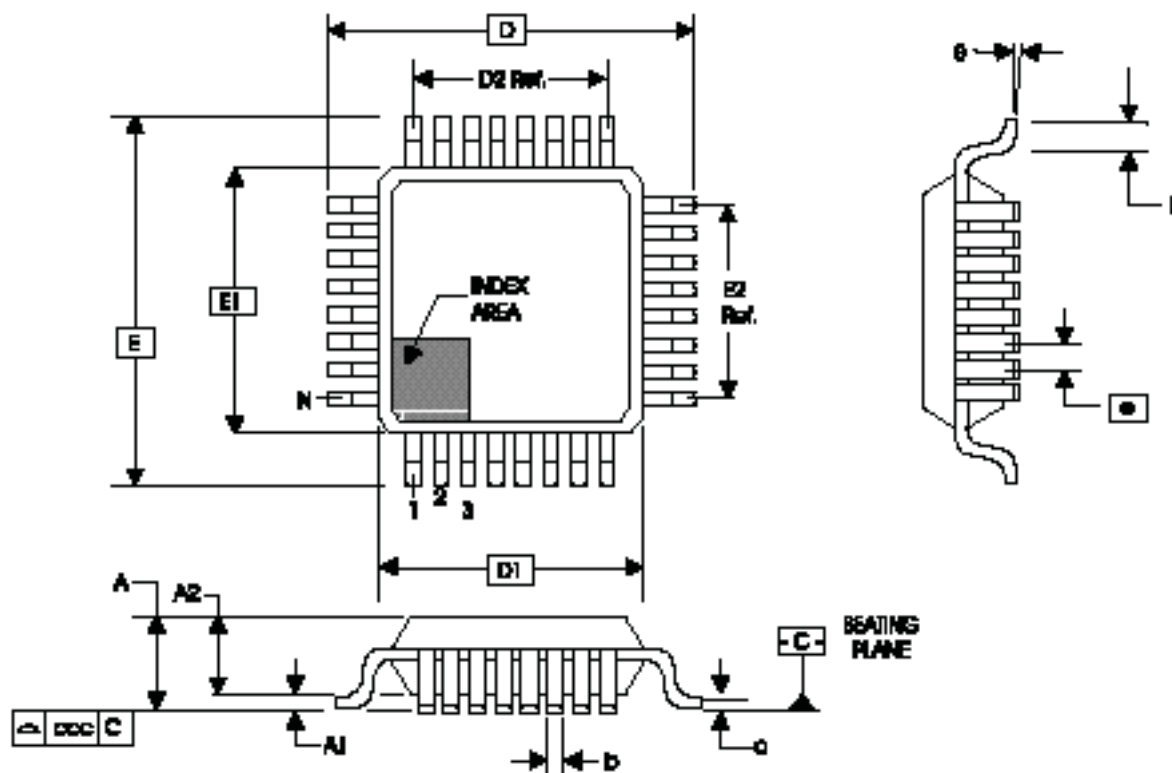


TABLE 7. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BBC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BASIC		
D1	7.00 BASIC		
D2	5.50 Ref.		
E	9.00 BASIC		
E1	7.00 BASIC		
E2	5.50 Ref.		
e	0.50 BASIC		
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

**TABLE 7. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8701CYILF	ICS8701CYILF	48 lead "Lead Free" LQFP	Tray	0°C to +70°C
8701CYILFT	ICS8701CYILF	48 lead "Lead Free" LQFP	Tape and Reel	0°C to +70°C

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	1 5A 5B	2	Updated format throughout the datasheet.	8/19/02
		5	Renamed LVCMOS_CLK to CLK.	
		7	Renamed V <sub>DDI</sub> to V <sub>DD</sub> .	
		8 - 10	Pin Description Table, revised nMR/OE description.	
		10	3.3V AC Characteristics Table, updated notes.	
		11	3.3V/2.5V Characteristics Table, updated notes.	
		12	Updated drawings.	
B	T2	1	Added Power Consideration and Driver Termination notes.	2/28/06
		3	Added Reliability Information and Transistor Count.	
		8	Revised Package Outline.	
		9	Features Section - added lead-free bullet.	
	T7	12	Pin Characteristics Table - changed CIN from 4pF max. to 4pF typical.	
		12	Parameter Measurement Information - added Bank Skew diagram.	
C	T7	12	Application Information - added <i>Recommendations for Unused Input and Output Pins</i> .	7/27/10
		14	Ordering Information Table - added lead-free part number, marking and note.	
C	T7	12	Updated format throughout the data sheet.	1/22/16
		12	Updated datasheet's header/footer with IDT from ICS.	
		12	Removed ICS prefix from Part/Order Number column.	
	T7	12	Added Contact Page.	
		12	Removed ICS from the part number where needed.	
	T7	12	Features Section - removed reference to leaded package.	
		12	Ordering Information - removed quantity for tape and reel. Deleted LF note below the table.	
	T7	12	Updated header and footer.	
		12		



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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

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